



Online Data Processing and DAQ for DarkSide-20k

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on behalf of the DarkSide-20k Collaboration



Overview



- DarkSide-20k as a Dark Matter Experiment and much more
- Light detection in DS-20k using novel SiPMs
- How to readout the signals from the SiPMs ? DS-20k data acquisition system
 - Overview of the system
 - The Quadrant: a mockup system for DS-20k data acquisition
- Conclusions and next steps

DarkSide-20k experiment

The Detector

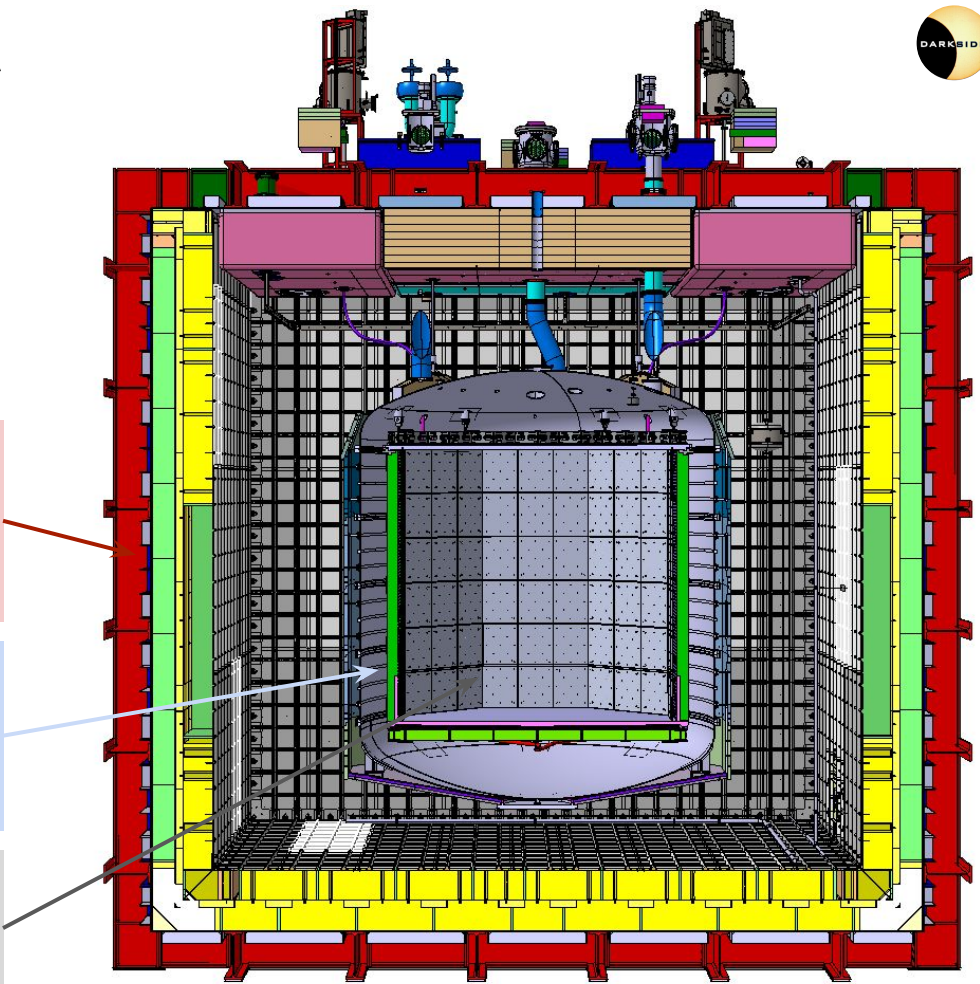


Dual phase Liquid Argon Time Projection Chamber currently under construction at Laboratori Nazionali del Gran Sasso (LNGS)

Cryostat filled with 650t of **Atmospheric Argon** (AAr) and instrumented with photodetectors to work as an outer veto

Inner Veto: 36t of Liquid Underground Argon within a stainless steel vessel and surrounding the TPC to work as a **neutron veto**

TPC: 50t of Liquid Underground Argon (20t) fiducial constituting the detector core.



DarkSide-20k experiment

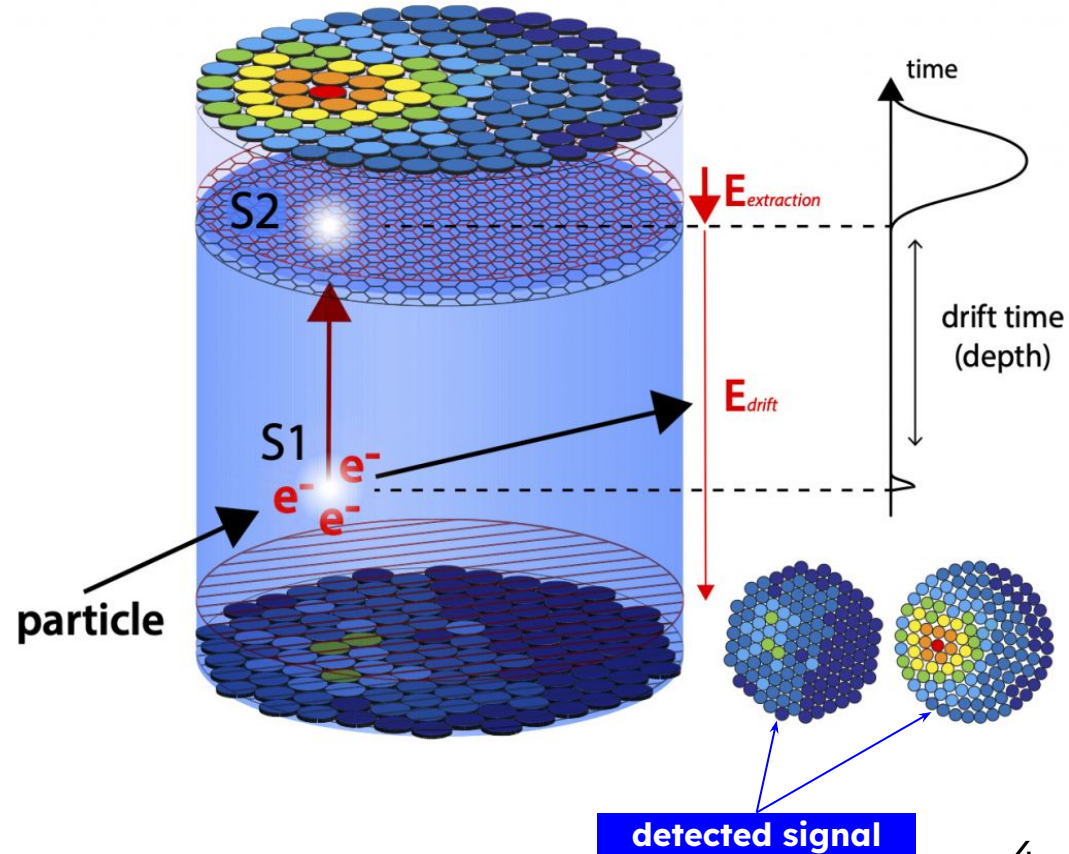
A Dark Matter search experiment..

WIMP - nucleus coherent elastic scattering \rightarrow single nuclear recoil, ROI: [30, 200] keVnr

Energy deposition in LAr produces scintillation photons and free electrons

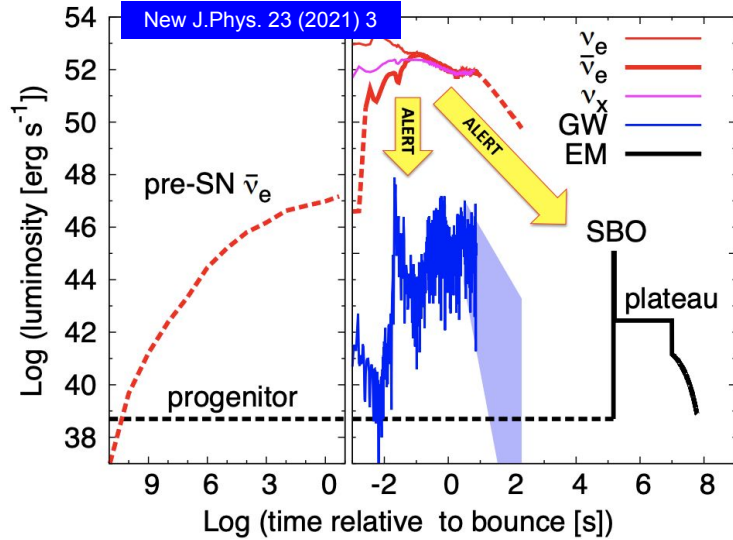
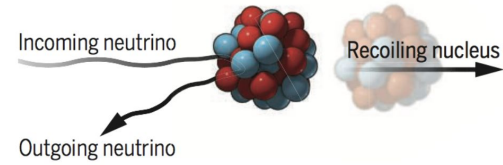
S1: primary scintillation in LAr (energy information and pulse shape discrimination)

S2: secondary scintillation from electroluminescence of electrons in gas pocket (energy information and position reconstruction)



... and much more !

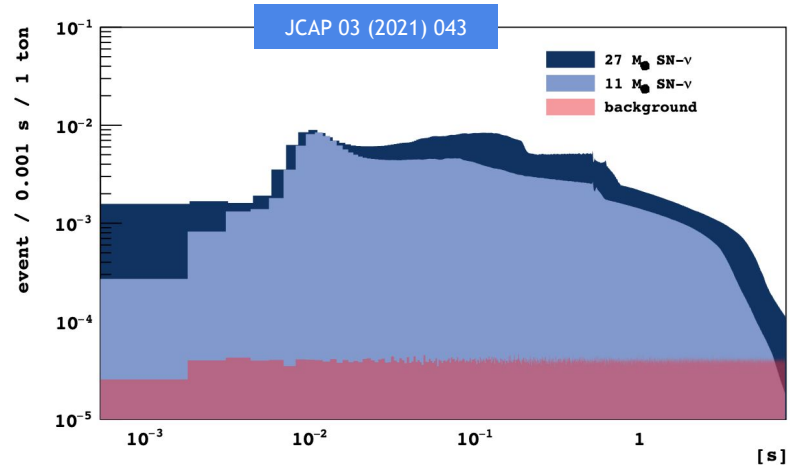
DS-20k as a Supernova detector



Neutrinos can serve as a prompt alert in case of a Supernova event via CEvNS, Coherent Elastic Neutrino-Nucleus Scattering → sensitive to all neutrino flavors!

DS-20k can be sensitive to CEvNS (sub-keV recoil energy) via S2-only analysis.

Expected contribution to Supernova Early Warning System (SNEWS 2.0)



Event time resolution is dominated by the electron drift time (maximum drift time ~ 3.5 ms)

Light detection in DS-20k

Silicon PhotoMultipliers (SiPM)



Single Photon Avalanche PhotoDiodes (SPADs) connected in parallel operated in reverse bias mode

Advantages:

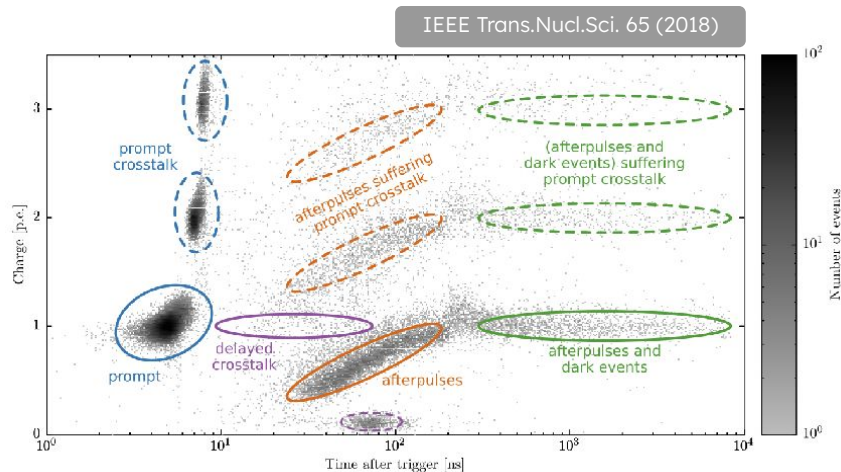
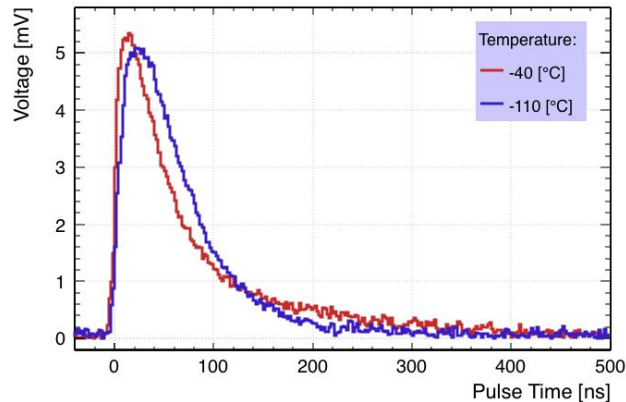
- High gain at low bias voltage
- Single photon detection resolution
- High radiopurity
- Suitable at cryogenic temperature
- High Photon Detection Efficiency (PDE)

Uncorrelated Avalanche Noise

- Dark Count Rate (DCR)

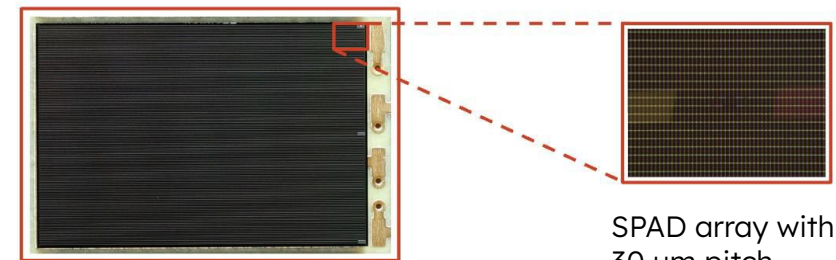
Correlated Avalanche Noise

- Afterpulse (AP)
- Internal Cross talk (CT), Prompt ($\ll 1$ ns) or Delayed ($>$ ns)
- External CT



Light detection in DS-20k

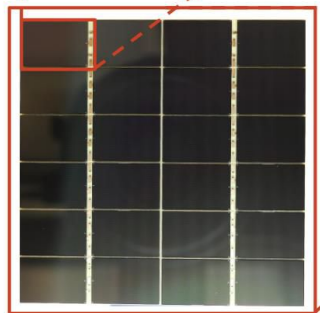
from SiPMs to PDUs



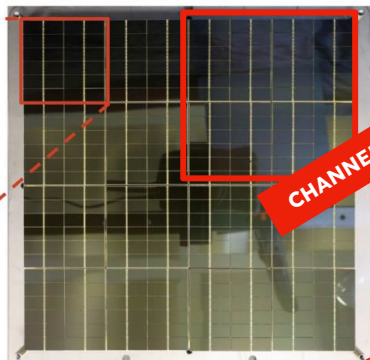
SiPM 11.8 x 7.9 mm²

SPAD array with
30 μm pitch

PDU: 16 Tiles, 20 x 20 cm²



Tile: 24 SiPMs, 4.95 x 4.95 cm²

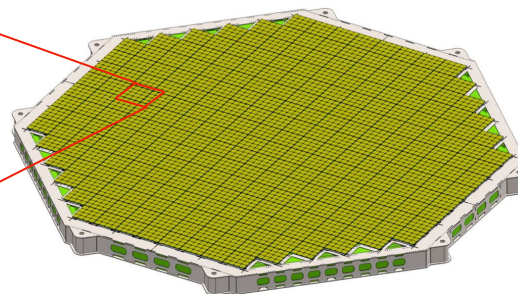


CHANNEL

The main detection unit is the Photo Detection Unit (PDU), made up of 16 Tiles, in turn composed of 24 cryogenic, low noise and low background SiPMs.

4 tiles (10 cm²x10 cm²) constitute a readout channel. Large area implies higher noise.

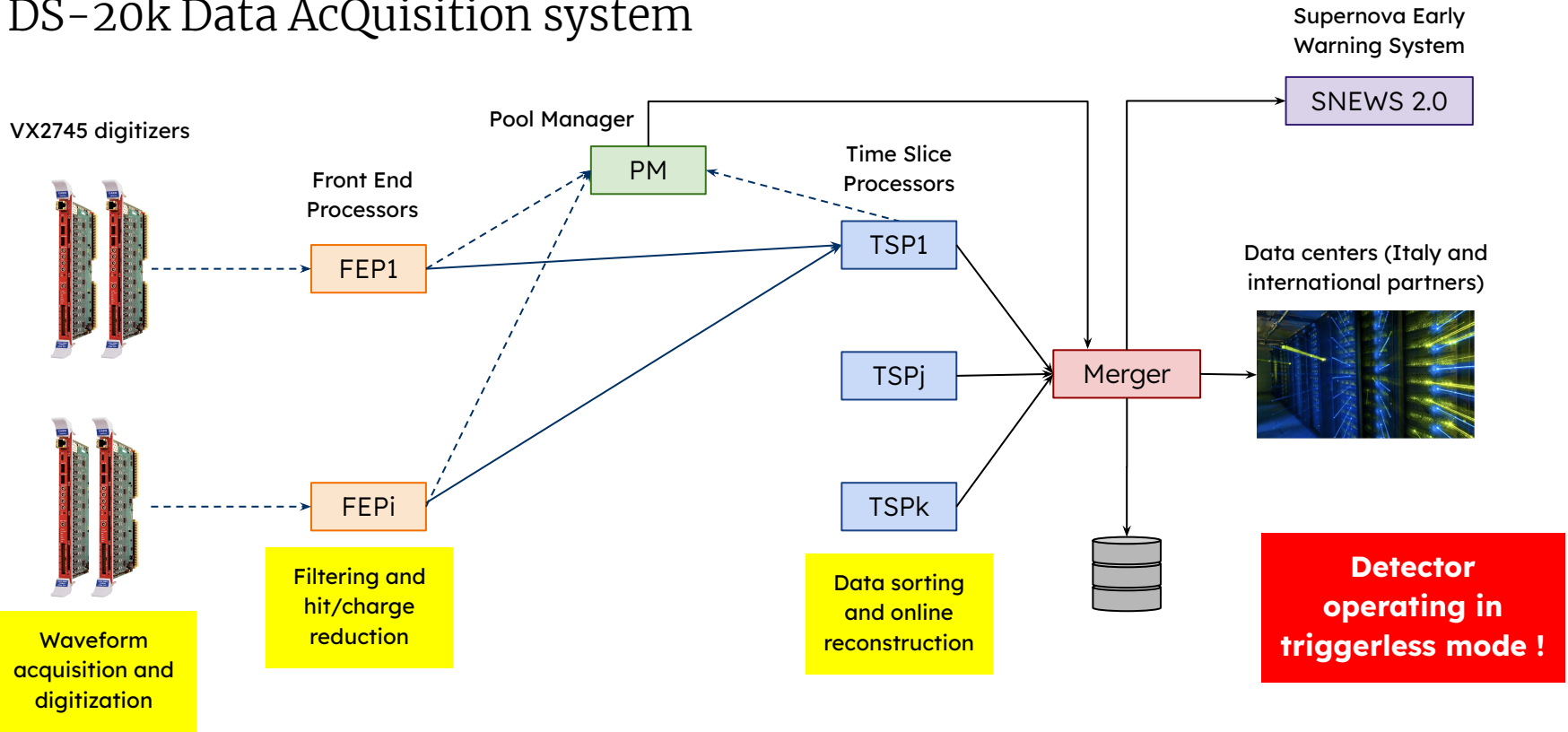
PDUs assembled in the cleanroom packaging facility Nuova Officina Assergi (NOA) at Laboratori Nazionali del Gran Sasso (LNGS).



21 m² optical planes

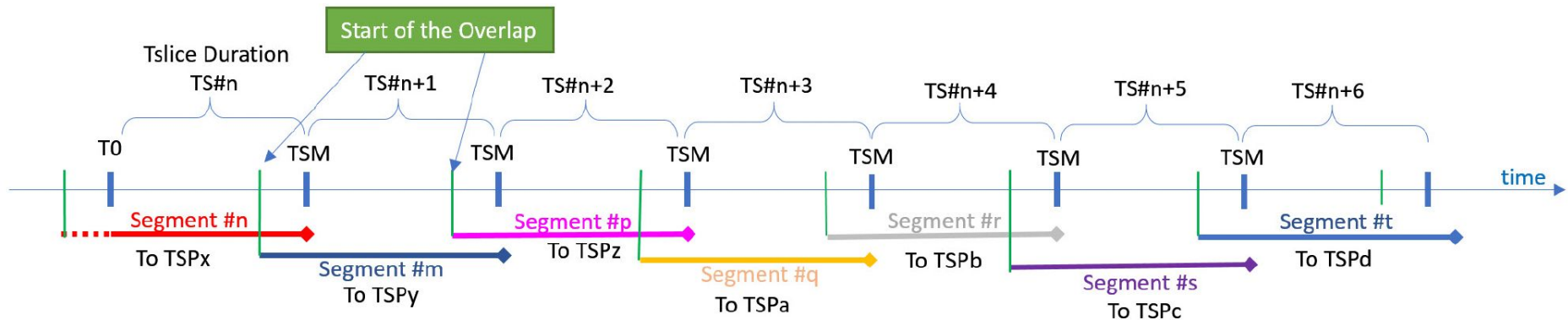
How to readout the signals from the SiPMs

DS-20k Data AcQuisition system



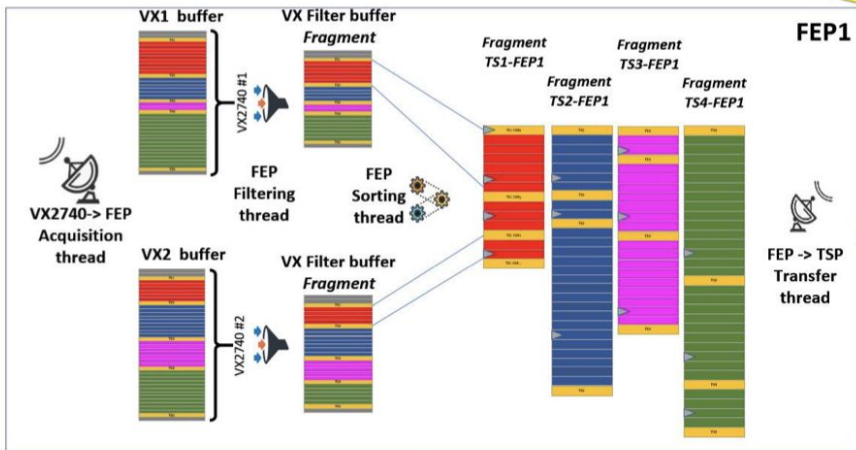
DarkSide-20k data acquisition

Time Slice concept

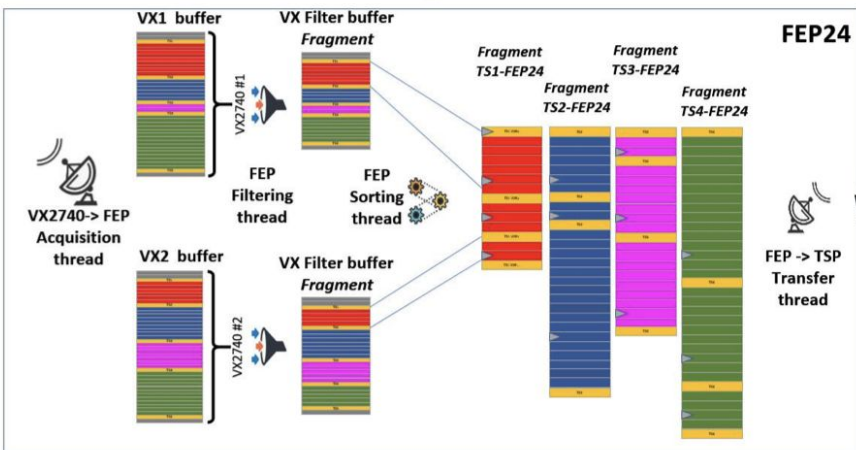


- Data acquisition divided into **time slices**
- A **time slice** is the complete collection of detector data over a fixed amount of time (with overlap with previous slice)
- Time Slices are submitted individually to a dedicated processor, TSP (see later)
- Time Slice Marker (TSM) is injected at the digitizer level

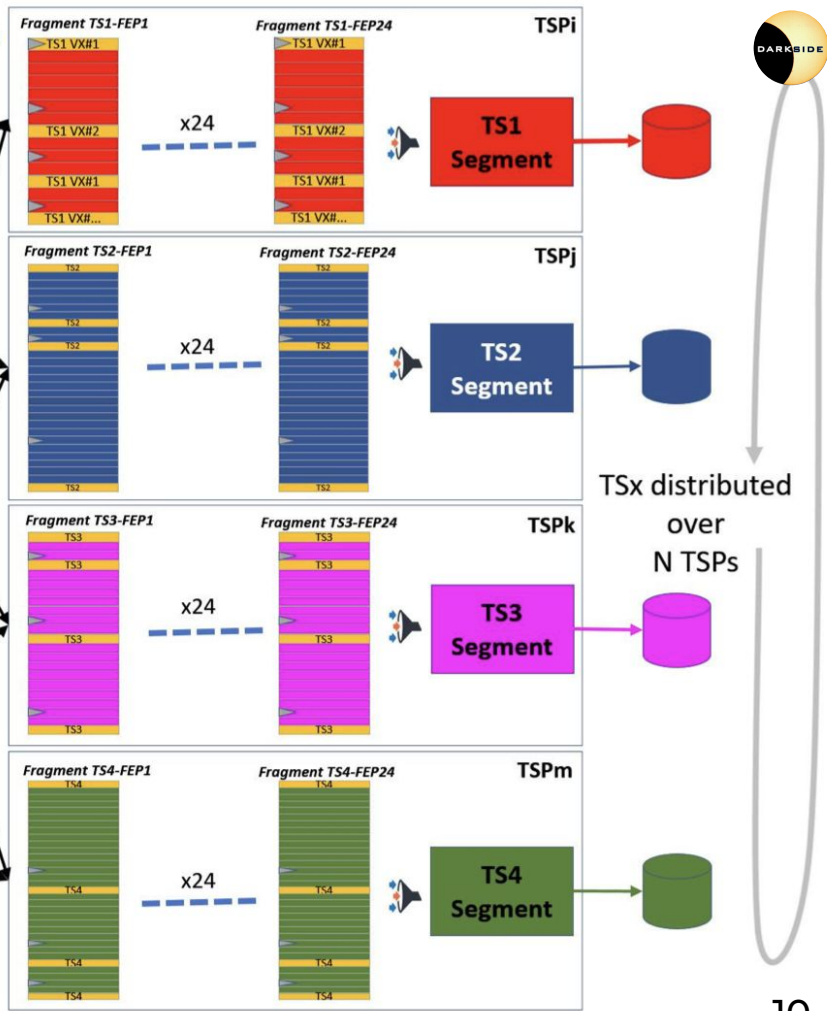
Data Flow [WFD-FEPs-TSPs, PM]



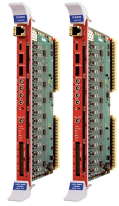
x24



Pool Manager



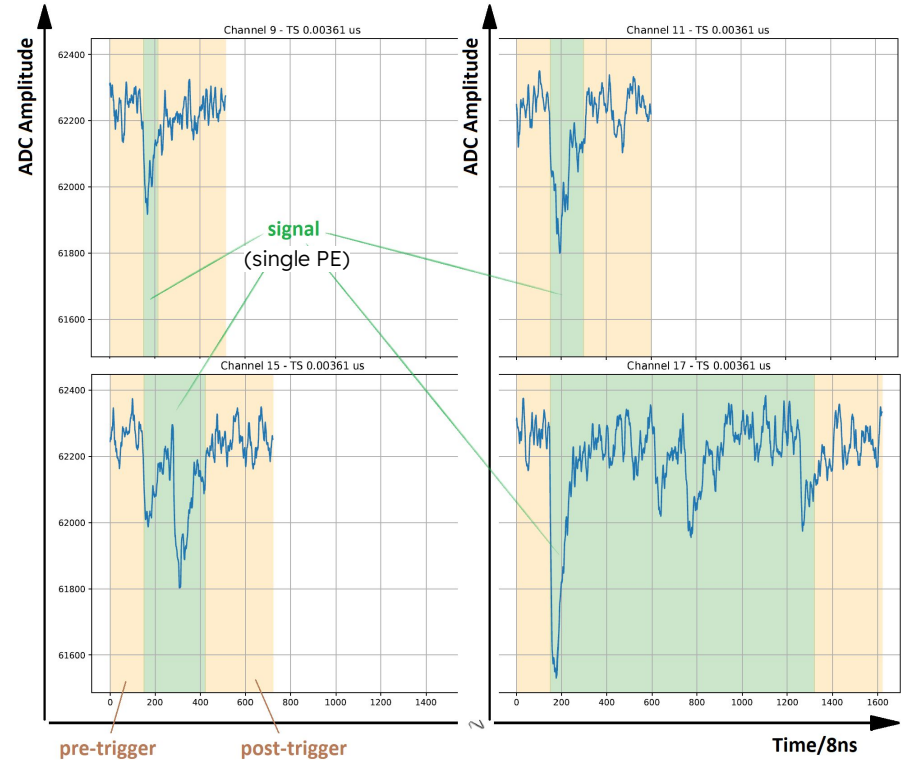
Waveform digitization



- Waveforms from the photosensors are digitized by **VME VX2745 CAEN** digitizer modules **16 bit, 125MS/s ADC**

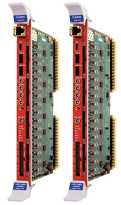


- **Custom firmware** developed at TRIUMF laboratory designed to identify only waveform segments containing a signal
- **Dynamic waveform window:** enlarge the gate if the post-trigger contains a new trigger

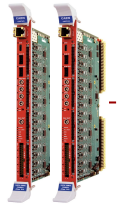


Front End Processors (FEPs)

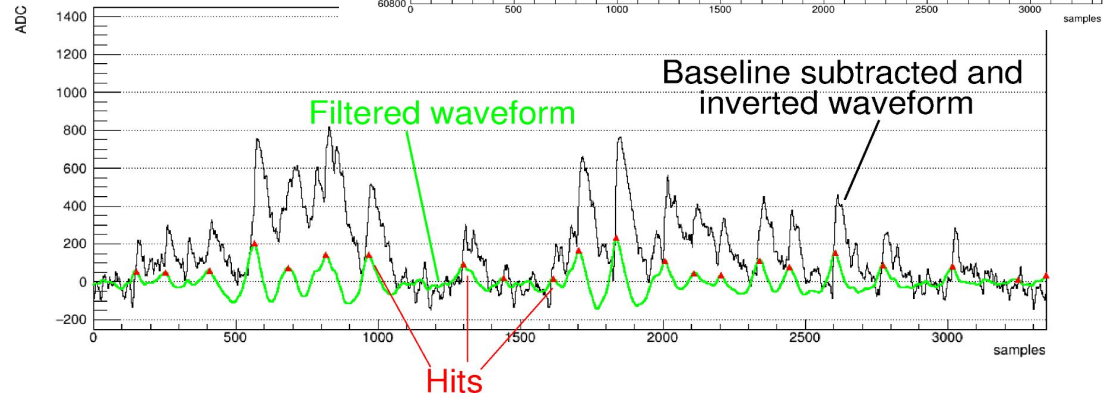
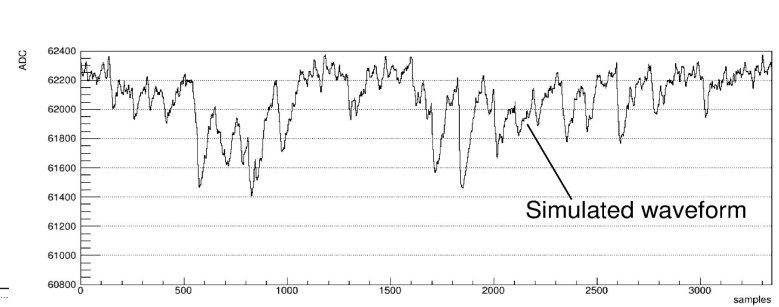
The challenge of data reduction



FEP1



FEPi

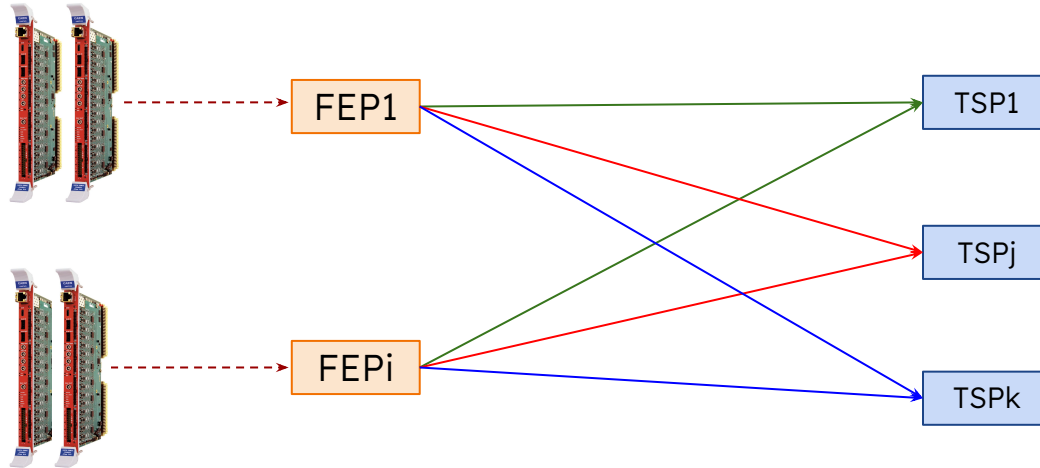


- DS-20k will operate in **triggerless mode**, with an expected event rate of **200 evts/s** → we cannot save all the individual channel waveforms to disk !
- Filtering is necessary to remove noise spikes (ARMA algorithm)
- Waveform **reduction to hit** time/charge (# PEs) is needed in real time (still **2PB/year!**)
- Data are sorted into 1 s time slices to be sent to the next acquisition stage



Time Slice Processors (TSPs)

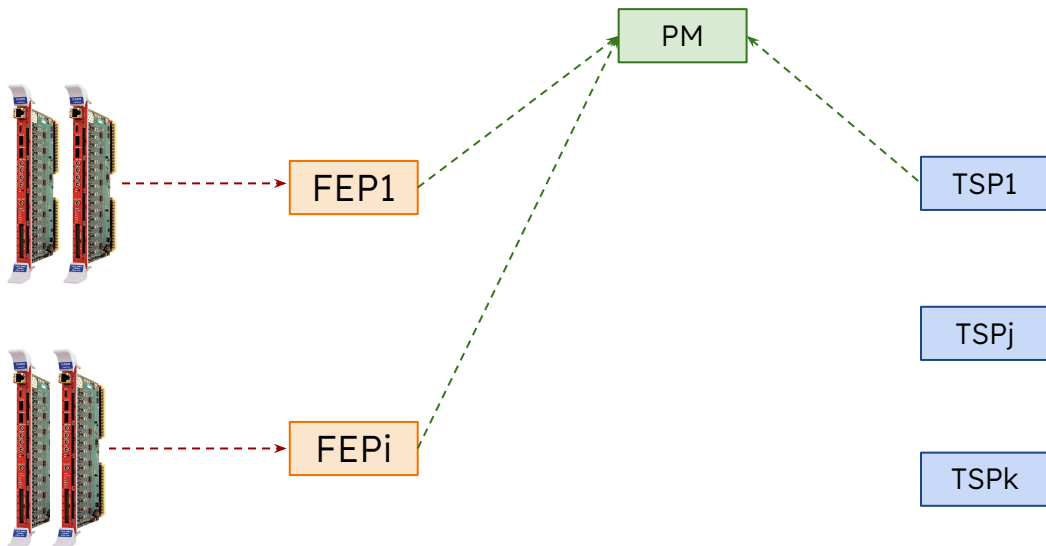
The challenge of data reduction



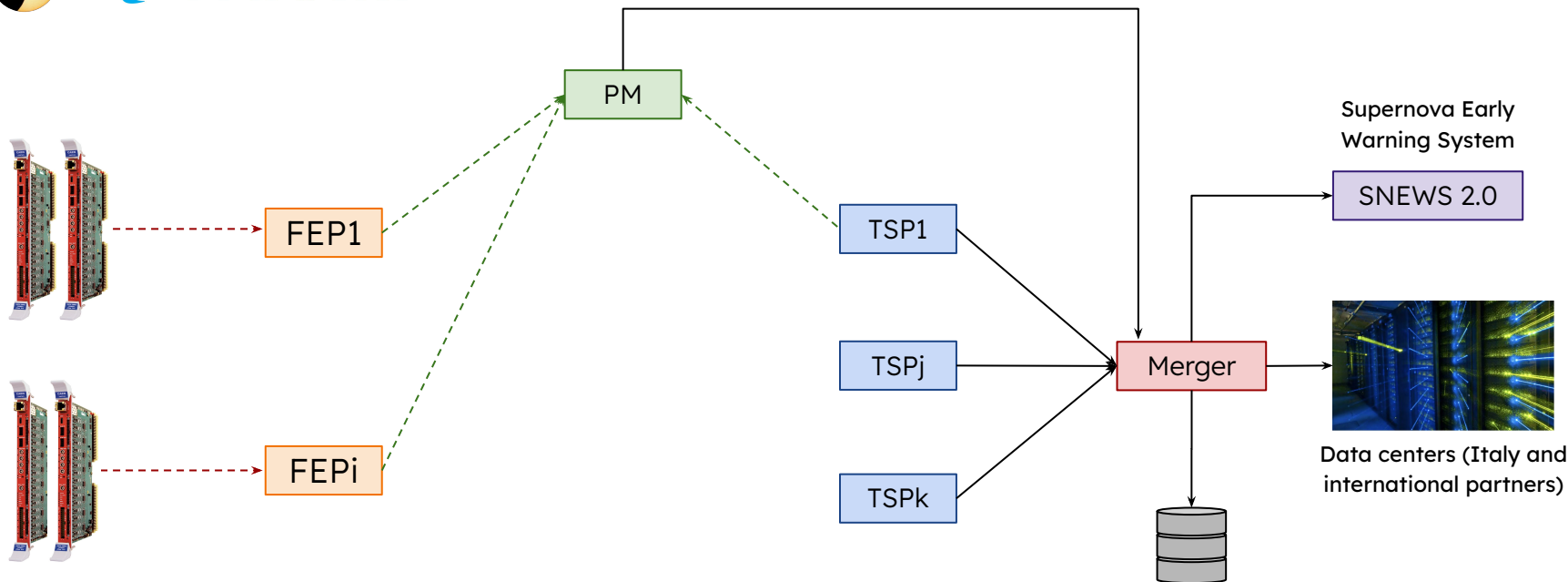
- Hits sequences belonging to the same 1 s time slice are gathered into the same online computing node
- Time slices are sent via raw TCP/IP sockets
- Perform high level analysis on the TSPs (hit clustering / pulse finding, energy, XY...)
- TSPs responsible for streaming data according to the physics event



Pool Manager (PM) Orchestrating the data flow



- The Pool Manager (PM) communicates with both the FEPs and TSPs via [ZeroMQ](#) message queue: it gets informed by the FEPs about the available time slices and from TSPs about their status
- The PM informs the FEPs of the next available TSPs



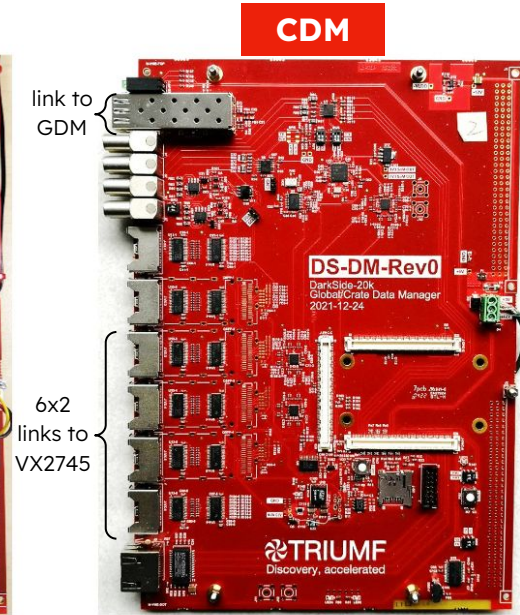
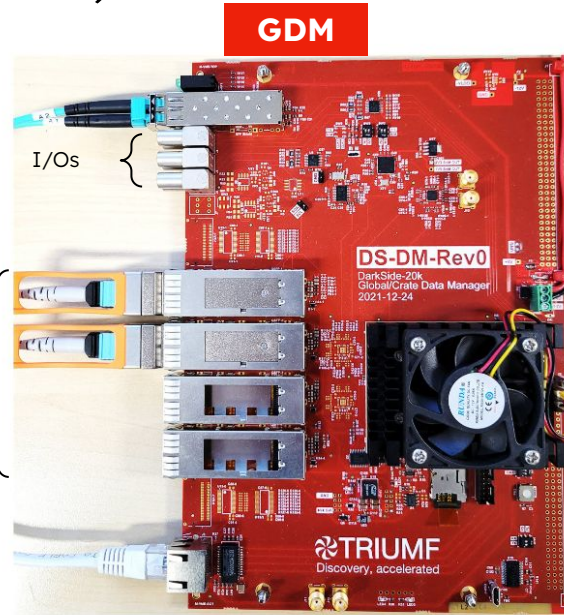
- Time slices from different TSPs are collected into the Merger, stored to disk and sent to Data Centers
- The Merger can also perform physics analysis on longer timescales like Supernova identification and send the results to the Supernova Early Warning System (SNEWS 2.0)

Global Data Manager (GDM) and Crate Data Manager (CDM)



4x3 optical links to CDM

Ethernet link



CDM

Transmits to 12 VX:

- Common clock
- VX commands

Collects up to 12 VX:

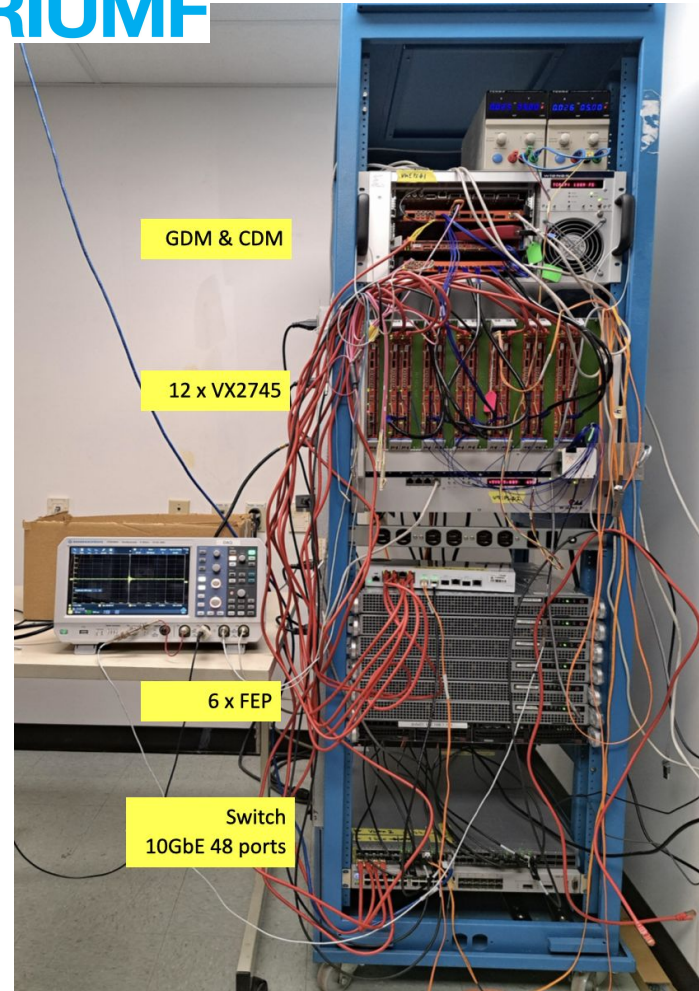
- Module busy bits
- Prompt “self-trigger “ bits

I/Os	Specification	Purpose
1 RJ45 port	1Gbit Ethernet	Configuration
4 QSFP+	2.5Gb/s communication to CDM	Clock Trigger
4 NIM inputs	IRIG-B, 10MHz Ref clock, Ext TrgIN-1, Ext TrgIN-II	GPS, Triggers
4 NIM outputs	1PPS, Ext TrgOUT-1	GPS, Trigger

The Quadrant

A test bench for DS-20k data acquisition

- ¼ of DarkSide-20k data acquisition system up and running at TRIUMF laboratory (Vancouver, Canada)
- System structure:
 - 1 x GDM
 - 1 x CDM
 - 12 x VX2745 digitizers
 - 6 x FEP computers
 - 1 x 48 ports 10 GbE switch
- The system allows for firmware testing, digitizer software and machine-specific softwares performing the online analysis



A mockup of DS-20k data flow

A software implementation of the full data flow

Input can be real data from the VX2745 or binary data with simulated waveforms

DAQ infrastructure built in MIDAS (Maximum Integrated Data Acquisition System) software package developed at TRIUMF and PSI

Monitoring system under development: key quantities displayed on a webpage

Run Status

Run 2635 Running <input type="button" value="Stop"/> <input type="button" value="Pause"/>	Start: Mon Oct 7 02:40:09 2024	Running time: 0h00m12s
Alarms: Off	Restart: Off	Data dir: /home/dsdaq/madry/data
Experiment Name: vslice		
Comment: FEP Hit Finder		
1728294020 02:40:20.092 2024/10/07 [TSP_003,INFO] Sending data to TSP merger, size 10556 bytes		

Equipment

Equipment +	Status	Events	Events[/s]	Data[MB/s]
FEP_000	Disabled	0	0.0	0.000
FEP_001	Sent slice 8, Last slice size 527360 (B)	0	0.0	0.000
FEP_002	Disabled		0.0	0.000
FEP_004	Disabled		0.0	0.000
FEP_MonitorHistos_001	FEP_001	0	0.0	0.000
PoolManager	idle: 2, receiving: 1, analyzing: 0	0	0.0	0.000
TSP_Pool	last slice: 7, tx: 0.09438 - 0.09523 MB/s, ana: 0.04281 - 0.04294 s	0	0.0	0.000
TSP_Tap	Frontend stopped	0	0.0	0.000
TSP_001	TSP_001@dsts01	0	0.0	0.000
TSP_002	TSP_002@dsts02	0	0.0	0.000
TSP_003	TSP_003@dsts03	0	0.0	0.000
TSP_004	Frontend stopped	0	0.0	0.000
TSP_005	Frontend stopped	0	0.0	0.000
Merger	Merger	0	0.0	0.000

Logging Channels

Channel	Events	MB written	Compr.	Disk Level
#0:	0	0.000	0.0%	0.0%
#1: run02635.mid.lz4	1	0.000	0.0%	35.1%
Lazy Label	Progress	File Name	# Files	Total

Clients

Logger [dsvslice.triumf.ca]	mserver [dsvslice.triumf.ca]	PoolManager [dsvslice.triumf.ca]
TSP_001 [dsts01]	TSP_002 [dsts02]	TSP_003 [dsts03]
Merger [dsvslice.triumf.ca]	FEP_001 [dsvslice.triumf.ca]	mhttpd [dsvslice.triumf.ca]

Conclusion and next steps

A lot of results...

- DAQ quadrant system operational at TRIUMF !
- System expected to be shipped to Laboratori Nazionali del Gran Sasso in Feb/March 2025

... and a lot more to come!

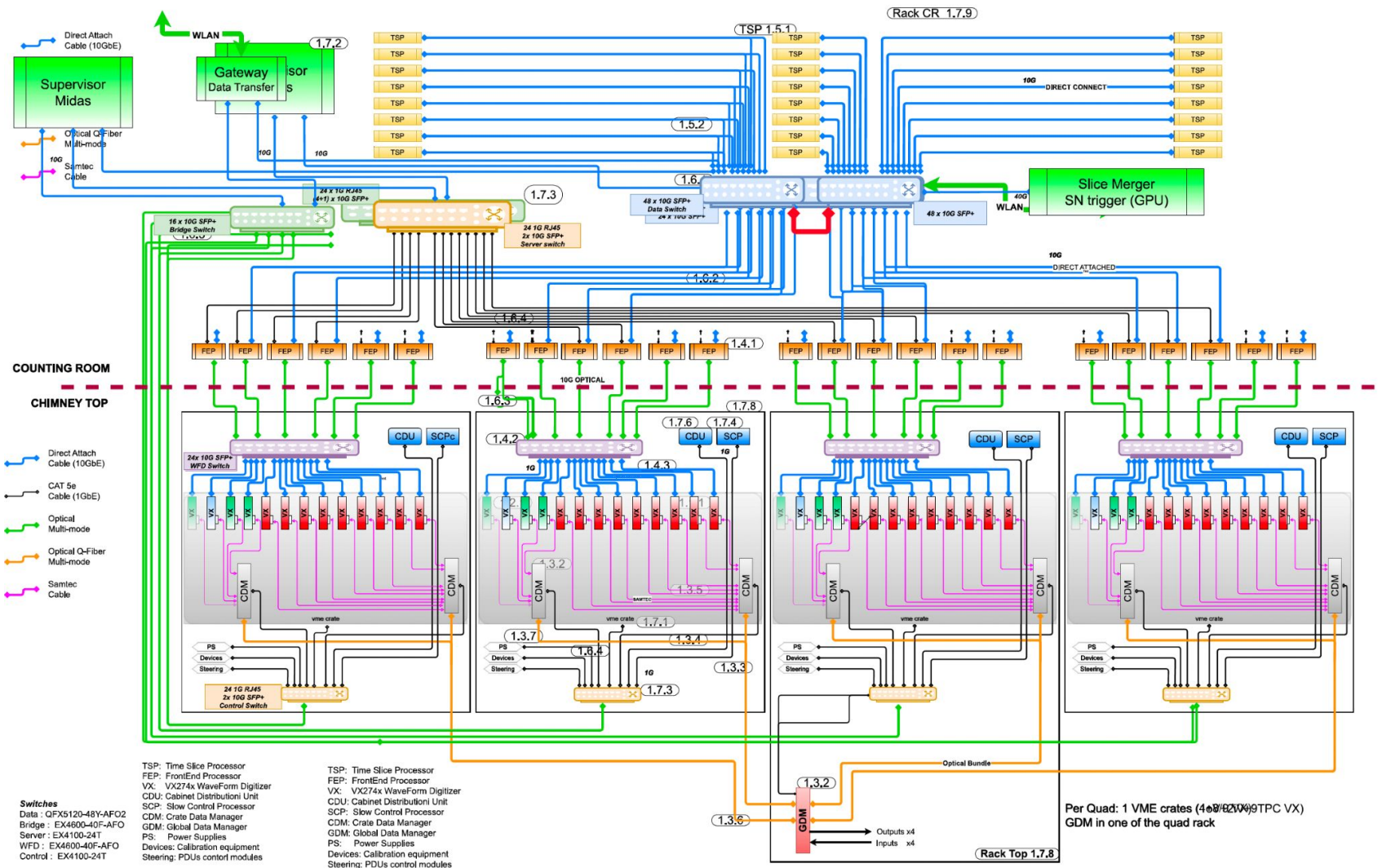
- Online analysis to be refined and tested
- Supernova trigger to be implemented
- DAQ chain and online analysis to be tested with data from DS-20k prototype, currently running at Università Federico II, Naples.

**THANK YOU FOR
YOUR ATTENTION!**

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Backup





COUNTING ROOM

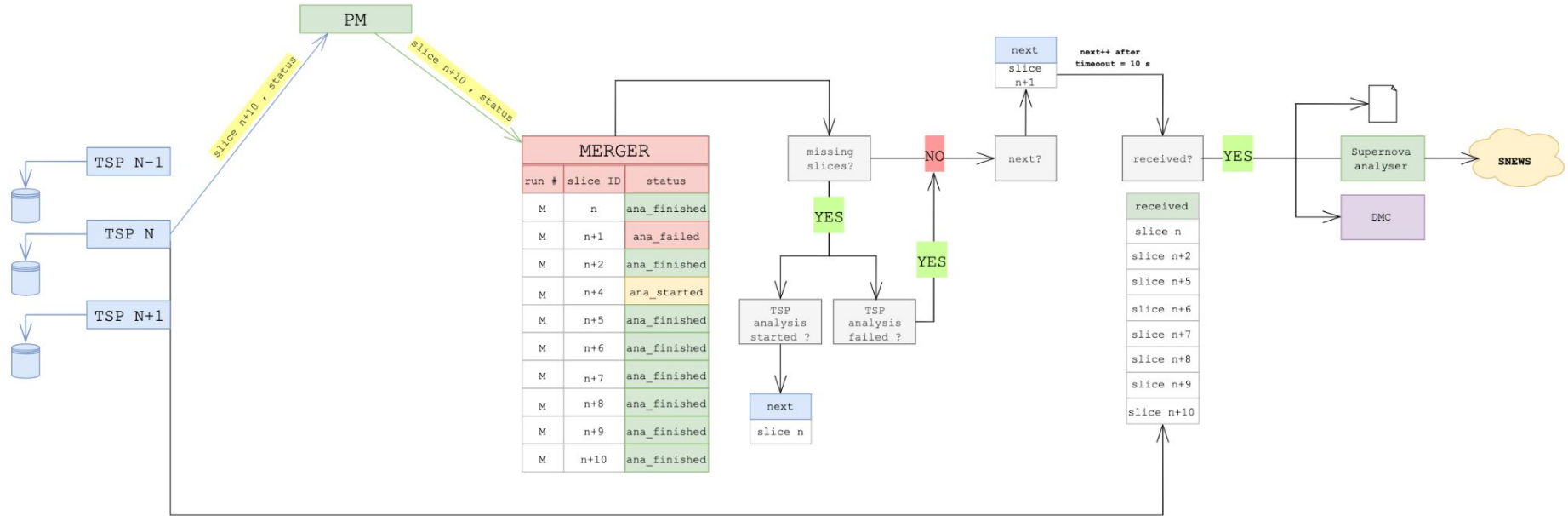
CHIMNEY TOP

- Direct Attach Cable (10GbE)
- CAT 5e Cable (1GbE)
- Optical Multi-mode
- Optical O-Fiber Multi-mode
- Samtec Cable

- | | |
|---------------------------------|---------------------------------|
| TSP: Time Slice Processor | TSP: Time Slice Processor |
| FEP: FrontEnd Processor | FEP: FrontEnd Processor |
| VX: VX274x WaveForm Digitizer | VX: VX274x WaveForm Digitizer |
| CDU: Cabinet Distribution Unit | CDU: Cabinet Distribution Unit |
| SCP: Slow Control Processor | SCP: Slow Control Processor |
| CDM: Crate Data Manager | CDM: Crate Data Manager |
| GDM: Global Data Manager | GDM: Global Data Manager |
| PS: Power Supplies | PS: Power Supplies |
| Devices: Calibration equipment | Devices: Calibration equipment |
| Steering: PDU's control modules | Steering: PDU's control modules |

Per Quad: 1 VME crates (4096/2048/9TPC VX)
GDM in one of the quad rack

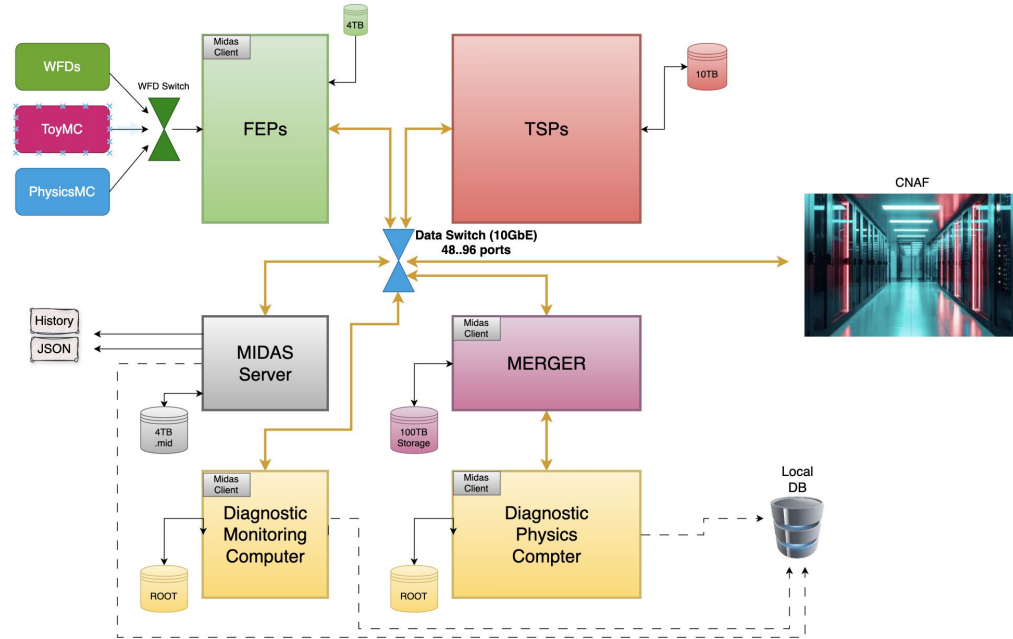
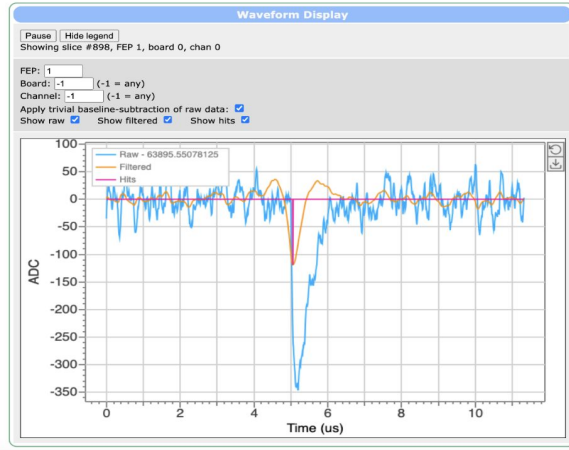
The merger



Monitoring system

3 groups of monitoring quantities:

1. per-channel monitoring: event variables such as fingerplots and hit rates, some expensive computations like noise FFTs, manual studies like individual waveforms visualization
2. detector-level monitoring: S1/S2 identification, energy spectra, pulse-level statistics
3. DAQ monitoring: transmission rates, buffer sizes, CPU usages



BUSY logic simulation: motivation

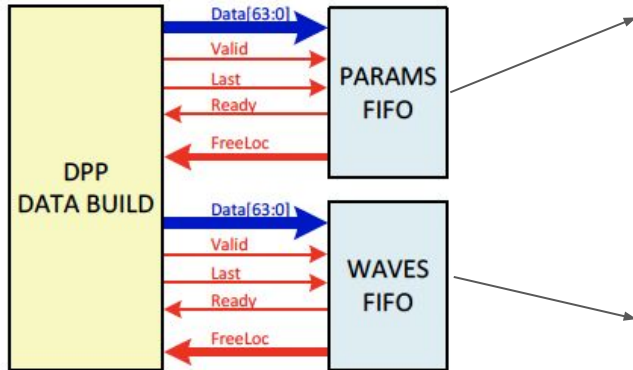
- Triggerless mode for maximum flexibility but event bursts can introduce dead time (DAQ BUSY)
 - multiple scattering events from gamma radioactivity
 - large pulses
- The goal of the effort is to simulate the BUSY mode of the digitisers (Vx2745, 16 bit) and evaluate impact on detector exposure
- The idea is to simulate a pattern of waveforms for each channel (64) and emulate the transfer logic within the module
- Compute the buffer level for each channel waiting to be transferred and track its evolution as a function of time

BUSY logic

Firmware



2 FIFO buffers per channel (either TPC or Veto):



- contains the metadata (channel, custom info, timestamp, user info, waveform size in samples ...)
 - maximum depth = 512 words (1 word = 64 bits)
 - every channel has 4 words → 128 words/ch
 - highly unlikely to be filled up
-
- contains the actual data (header plus waveforms).
 - maximum depth = 4095 words (16380 samples)
 - more likely to be filled up

BUSY logic

Firmware

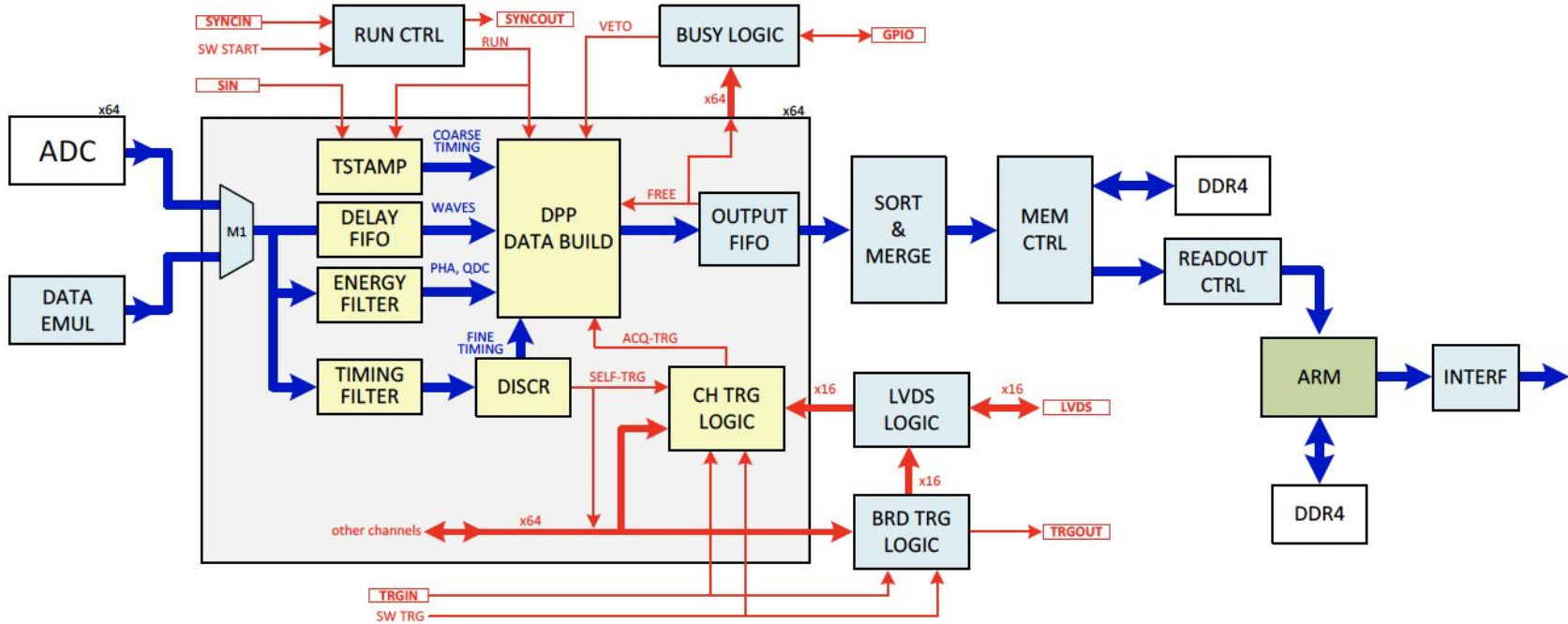
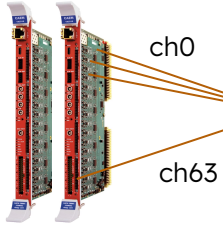


Fig. 3.1: Block Diagram of the DDP firmware

BUSY logic

Firmware

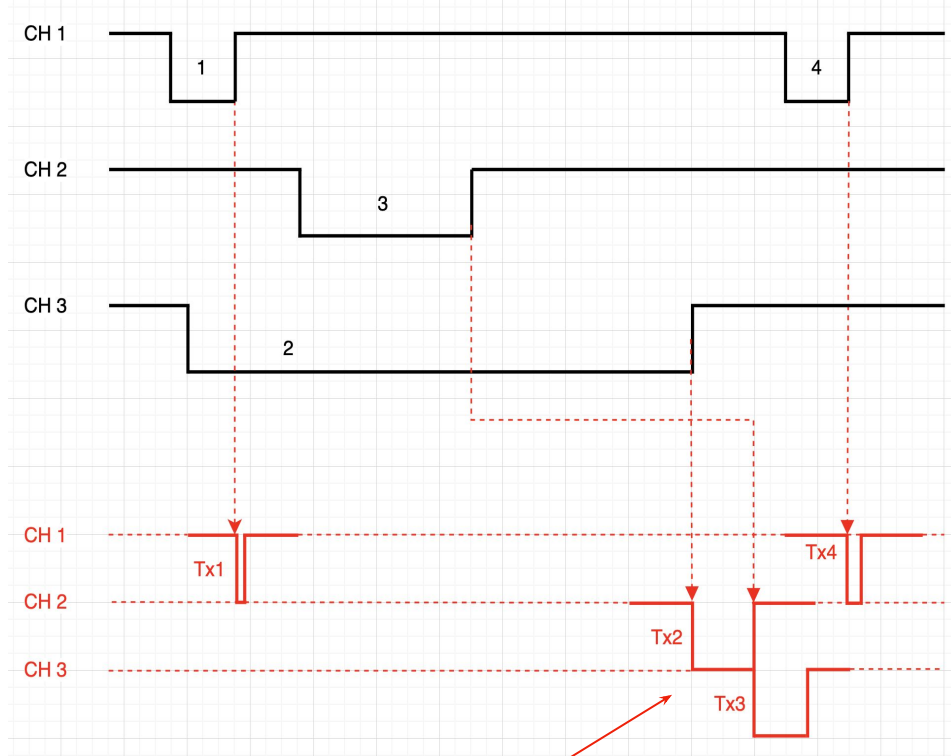


Time sorting + merging buffer

64 channels/module merged in the same buffer where they are sorted in time

— = Input

— = Transmission (Tx) output
FIFO to sorting buffer



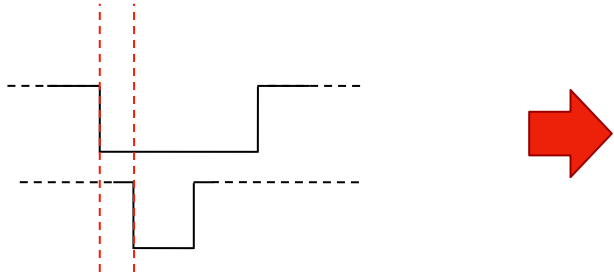
The readout is **16 bits per 8 ns**

The Tx to the sorting is 64 bits per 4 ns = **8x faster than the readout**

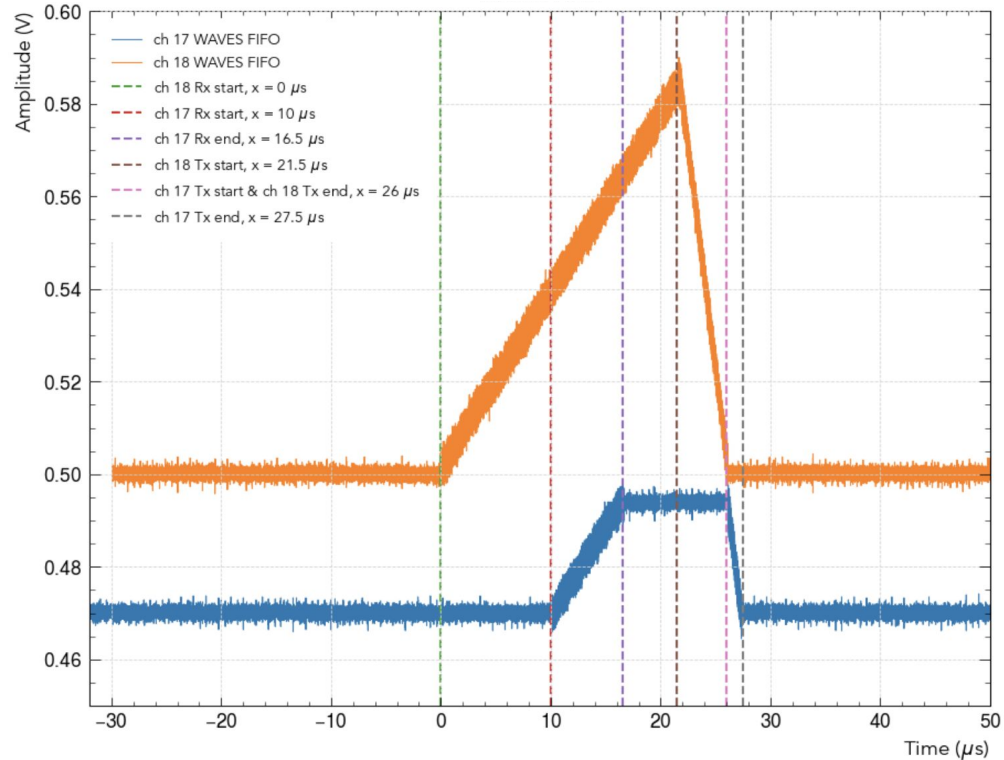
“Ladder” trend expected due to time sorting

BUSY logic

Simulation vs data comparison

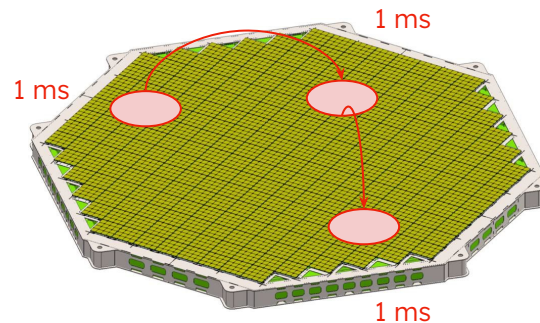


- Same waveform pattern can be fed into the digitizers
- Buffer level of each channel can be read out from the front panel and fed into an oscilloscope
- The firmware implementation also allows for the most occupied channel buffer to be retrieved



BUSY logic Simulation

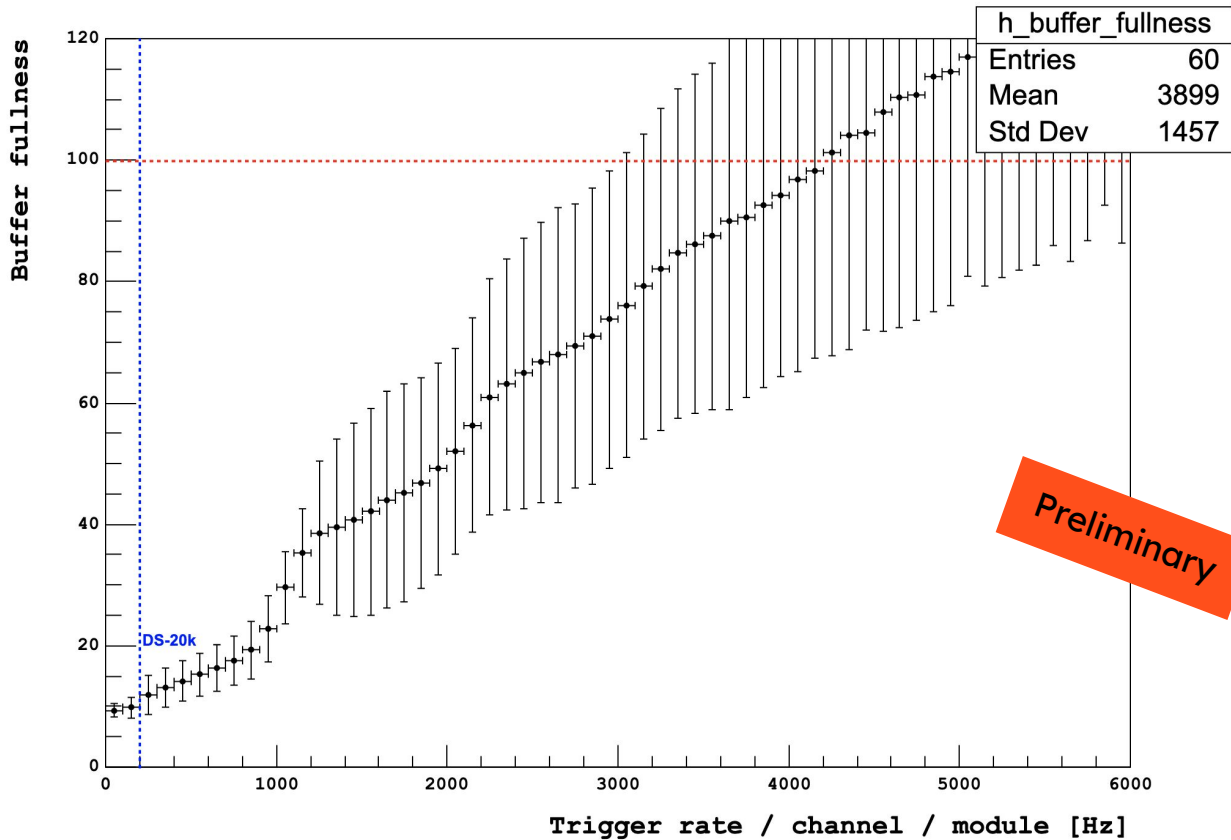
- Input: time slices from the full background simulation from the Event Mixer
- Output: buffer occupancy as a function of time
- Simulation details:
 - 1 s time slice split into 1ms blocks for faster processing
 - for each ms select a random channel in the TPC and build an ADC out of it by taking the 64 channels surrounding this channel (full sampling of the whole TPC)
 - for each ms, retrieve the waveform (ToT) pattern over time and feed it into the busy logic simulation



BUSY logic

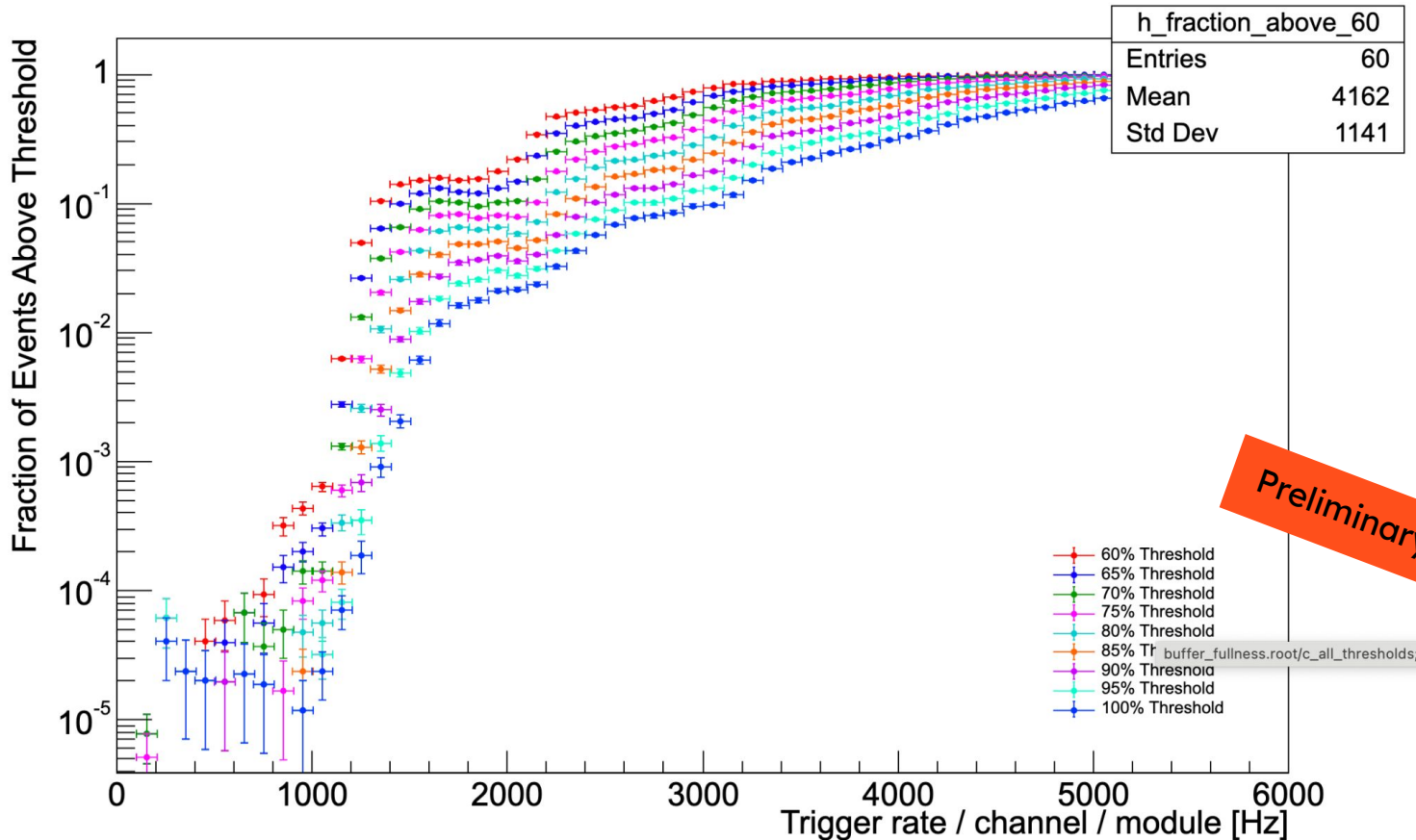
Results

Not an issue for standard events but the tails of the distribution might be problematic



BUSY logic

Results



BUSY logic

Fraction per module



Fraction of events above threshold as a function of the threshold within a single module

Worst case scenario without any mitigation

