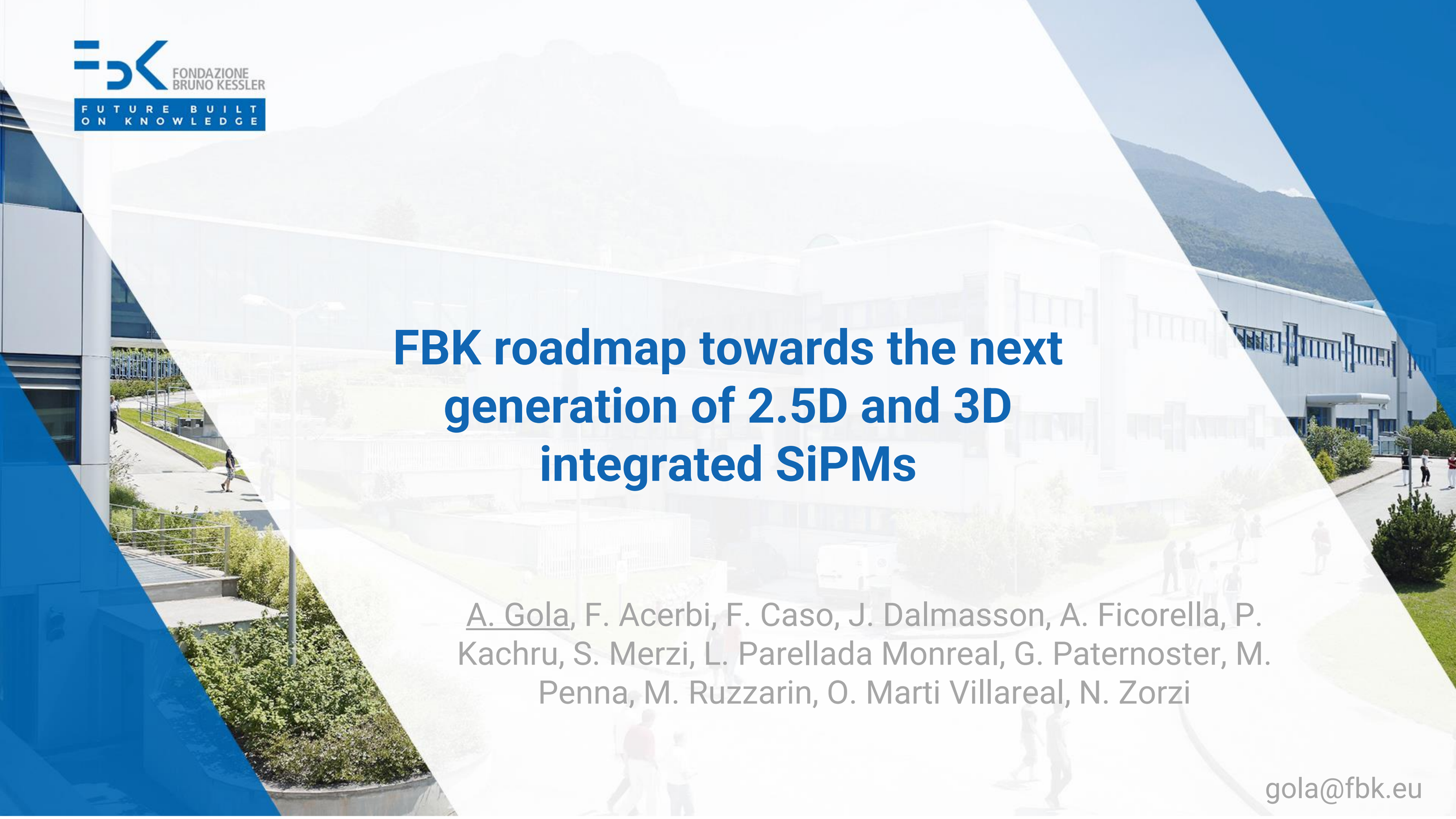


FBK roadmap towards the next generation of 2.5D and 3D integrated SiPMs

A. Gola, F. Acerbi, F. Caso, J. Dalmasson, A. Ficorella, P. Kachru, S. Merzi, L. Parellada Monreal, G. Paternoster, M. Penna, M. Ruzzarin, O. Marti Villareal, N. Zorzi

gola@fbk.eu

Outline

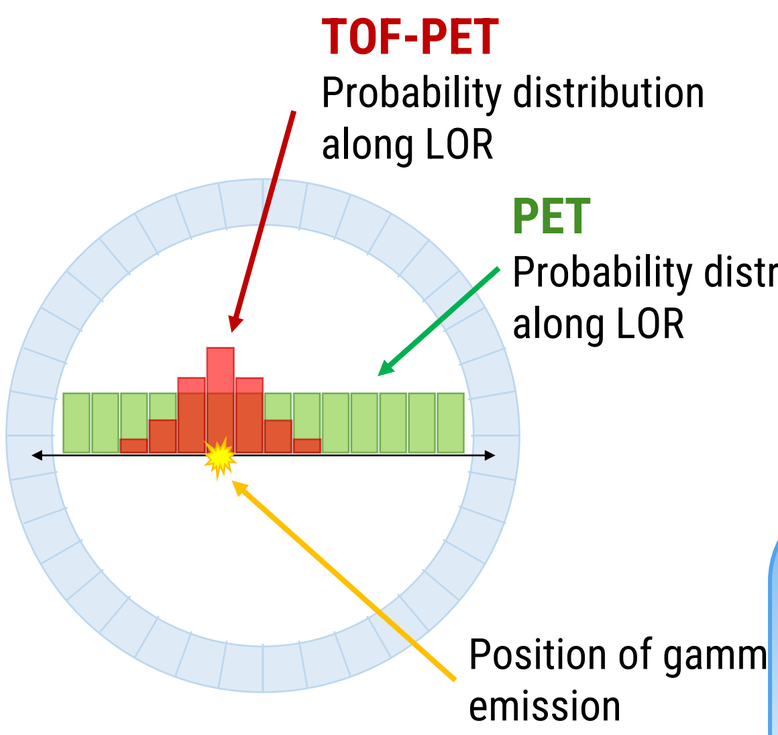
- Motivation to develop Hybrid SiPMs / SPAD arrays
- 2.5D and 3D integration activities on SPADs / SiPMs at FBK
- NUV-BSI Update
- Perspectives

Motivation to develop Hybrid SiPMs / SPAD arrays

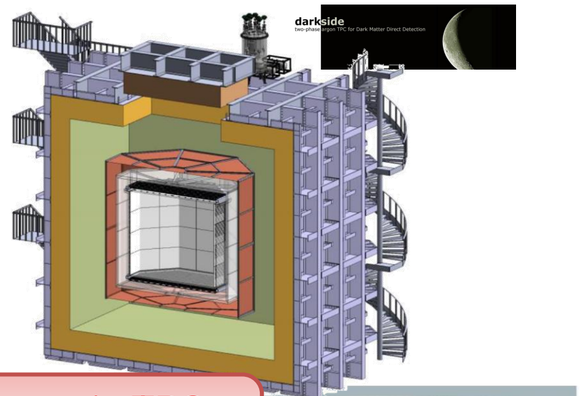
FBK SiPM technologies
Typical Applications

The traditional application of SiPMs is the ToF-PET. In addition, thanks to the *constant improvement of SiPM performance*, they are being evaluated in the *upgrade of several Big Physics Experiments*.

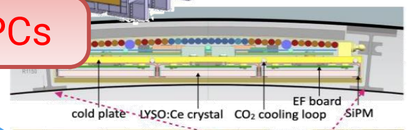
Positron Emission Tomography

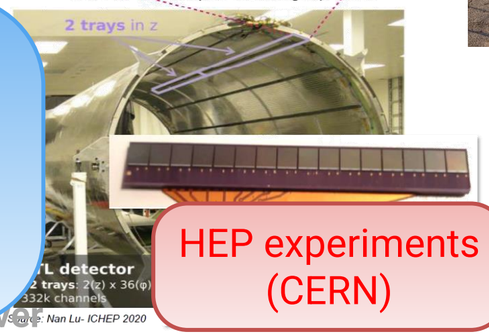


Big Physics Experiments



Cryogenic TPCs





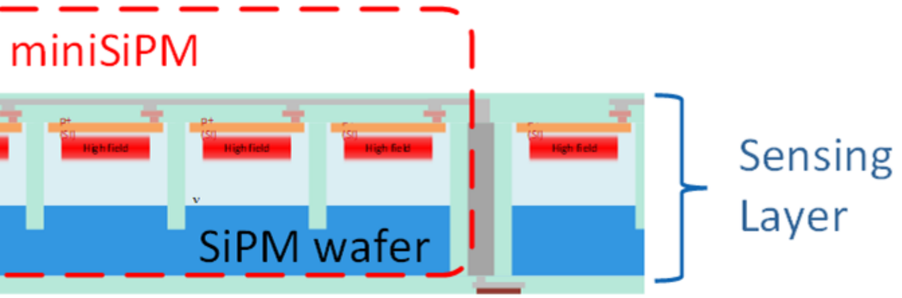
HEP experiments (CERN)

Astrophysics and space

Examples of Big Physics experiments FBK is currently working on.

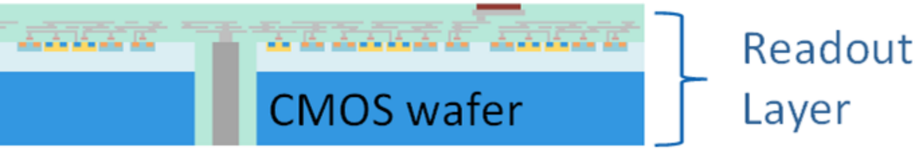
Technology customization is almost mandatory!

Why Hybrid SiPMs?
Advantages of separated sensing and readout layers



***Custom SiPM technology* for sensing layer**:

- CMOS-compatible → transfer to *large-volume foundries* is possible
- ~10 lithographic masks → *Lower cost per unit area* compared to full CMOS process (> 40 masks)
- Customized fabrication process, no constraint form transistor fabrication → *best electro-optical performance possible*, also after irradiation (e.g. DCR, DCR vs.T, PDE, correlated noise, etc..)
- *Cheap to iterate / adjust the design* → Different sensing layers for different applications, room for subsequent upgrades without changing readout ASIC
- All the wafer area is sensitive to light → *maximum detection efficiency* (PDE)



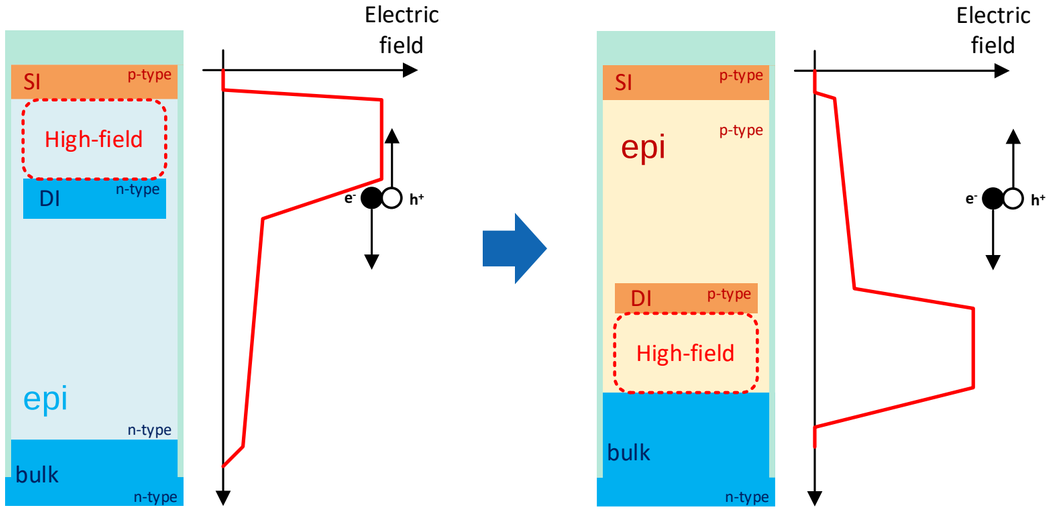
***CMOS technology* for readout layer**:

- *Free choice of CMOS node* → optimal performance of readout.
- *CMOS area can be smaller than sensing area* (2.5D) → lower cost
- *Independent design cycles* of sensing layer and readout layer → more efficient R&D phase

Customized sensing layer
NUV-DJ development

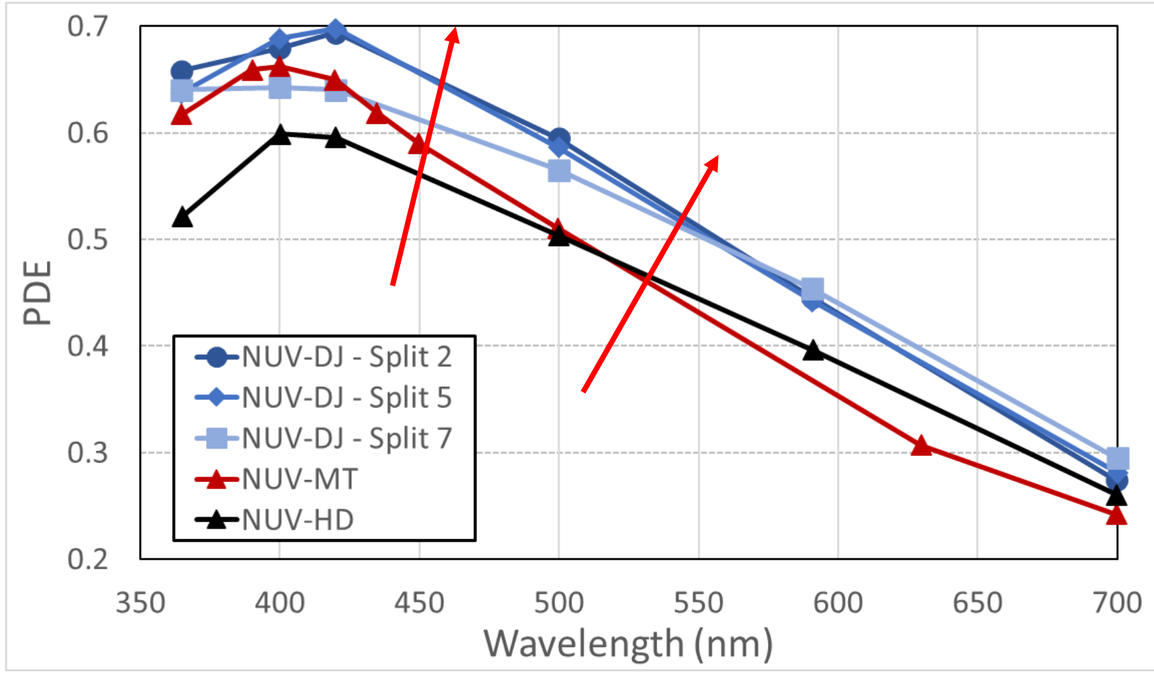
By *moving the high-field region towards the bottom of the epitaxial layer*, the PDE is enhanced.

Avalanche is mostly *triggered by electrons.*



Conceptual drawing of the different NUV.MT and NUV-DJ microcell structures (cross-sections, not to scale)

PDE increase: from holes to electrons triggering the avalanche



PDE vs. wavelength measured on the 45 µm cell of the NUV-HD-MT technology (12 V) and on the 40 µm cell of the NUV-HD and of the newly introduced NUV-DJ SiPM technologies (9 V).

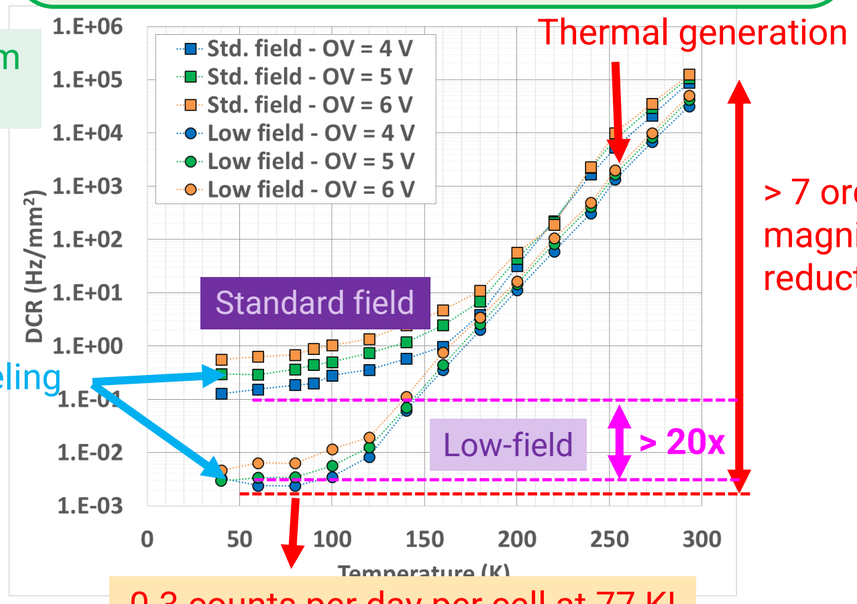
Results presented at NSS2024:
N-05-03 presentation

Customized sensing layer
Cryogenic and VUV-sensitive SiPMs

NUV-HD-Cryo SiPM technology is an *enabling technology for the DarkSide-20k* experiment, currently under construction.

Exceptionally low DCR is achieved thanks to custom technology development

25 um cell

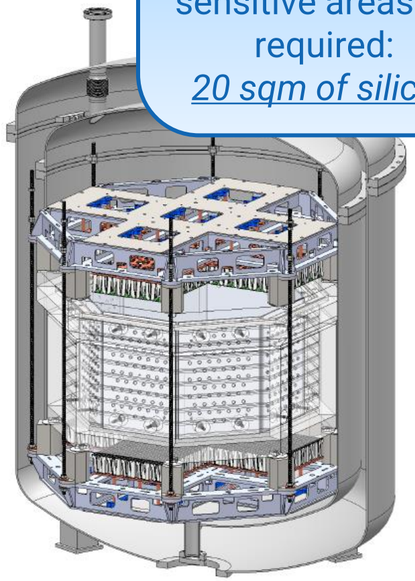


0.3 counts per day per cell at 77 K!

A 10x10 cm² SiPM array would have a total DCR < 100 cps!

Reduction of Dark Count Rate at cryogenic temperature thanks to electric field engineering in FBK SiPMs.

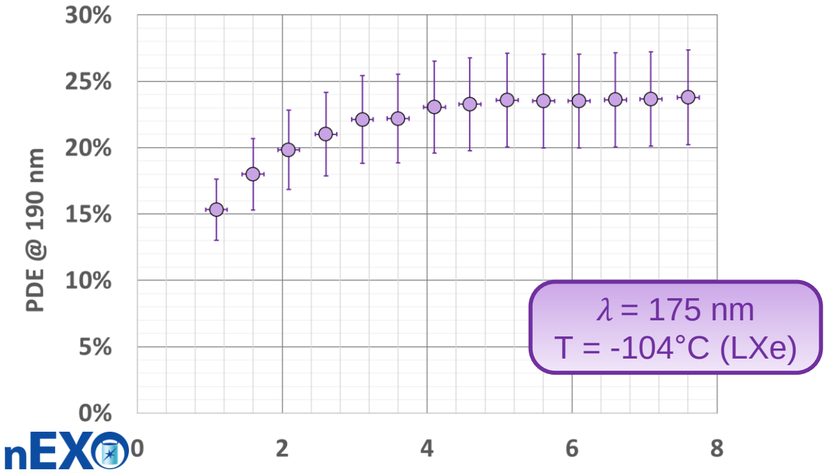
Usually, large light-sensitive areas are required:
20 sqm of silicon

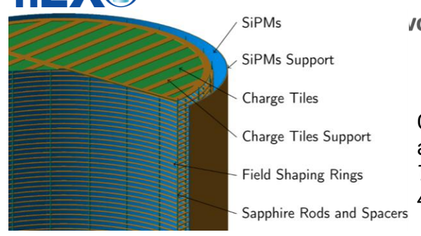


Darkside-20k experiment under construction at LNGS using FBK SiPMs fabricated at Lfoundry: *20 m² of SiPMs* operated at 87 K.

Acerbi, Fabio, et al. "Cryogenic characterization of FBK HD near-UV sensitive SiPMs." *IEEE Transactions on Electron Devices* 64.2 (2017): 521-526.

VUV sensitivity for direct detection of Lxe scintillation light, Timing with BaF2, etc..



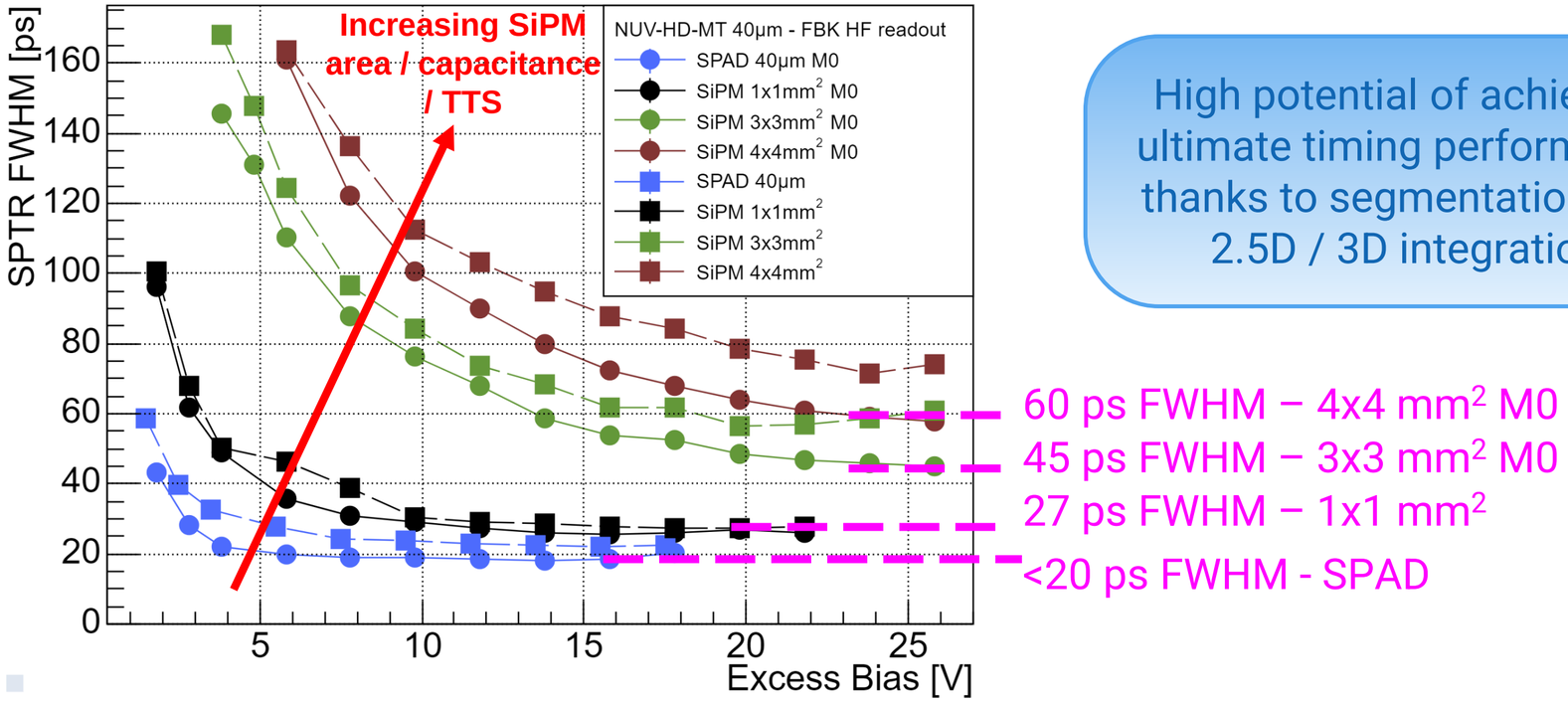


Gallina, G., et al. "Characterization of SiPM avalanche triggering probabilities." *IEEE Transactions on Electron Devices* 66.10 (2019): 4228-4234.

Segmentation of SiPM Active Area
Effect of SiPM area on SPTR

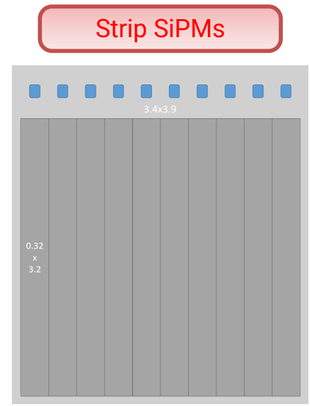
SPTR and CTR *performance is degraded* when reading out SiPMs with large areas, mainly *because of SiPM large output capacitance, of poor signal extraction and of SiPM transit time Spread* (TTS).

With larger SiPMs, the SPTR can be preserved by *segmenting the active area into smaller pixels, or miniSiPMs, with separate 2.5D / 3D connection to readout*, followed by suitable combination of time pick-off information.



SPTR vs. excess bias for NUV-HD-MT 1x1 mm² SiPMs and SPADs, featuring a *layout optimized for timing and using a high-frequency amplifier*.

High potential of achieving ultimate timing performance thanks to segmentation and 2.5D / 3D integration



10 strips 0.32 x 3.2 mm² each, no dead border between strips

Results presented at NSS2024: N-05-04 presentation

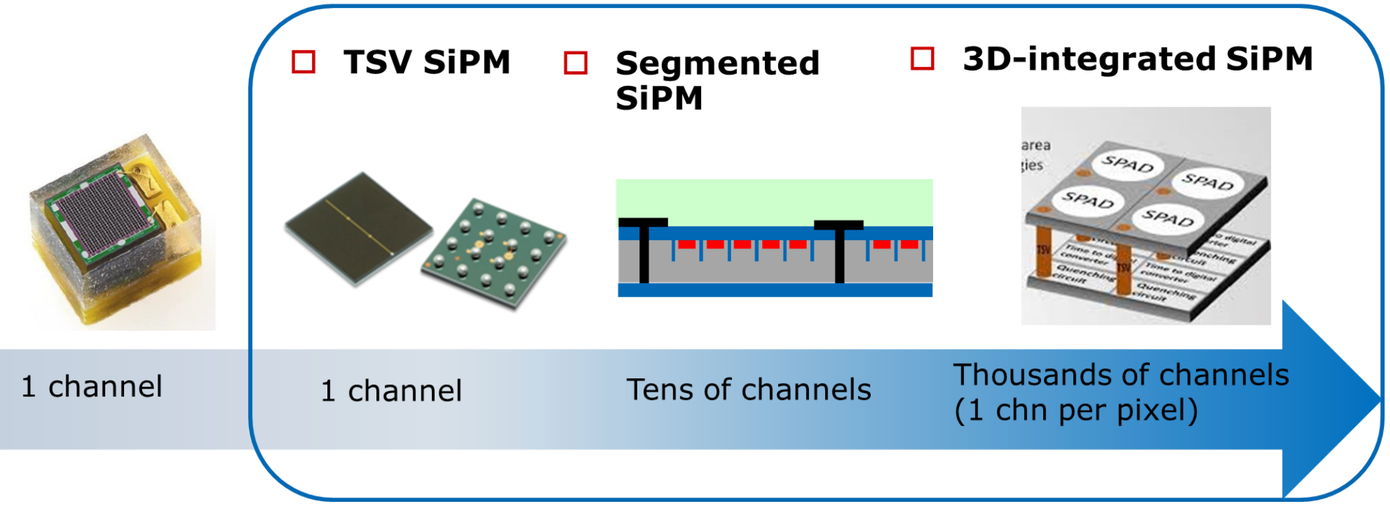
2.5D and 3D integrated SiPMs / SPADs at FBK

2.5D and 3D Integration
FBK IPCEI clean-room upgrade

FBK is part of the *IPCEI on microelectronics* project (Important Project of Common European Interest - €1.75 billion total public support, 12 M€ to FBK).

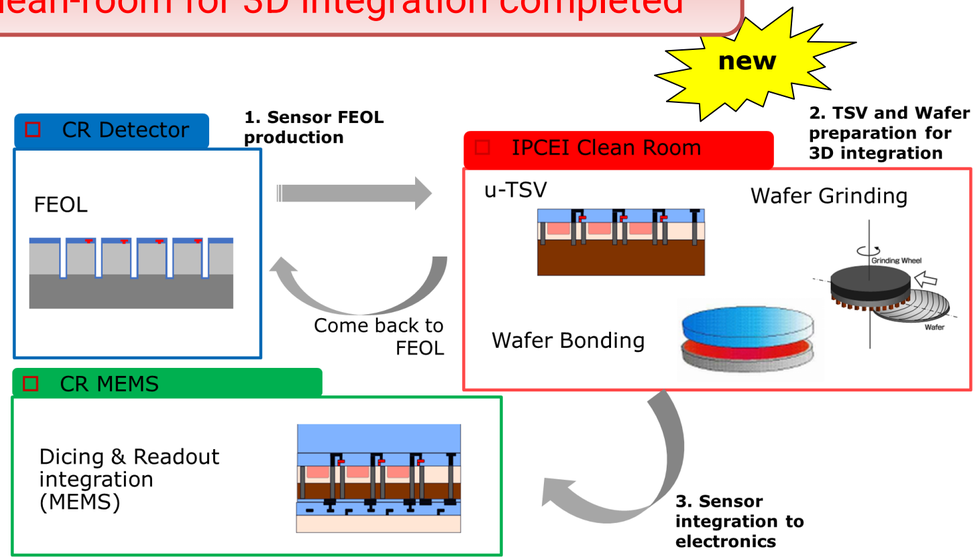
The goal for FBK is upgrading its optical sensors technologies, by *developing TSVs, micro-TSV and Backside Illuminated SiPMs*. This will allow high-density interconnections to the front-end and high-segmentation.

Customized TSVs will be optimized to preserve the NUV-HD electro optical and timing performance.



Range of technologies being developed within IPCEI

New clean-room for 3D integration completed

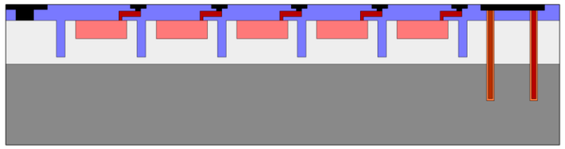


The complete system composed of 3 research clean-rooms in FBK.

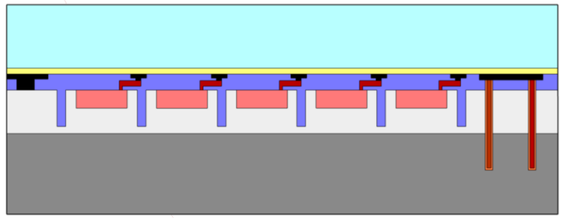
2.5D and 3D Integration
TSV – via mid: process flow

In the via-mid process, the *TSV is formed during the fabrication of the SiPM, modifying its process flow*.
In the via, the *conductor is the highly-doped silicon bulk*.

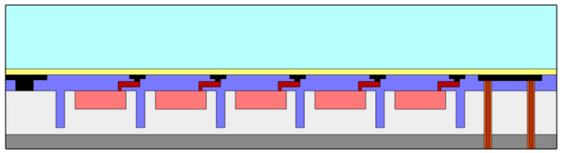
- SiPM fabrication + TSV formation



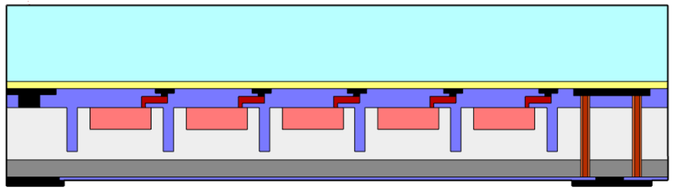
- Edge Trimming + BONDING



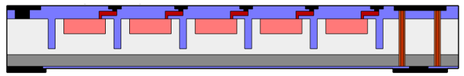
- THINNING



- Contacts formation



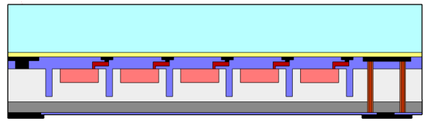
- DEBONDING



Thickness at least 150 um

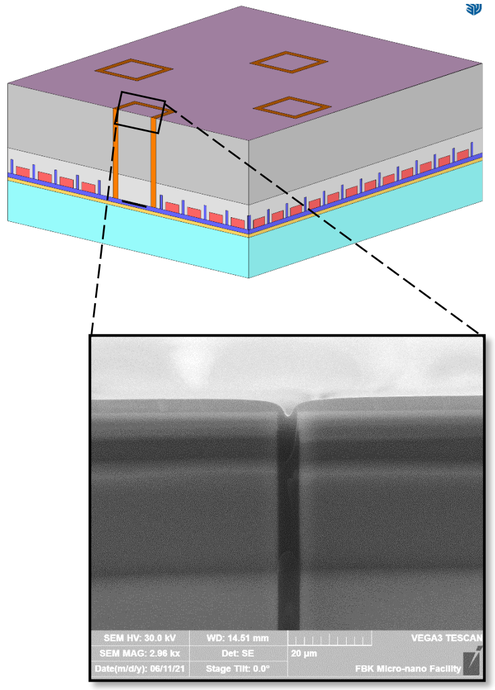
Glass-less TSV
concept
500 um SiPM pitch

- NO-DEBONDING



Thickness 10-50 um

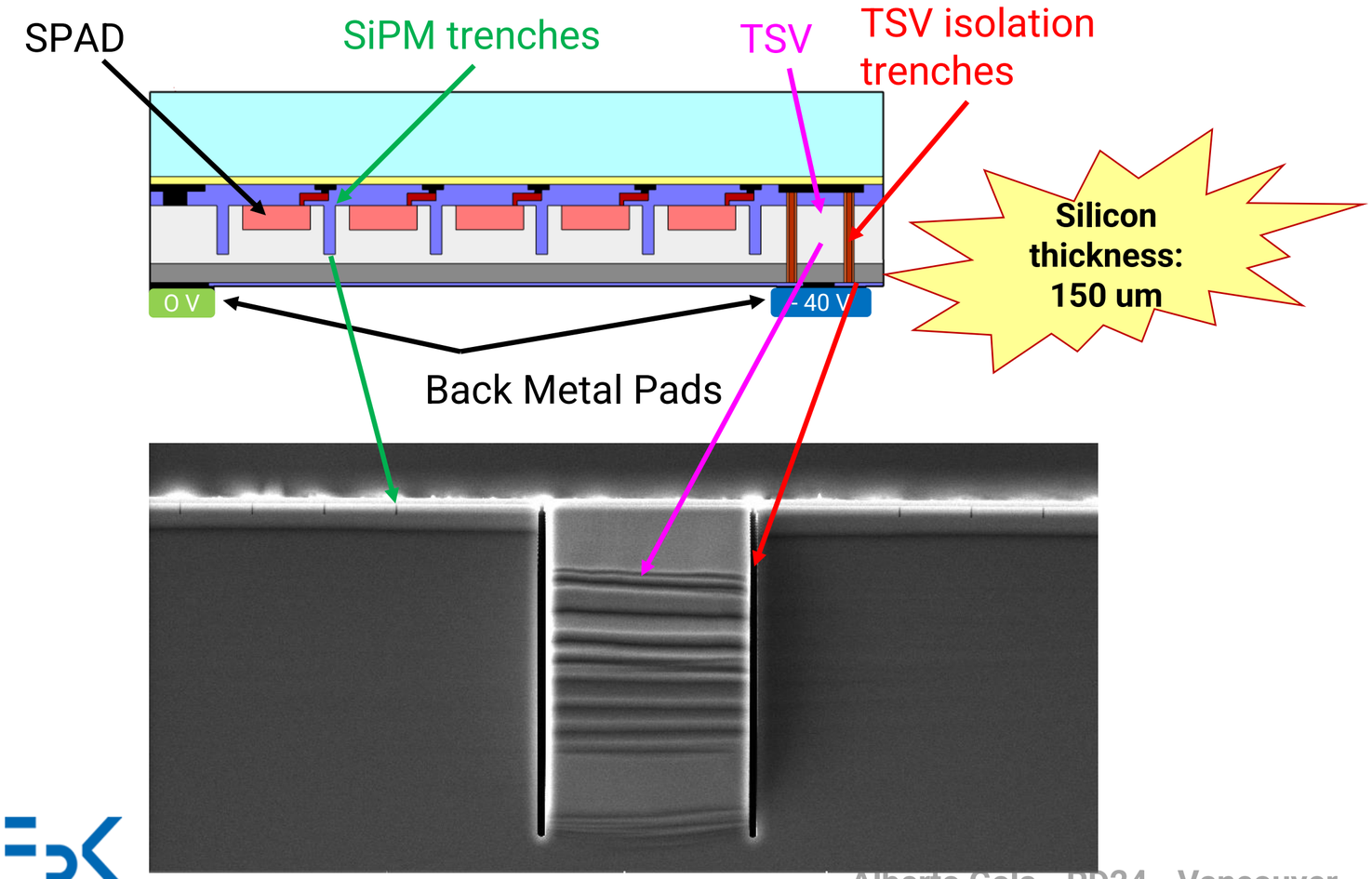
Standard TSV
microTSV
< 50 um SPAD pitch



- Metal-free TSV
- Flexible TSV layout and size
- Low bulk resistivity

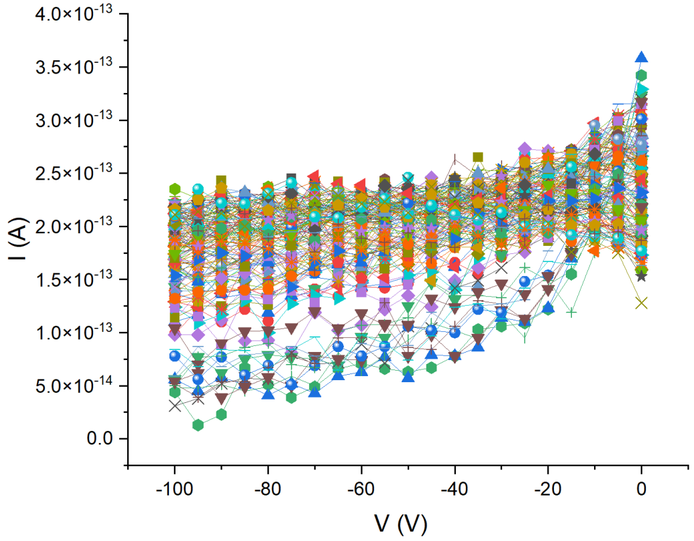
2.5D and 3D Integration
TSV – via mid: first results

Preliminary results on TSV via-mid development, with partial SiPM process, to *check isolation and continuity* (no Geiger-mode multiplication).



At **-100 V** of bias applied the intensity varies from **30 to 200 fA**

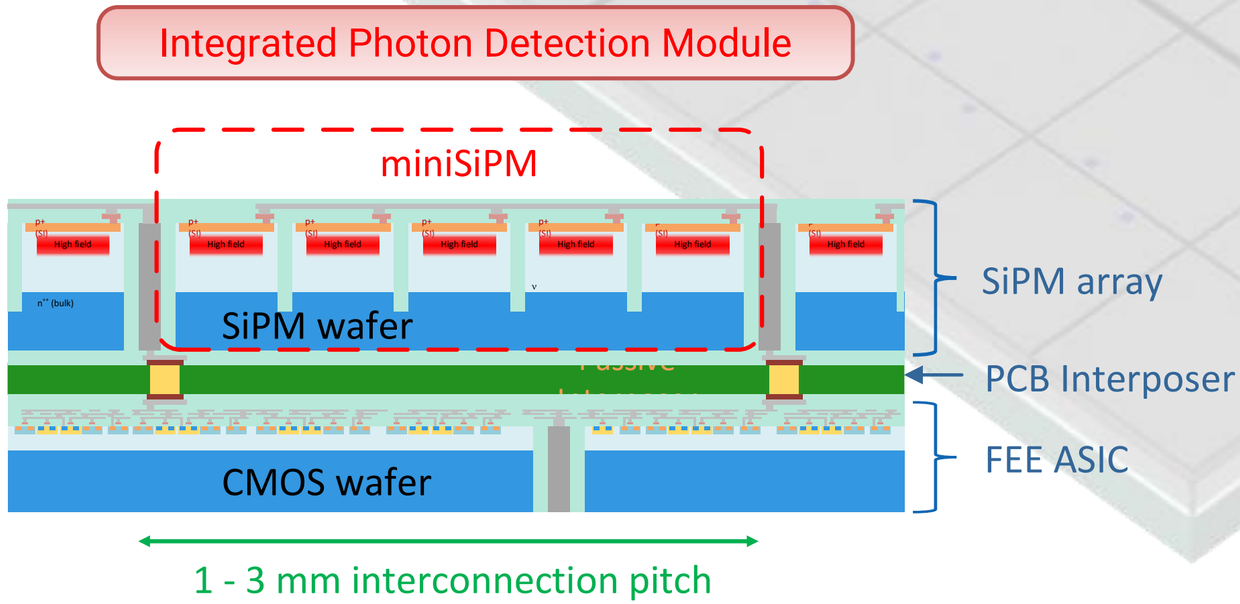
Trough Silicon Vias – Via Mid are isolated from the bulk silicon contact



2.5D and 3D Integration
2.5D integrated SiPM tile

In the *short and medium term*, medium density interconnection seems the sweet spot to obtain *excellent performance (e.g. timing) on large photosensitive areas while not increasing complexity and cost too much*.

We propose a Photon Detection Module (PDM) in which *SiPMs with TSVs down to 1 mm pitch* are connected to the *readout ASIC on the opposite side of a passive interposer*, in a *2.5D integration scheme*.



Core partners:

Jožef Stefan Institute

ICCUB Institut de Ciències del Cosmos

MASSACHUSETTS GENERAL HOSPITAL

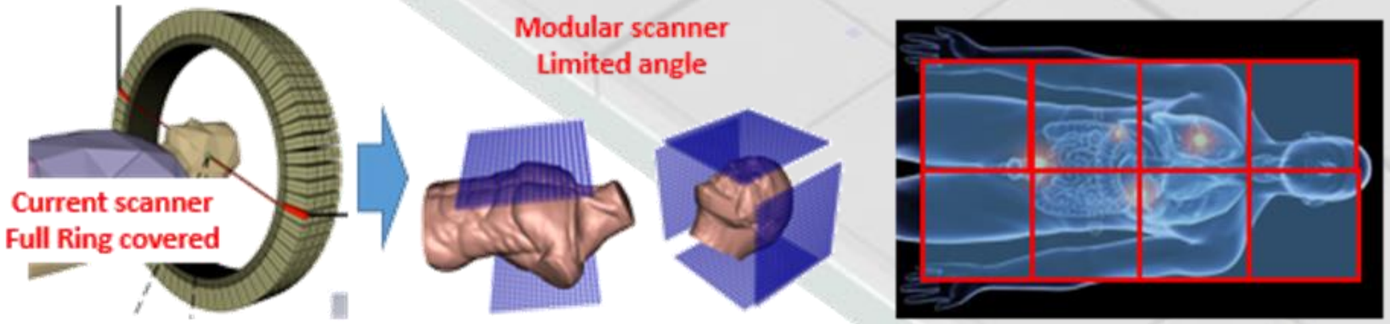
ONCO VISION

Hybrid SiPM module being developed for ultimate timing performance in ToF-PET

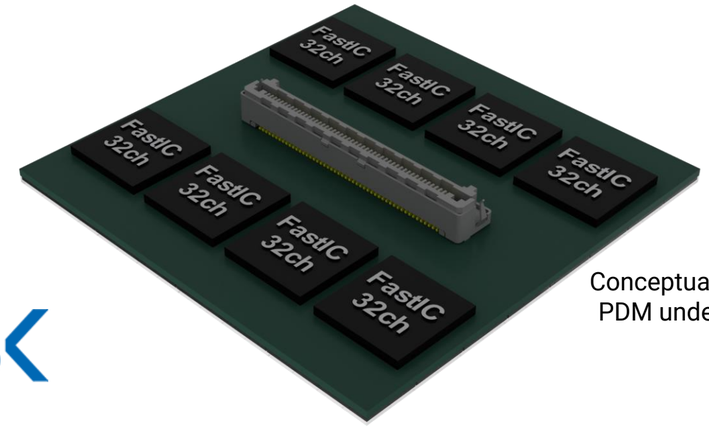
2.5D and 3D Integration
2.5D integrated SiPM tile for timing

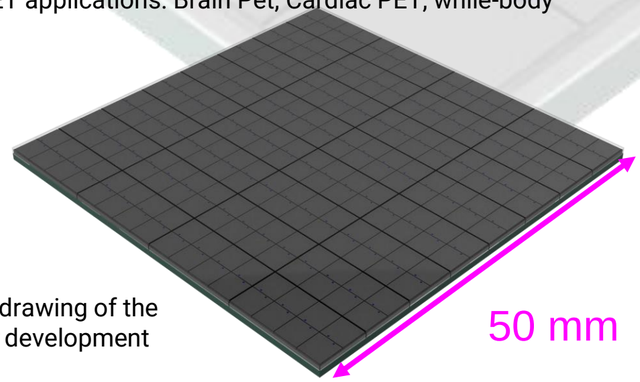
The 2.5D integrated PDM (50x50 mm^2) will be the basis of a *30x30 cm^2 ToF-PET panel*, which will be used to build limited-angle ToF-PET systems, for brain PET, Cardiac PET and full-body scanners.

We *expect very good timing performance*, supported by preliminary measurements achieved with NUV-HD SiPMs coupled to FastIC ASIC.

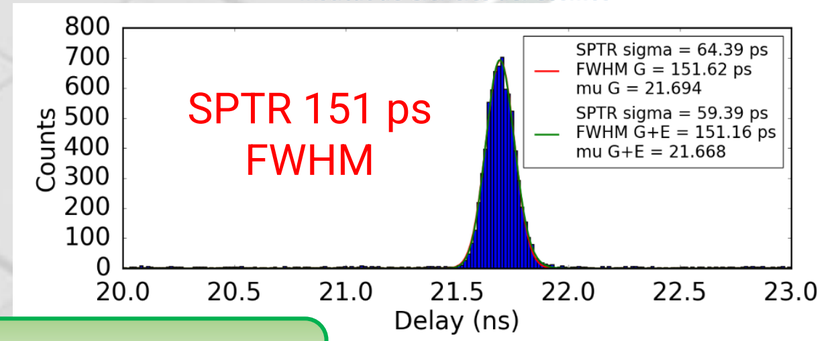


Application of the PDM to build large panes used in new, limted-angle PET applications: Brain Pet, Cardiac PET, while-body PET

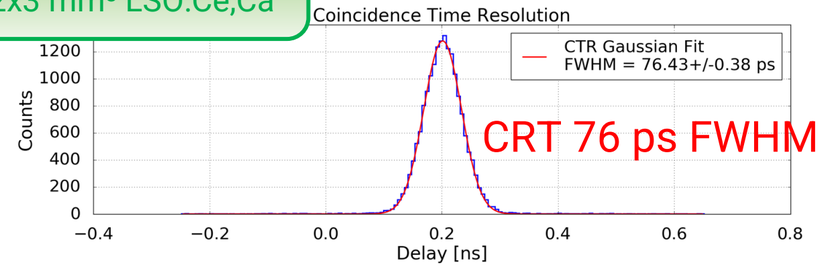




Conceptual drawing of the PDM under development



2x2x3 mm^3 LSO:Ce,Ca



SPTR and CRT measured at FBK NUV-HD-SiPMs read by the FastIC ASIC developed by ICCUB.
Sensor: NUV-HD-LFv2 SiPMs, 3x3 mm^2
Scintillator: 2x2x3 mm^3 LSO:Ce,Ca
Power consumption: 3 mW / channel

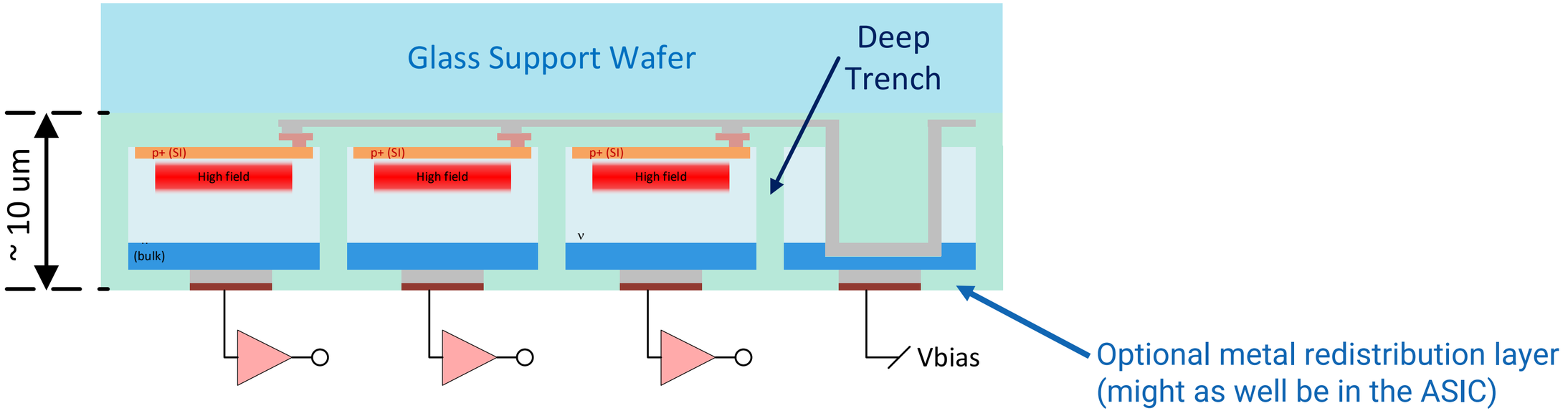
Single-SPAD TSV
Cross-section

Exploiting the Deep Trench Isolation, which is anyway present between adjacent SPADs in most SiPMs, we can achieve single SPAD isolation if we thin the wafer down sufficiently (use of a glass support wafer is needed).

We can exploit this isolation to *build a "bulk" TSV just below and coincident with each single SPAD*.

The *resistors* are still on the front-side (no change in signal shape is expected).

Common connection for bias is on the front and requires a TSV to bring it from the bottom.



Single-SPAD TSV
Advantages / Drawbacks

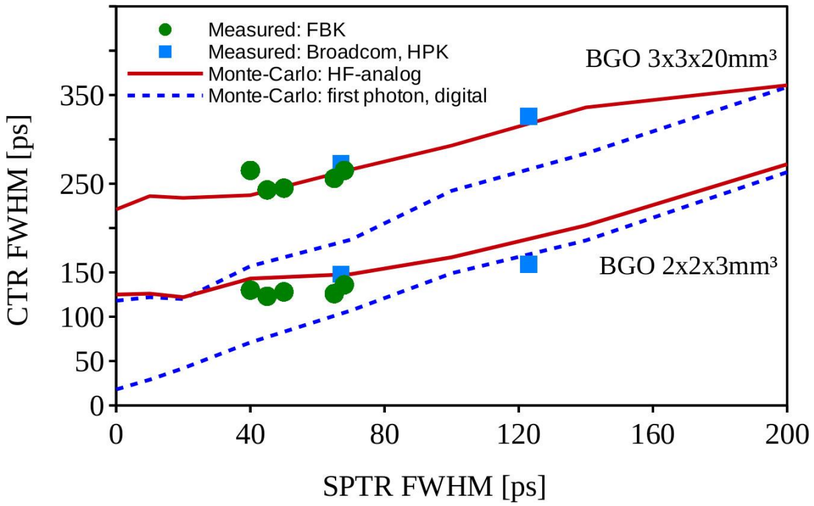
Advantages:

- (Almost) *no changes to the state-of-the-art, FSI, NUV-sensitive SiPMs* → conservative approach.
- It might be the only wat to have fine-pitch TSVs (around 50 um) with ***no loss of FF*** for the SiPMs.
- No additional trenches needed → simpler.
- Flexibility to have single-cell access, when needed, but also miniSiPMs and ***microSiPMs***, through *either a redistribution layer* on the SiPM backside or directly in the *3D integrated ASIC*
- *Connection for the topside metal* can be obtained through the same type of vias (possibly with epitaxial layer removal).

microSiPM
High-density integration: DIGILOG

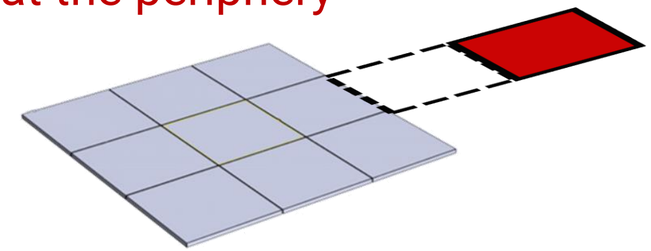
DIGILOG investigates higher density interconnections to *approach the dSiPM performance without the complexity of single-SPAD access*.

FBK will employ the Single-SPAD TSV to support the DIGILOG project, removing the need to replace the central SPAD in the uSiPMs with a TSV, thus achieving the *highest PDE possible*.

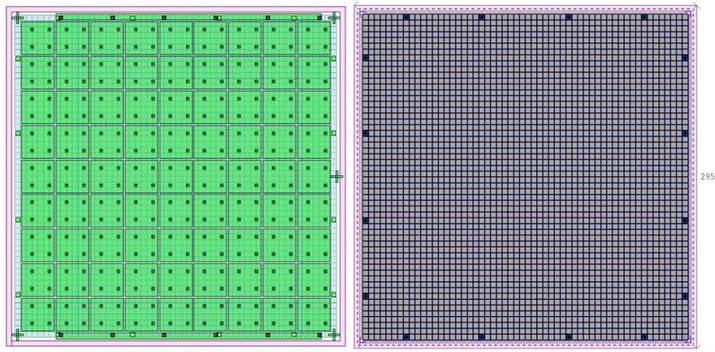


S. Gundacker, et al., A. Gola, E. Charbon, V. Schultz *NSS* 2023
S. Gundacker, et al., *to be published* 2023

SPAD size: 50x 50 µm^2
µSiPM: 3x3 or 6x6 microcells
µTSVs at the periphery



- µSiPMs with µTSVs
- µASICs with *in situ* TDCs

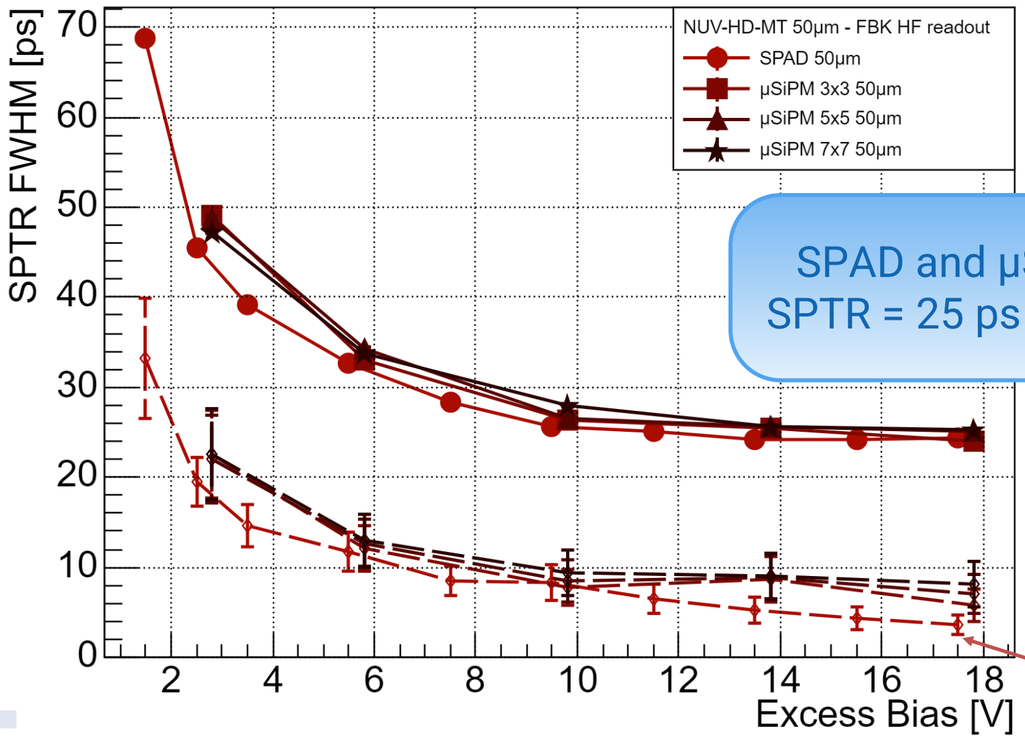


DIGILOG chip under fabrication at FBK:

- 3x3 mm^2, 50 µm cell, M0 layout
- Bias contacts at periphery
- 6x6-element µSiPM

microSiPM
Timing performance: SPTR with µSiPMs

Segmentation of the SiPM active area in *µSiPMs preserves the SPAD Single Photon Time Resolution*, when using the high-frequency readout (FBK implementation).



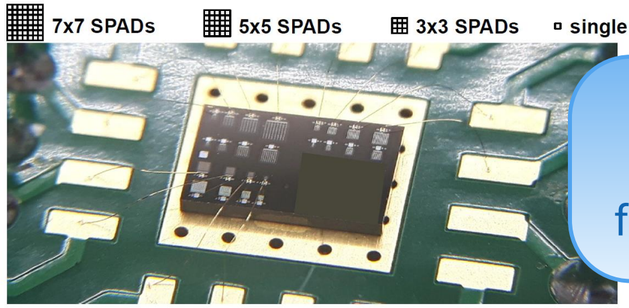
SPAD and µSiPM:
SPTR = 25 ps FWHM

(calculated) time jitter caused by the front-end electronic noise

SPTR measured on SPADs and µSiPMs, built with the NUV-MT FBK SiPM technology and featuring 50 µm microcell size and M0 layout, optimized for timing.

Additional challenges:

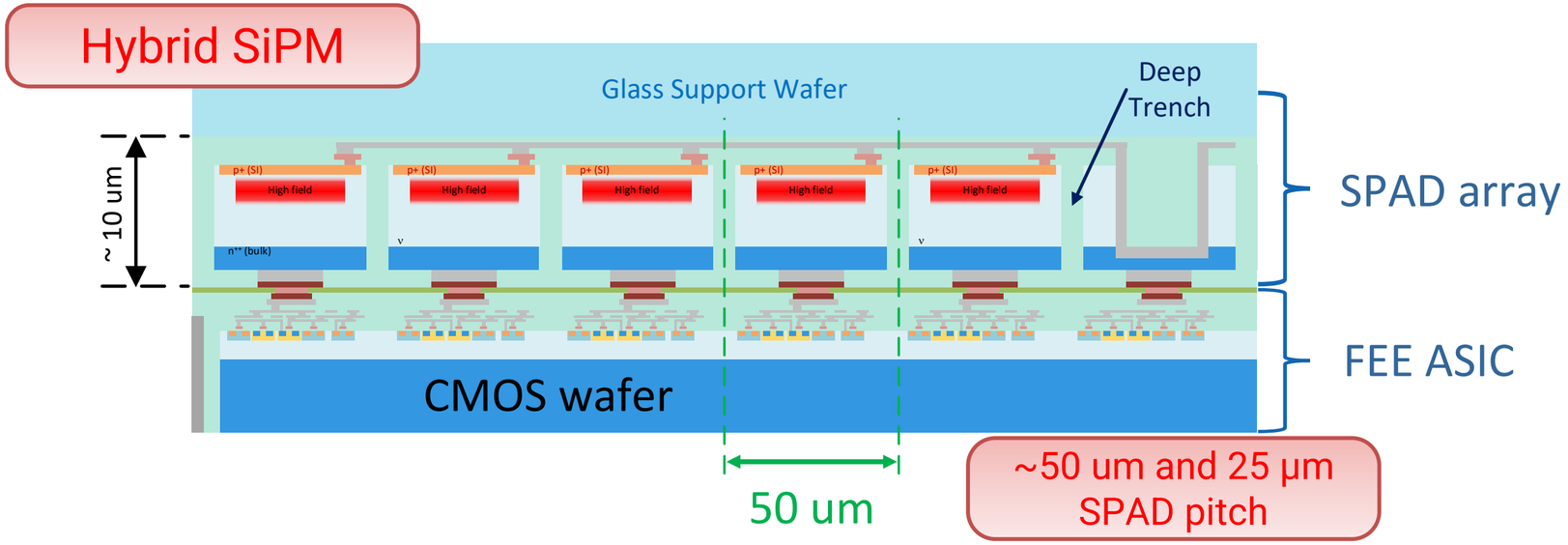
- Get the *same timing performance with ASIC readout*
- How to better exploit time information
- *3D integration to ASIC at 150 – 300 µm pitch*, less complex than with fully digital approach.

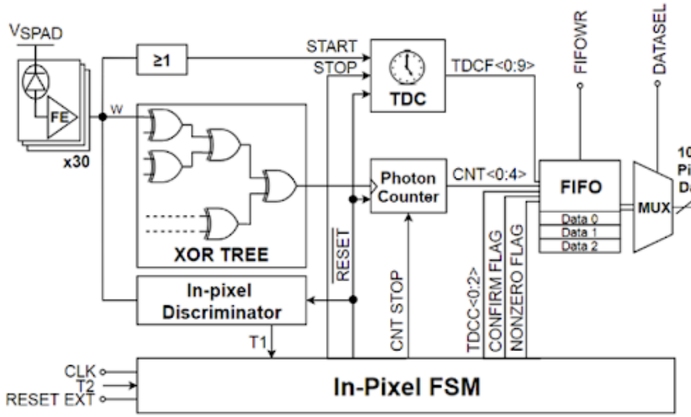


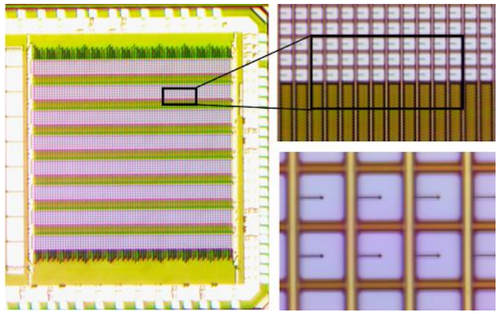
µSiPM test structures fabricated by FBK

3D Integration
Full 3D integration with micro TSVs: Hybrid SiPM

FBK will also employ the single-SPAD TSV to achieve *single cell connection*. While complexity of the system increases, it might provide *ultimate timing performance*.







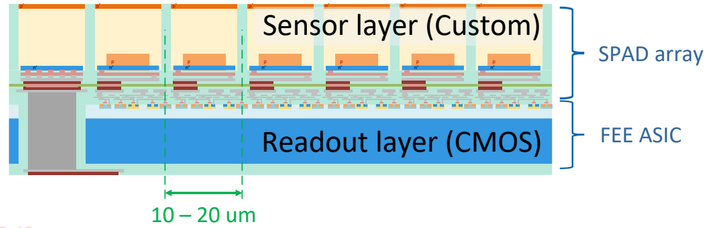
Example of dSiPM architecture developed at FBK (SBAM project)

- FBK can apply all the *know-how on system architecture* already developed in the filed of digital SiPMs.
- Finally solve the duality between analog and digital SiPM: *Hybrid SiPM concept*.

NUV-BSI SiPMs
Next-generation development: Backside Illuminated SiPMs

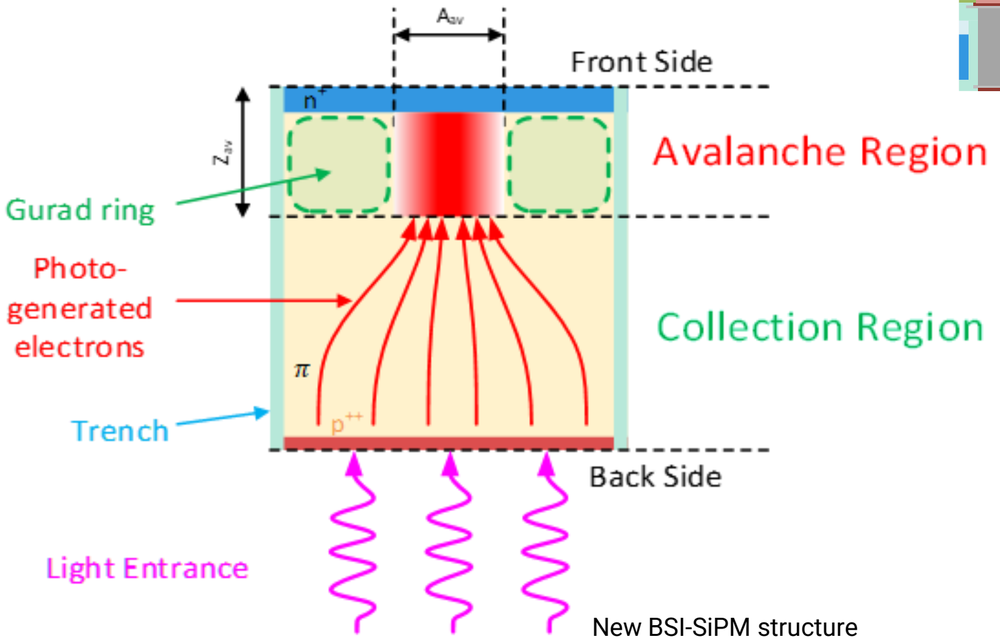
The next-generation of developments, currently being investigated at FBK, is building a *backside-illuminated, NUV-sensitive SiPM*. Several technological challenges should be overcome.

Clear *separation between charge collection and multiplication regions*.



Potential Advantages:

- Up to 100% FF even with small cell pitch
- Ultimate Interconnection density: < 15 um
- High speed and dynamic range
- Low gain and external crosstalk
- (Uniform) entrance window on the backside, ideal for enhanced optical stack (VUV sensitivity, nanophotonics)
- Local electronics: ultra fast and possibly low-power.



New BSI-SiPM structure

Development Risks:

- Charge collection time jitter
- Low Gain → SPTR?
- Effectiveness of the new entrance window

Radiation hardness:

- The SiPM area sensitive to radiation damage, is much smaller than the light sensitive area
- **Assumption**: the main source of DCR is field-enhanced generation (or tunneling).

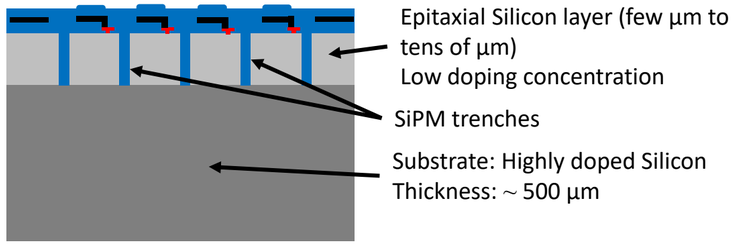
NUV-BSI Update

NUV-BSI SiPM technology
Backside process flow

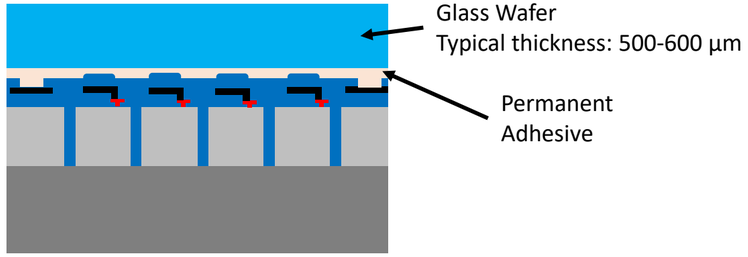
One of the most important challenges in the development of the NUV-BSI process flow is *achieving small total thickness variation (TTV)* after wafer thinning, to ensure *consistent SPAD performance across the wafer*.

TTV after chemical mechanical polishing is too high → *study of additional TTV reduction process*.

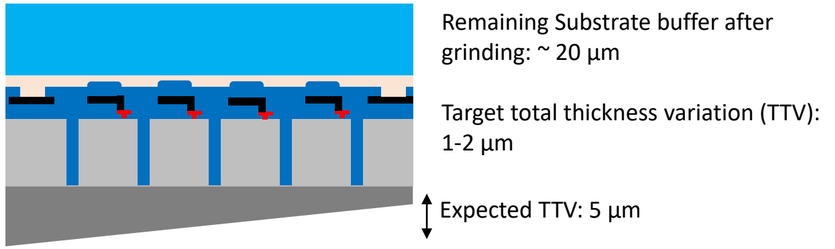
1. Starting Wafer (6”)



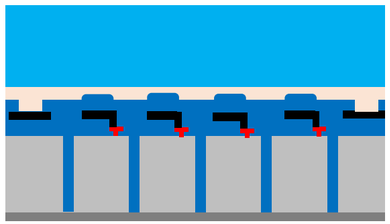
2. Adhesive Permanent Bonding to Glass Wafer



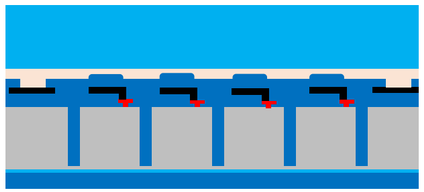
3. Wafer thinning (Substrate Removal)
Coarse + Fine grinding



4. TTV minimization step



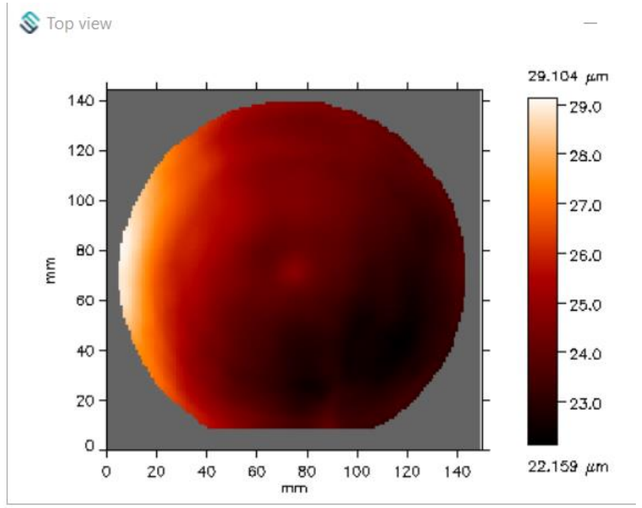
5. Back/surface passivation



NUV-BSI SiPM technology
Development of TTV reduction process

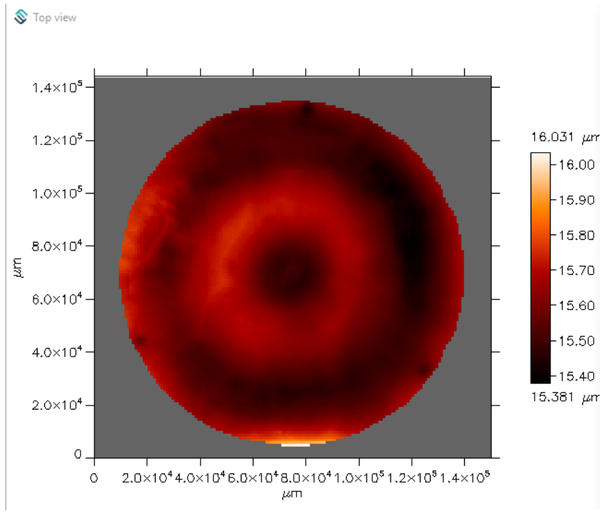
After optimization of recipes and procedures, *a TTV of less than 1 um was achieved*. *TCAD simulations confirmed that it is within the design specification for the NUV-BSI SPAD* structure.

Grinding



TTV = 7 um
(worst case)

Grinding + TTV reduction



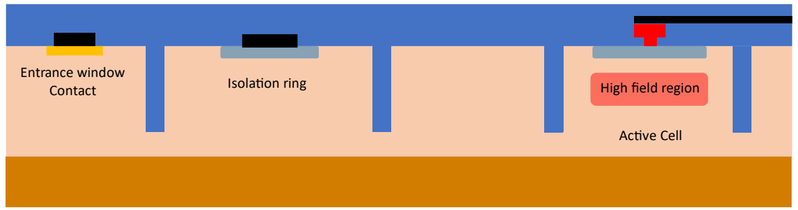
TTV = 0.8 um

Run IBIS#1 – First wafer-level characterization
Median IV Comparison IBIS run – Wafer#3

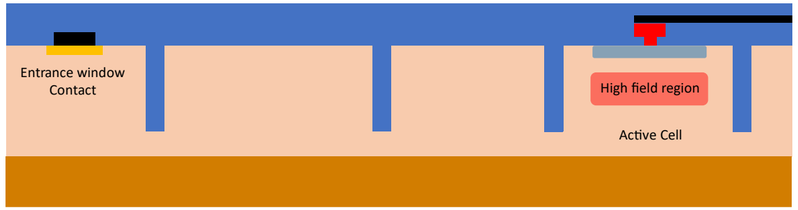
Preliminary

The run IBIS#1, supported by INFN, is being processed in FBK cleanroom and *has just completed the microfabrication on the front side*.

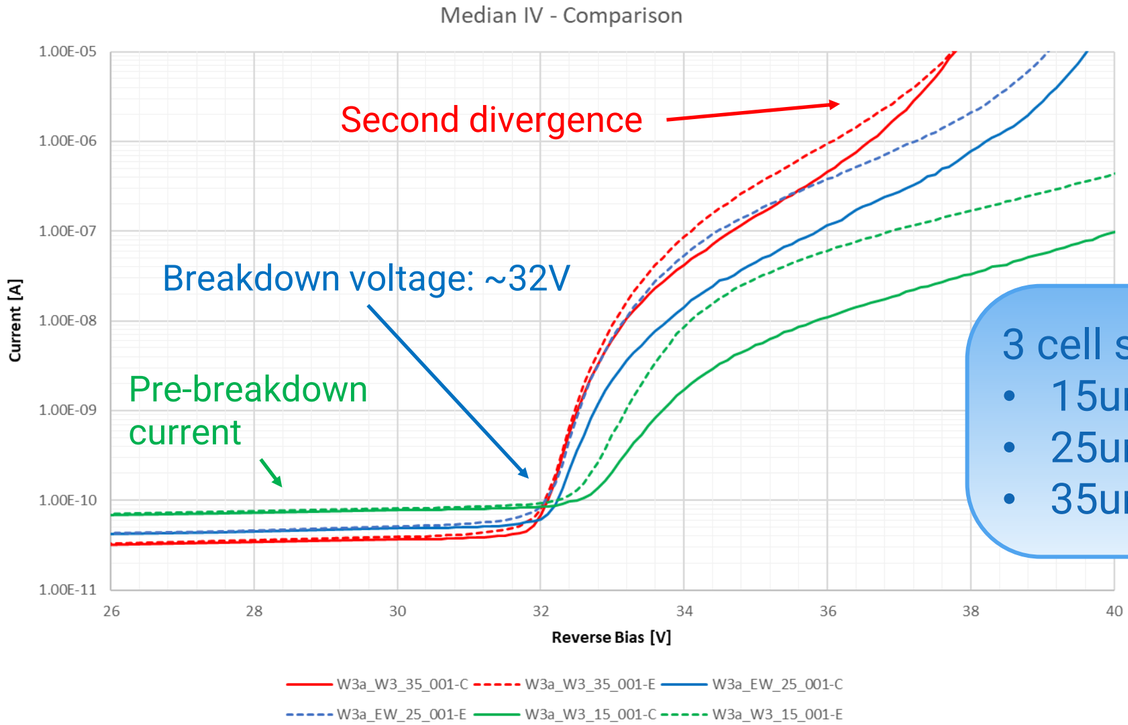
C type layout



E type layout



The first measurements were carried out on a few wafers, whose microfabrication was stopped before the backside processing.



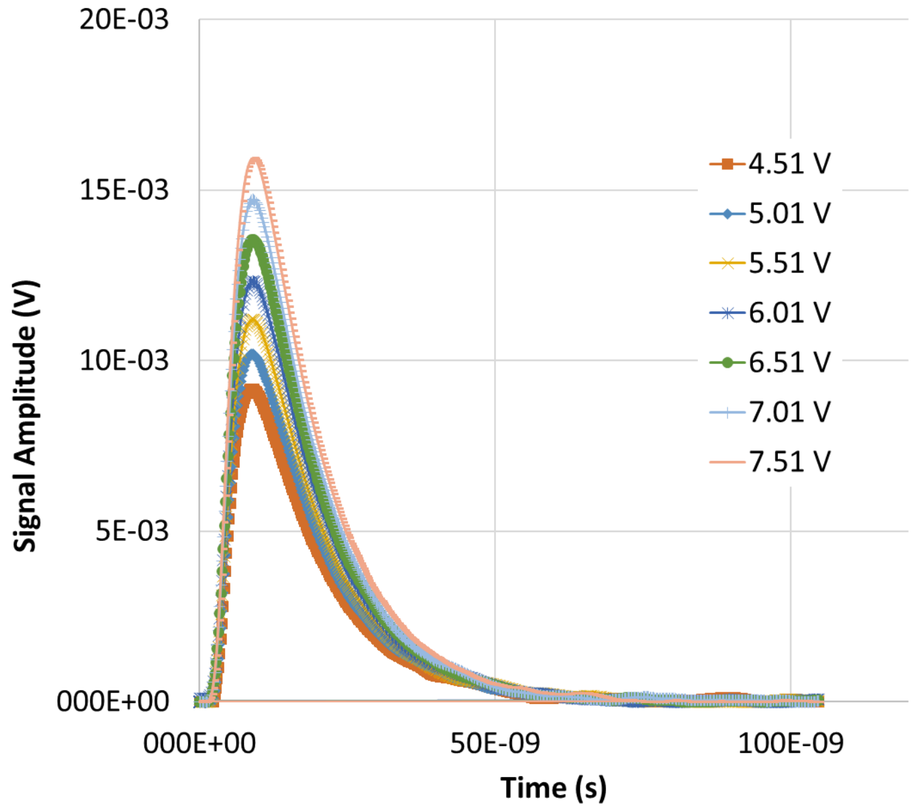
3 cell sizes tested:
- 15um
- 25um
- 35um

Reverse current measured on different microcell sizes of one layout split from the IBIS INFN NUV-BSI run, with (C-type layout) and without (E-type layout) the Isolation connection.

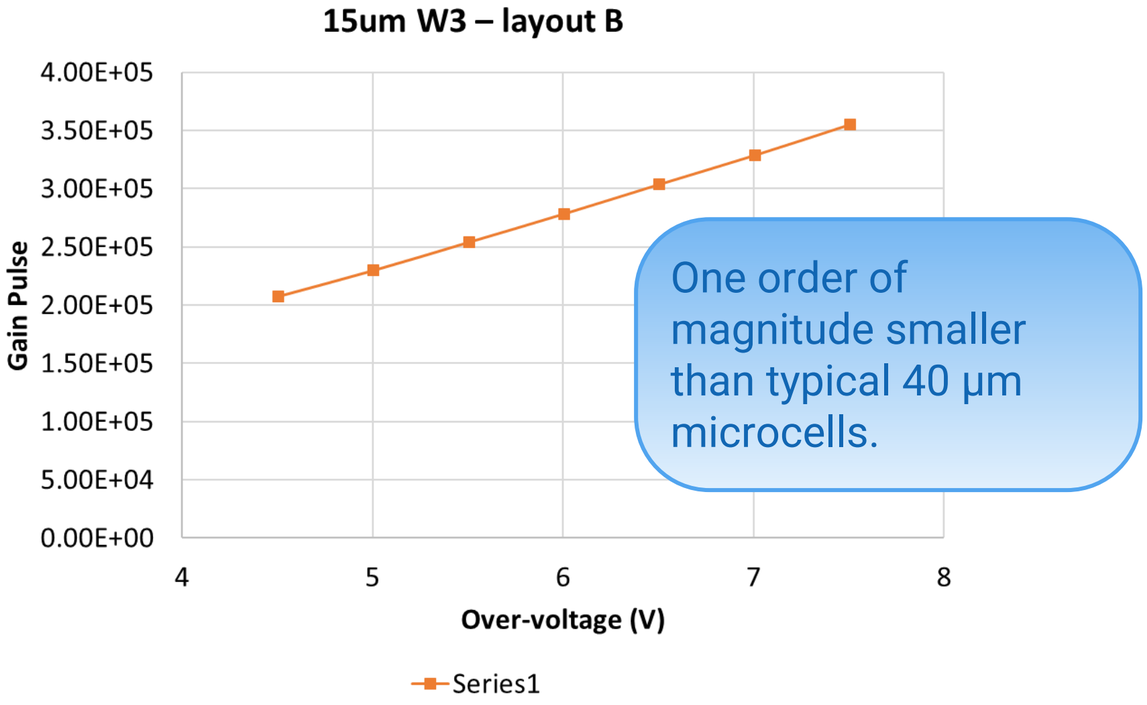
When increasing the cell size, the dark current increases and the second divergence is anticipated. Pre-breakdown current decreases as the cell size increases.

Run IBIS#1 – Preliminary Functional measurements
15 um cell – Signal shape and Gain

Preliminary



Average signal shape measured on the 15 µm cell size of the NUV-BSI SiPMs at different value of the overvoltage



One order of magnitude smaller than typical 40 µm microcells.

Avalanche gain measured on the 15 µm cell size of the NUV-BSI SiPMs

Perspectives on SiPM Radiation Hardness

Perspectives for R&D on SiPM rad hardness
Putting it all together

By *combining all the techniques identified* to improve SiPM radiation hardness together, a ***very significant DCR reduction seem within reach***.

Under *moderately optimistic hypotheses*, the *DCR suppression factor* R_{DCR} can be estimated as follows:

-50°C

$$R_{tot}^{DCR} = R_{microlens}^{DCR} * R_{chargefocus}^{DCR} * R_{annealing}^{DCR} * R_{cooling}^{DCR} =$$

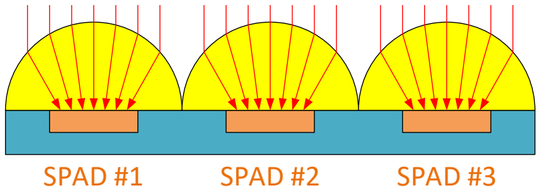
Is this reasonable? R&D needed to confirm

conservative $\cong \quad 3 \quad * \quad 5 \quad * \quad 10 \quad * \quad 30 \quad = 5 * 10^3$

$$\approx DCR < 5 * 10^5 \; cps/mm^2 \; @ \; 10^{12} \; 1 \; MeV \; n_{eq}/cm^2$$

realistic $\cong \quad 5 \quad * \quad 15 \quad * \quad 100 \quad * \quad 60 \quad = 5 * 10^5$

$$\approx DCR < 5 * 10^3 \; cps/mm^2 \; @ \; 10^{12} \; 1 \; MeV \; n_{eq}/cm^2$$



Possible use of micro lenses to implement a *sparse light readout* that could improve the radiation tolerance of the detector.

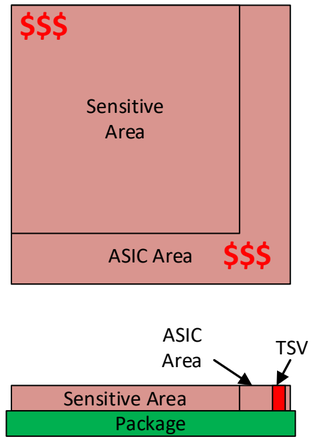
Challenging, but very promising R&D roadmap!

Monolithic vs. 2.5D / 3D Integration

Cost Estimation
Very preliminary comparison of different approaches

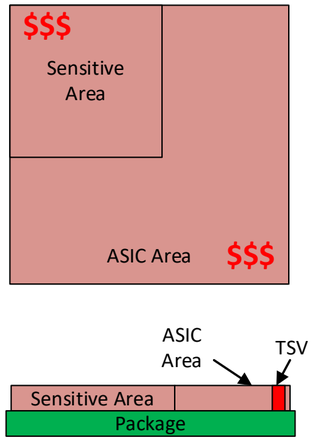
The choice of the best solution *depends on the specifications*. For example: *how much processing area (ASIC) do we need* for a given sensitive area of silicon? Also depends on the miniSiPM pitch. Some hypotheses:

a. ASIC area = 10% of sensing area for 1 mm^2 pitch.
b. ASIC area = 50% of sensing area for 0.1 mm^2 pitch.



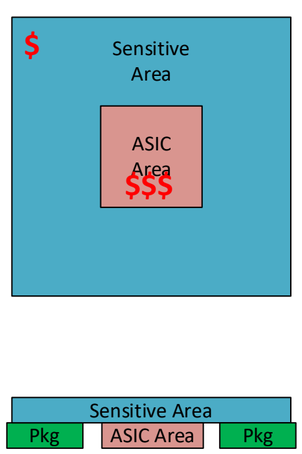
Fully CMOS – large pitch:

- Only CMOS
- TSV needed



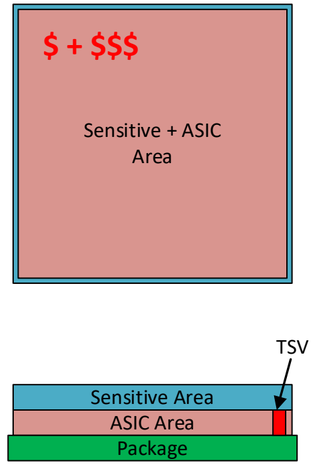
Fully CMOS – small pitch:

- Only CMOS
- TSV needed.



Hybrid – large pitch:

- Custom sensor
- CMOS readout ASIC
- Chip-to-wafer bonding
- *Redistribution layer* on sensor



Hybrid – full 3D – small pitch:

- Custom sensor
- CMOS readout ASIC
- Wafer to wafer bonding
- TSV needed

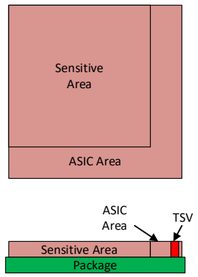
Cost Estimation
Very preliminary comparison of different approaches

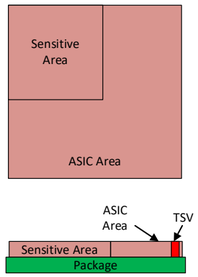
We assume that the *price per unit area of a custom SiPM wafer* (built in large external foundry) *scales in the same way as engineering CMOS run*.

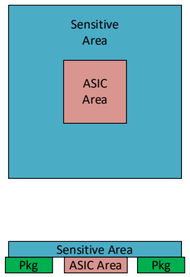
As a first order approximation, the price of the wafer is proportional to the number of lithographies in the process.

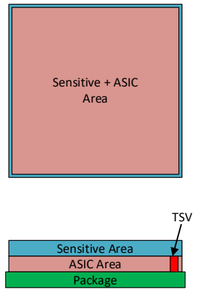
$$CMOS \cong 45\ lithos$$
$$Custom\ SiPM \cong 12\ lithos$$

$$\Rightarrow \quad Cost_{SiPM} \cong {}^{1}/_{4}\, Cost_{CMOS}$$





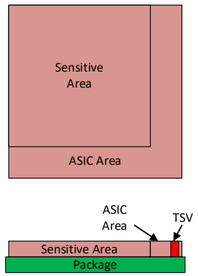


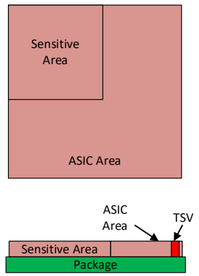


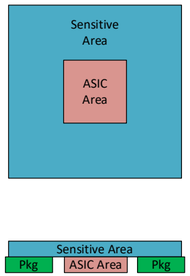
	CMOS – large pitch	CMOS – small pitch	Hybrid – large pitch	Hybrid – small pitch
Custom SiPM area	$A_{SiPM} = 0$	$A_{SiPM} = 0$	$A_{CMOS} = 1/10 * A_{SiPM}$	$A_{SiPM} = A_{CMOS}$
Silicon Cost	$C_T = C_{CMOS}$	$C_T = C_{CMOS}$	$C_T = 0.1 * C_{CMOS} + 0.25 * C_{CMOS} = 0.35 * C_{CMOS}$	$C_T = C_{CMOS} + 0.25 * C_{CMOS} = 1.25 * C_{CMOS}$

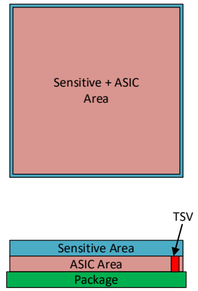
However, integration costs and packaging costs should also be considered.

Cost Estimation
Very preliminary comparison of different approaches









\	CMOS – large pitch	CMOS – small pitch	Hybrid – large pitch	Hybrid – small pitch
Detection Efficiency	**Medium**	**Low**	**High**	**High**
Pitch	Large	Small	Large	Small
Silicon Cost	**$C_T = C_{CMOS}$**	**$C_T = C_{CMOS}$**	**$C_T = 0.35\ C_{CMOS}$**	**$C_T = 1.25\ C_{CMOS}$**
TSV	**Yes**	**Yes**	**No**	**Yes**
3D Integration cost	**0**	**0**	**TBD (chip to wafer)**	**TBD (wafer level)** **Depends on pitch**
Packaging	**Normal**	**Normal**	**More complex**	**Normal**
Notes	Poor performance? Radiation hardness?	Poor performance? Radiation hardness?	Signal integrity? Package complexity?	Highest performance? Need for single cell?

Probably, a more detailed study is needed to select the best option based on the experiment specifications.

Thank you!

We are hiring!

https://jobs.fbk.eu/

Thanks to all the members of the team working on custom SiPM technology at FBK:

- **Fabio Acerbi**
- **Ibrahim Mohamed Ahmed**
- **Lorenzo Barsotti**
- **Fabiola Caso**
- **Jacopo Dalmasson**
- **Andrea Ficorella**
- **Priyanka Kachru**
- **Oscar Marti Villareal**
- **Stefano Merzi**
- **Giovanni Palù**
- **Laura Parellada Monreal**
- **Giovanni Paternoster**
- **Michele Penna**
- **Maria Ruzzarin**
- **Gianluca Vedovelli**
- **Nicola Zorzi**