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LightPix: Scalable readout for SiPMs in cryogenic environments

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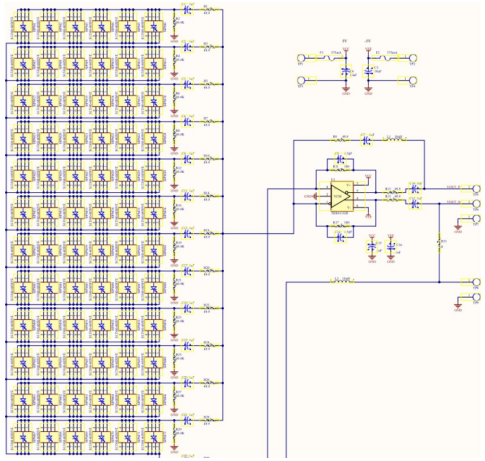
PD24 Workshop, November 20, 2024

Large Area Cryo-SiPM Challenges

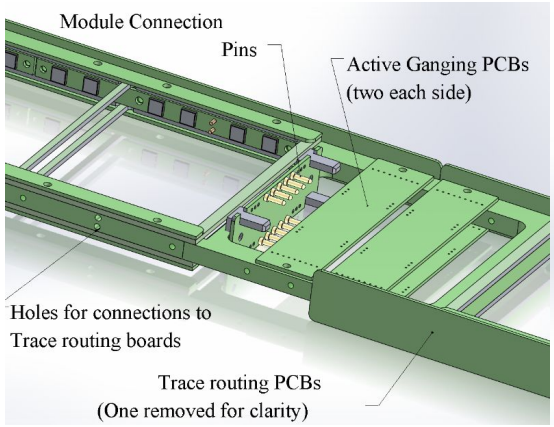
High readout burden→high power, summing electronics

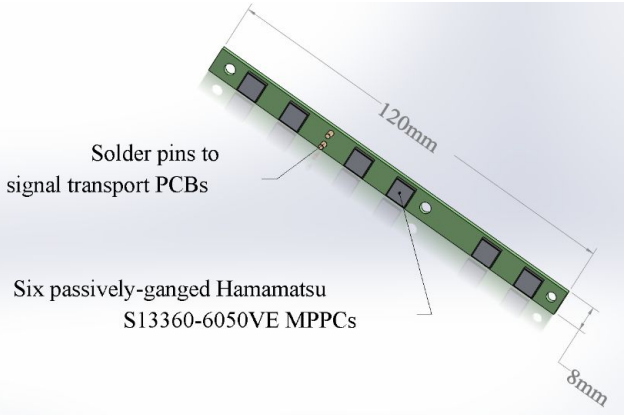
- Minimize cabling + cryostat penetrations → prefer cold electronics
  - Very low power required to prevent boiling
  - Cryo-robustness
- High granularity→high channel count electronics or SiPM summing/ganging
- High dark count rate



DUNE PDS, from TDR:
https://iopscience.iop.org/article/10.1088/1748-0221/15/08/T08010

Example from DUNE:
6x passive ganging + 8x active ganging
48 SiPM sum per readout

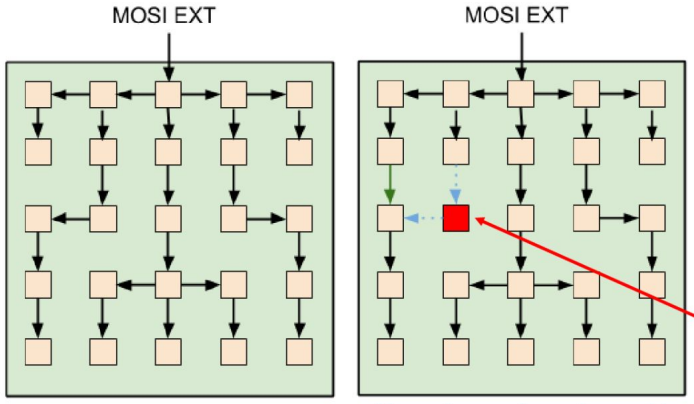


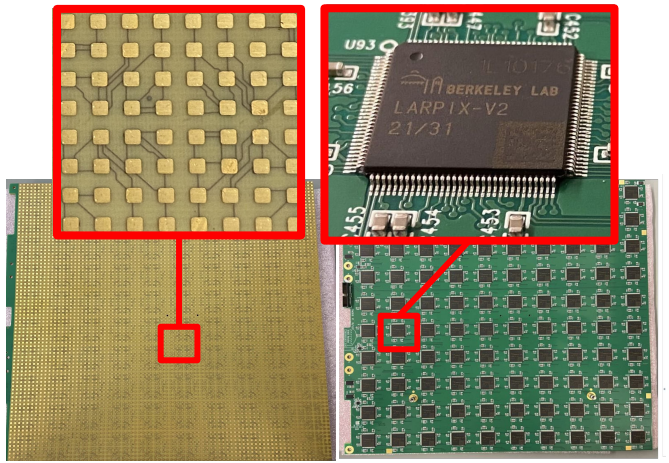


Background: LArPix Scalable cryo-readout

3D Cryo-Readout for Ionization Electrons in LAr

- 64 self-triggering channels per ASIC
  - Per channel tunable thresholds
- Low power analog front-end <200 uW/channel
- Highly multiplexed digital I/O
  - 10,240 channels/cable
  - 102,400 channels/warm controller
- Scalable at cost (O($0.10) per channel, including cables/controllers/assembly/etc.)

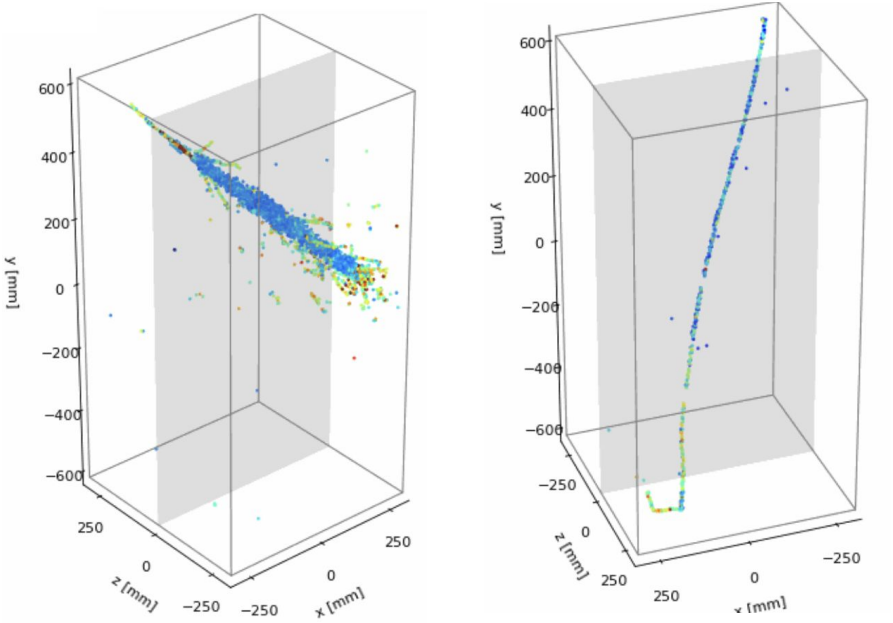




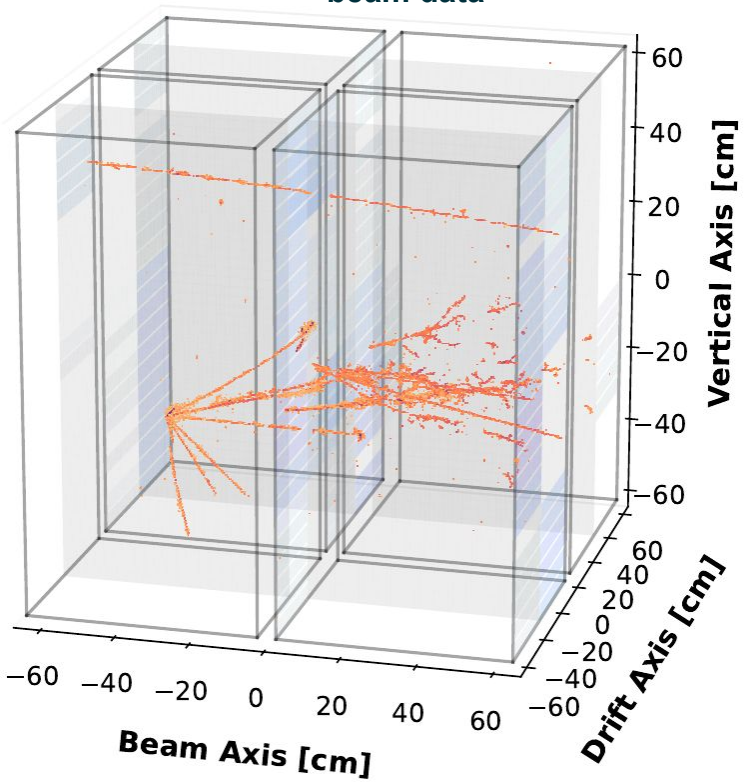
LArPix pixel tile PCB with 100 ASICs

Background: LArPix Scalable cryo-readout

- Several O(10^5) channel detectors constructed to date



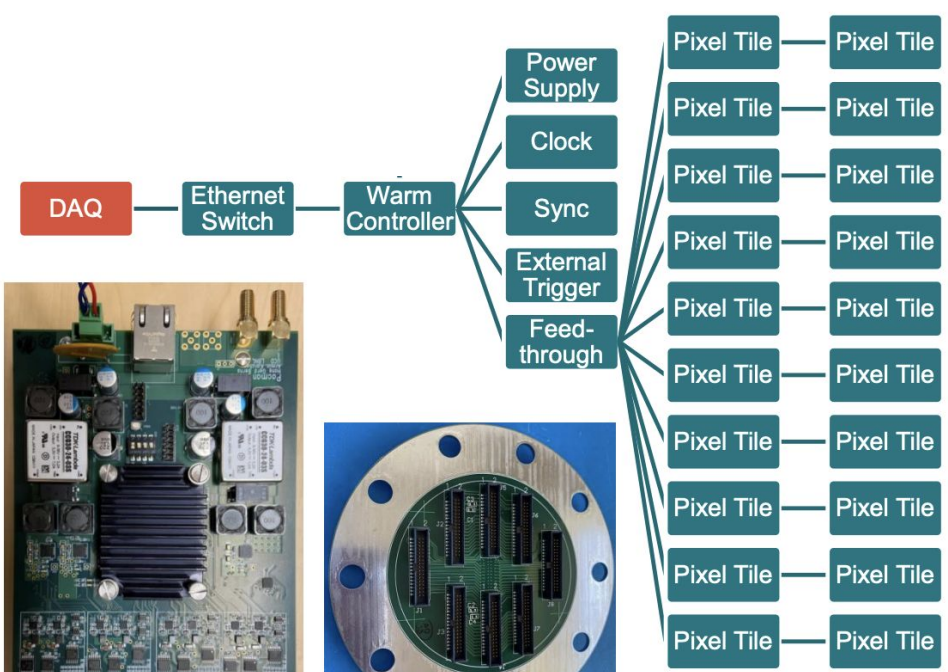
DUNE 2x2 neutrino beam data



DUNE Collaboration, Performance of a Modular Ton-Scale Pixel-Readout Liquid Argon Time Projection Chamber. Instruments 2024, 8, 41. https://doi.org/10.3390/instruments8030041

LightPix/LArPix Full Detector System

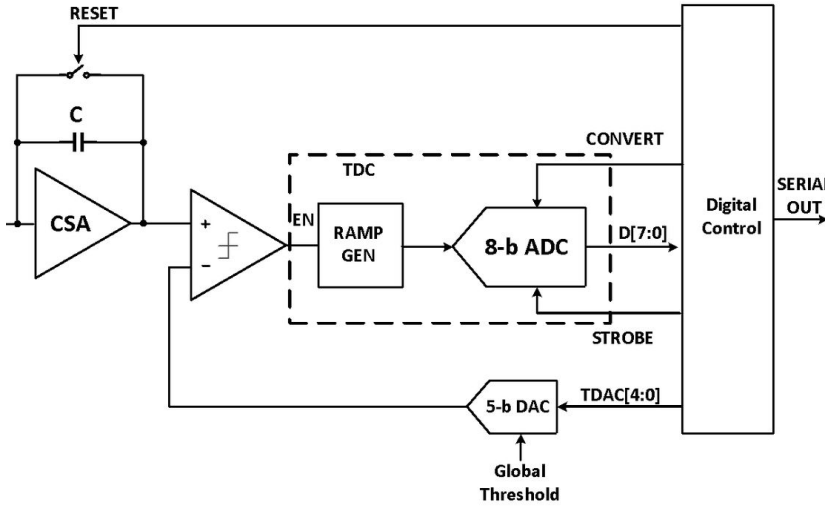
- Single cable per tile carries power/data/configuration commands
- Control and DAQ from PACMAN board at cryostat feedthrough
- Data streamed continuously over ethernet to host machine



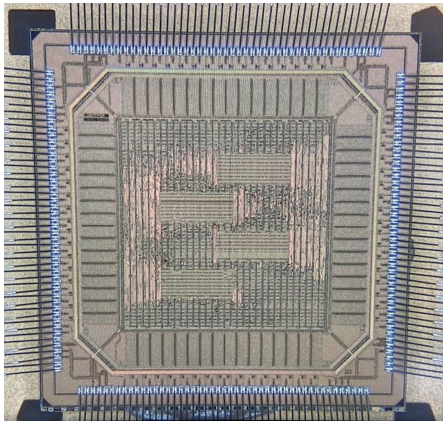
LightPix Concept

R&D towards scalable cryo-SiPM readout

- Cryo-compatible, ‘pixelated’ SiPM readout
- LArPix scalability and shared digital core
  - Low-swing differential I/O and ‘Hydra networking’
  - Demonstrated manufacturing: full-industry, O(10^6) channels produced
  - Readout of >10^5 channels/cable with PACMAN controller
- Unique channel for every SiPM (no analog ganging) → Highly granular detector



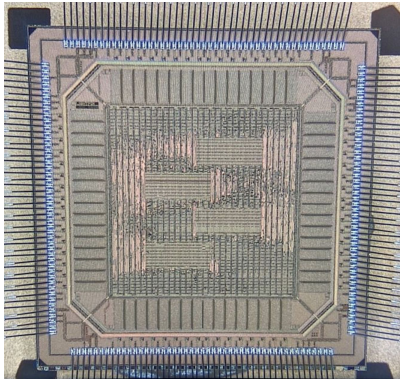
LightPix-v1 packaged chip on PCB



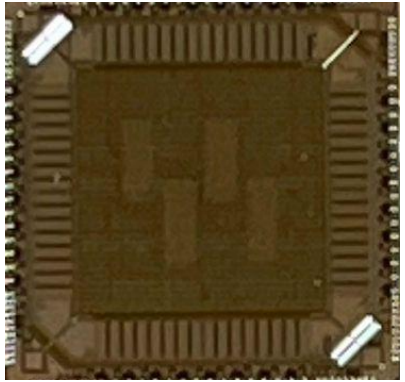
LightPix-v1 die (180nm CMOS)

LightPix Versions

- All ASIC versions in TSMC 180nm CMOS
- TDC with (sub-)ns precision
- Tuneable hit coincidence requirements (1-64 channels hit over 100 ns-13 μs)



LightPix-v1 die



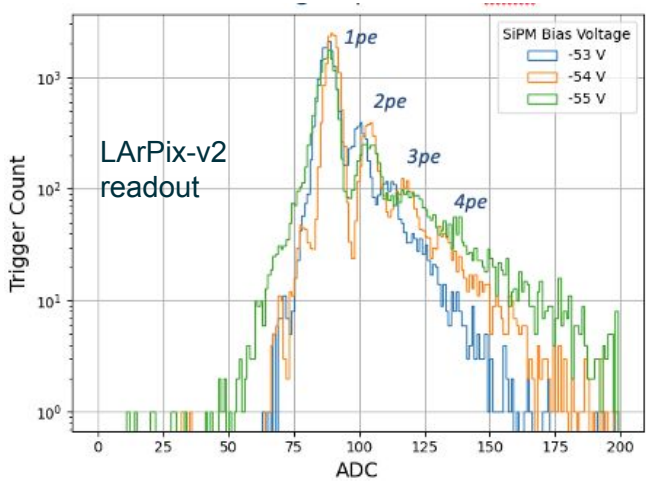
LightPix-v3 die

ASIC Version	Analog Front End	Digital I/O	Calorimetry?	Received
1	CSA	Single-ended	N	Aug. 2021
2	CSA	Single-ended	N	N/A
3	TIA	Differential	Y	Nov. 2024

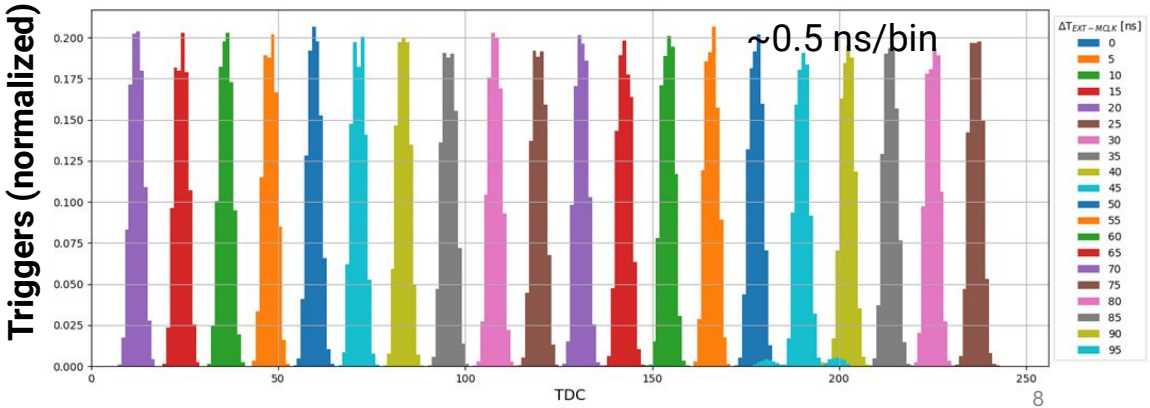
LightPix-v1 ASIC

O(ns) TDC performance and hit coincidence logic

- Functional digital core and hit coincidence logic
- TDC evaluation for ~SPE inputs
  - Linear to <1 ns over 100 ns timing range
  - < 1 ns jitter
  - < 2 ns time-walk bias
- Compromises in design
  - Front-end (CSA) recycled from LArPix
  - Strong pickup from clock/single ended I/O



LightPix TDC ~ns Precision w/ Charge Injection

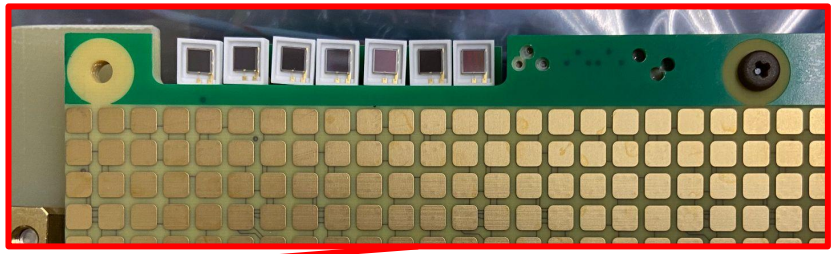


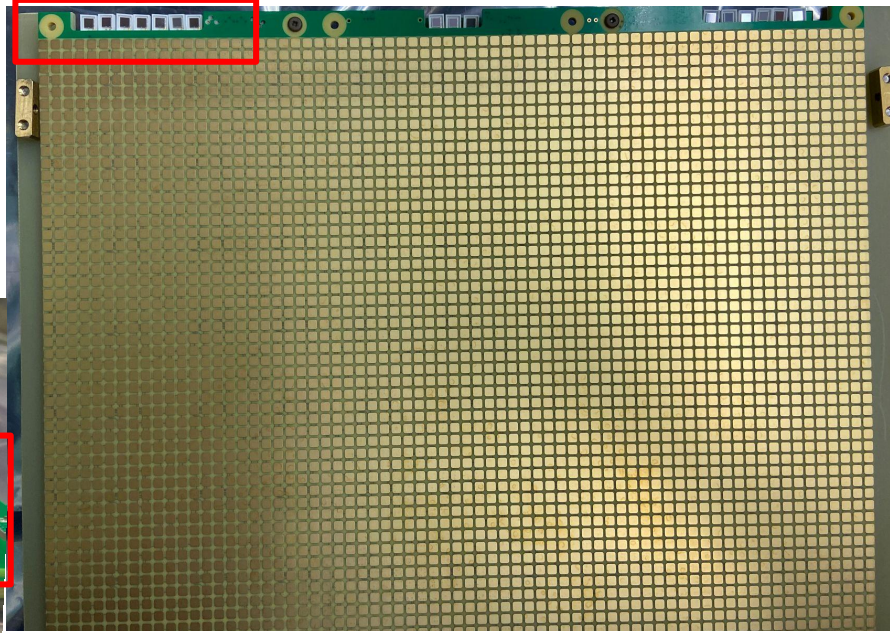
LightPix-v1 LArTPC Readout

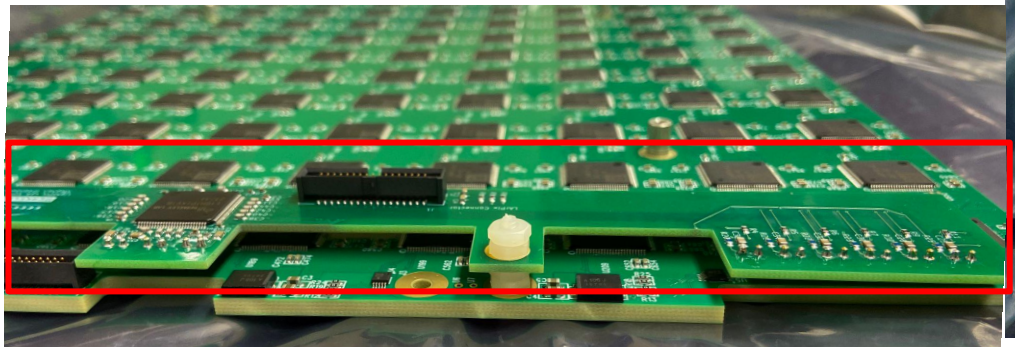
Direct VUV Light Detection in LArTPC

- Proof of concept for joint charge/light readout
- Direct VUV SiPMs visible to active LAr volume
- SiPM PCB attaches directly to LArPix tile
- 1 LightPix ASIC / 16 SiPM channels/board
  - SiPMs ~5mm behind anode plane
- Single PACMAN controller, two shared data/power cables

HPK Direct VUV SiPMs (3mm x 3mm)







LightPix-v1 LArTPC Readout

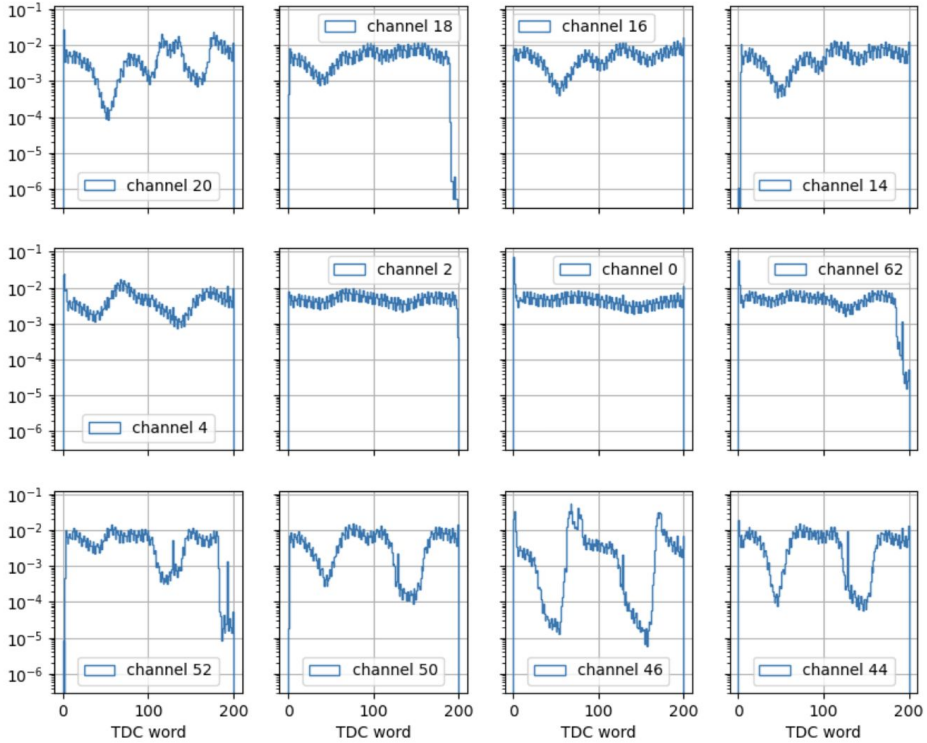
Direct VUV Light Detection in LArTPC

High Purity test stand at LBNL with SingleCube 30cm drift LArPix TPC

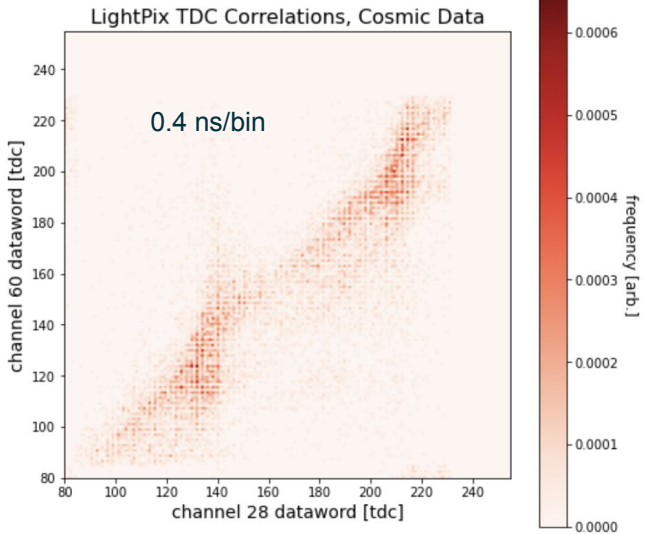
Assembled 30cm drift and LArPix TPC with LightPix SiPM board

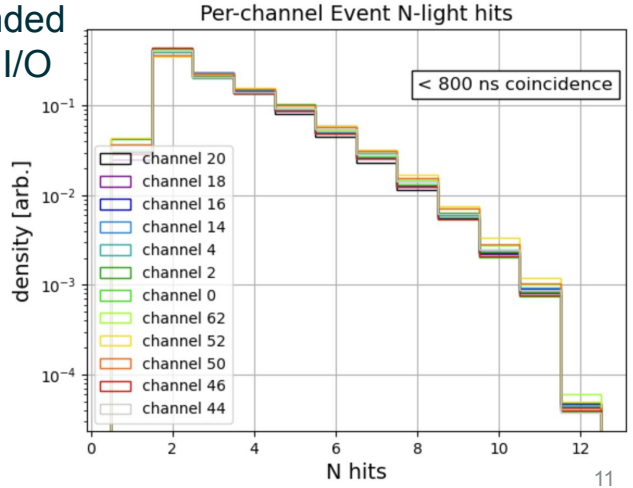
LightPix-v1 LArTPC Readout

LightPix-v1 TDC word Distributions



Per-event timing correlations slewed by pickup from single-ended clock + digital I/O

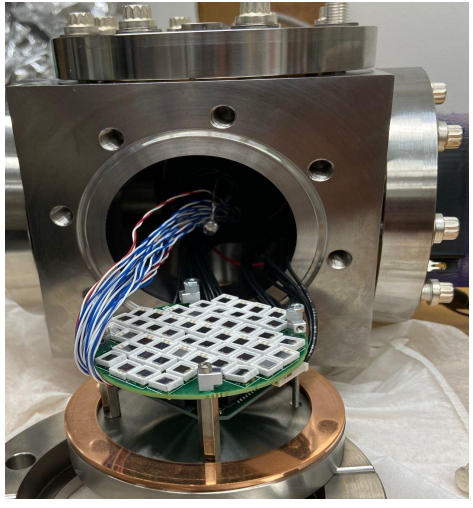




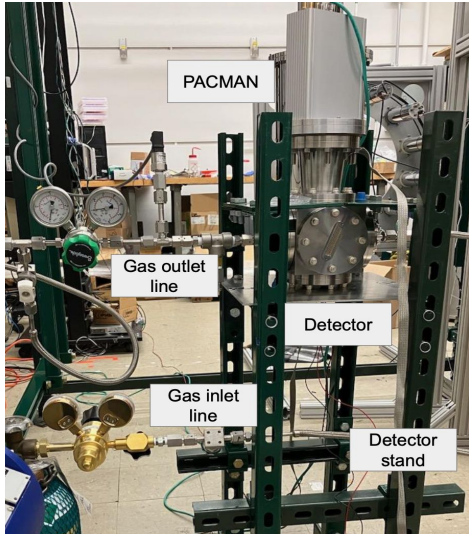
GHe Neutron Detector

Room temperature detector with GHz DCR suppression

- R&D towards novel **room temp** neutron detector
  - High pressure (10-15 bar) GHe+% level GAr
  - 300 3x3 mm^2 direct VUV SiPMs→**GHz DCR**
- **1 LightPix ASIC / 50 SiPMs**
  - No summing/ganging→fully pixelated
- First prototype goals: demonstrate neutron sensitivity with DD neutron generator
  - Scientific goals: understanding helium scintillation and excimer formation
- Decoupled SiPM / LightPix readout boards→potential for upgrade with newer LightPix versions



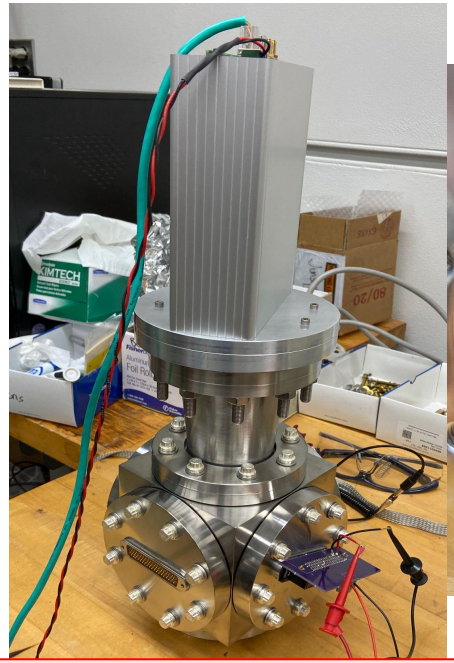
50 3x3 mm^2 SiPMs on single detector wall



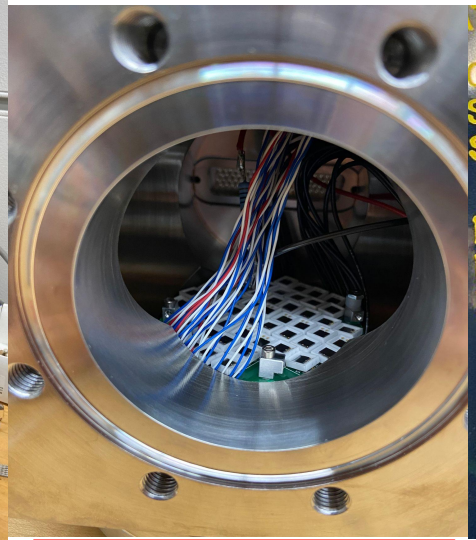
GHe test stand at UC Berkeley

GHe Neutron Detector

Room temperature detector with GHz DCR suppression

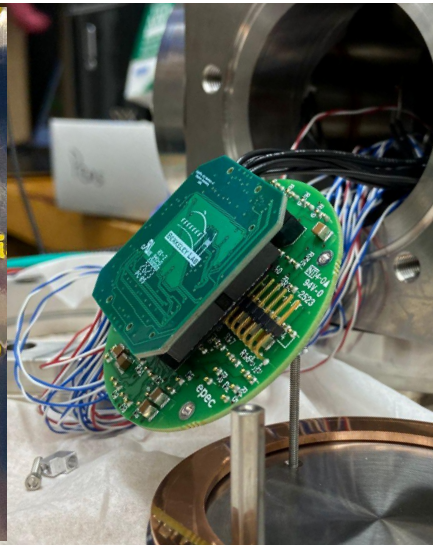


Conflat cube with PACMAN



SiPMs inside detector

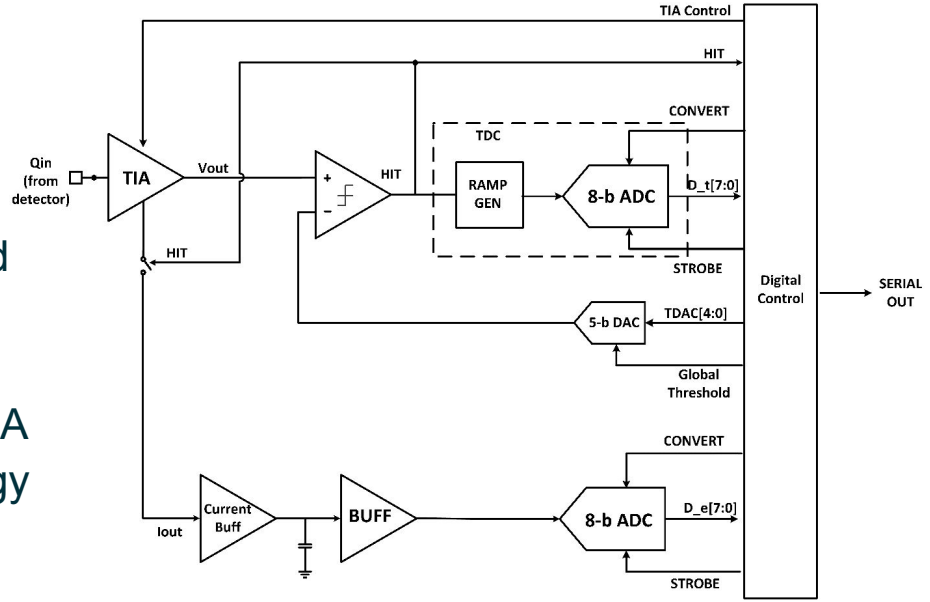
LightPix readout PCB

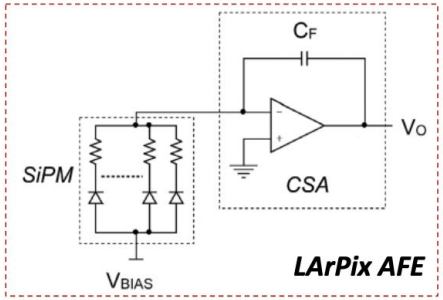


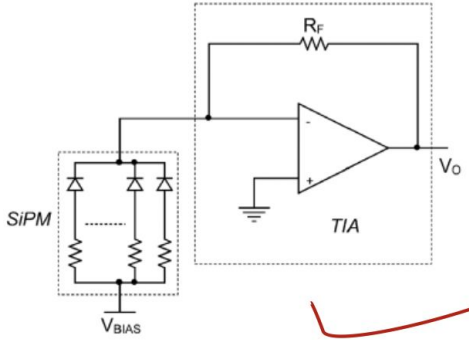
LightPix board mounted to SiPM board

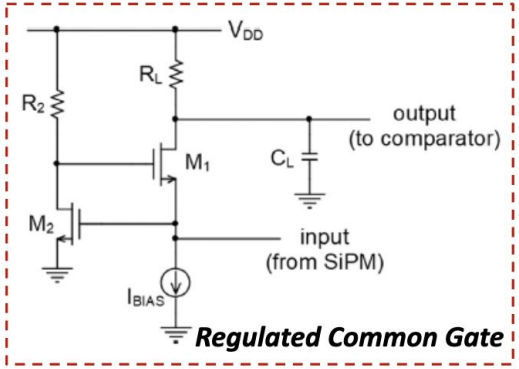
LightPix-v3 Design

- Significant re-design of ASIC analog front-end (AFE)
  - Increased power budget and decreased gain requirements: move from CSA to TIA
- 32 “super channels” with sub-ns timing+energy
- Fully differential clock and digital I/O





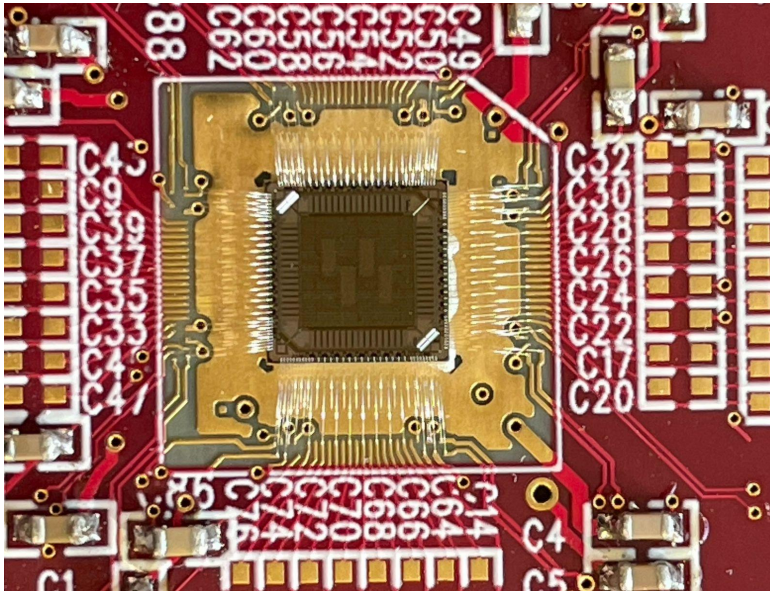




LightPix-v3 Status

- Design started Spring ‘24
- Submitted as multi-project wafer Summer ‘24
- First die in hand Nov. 12!
  - Verified basic functionality and power
  - Verified new digital features and low-swing differential I/O

Next few weeks: characterization of new front end (TIA) and calorimetric performance

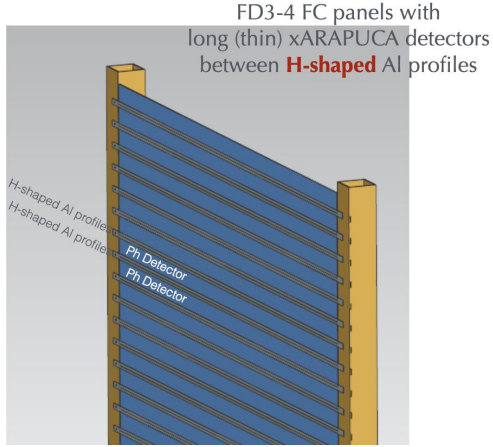


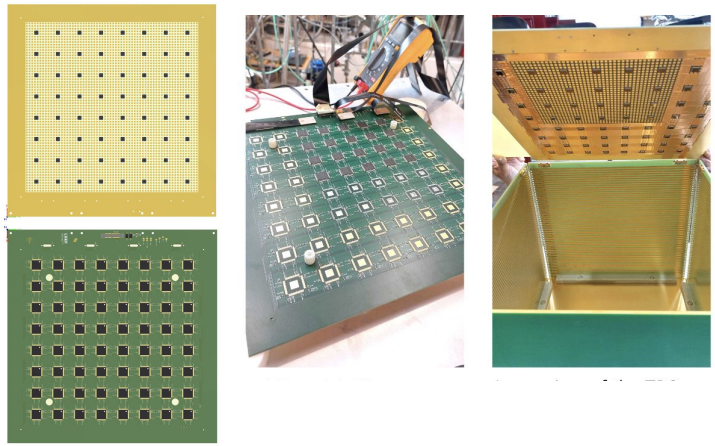
LightPix-v3 bare die on test PCB from Nov. 2024

Next Generation Detectors

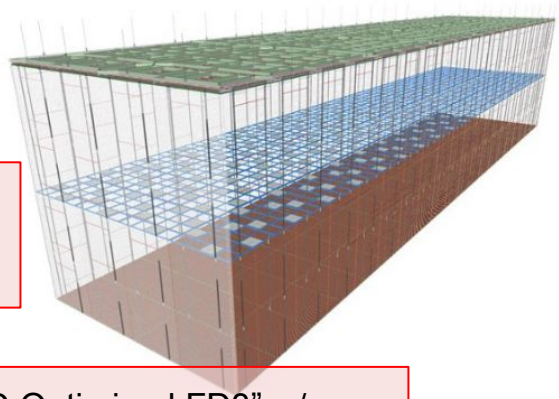
LightPix features aligned with community needs

- Major focus on enhanced photon detection systems and increased SiPM channel count for DUNE FD3/4
- LightPix suitable to retain granularity, ns timing





SoLAr-v2 design (left) and realized prototype (right) from S. Parsa



SoLAr: https://arxiv.org/abs/2203.07501

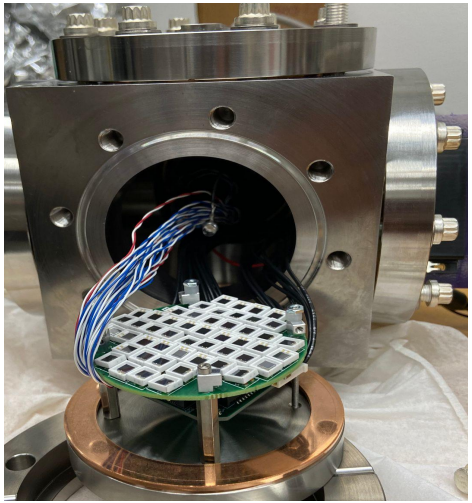
Example: “VD Optimized FD3” w/ enhanced PDS (*F. Cavanna*)
https://indico.fnal.gov/event/59908/

Summary

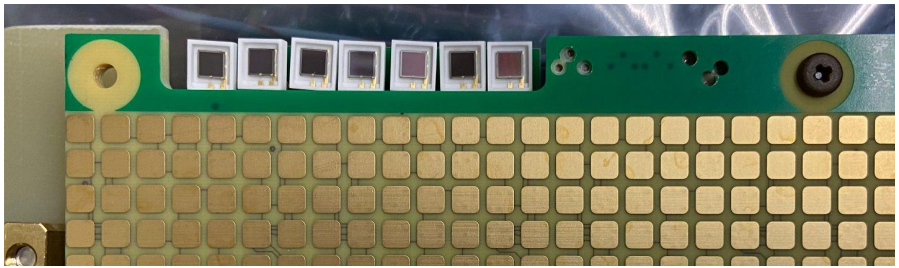
LightPix: scalable cryo-SiPM readout

- **LightPix: maintain granularity in large area cryogenic applications**
  - Utilizing technologies demonstrated by LArPix
  - Synergy with LArPix for scalable combined detectors
- Proof-of-principle demonstrations with LightPix-v1
  - LArTPC light readout with direct VUV technology
  - Room temperature GHe neutron detector
- Next generation ASIC with considerable front-end improvements + calorimetry in hand
- Suitable for large scale experiments
  - O(ns) timing, granular, low occupancy

LightPix-v1 die in 180nm CMOS



SiPM integrated with LightPix in LArTPC



Backup

LArPix ASIC

3D Cryo-Readout for Ionization Electrons in LAr

- 64 self-triggering channels per ASIC
  - Charge sensitive amplifier
  - Per channel tunable thresholds
- Low noise, low power analog front-end
  - <200 uW passive per channel
  - ~800 e- ENC rms
- Highly multiplexed digital I/O
  - 6400 channels/cable
  - 51,200 channels/warm controller
- Scalable at cost (O($0.10) per channel, including cables/controllers/assembly/etc.)

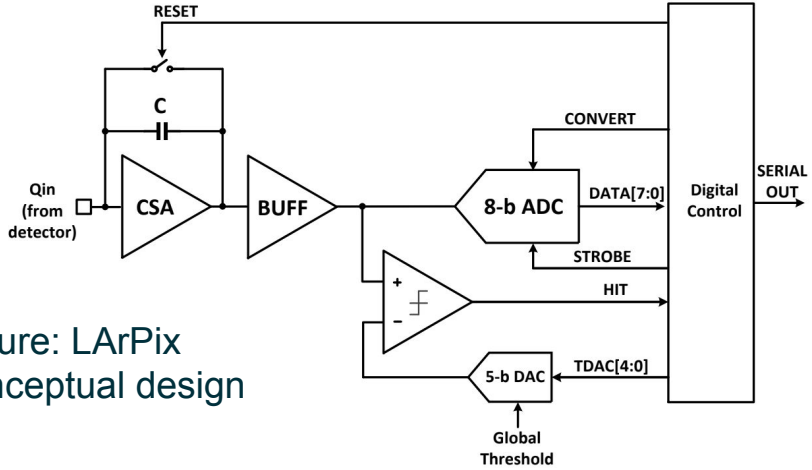
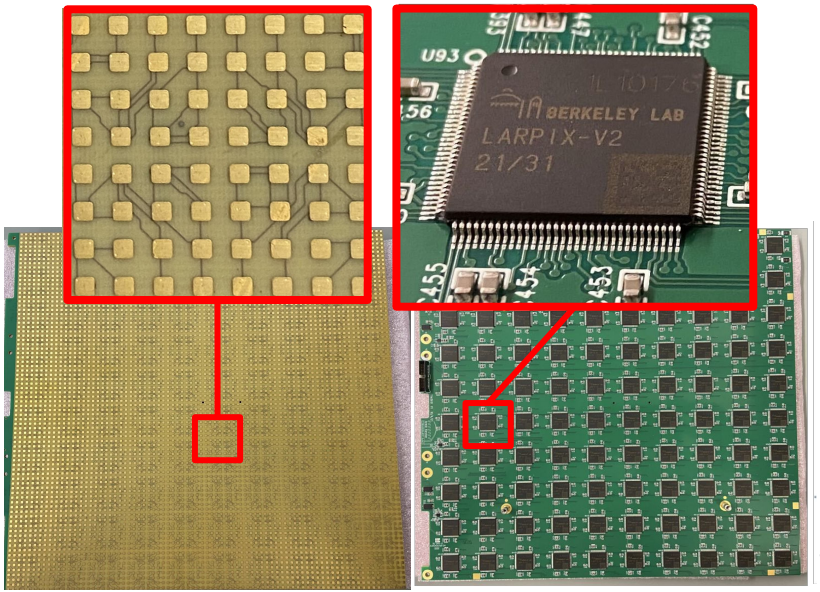
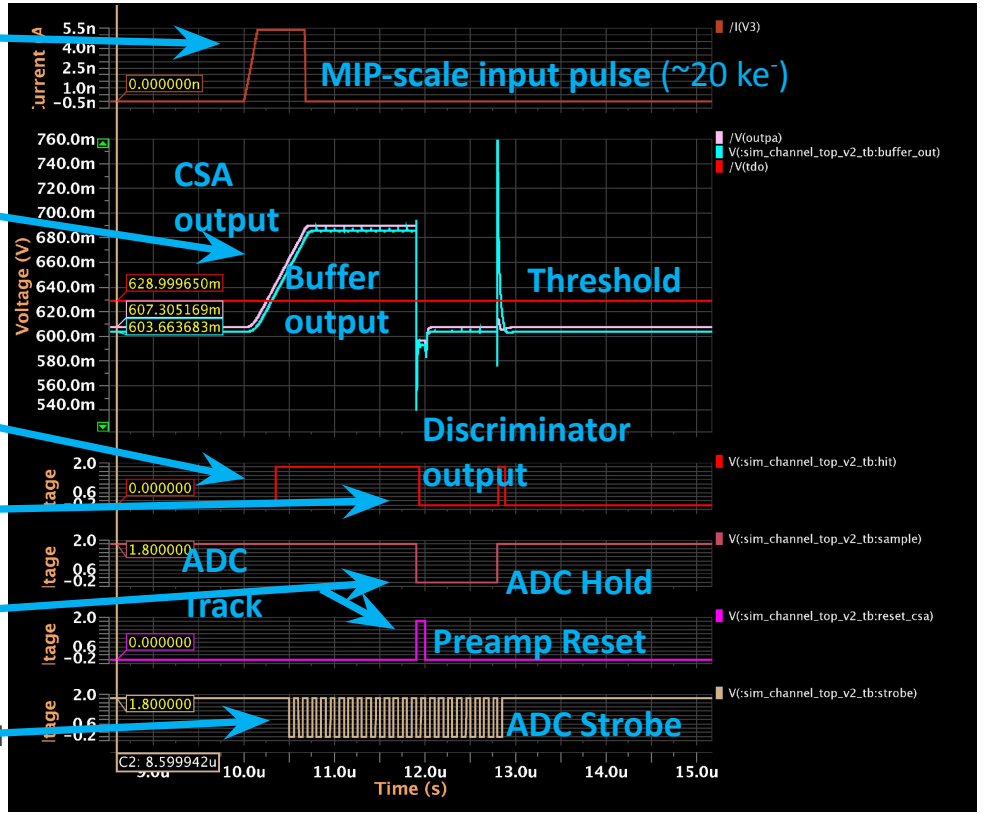


Figure: LArPix conceptual design



LArPix/LightPix Self-Trigger Cycle

1. Charge input to channel
2. CSA integrates current, buffer drives current to discriminator and ADC.
3. Signal exceeds discriminator threshold, hit cycle begins.
4. Channel ‘waits’ a tunable delay (typically 1.8 us) for full drift signal integration.
5. If discriminator still high after wait, ADC ‘holds’ signal and front-end is reset to discard charge on pixel. Channel ready for next signal.
6. ADC ‘strobes’, converting held signal to digital value. Sends ADC value, timestamp, and chip/channel ID to serial out.



Optional Burst Modes:

‘Fixed’ Burst:
Process ‘n’ hit cycles for each self trigger

‘Dynamic’ Burst:
Continue to process hit cycles until change in ADC value is below set value.

Note:
CSA does not reset until end of burst.

LArPix / LightPix Co-Design

Single-cable charge+light readout in LArTPC

- Interest in direct light detection with VUV SiPMs integrated into TPC anode
  - E.g. SoLAr concept
- **Chip-to-chip I/O is ASIC-family independent**
  - LArPix+LightPix: shared power/IO/single cable

LArPix/LightPix dual charge+Light anode prototype design