Overview of 3D Integrated Photon-to-Digital Converters for Particle Physics and Medical Imaging.

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O. Lepage[1], R. A. Giampaolo[1], S. Prentice[1], G. Théberge Dupuis[1], R. Scarpellini[1],
P. A. Hausladen[2], F. Retière[3], S. A. Charlebois[1], J-F Pratte[1]

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Vancouver, Canada

1. Université de Sherbrooke,
Institut Interdisciplinaire d'Innovation Technologique (3iT)
2. Oak Ridge National Laboratory, Oak Ridge, Tennessee, USA
3. TRIUMF, Science Technology Department

Outline

- Advantages of going digital and vertical integration
- Designing PDCs for different applications
- What technologies are available/being developed?
- Our 3D bonding process
- Results

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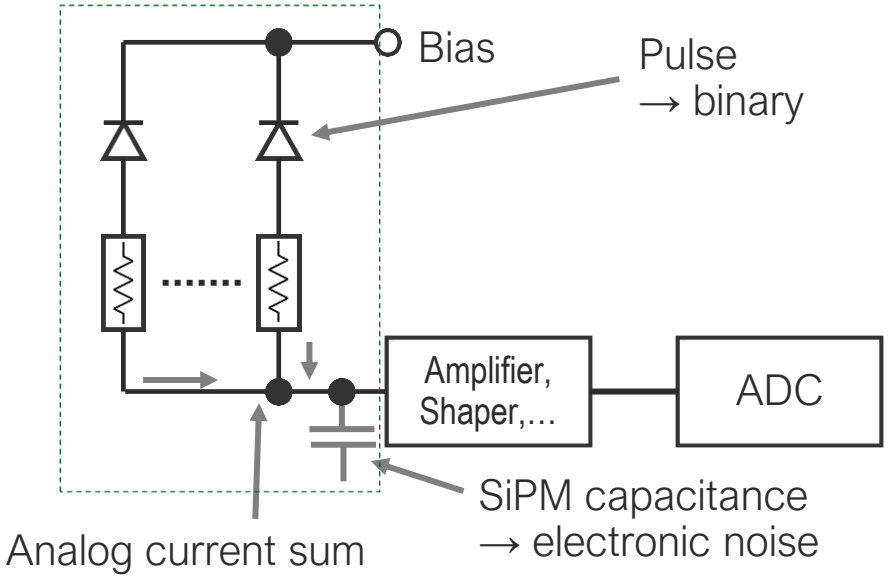
Analog vs Digital SiPMs and Vertical Integration

Analog SiPMs



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Analog vs Digital SiPMs and Vertical Integration

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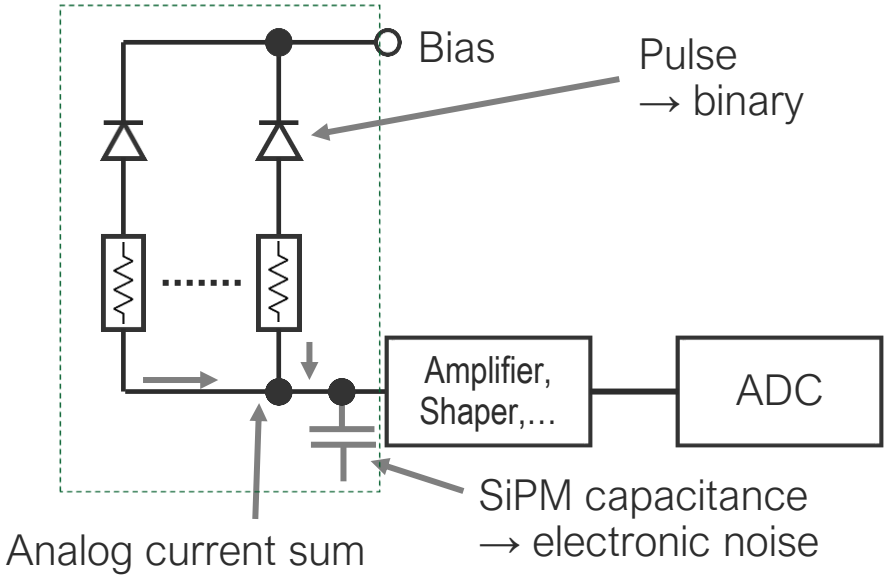
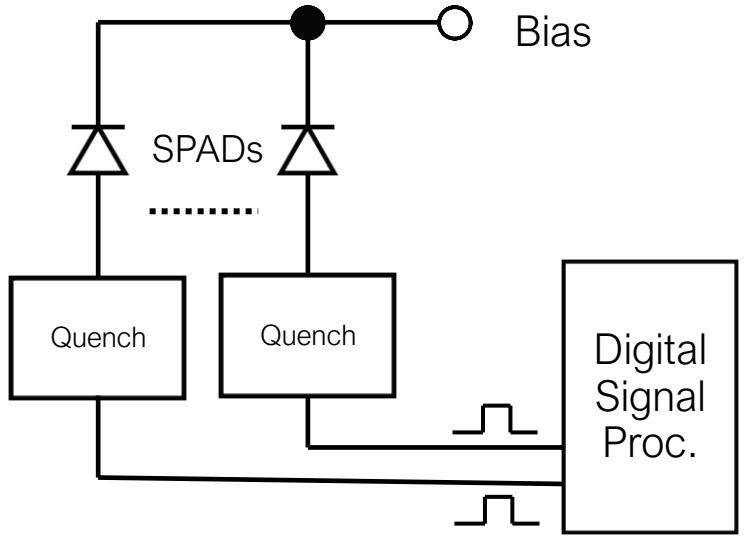


Digital SiPMs / PDCs



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Analog vs Digital SiPMs and Vertical Integration

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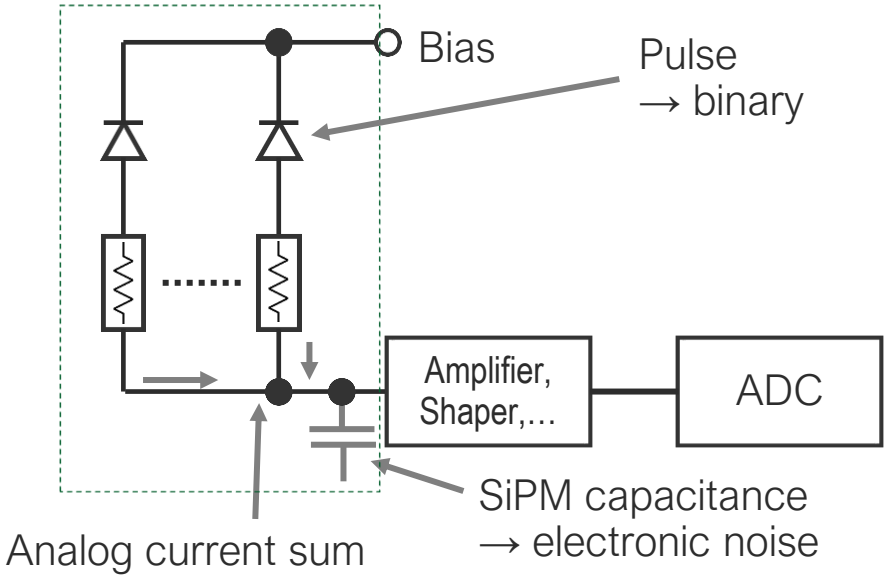

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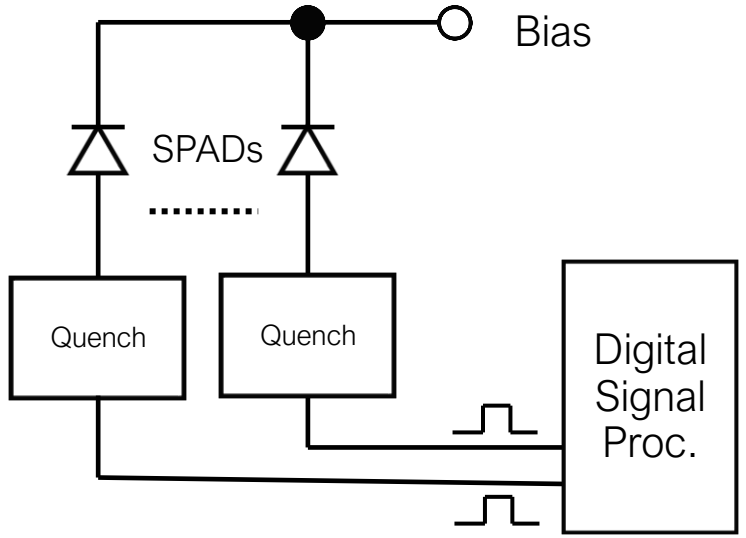
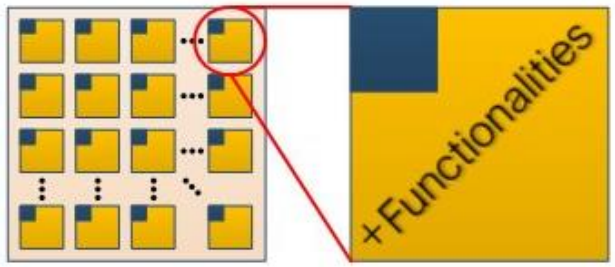


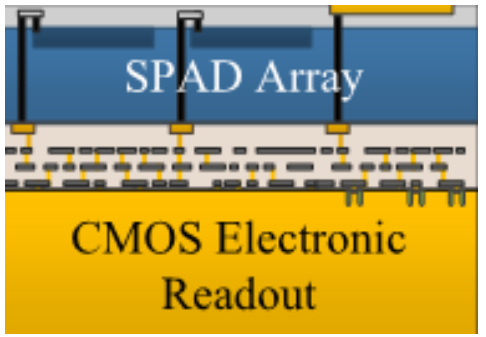


or

= SPAD layer

= CMOS electronics layer

3D



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Benefits of Digital SiPM?

- Ultimate Single Photon Counting Resolution
  - Time of arrival/flight applications
  - Pulse-shape discrimination

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  - Lower overall DCR by disabling « screamers » [1]
  - Mitigation of afterpulsing with hold-off/recharge times
  - Better SNR, dead-time, …

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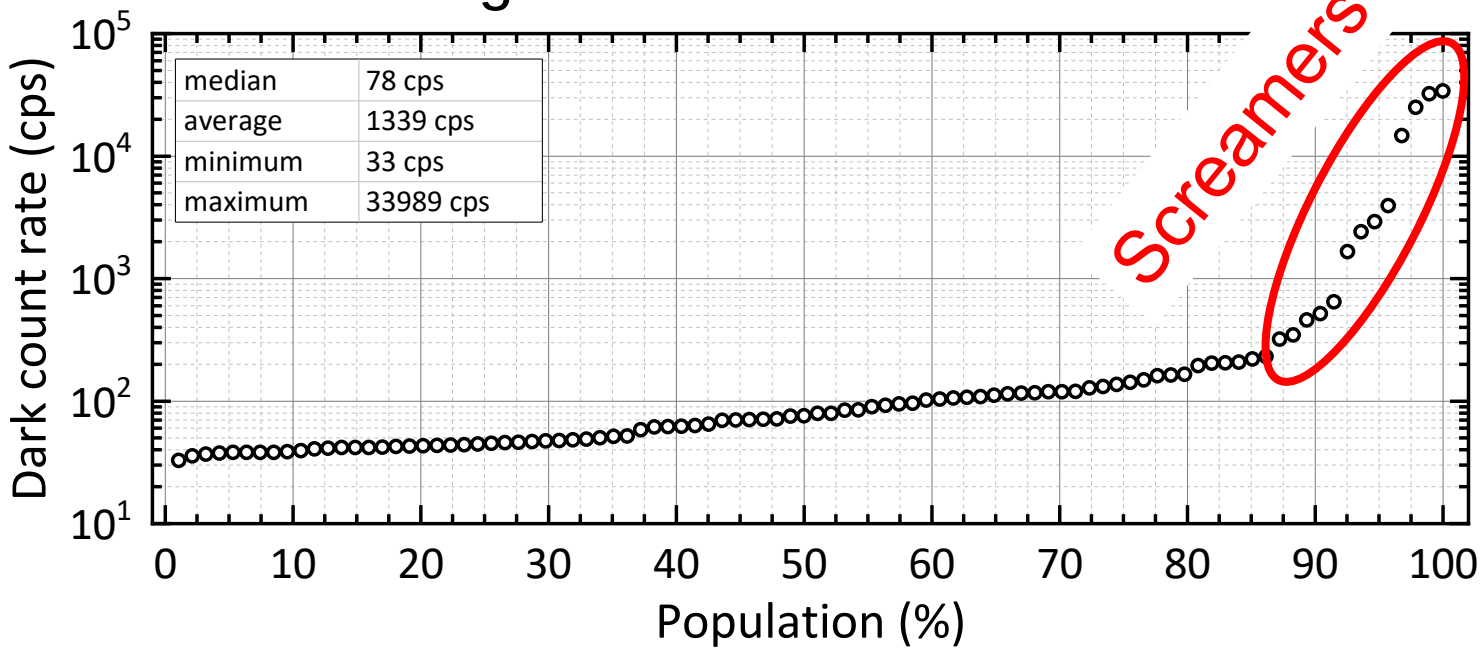

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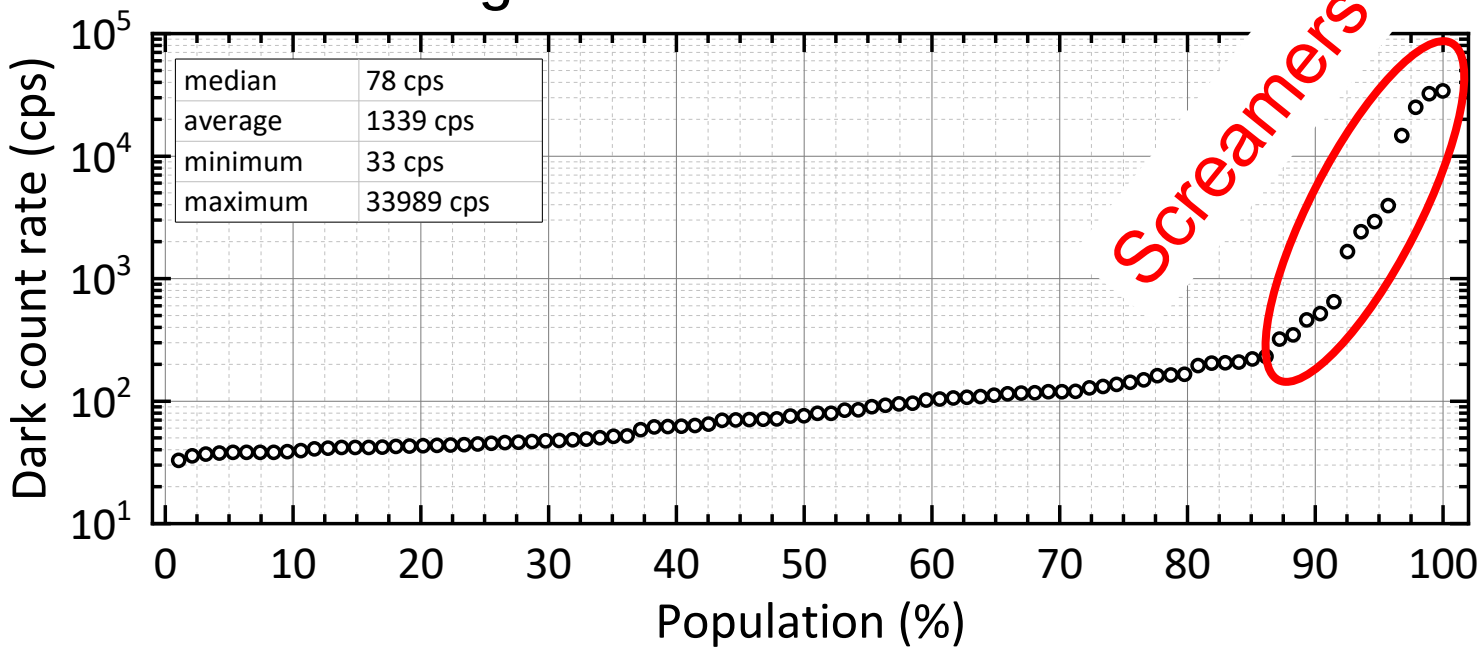
  - Lower overall DCR by disabling « screamers » [1]
  - Mitigation of afterpulsing with hold-off/recharge times
  - Better SNR, dead-time, …
- Decrease power consumption
  - Proportional to event rate



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Targetted Application and Different PDC flavors

UDS

Two main tracks for applications

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Low-power applications

- Cryogenic applications
- Large area (many m^2)
  - nEXO, DUNE, ARGO
- Photon-starved environments

180 nm CMOS

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Targetted Application and Different PDC flavors

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Low-power applications

- Cryogenic applications
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  - nEXO, DUNE, ARGO
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180 nm CMOS

Precise timing (<10 ps) applications

- ToF Medical Imaging (PET & CT)
- High event count, higher datarate
- Quantum Key Distribution and Wafefront Sensing
- Radiation hardness requirements

65 nm CMOS

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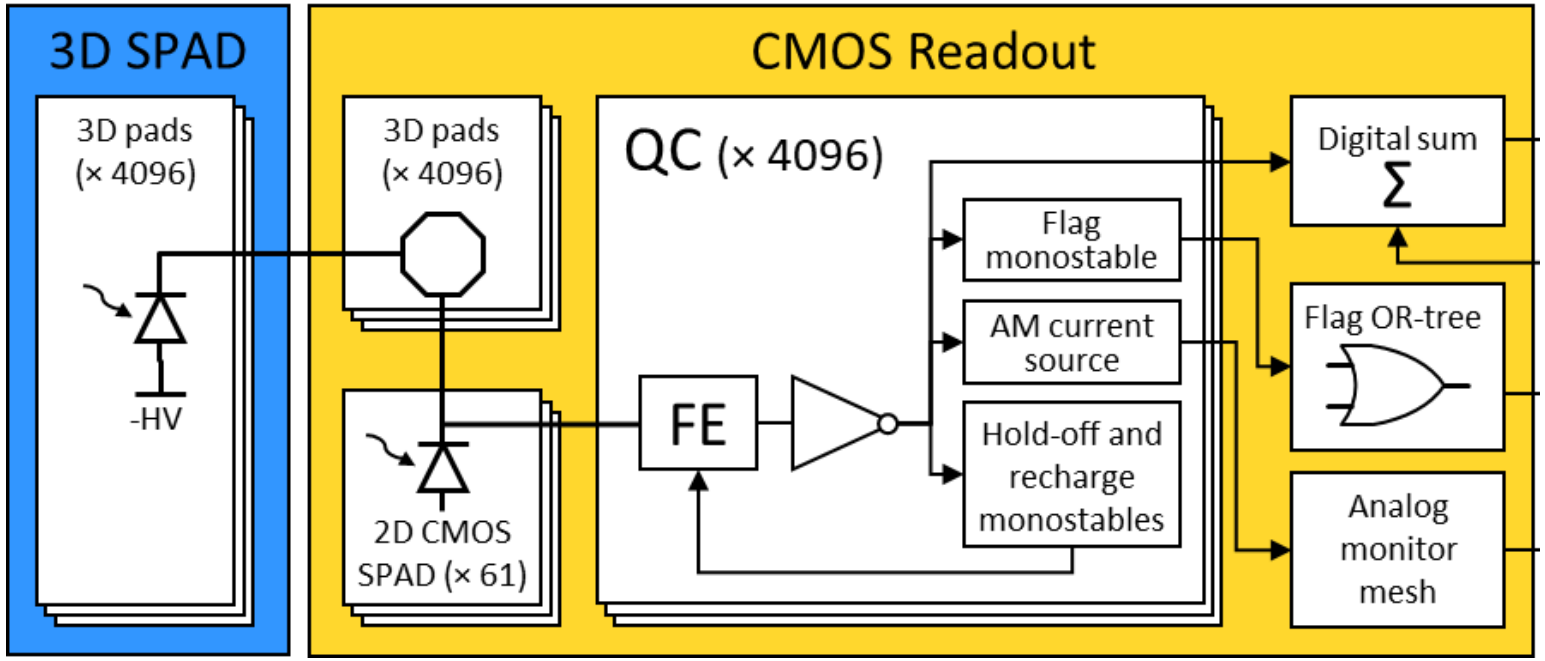
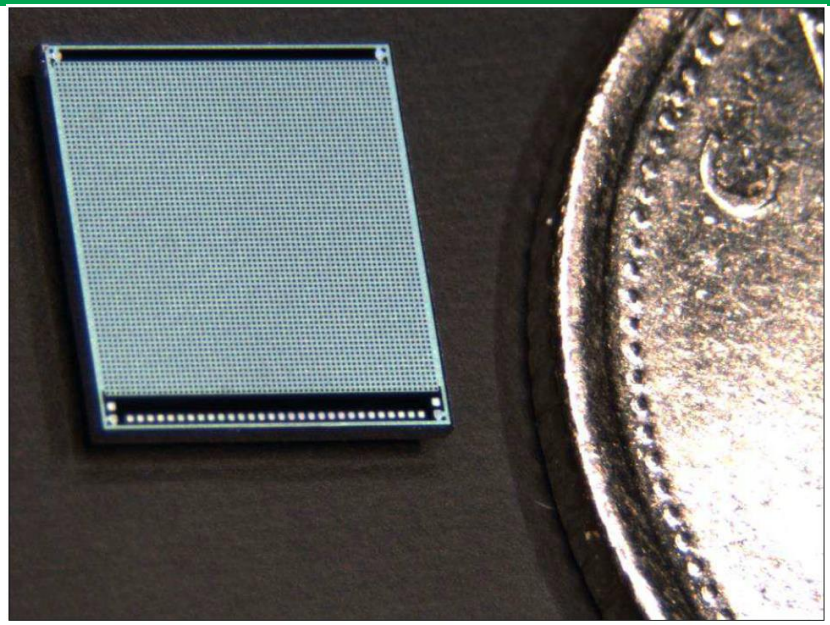
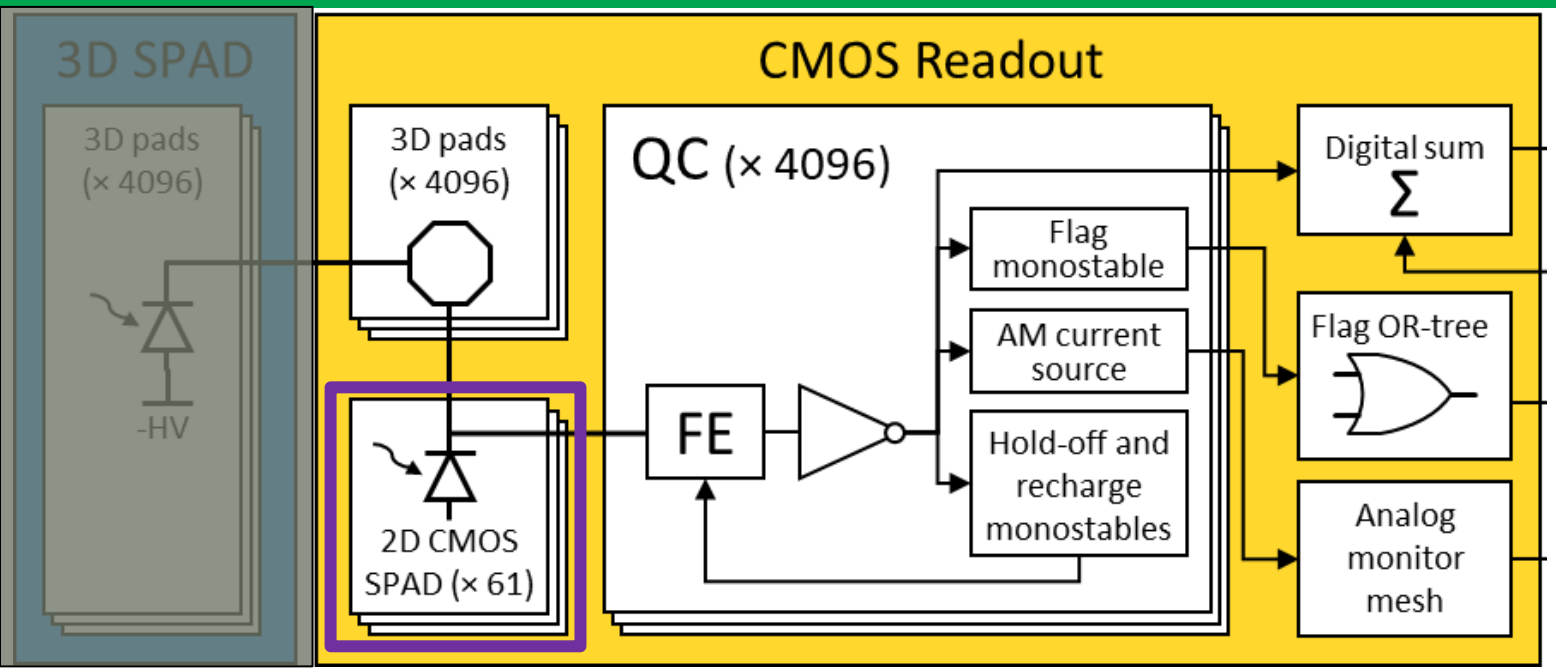
CMOS Readout Implementation (TSMC 180 nm)

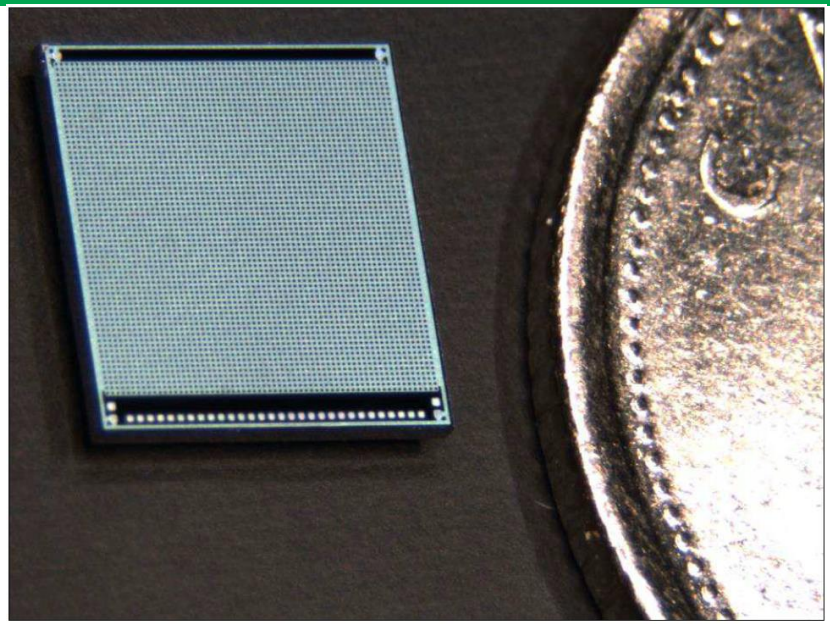




[2]

CMOS Readout Implementation (TSMC 180 nm)





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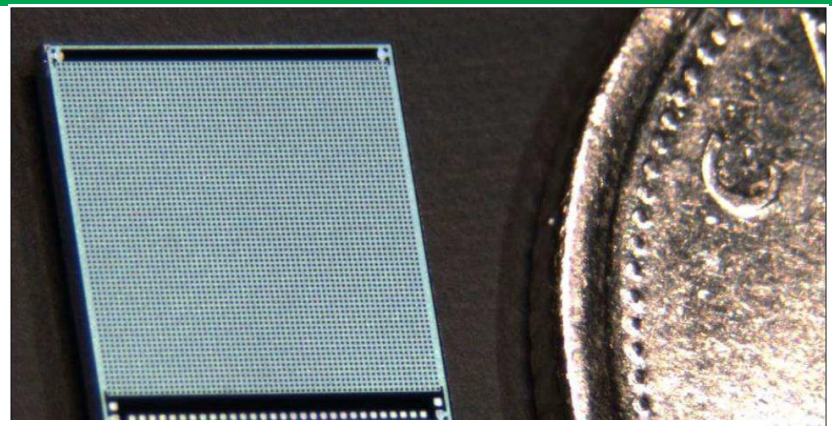

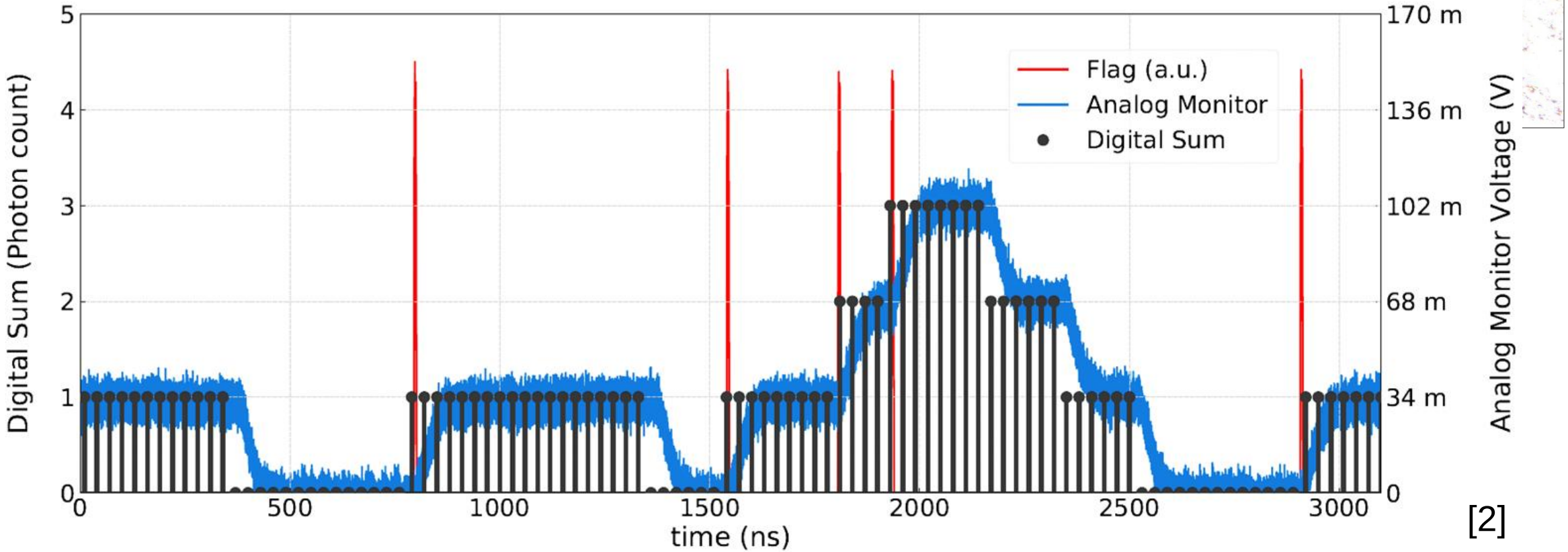

[2]

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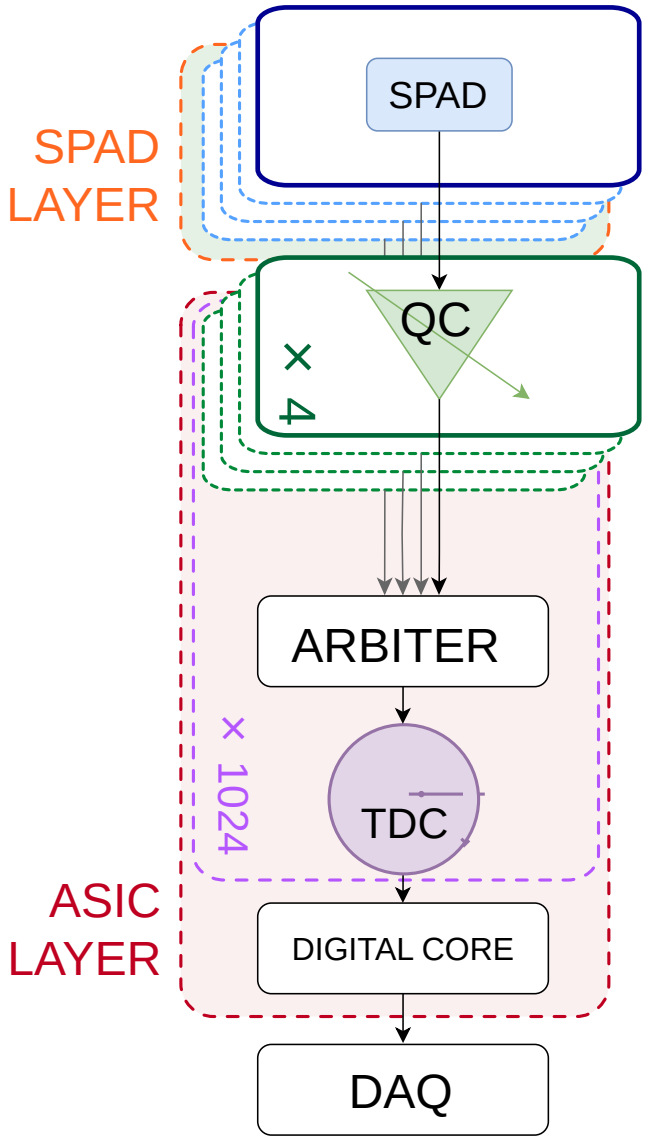
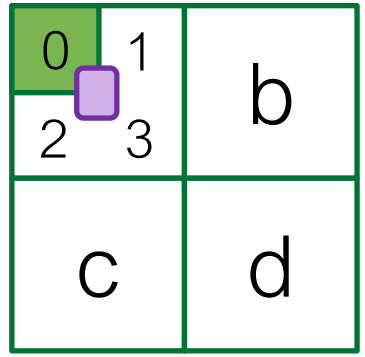
Future Implementation for Precise Timing Applications (TSMC 65 nm)



The future 5 × 5 mm² 65 nm PDC will feature:

- **Same SPAD layer** as 180 nm (4096 SPADs
- Expected **sub-10 ps QC timing jitter**;
- **Configurable holdoff and recharge duration**;
- 1 **Time-to-Digital Converter** (TDC) / 4 **pixels**
- Configurable **post-processing** modes



1 Macro-pixel
(16 pixels, 4 TDCs)

[3] Development of a Configurable Photon-to-Digital Converter in 65 nm, Raffaele Aaron Giampaolo,NSS-MIC-RTSD 2024

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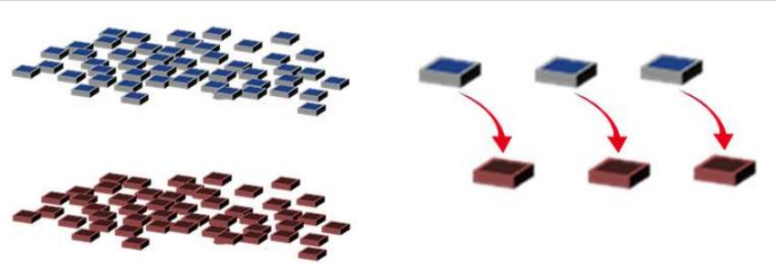
Available Technologies and Recent Trends

3D Integration for Image Sensors

[4] Rethinking boundaries: 3D integration and advanced packaging as performance drivers, Perceval Coudrain (CEA), ISSW2024, R01.3

3D Integration for Image Sensors

Die-to-Die



Known-good die
Heterogeneous
but…
Low throughput
Lower accuracy
High cost

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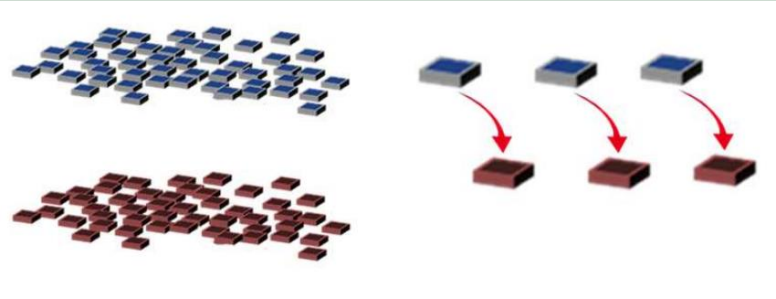
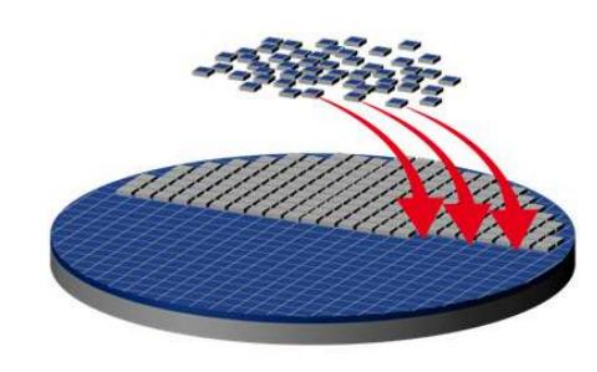
3D Integration for Image Sensors

Die-to-Die	Die-to-Wafer
	
Known-good die Heterogeneous but… Low throughput Lower accuracy High cost	Known-good die Heterogenenous but… Low throughput Need a breakthrough for accuracy for pitch required

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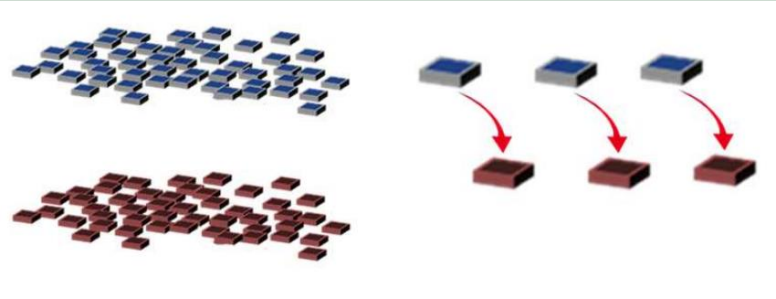
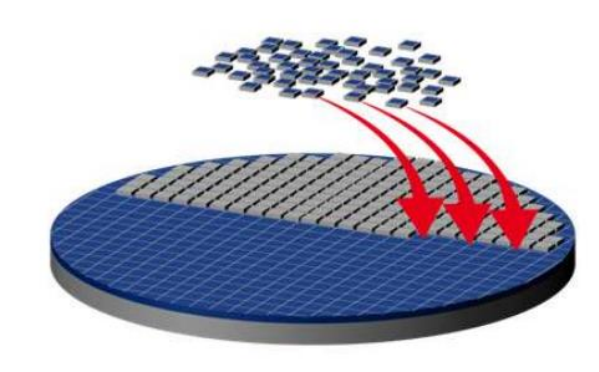
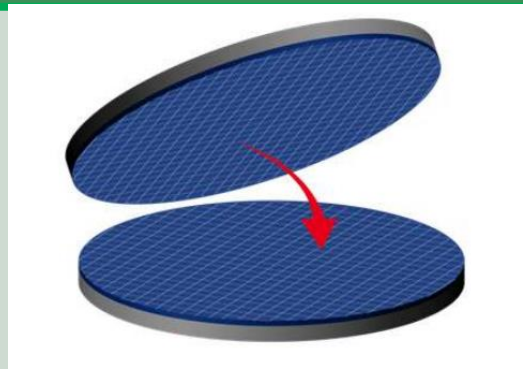
3D Integration for Image Sensors

Die-to-Die	Die-to-Wafer	Wafer-to-Wafer
		
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3D Integration for Image Sensors

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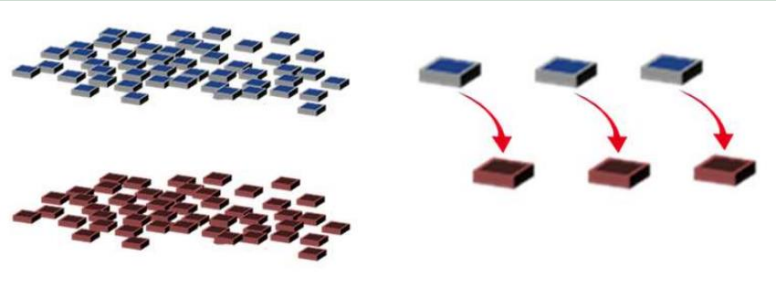	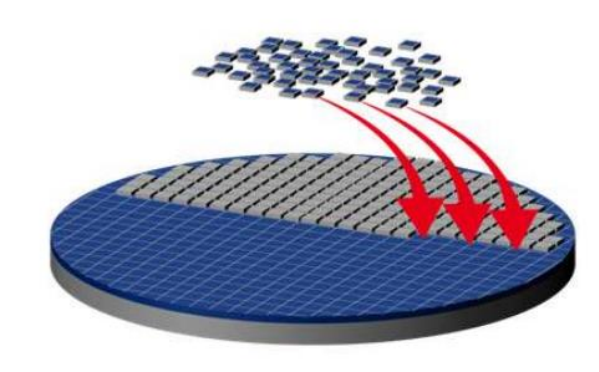	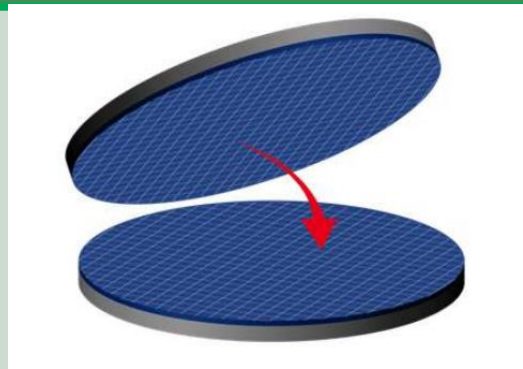
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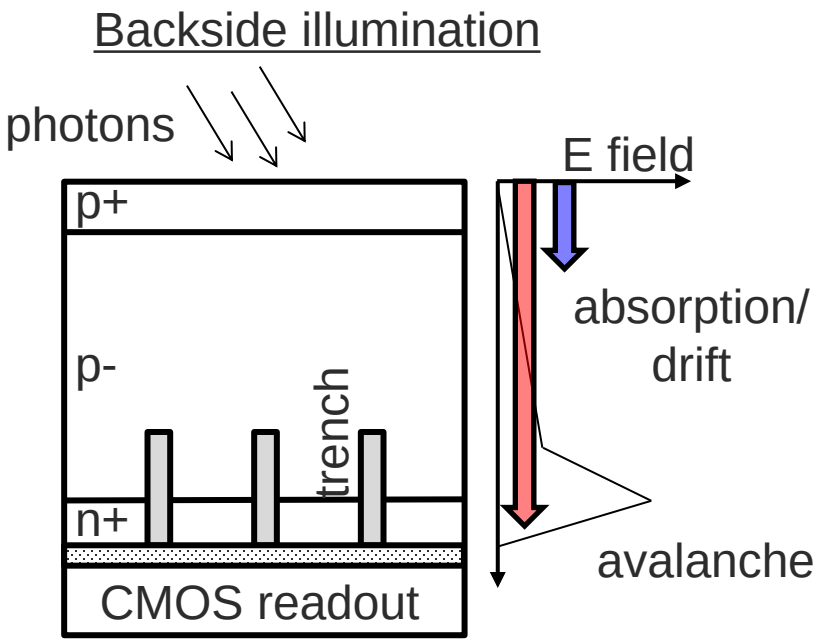
3D SPAD Array: Backside Illumination (BSI) vs Frontside Illumination (FSI)



PROS

- λ **range: red-NIR (LiDAR, camera)**
- high fill factor (FF)
- easy access to backside surface

CONS

- photoelectron drift (limited timing)
- cross-talk

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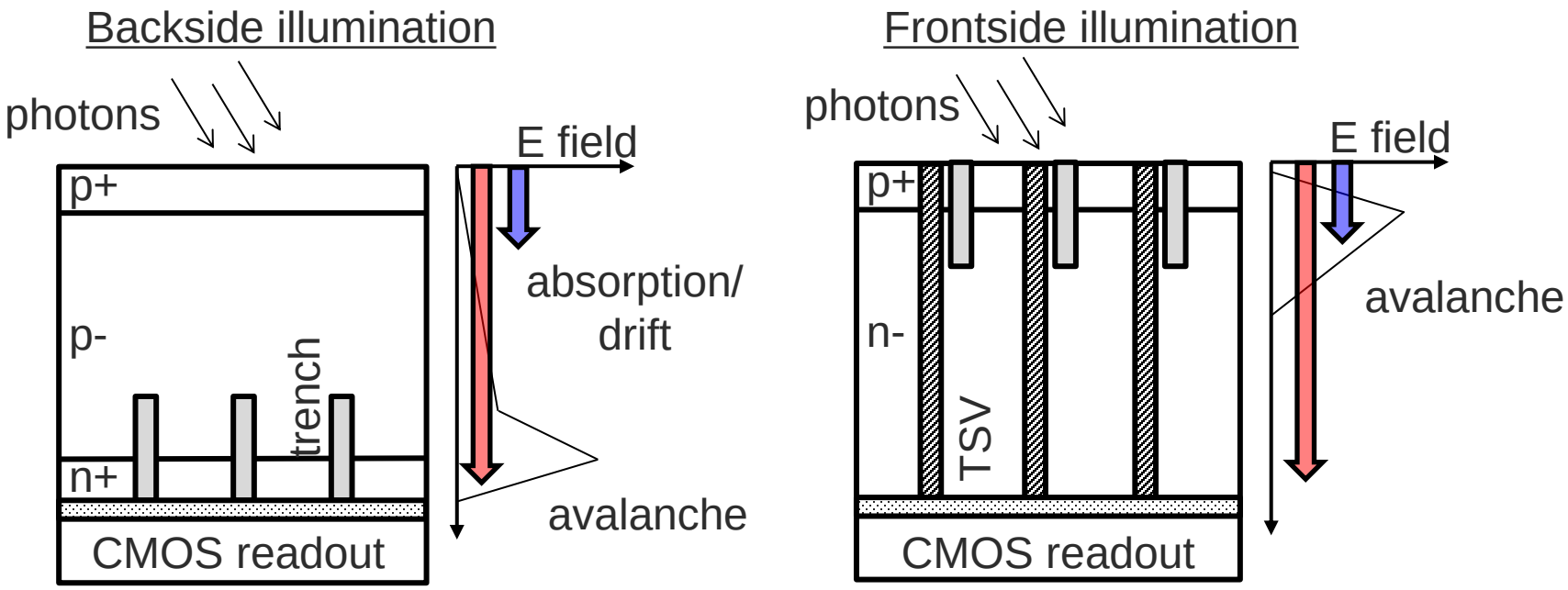

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- λ **range: red-NIR (LiDAR, camera)**
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- λ **range: blue-UV (our interest)**
- planar SPAD for timing resolution

CONS

- photoelectron drift (limited timing)
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- through silicon vias (lower FF, parasitics)

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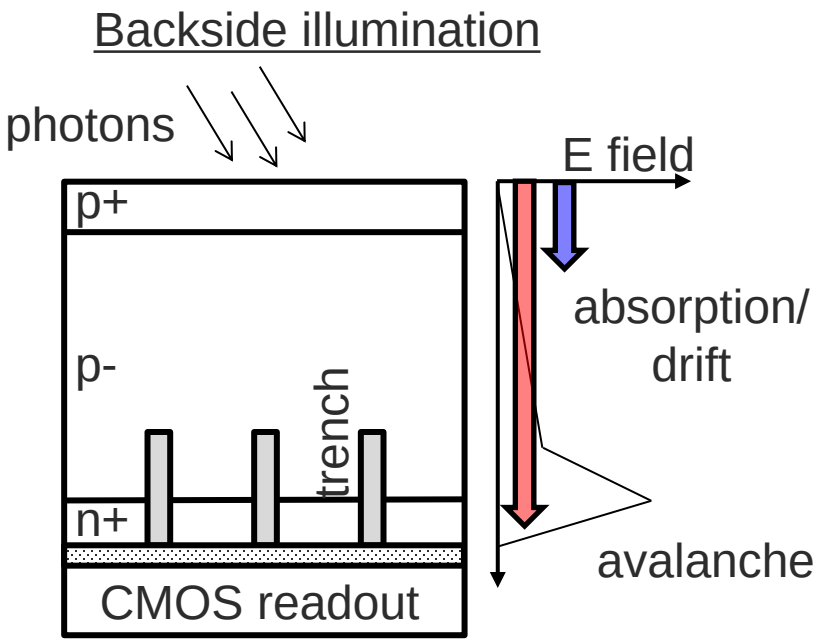

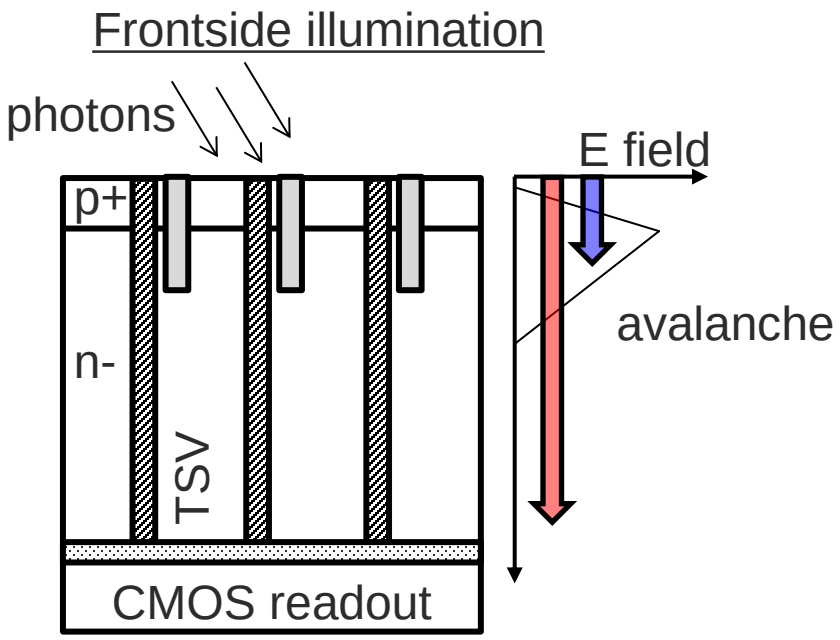

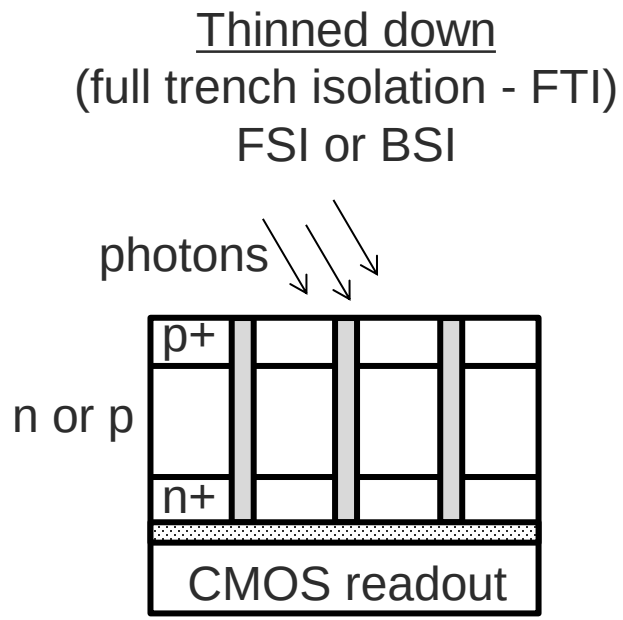

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- high fill factor (FF)
- easy access to backside surface

- **λ range: blue-UV (our interest)**
- planar SPAD for timing resolution

- **λ range: UV-VIS-NIR**
- timing resolution
  - less photoelectron drift
- high FF: no TSV

CONS

- photoelectron drift (limited timing)
- cross-talk

- through silicon vias (lower FF, parasitics)

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Industry trends: Camera and LIDAR

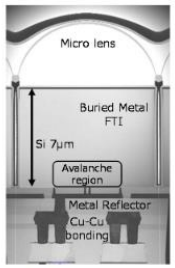
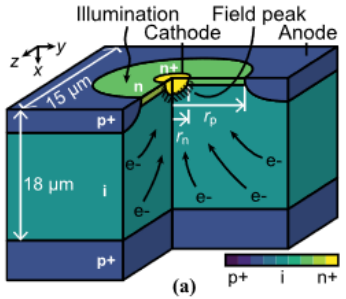


Fig. 3 Pixel cross-section view

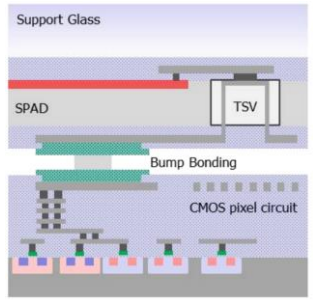
[5]

A Back Illuminated 10µm SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm
K. Ito et. al. (**Sony**), 2020.



[9]

A Near-Infrared Enhanced Silicon Single-Photon Avalanche Diode With a Spherically Uniform Electric Field Peak
E. Van Sieleghem, et. al. (**IMEC, OmniVision**), 2021.



[10] Silicon hybrid SPAD with high-NIR-sensitivity for TOF applications
T. Baba, et. al. (**Hamamatsu Photonics K.K.**), 2017.

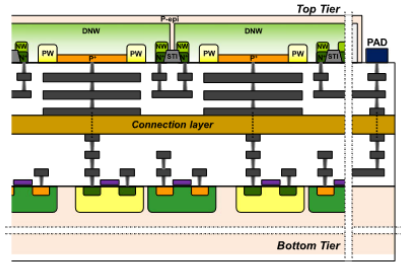


Fig. 3. Cross section of the proposed back-illuminated 3D-integrated SPAD.

[6]

High-Performance Back-Illuminated Three-Dimensional Stacked Single-Photon Avalanche Diode Implemented in 45-nm CMOS Technology
M.-J. Lee, et. al. (**EPFL, TUDelft, TSMC**), 2018.

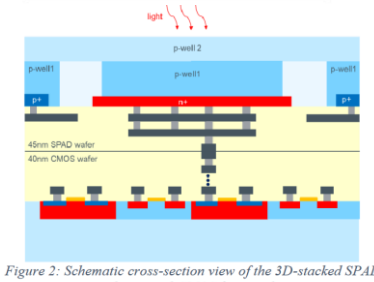


Figure 2: Schematic cross-section view of the 3D-stacked SPAD device and CMOS front-end.

[11] A Reconfigurable QVGA/Q3VGA Direct Time-of-Flight 3D Imaging System with On-chip Depth-map Computation in 45/40nm 3D-stacked BSI SPAD CMOS
D. Stoppa, et. al. (**ams OSRAM**), 2021.

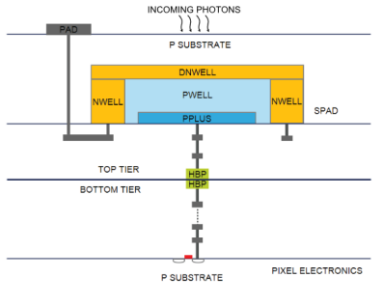


Fig. 1. p-well/deep n-well SPAD [6] in 65/40 nm 3D IC CMOS technology.

[7]

A High-PDE, Backside-Illuminated SPAD in 65/40-nm 3D IC CMOS Pixel With Cascoded Passive Quenching and Active Recharge
S Lindner, et. al. (**EPFL, STMicro**), 2017.

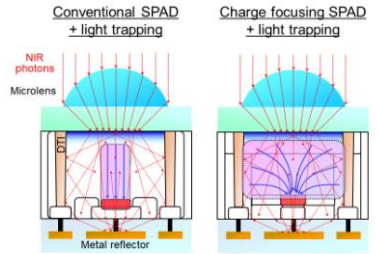


Fig. 2. Cross-sectional views of conventional BSI SPAD (left) and BSI charge focusing SPAD (right) with light trapping technique.

[12] 3.2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing
K. Morimoto, et. al. (**Canon Inc**), 2021.

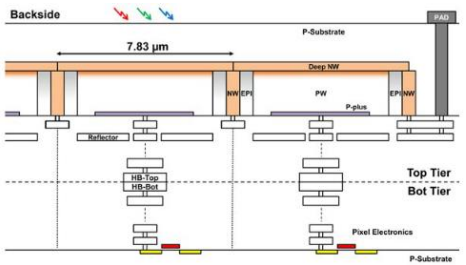
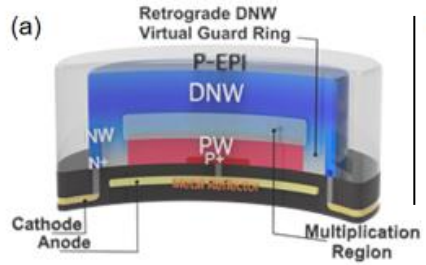


Fig. 4. Array layout cross section.

[8]

Backside Illuminated SPAD Image Sensor with 7.83µm Pitch in 3D-Stacked CMOS Technology
T. Al Abbas, et. al. (**Uni. Edinburg, STMicro**), 2016.

And more…



[13] Back-Illuminated SPADs in Stacked 40nm CIS Technology
M.-J. Lee, et. al. (**KIST, Uni. Yonsei, SK hynix**), 2022.

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Radiation Instrumentation/Large-Area Experiments (E. Charbon, C. Bruschini, EPFL)

3D-stacked frontside-illuminated (FSI) multi-channel digital silicon photomultipliers (MD-SiPM) at EPFL

- Top- and bottom-tier in 0.18 µm CMOS technology
- 3D integration: Through-silicon vias (TSVs) and bump-bonds

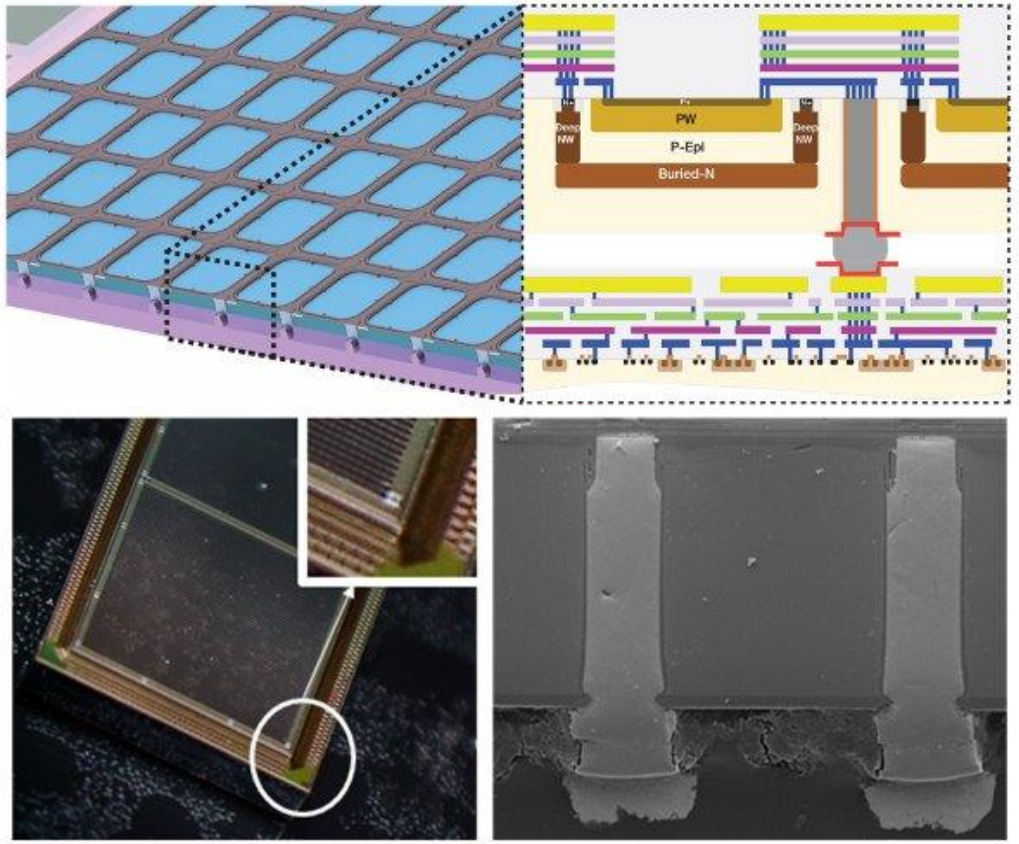

Fig. 1. *Top:* the top tier houses square SPADs with rounded corners and is 3D-stacked to the bottom-tier chip (*left*). The bonding with the bottom-tier chip is ensured through TSVs and micro-bump connections (*right*). *Bottom:* Optical microscope image of the final implementation *(left);* SEM image of the cross section (*right*).

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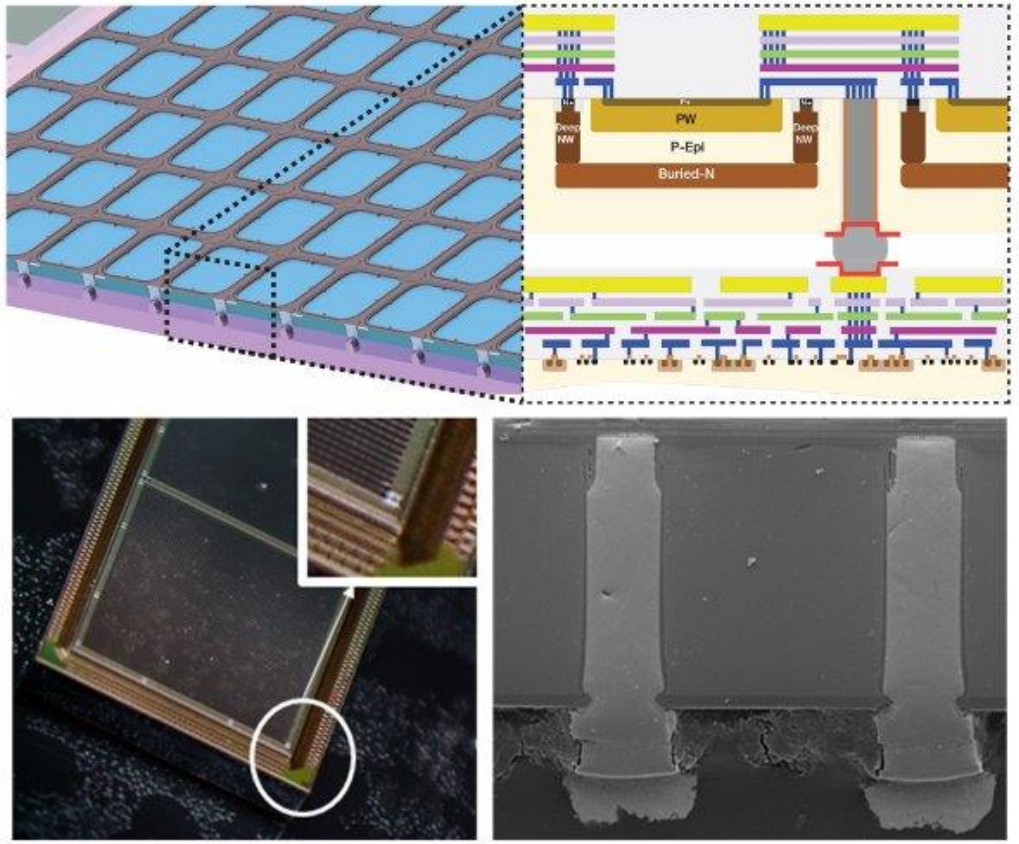
  - 50 µm pitch, 67% fill factor
  - 2x arrays 64x64 SPADs (8x8 cluster of 64 pixels)
  - Vbr: 22 V
  - peak PDP: 55% at 500 nm at Vov = 6 V



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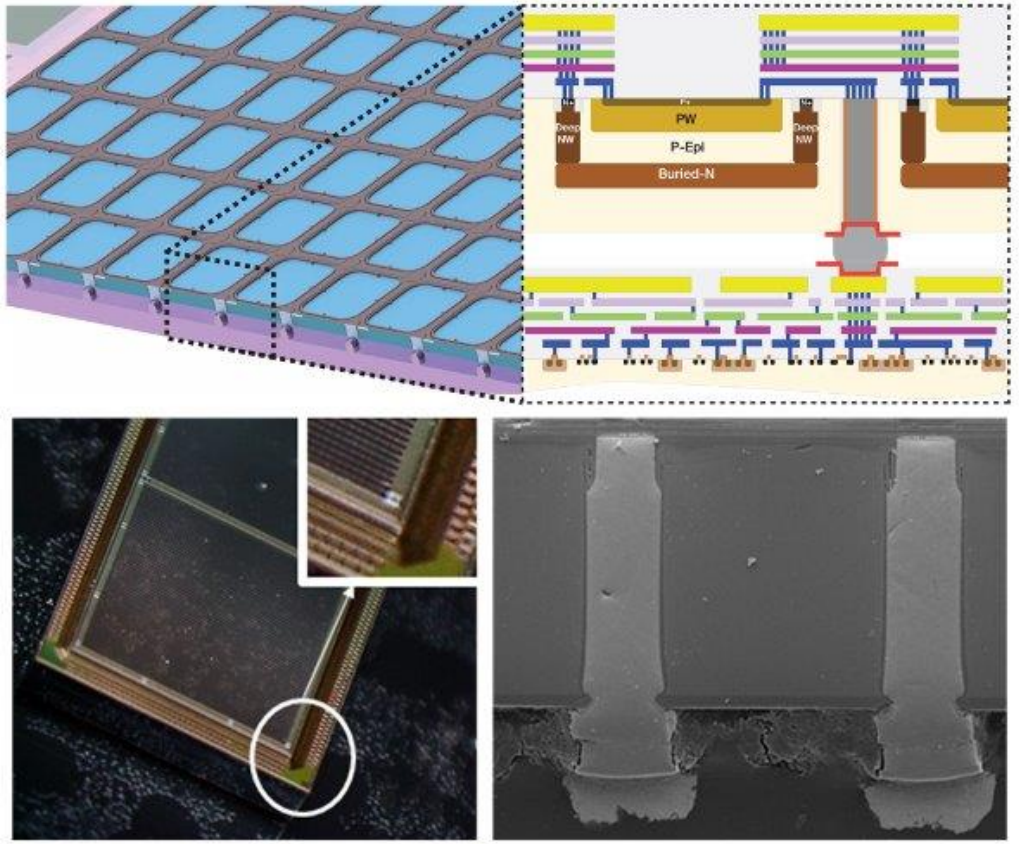
- Bottom-tier: readout electronics
  - SPAD address tree
  - photon counters
  - time-to-digital converters + calibration
  - data distribution
  - readout scheduler



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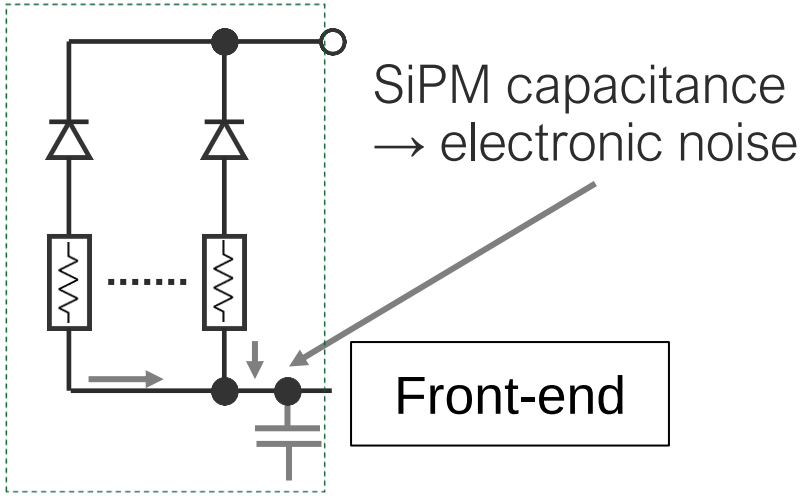
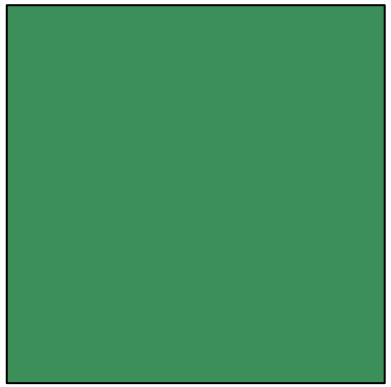
Other Approaches – SiPM Segmentation

Conventional SiPMs



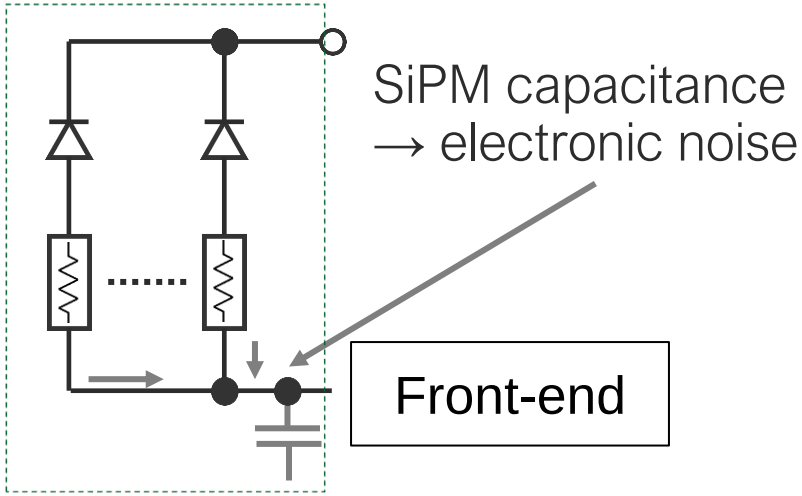


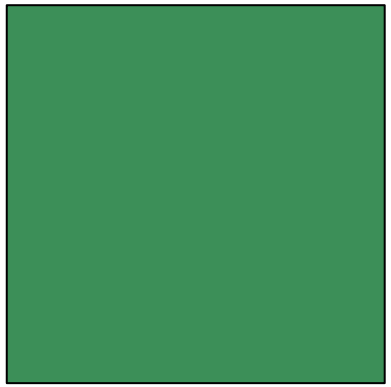
Single SiPM

Gabriel.Lessard@USherbrooke.ca

Other Approaches – SiPM Segmentation

Conventional SiPMs





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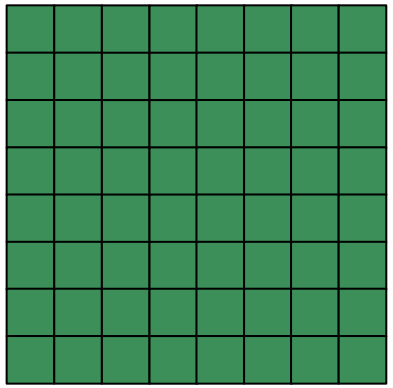

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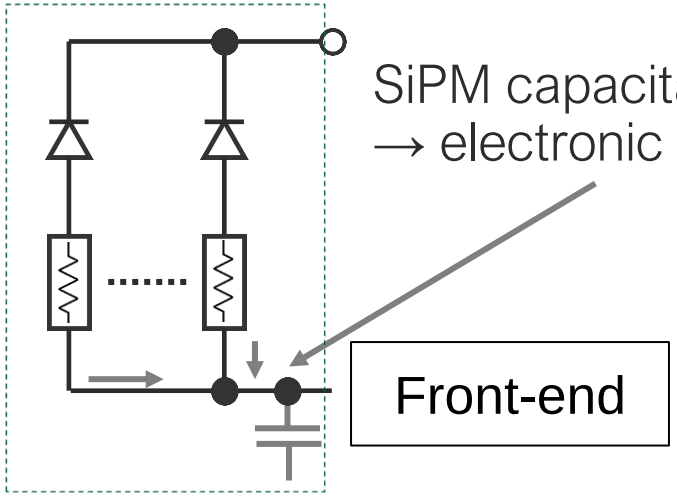
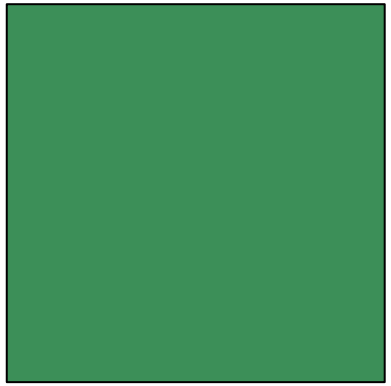


SiPM capacitance
→ electronic noise

→

Less SPADs/F.E.
→ lower capacitance
→ lower noise



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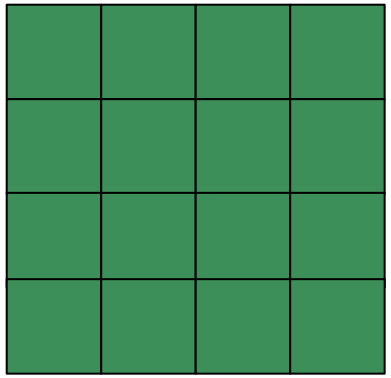
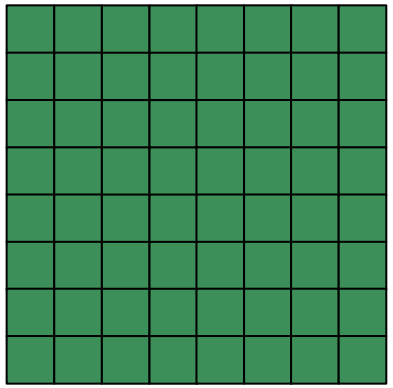


Segmented



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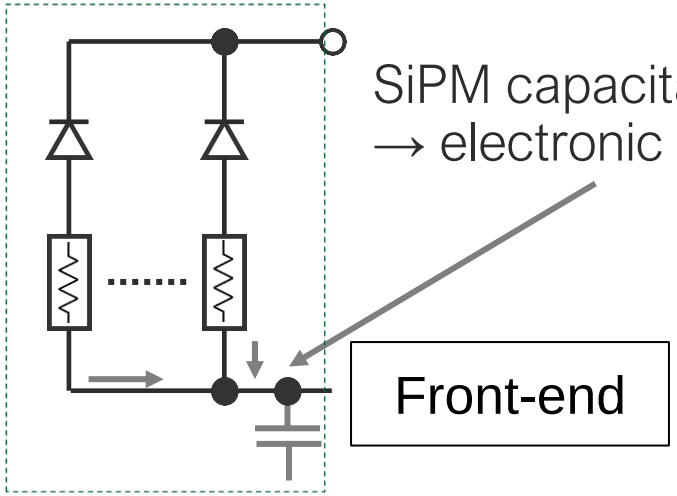

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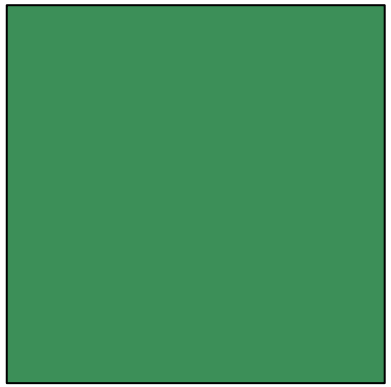
Same goal of large area, high fill factor



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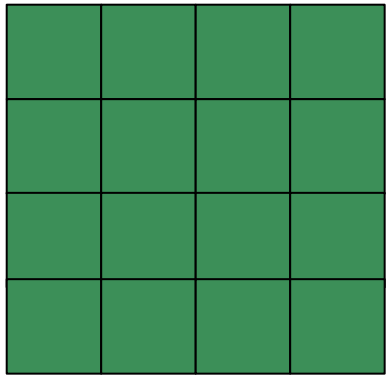

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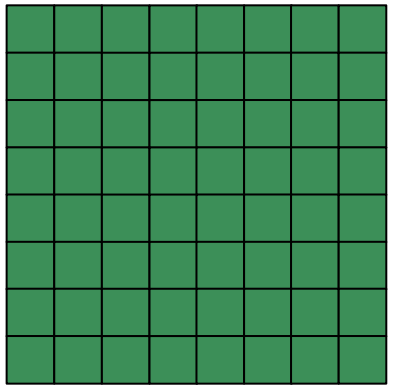

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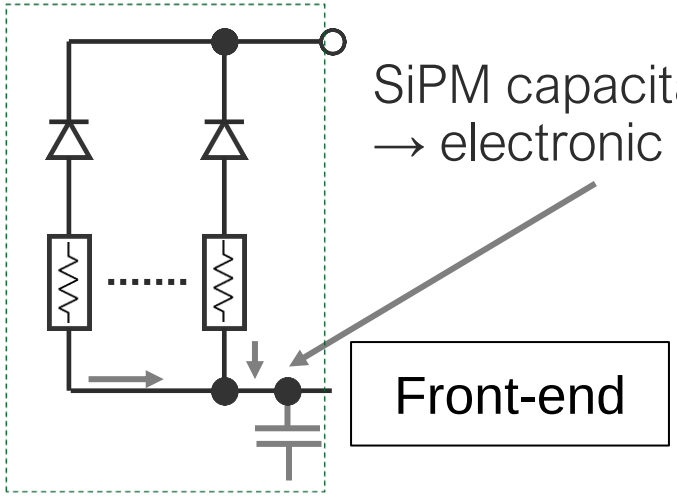
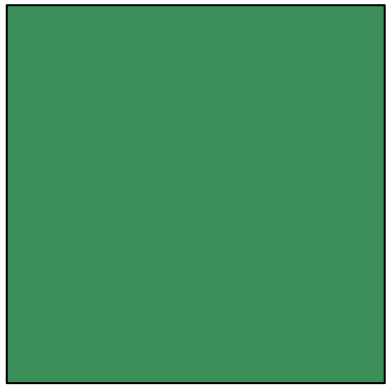


SiPM capacitance
→ electronic noise

What is the optimal segmentation for a given area?

Less SPADs/F.E.
→ lower capacitance
→ lower noise

Same goal of large area, high fill factor



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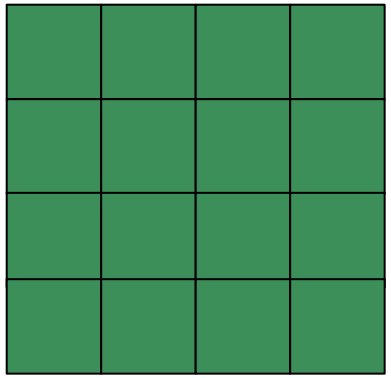

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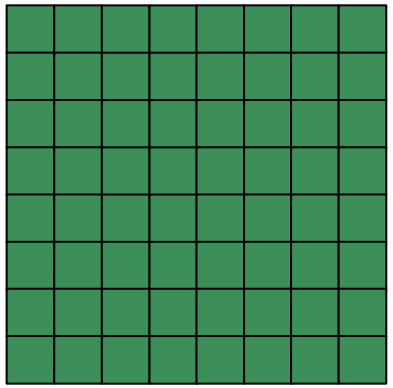
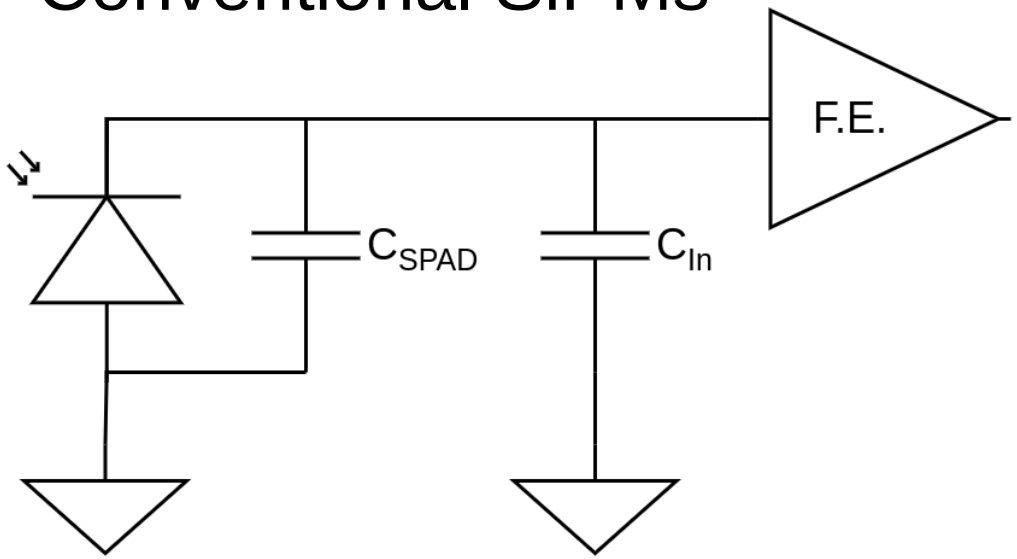


Individual SPADs

Other approaches – SiPM Segmentation Optimization

Conventional SiPMs



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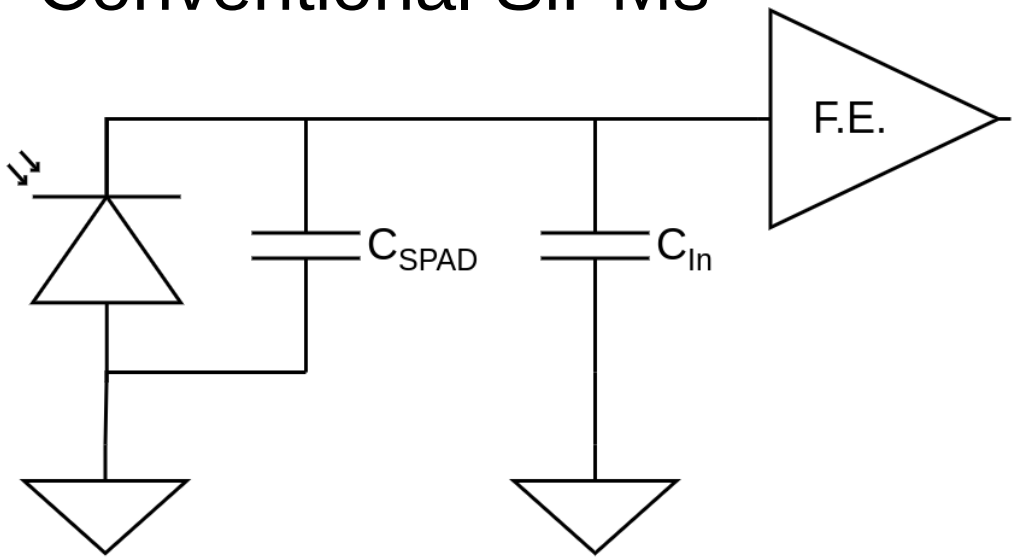

Single array:

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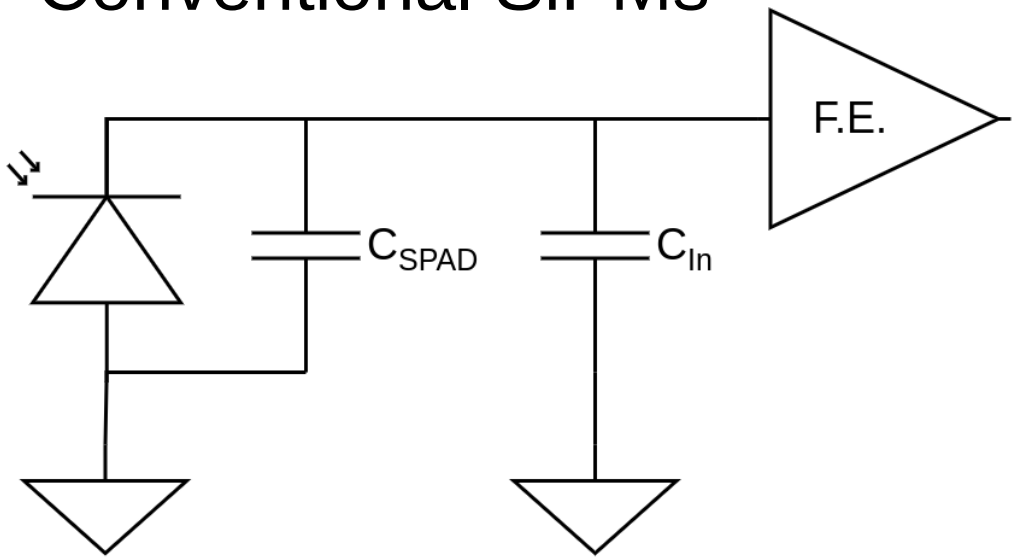
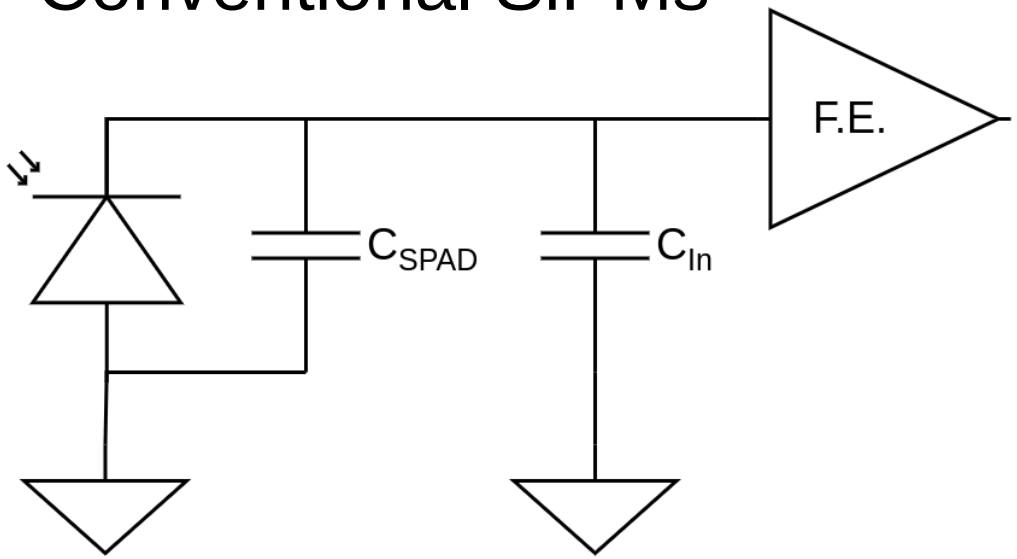


Single array:

$$P \propto [C_{SPAD} + C_{In}]^2$$

Other approaches – SiPM Segmentation Optimization

Conventional SiPMs



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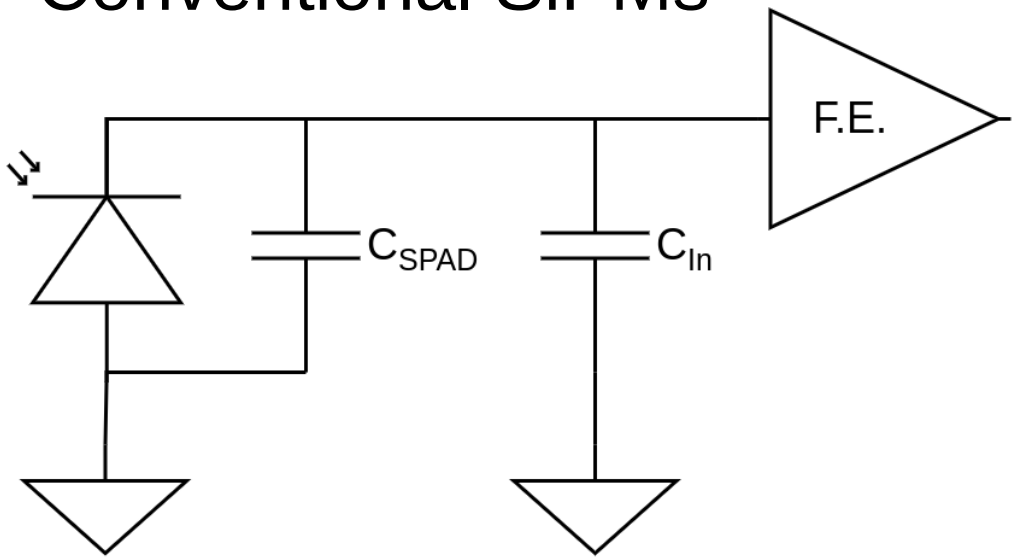

Single array:

$$P \propto [C_{SPAD} + C_{In}]^2$$

Segmented array:

$$P(N_{seg}) \propto \sum^{N_{seg}} \left[\frac{C_{SPAD}}{N_{seg}} + C_{In}\right]^2$$

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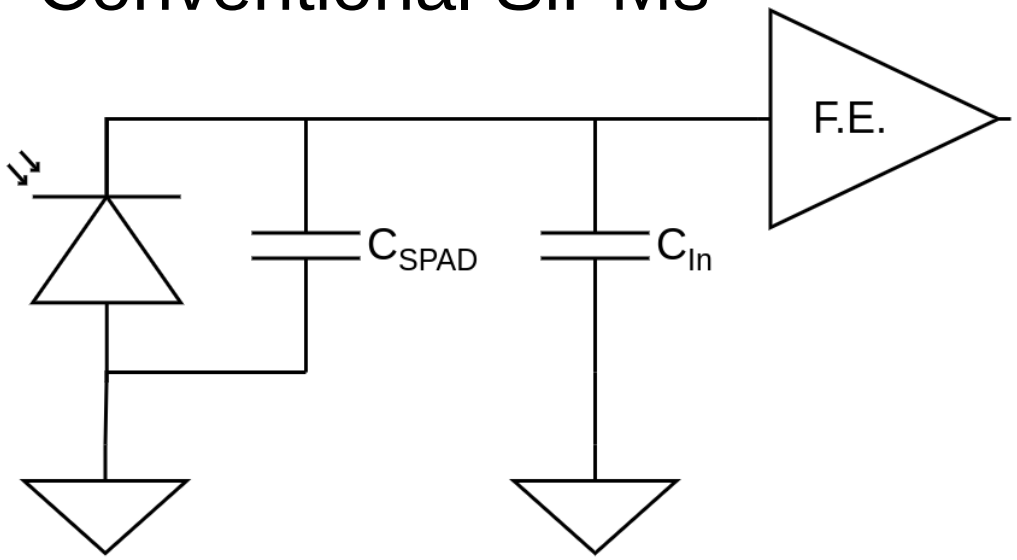
Other approaches – SiPM Segmentation Optimization

Conventional SiPMs



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How can C_{in} be optimised… ?

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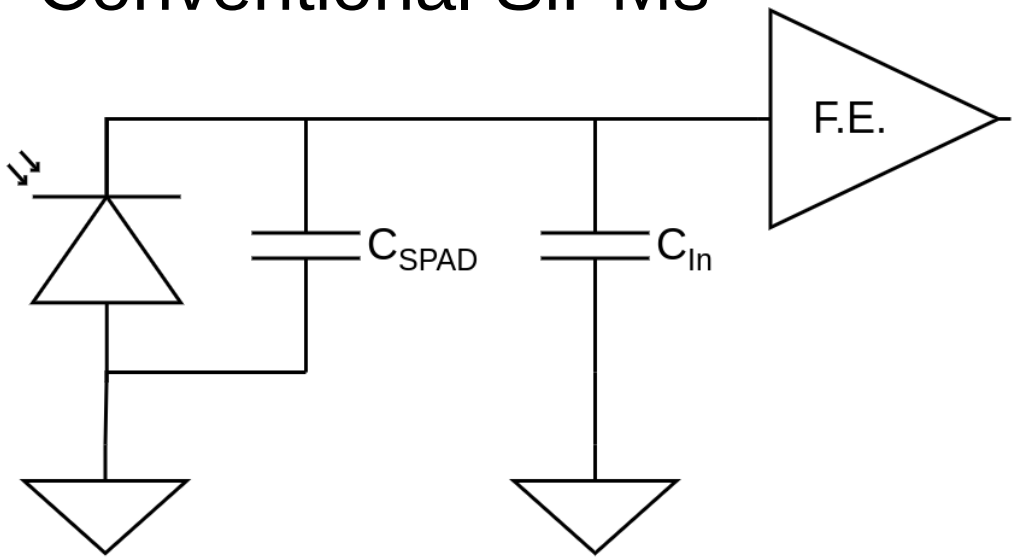
Other approaches – SiPM Segmentation Optimization

UDS

Conventional SiPMs



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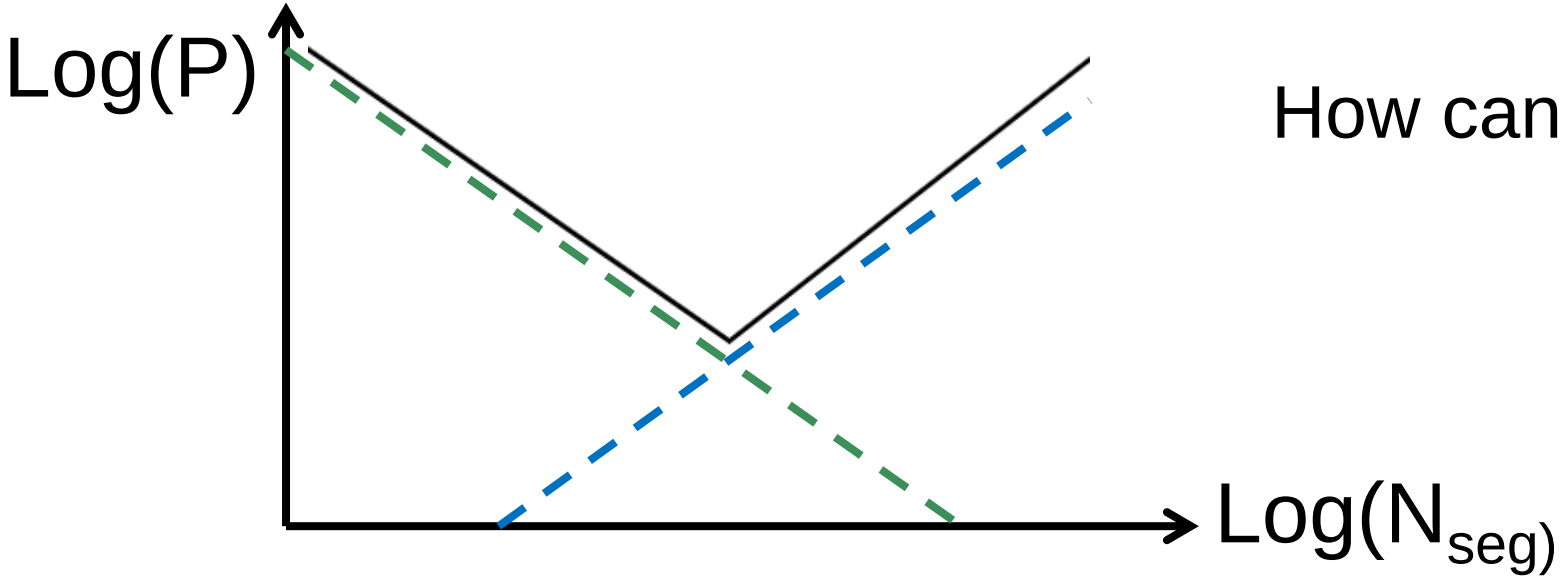

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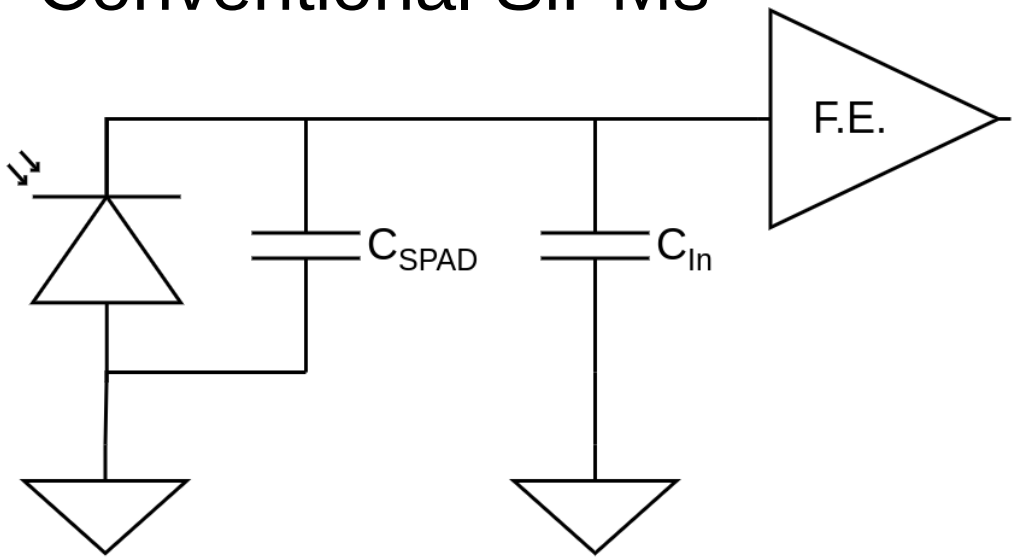

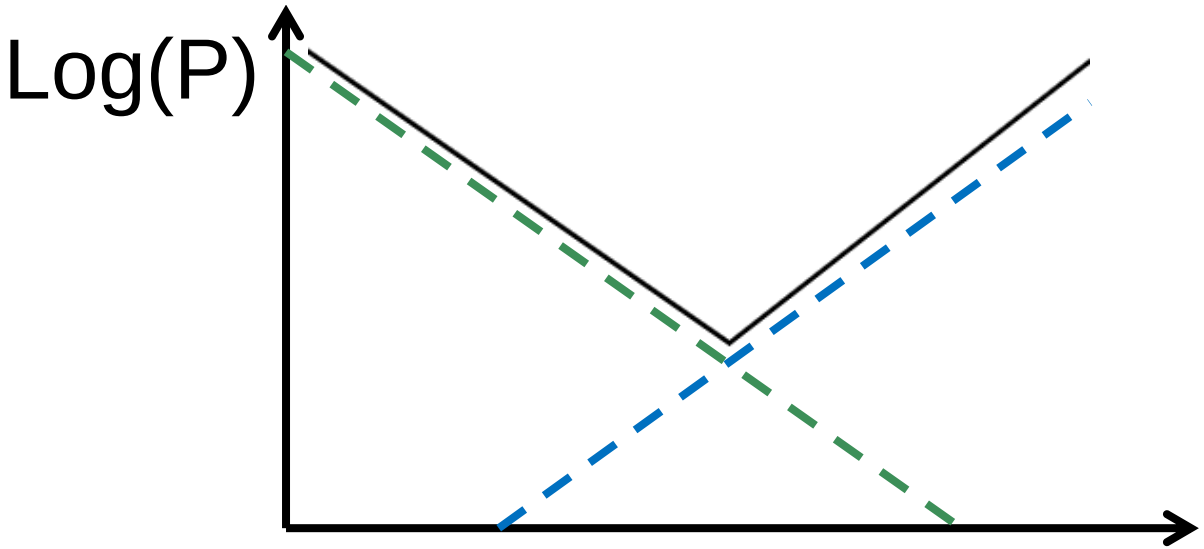

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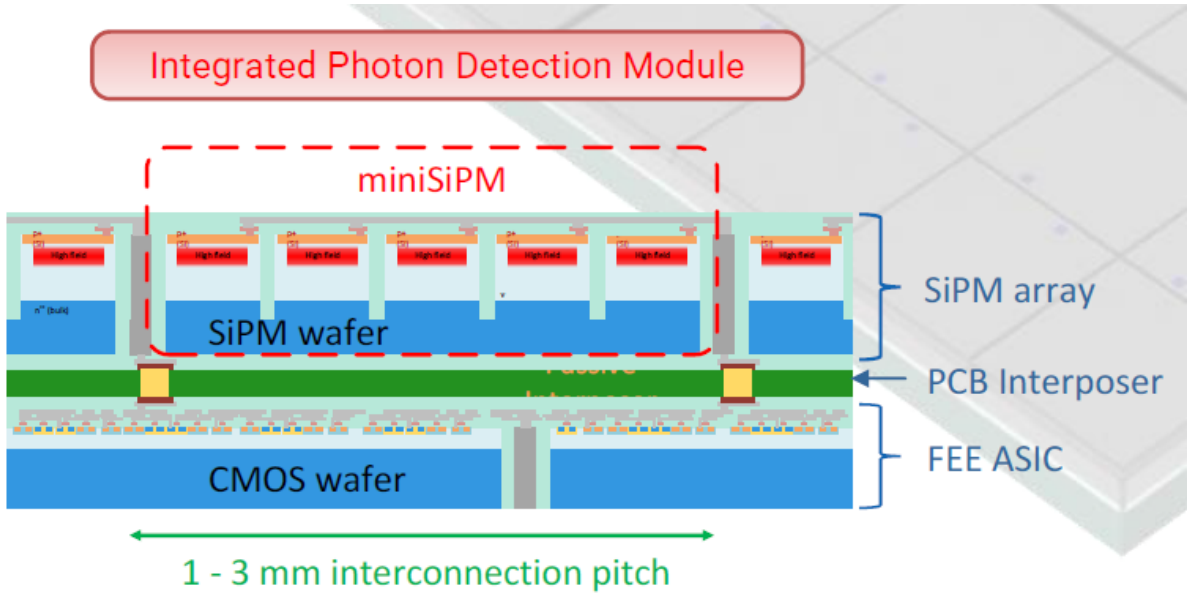
How can C_{in} be optimised… ?

For what N_{seg} do you reach the optimal power consumption?

Gabriel.Lessard@USherbrooke.ca

Segmented SiPM for 3D integration

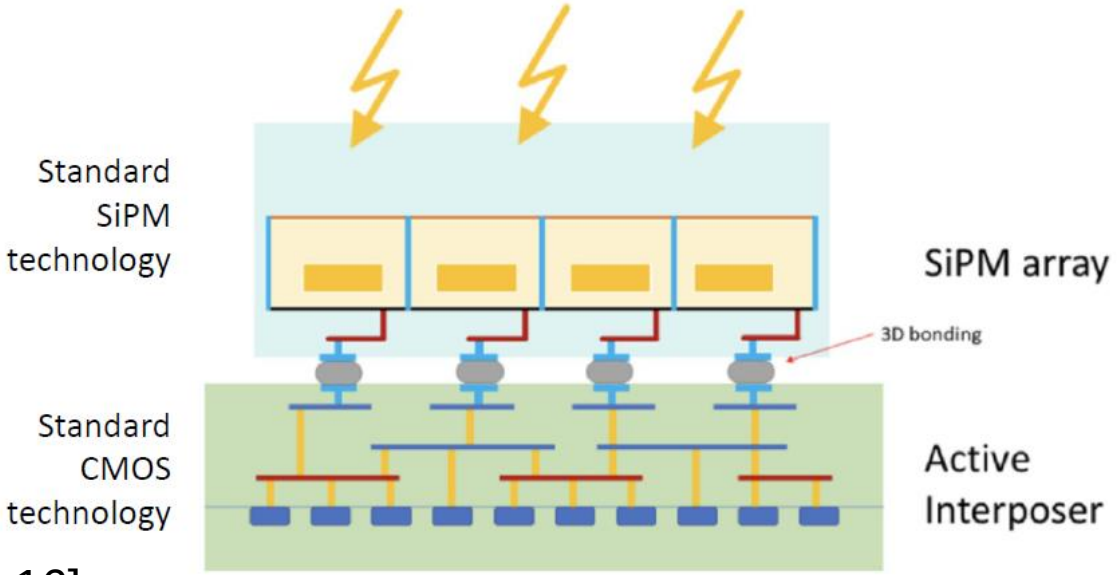
- Coarser pitch for interconnects
- Interposer strategies
  - Passive - PCB
  - Active - CMOS



FONDAZIONE BRUNO KESSLER
FUTURE BUILT ON KNOWLEDGE

A. Gola, next presentation

and partners…



[15,16]

Our 3D Bonding Process

Our strategy for wafer to wafer

Combining high-end optoelectronic process (CCD) with MEMS-type 3D integration technologies

3 substrates, 2 wafer bonding steps, 16 masks and >350 fabrication steps

All at Teledyne DALSA facility (Bromont, Québec)

SPAD

1.SPAD frontend (p^+n & trenches)

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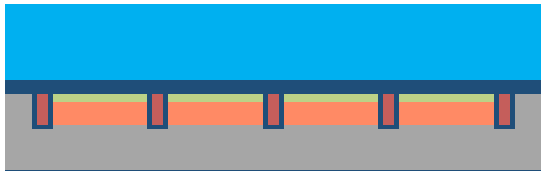

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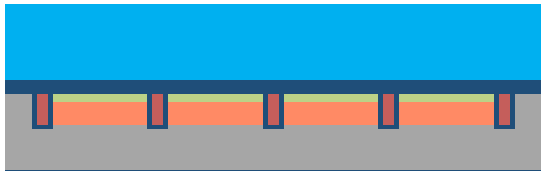

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3. SPAD backside thinning

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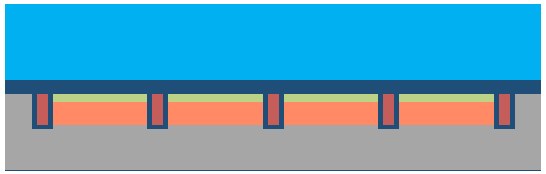

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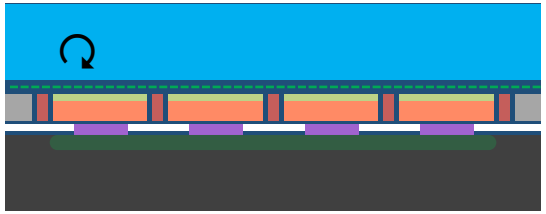

4. Al-Ge wafer-to-wafer 3D bonding

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SPAD
Handle
CMOS

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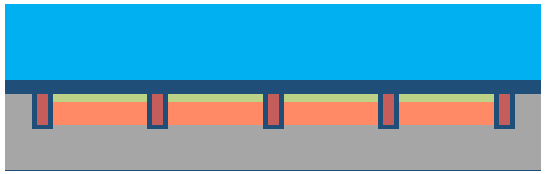

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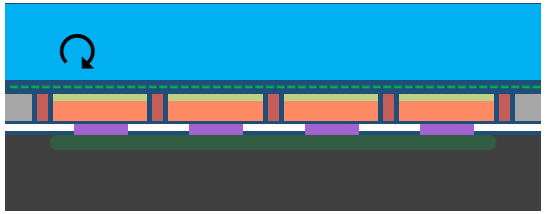
3. SPAD backside thinning



4. Al-Ge wafer-to-wafer 3D bonding

5. Handle wafer removal

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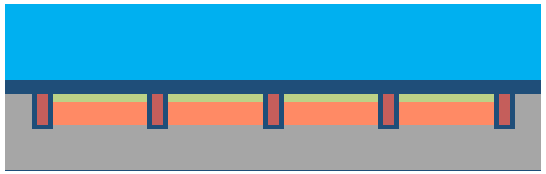
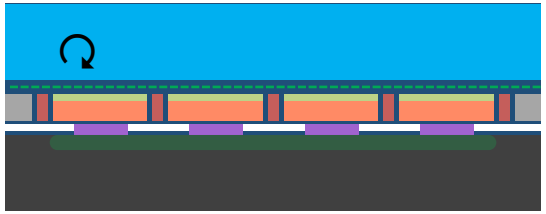


2. Handle wafer direct bonding

3. SPAD backside thinning



4. Al-Ge wafer-to-wafer 3D bonding

5. Handle wafer removal

6. SPAD backend (metal contacts)

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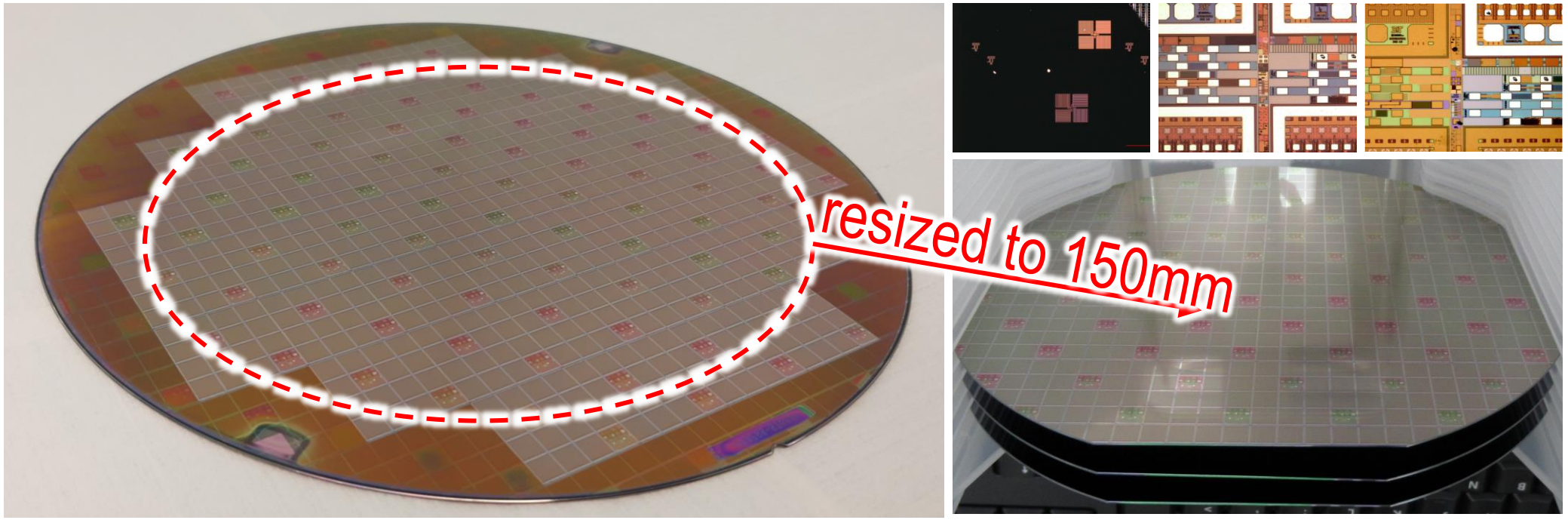
Our strategy for wafer to wafer - alignment

- Wafer size mismatch between TSMC and DALSA*
- 2 dies in 4x4 shot reserved for PCM structures
  - Alignment
  - Process Control Monitoring (PCM)



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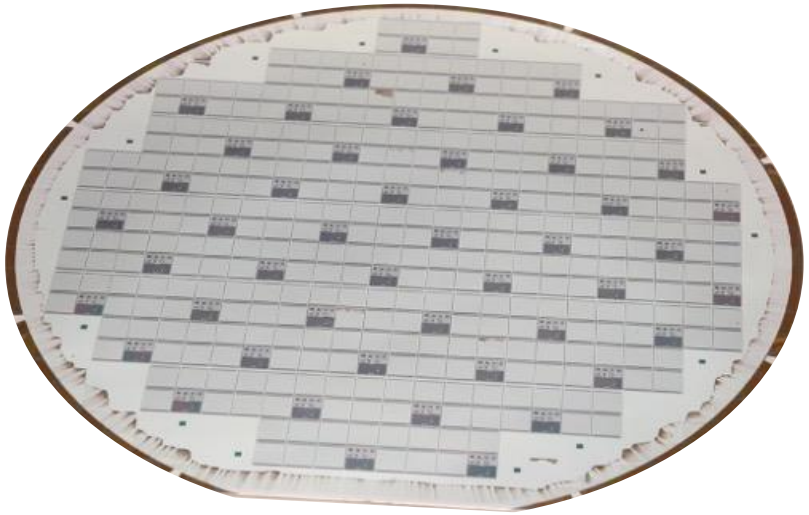
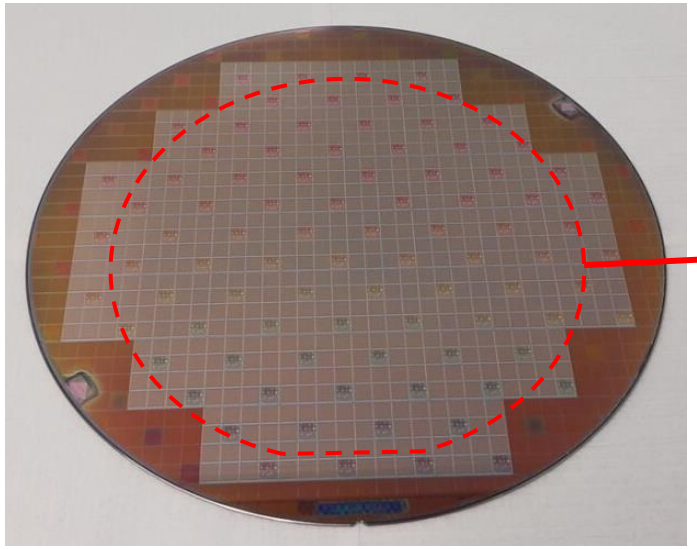
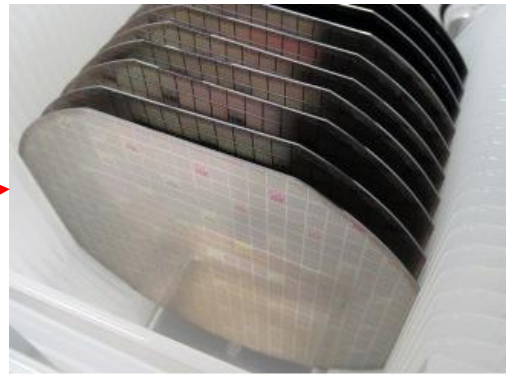
Finally, pictures of a real bonded PDCs!



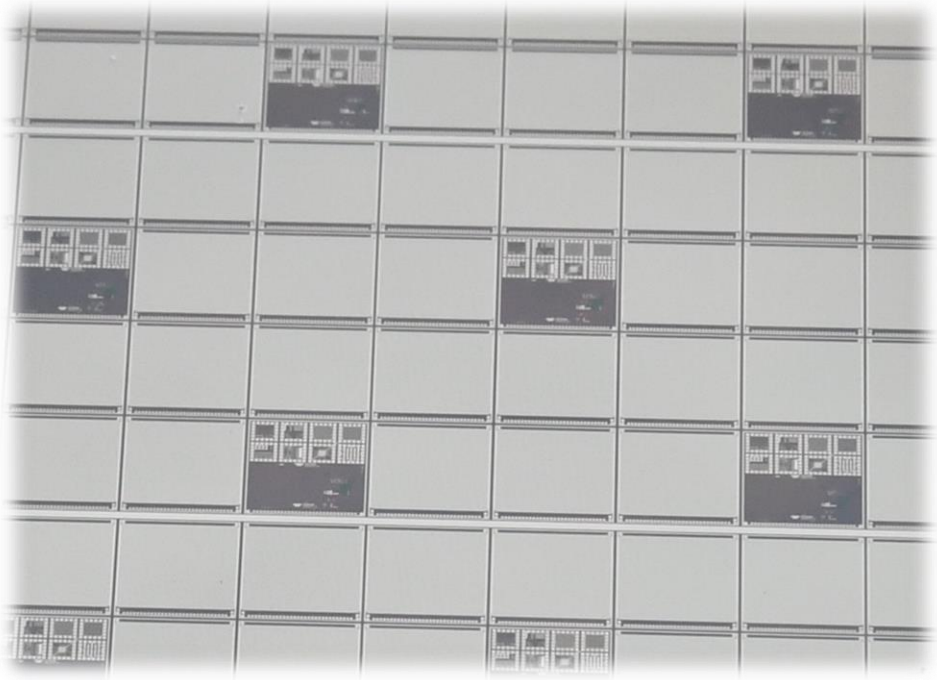
First 3D bonded wafers, received October 13th



200 mm TSMC 180 nm CMOS wafer



Resized to 150 mm



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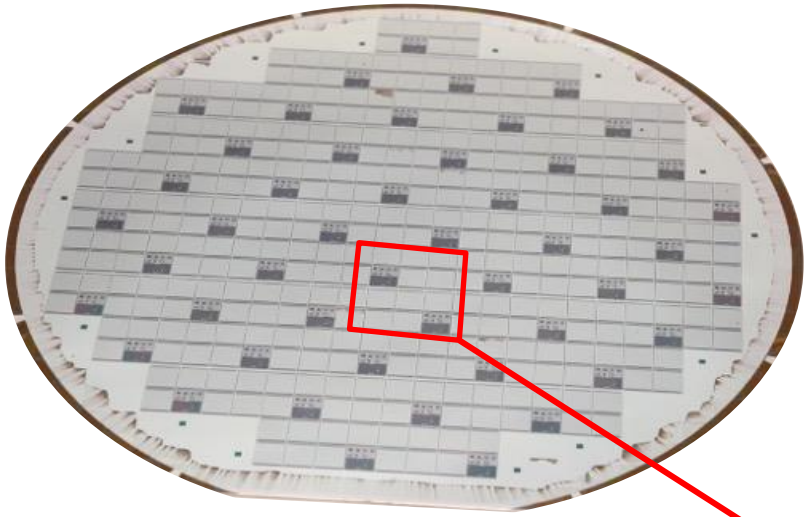
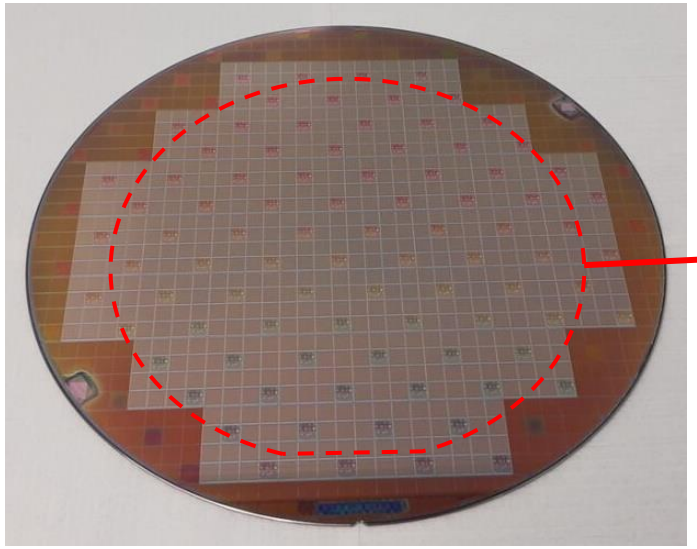


First 3D bonded wafers, received October 13th

Repeated pattern over the whole wafer



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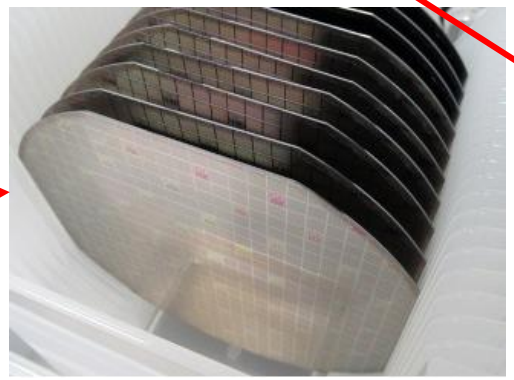

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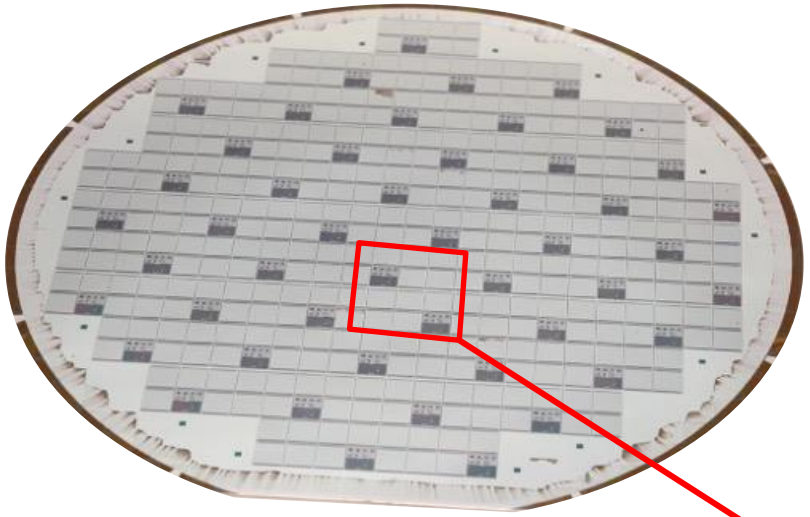


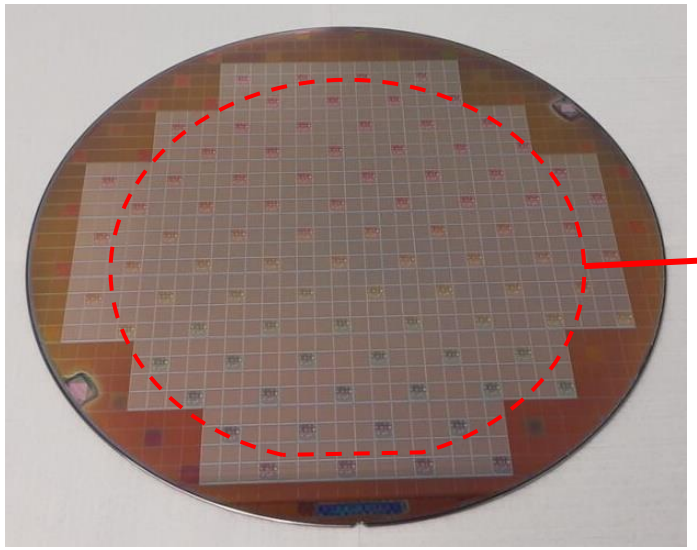
Repeated pattern over the whole wafer

Process monitoring structures

and

bonding alignment

First 3D bonded wafers, received October 13th



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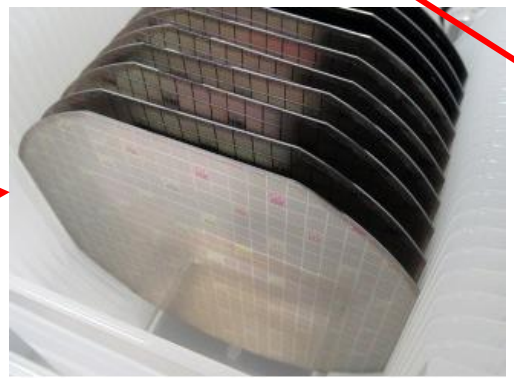
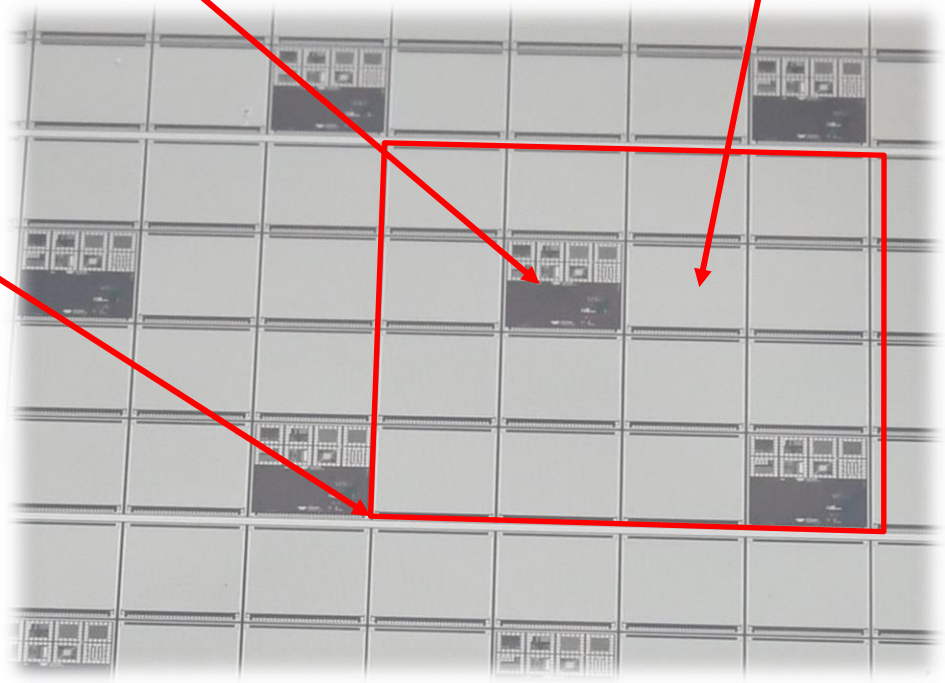


Resized to 150 mm

“Real” PDC



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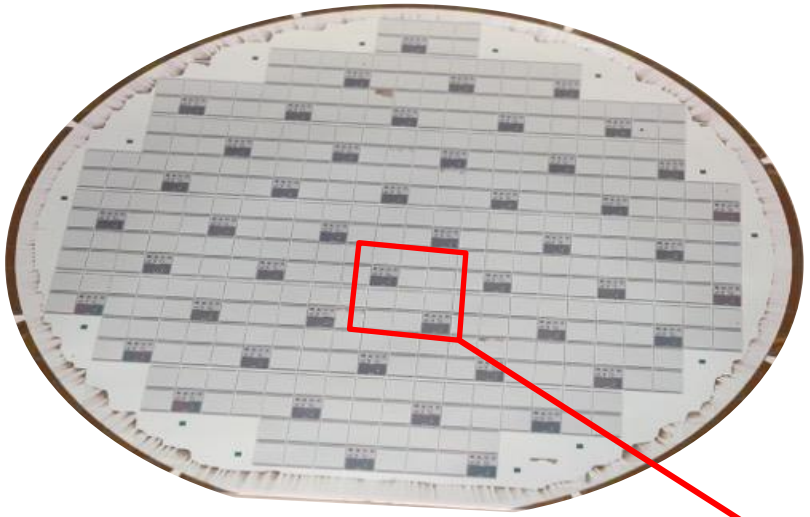

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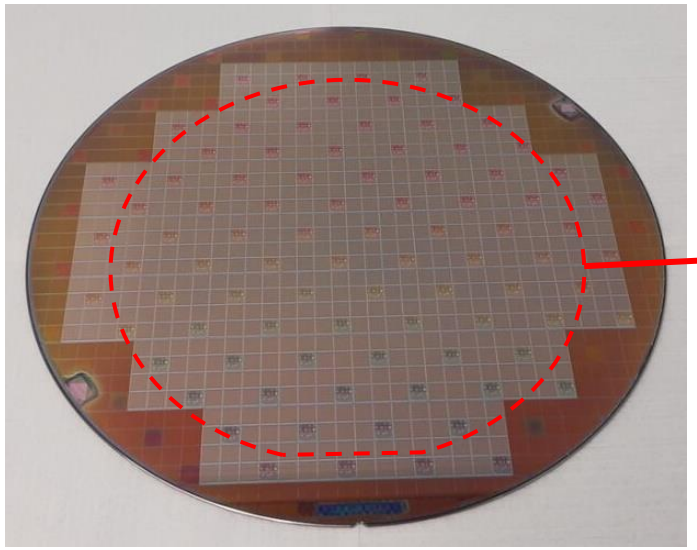

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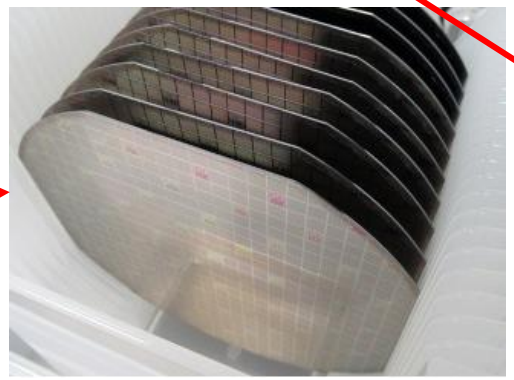

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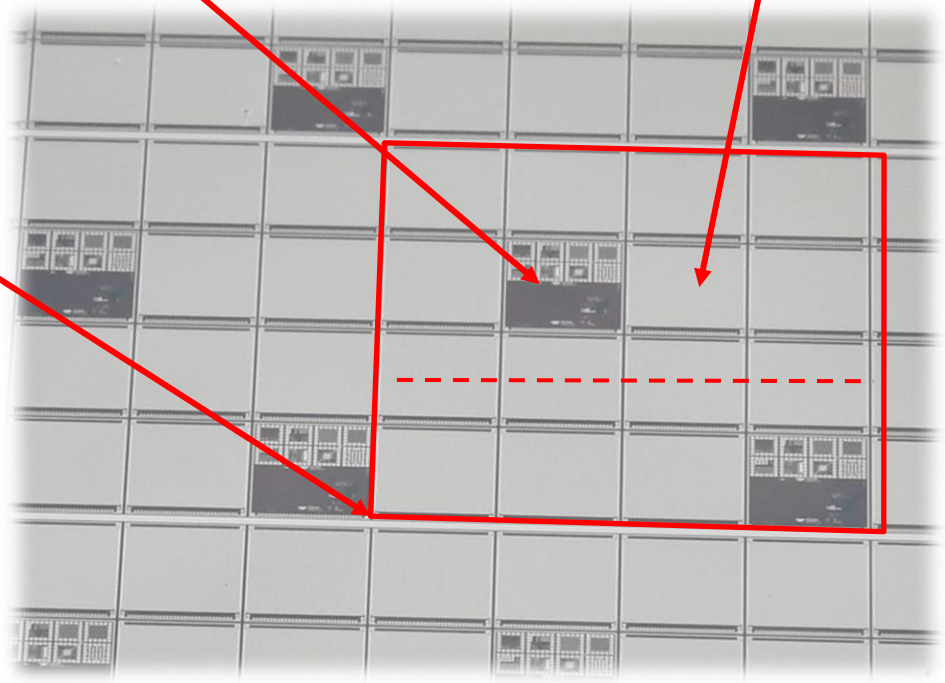

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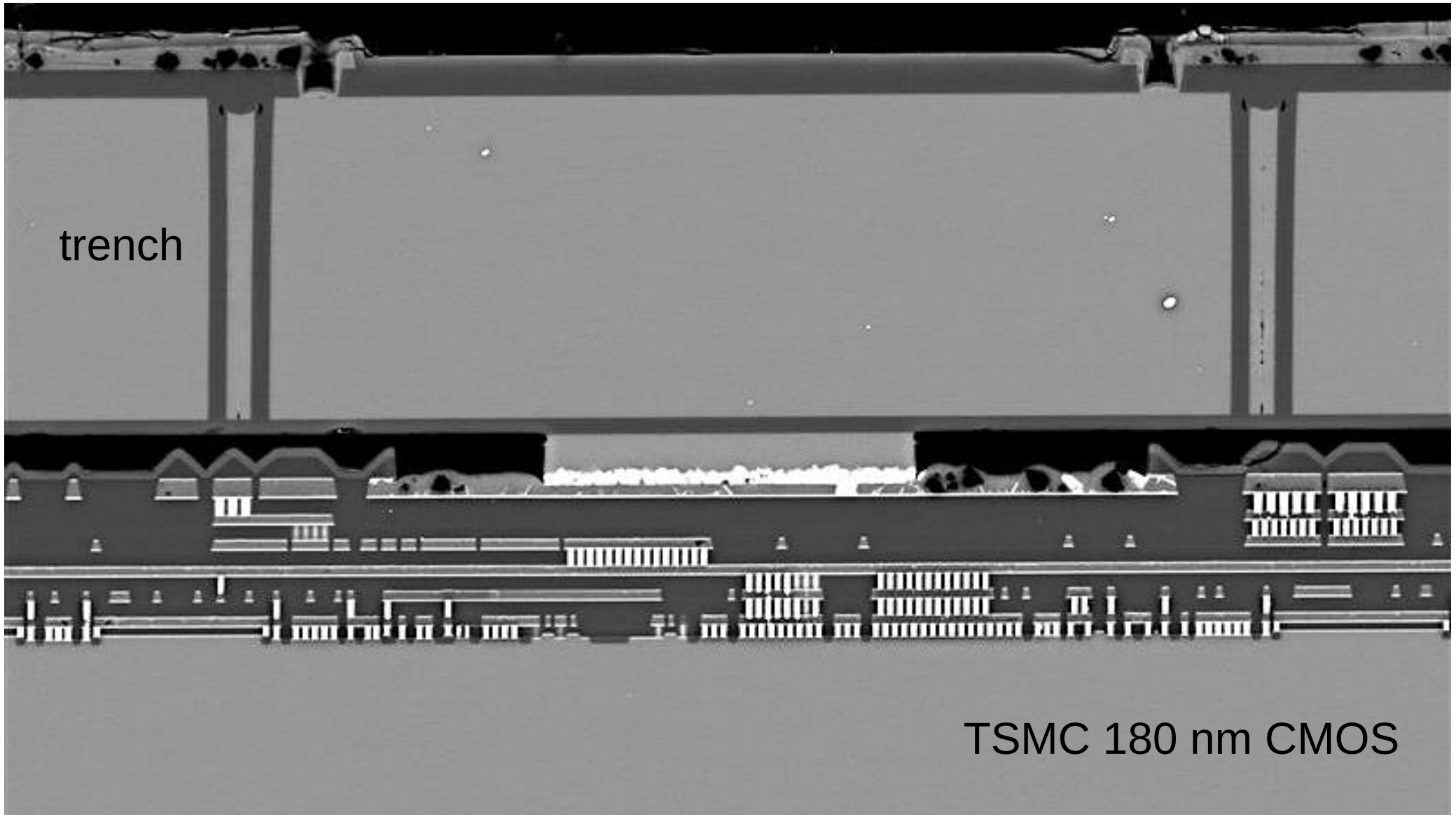
Side view of bonded SPAD



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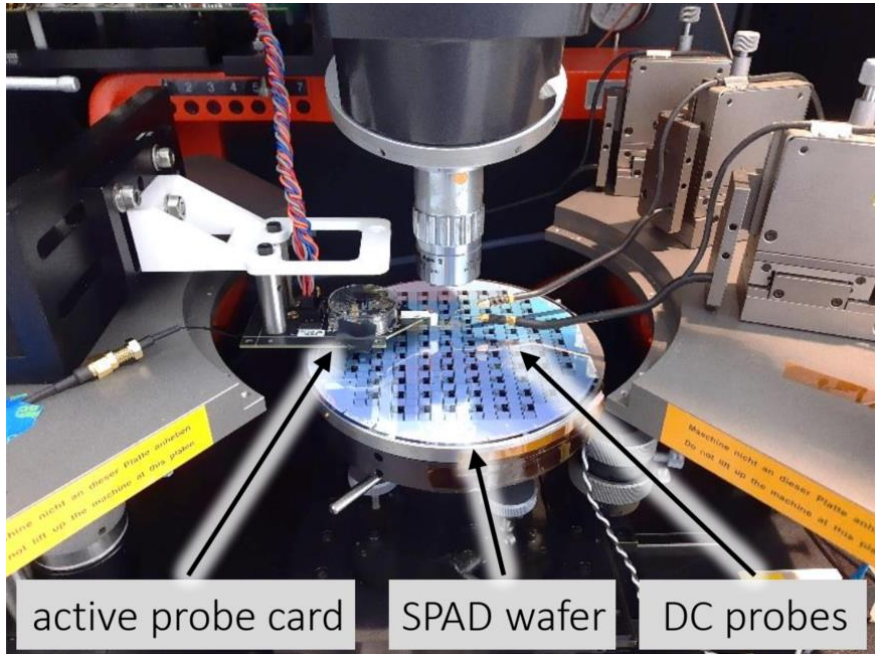
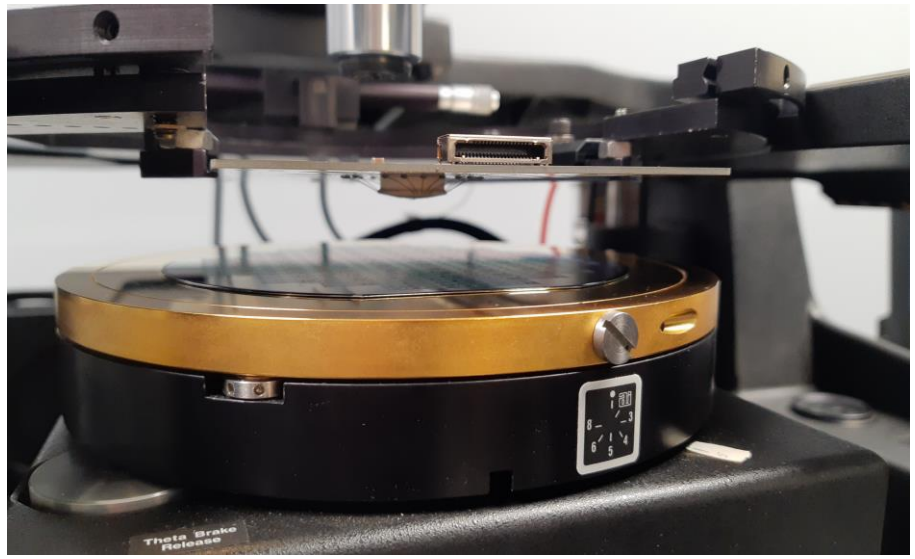
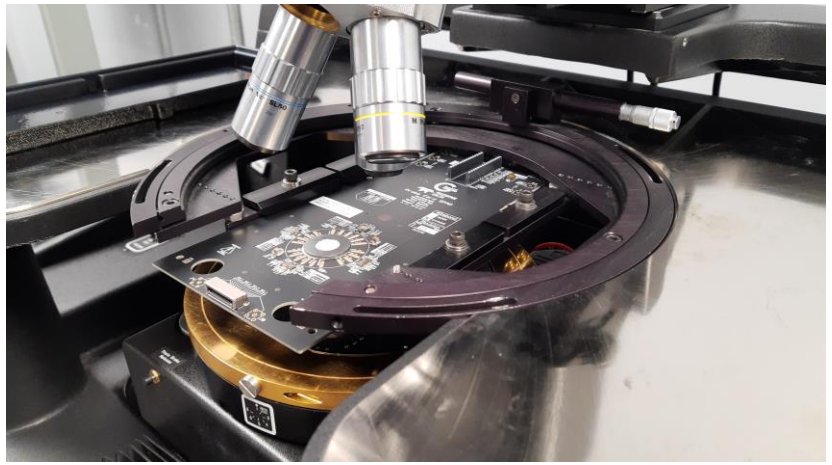
SPAD and CMOS oriented setups



Single-probe quenching circuit for SPAD testing in Geiger-mode [1,17]



View from the front of the probe card



Probe card on the station

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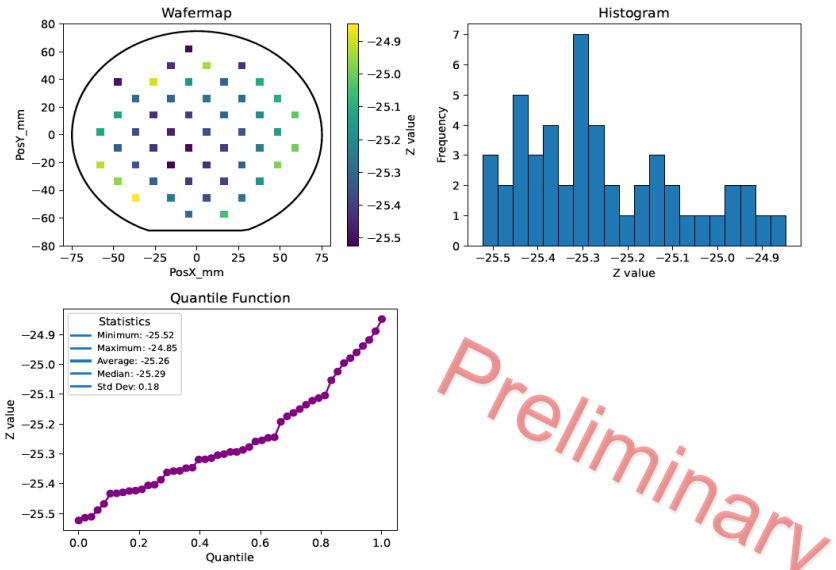
Prelimary Results on 3D Bonded Wafers - SPADs

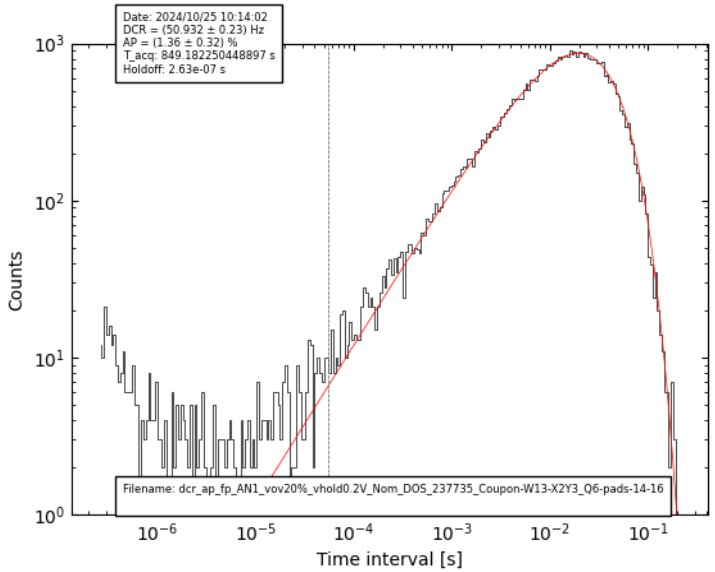
Foundry process monitoring measurements

- All in specs on the 3 wafers
- Breakdown voltage on specifications: 25.28V ± 0.18Vσ

Breakdown voltage



Preliminary



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SPAD performances: comparable to our previous SPADs

- DCR ~ 50-60 cps/SPAD @ 20-25% OV @ RT→ ~0.03 cps/µm^2
- Afterpulsing 1.3%

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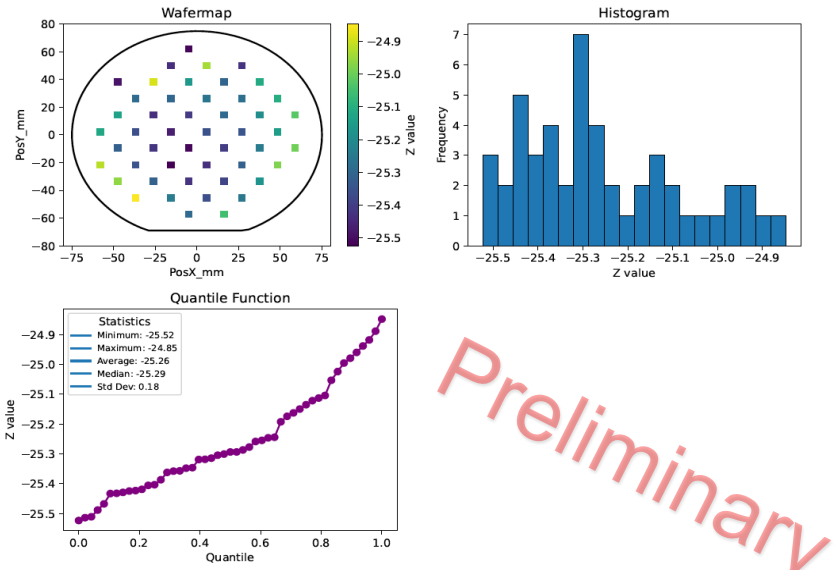

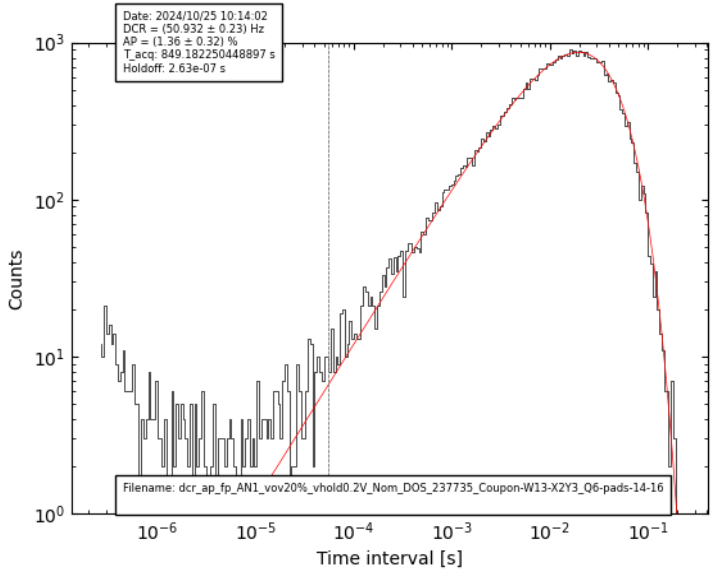

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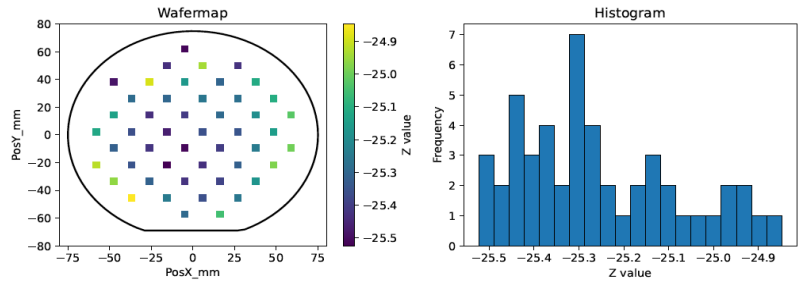
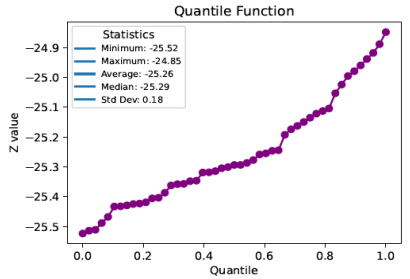
Measurements to come for PDP and timing resolution, with expectations of:

- PDP: ~50% from 400 to 550 nm
- Timing:~20 to 30 ps @ 410 and 820 nm respectively

Breakdown voltage





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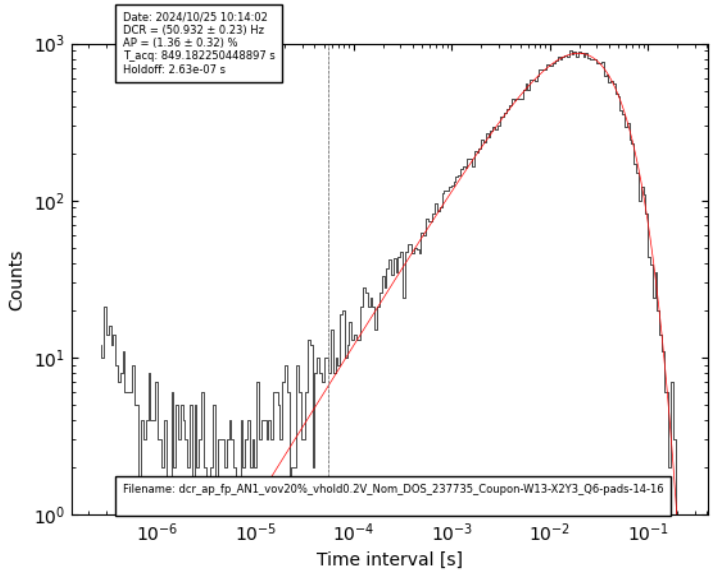

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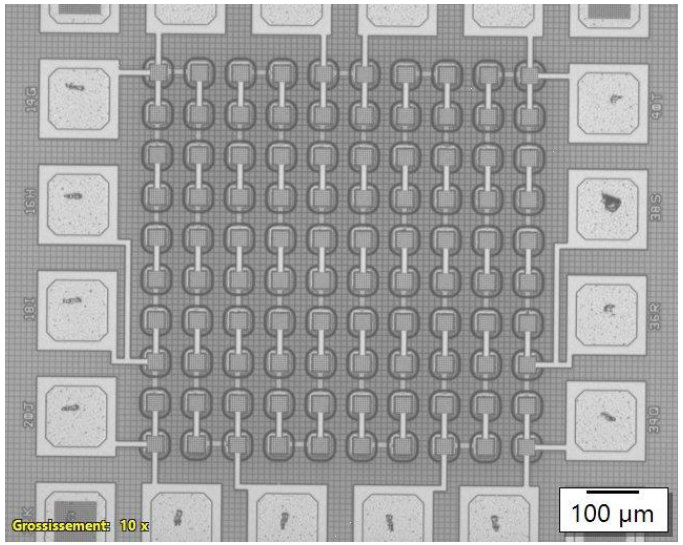
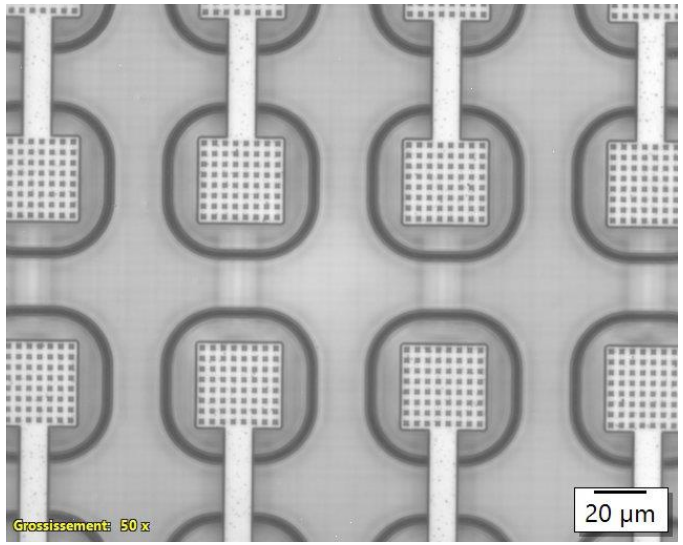
Prelimary results on 3D bonded wafers - Contacts

Contacts top layer to CMOS (Al-Ge eutectic + SiTSV)

- 14 112 connections tested
- **Yield higher than 99.7%** @ 6σ confidence → 2 defective per 1000





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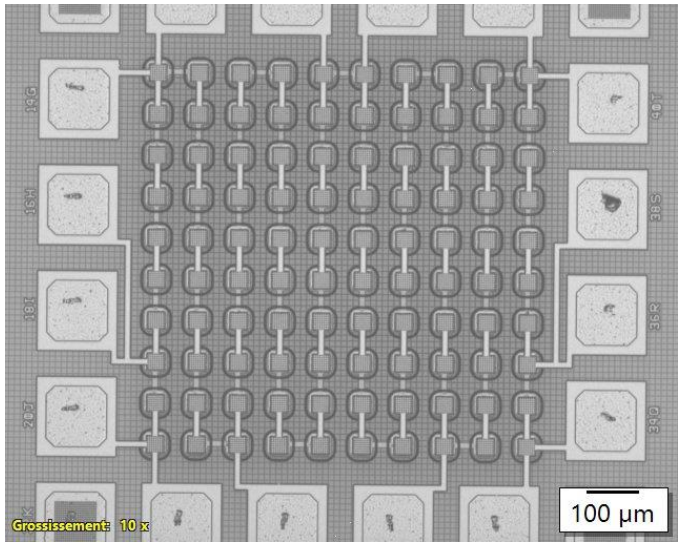

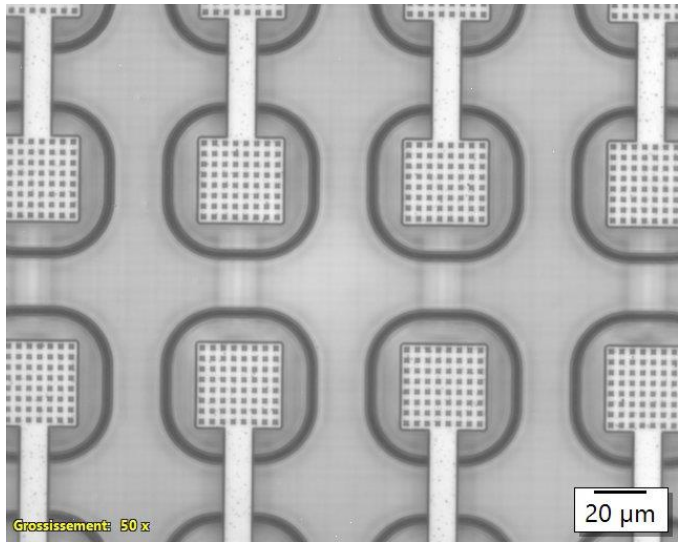

Measurements to come

- Defining and measuring yield based on CMOS functionalities and power draw
- Identifying “patterns” in our wafer layout → yield optimisation

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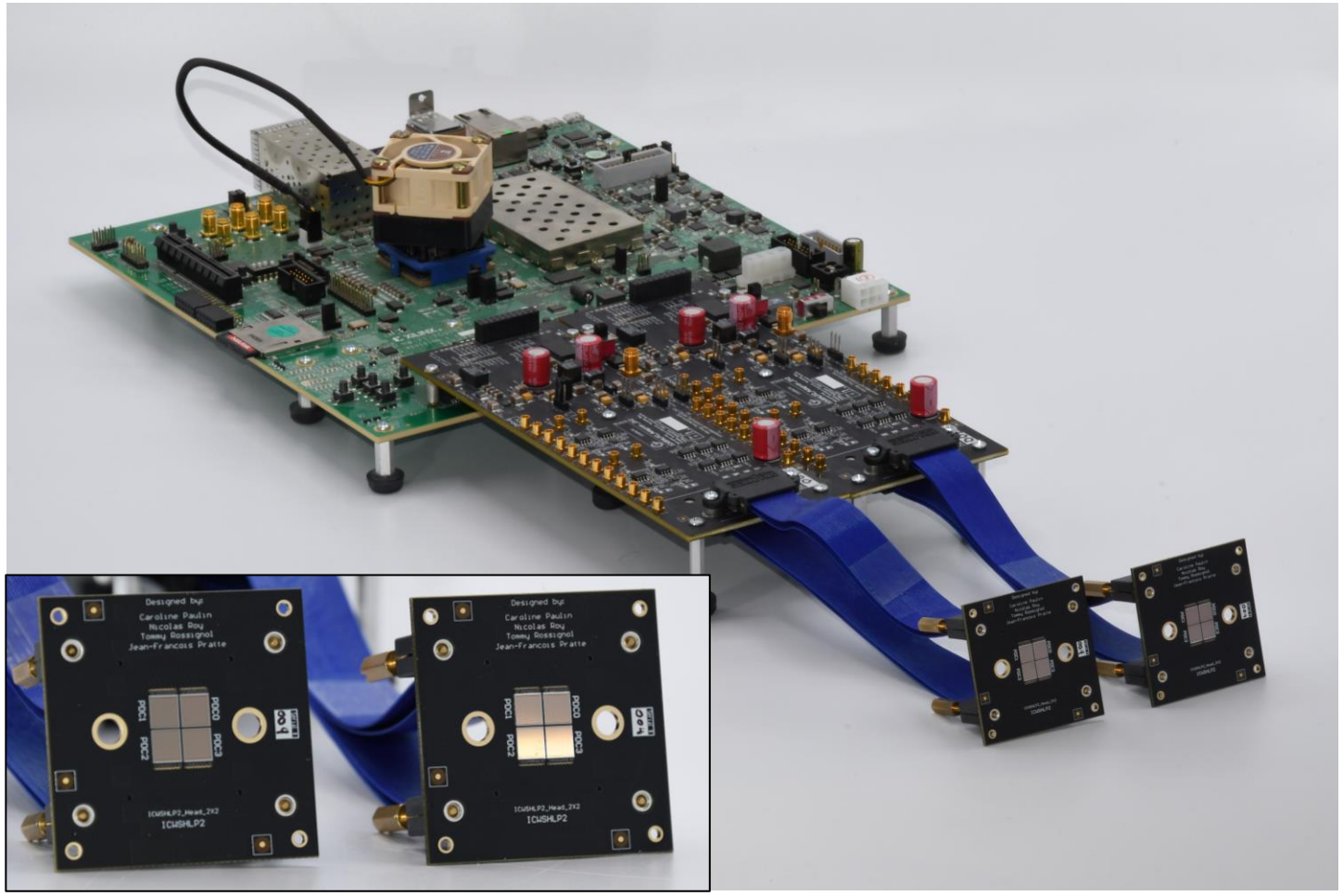
Powering those measurements: Our Test Platform

- Readout and control implemented in ZCU102 FPGA dev-board



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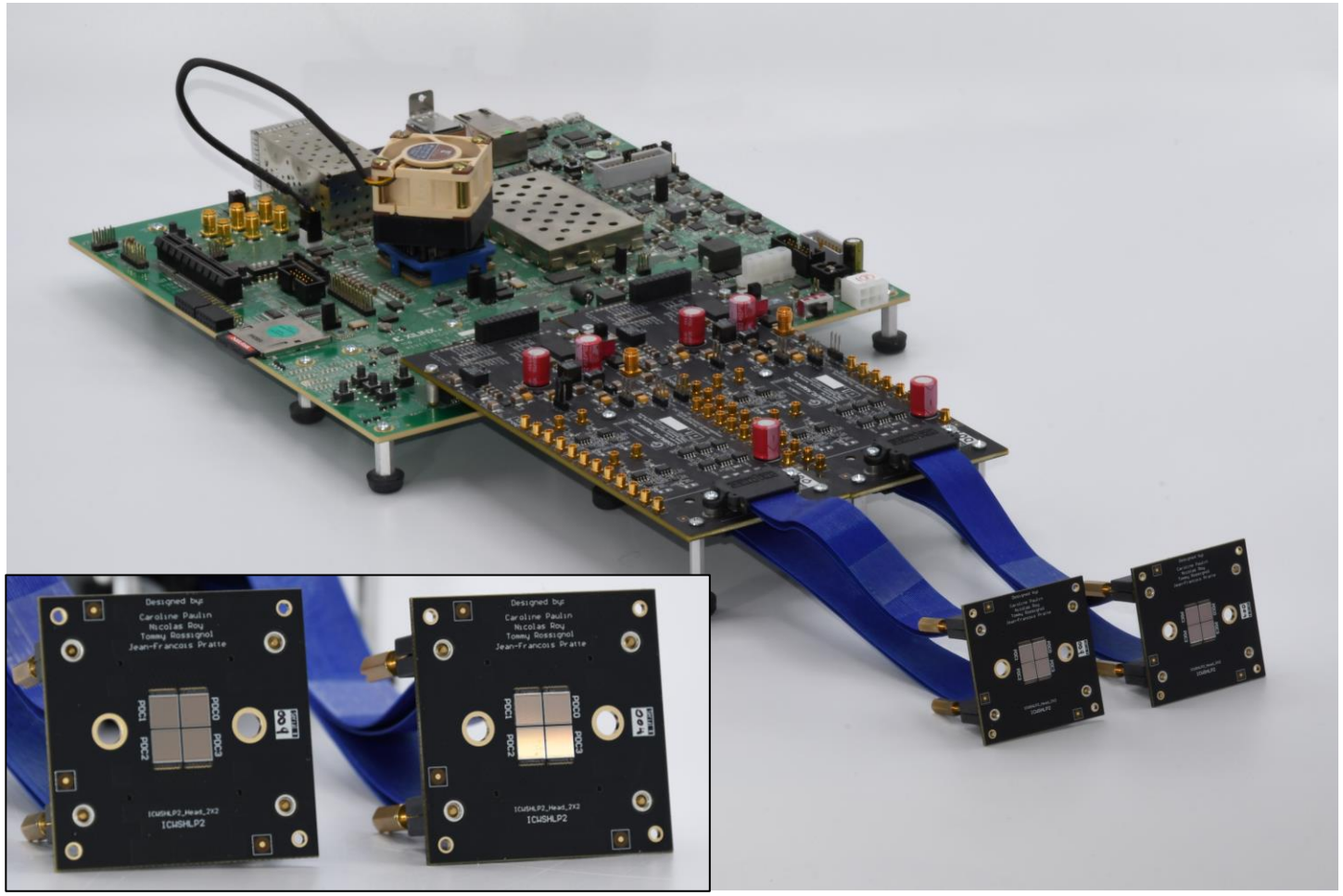

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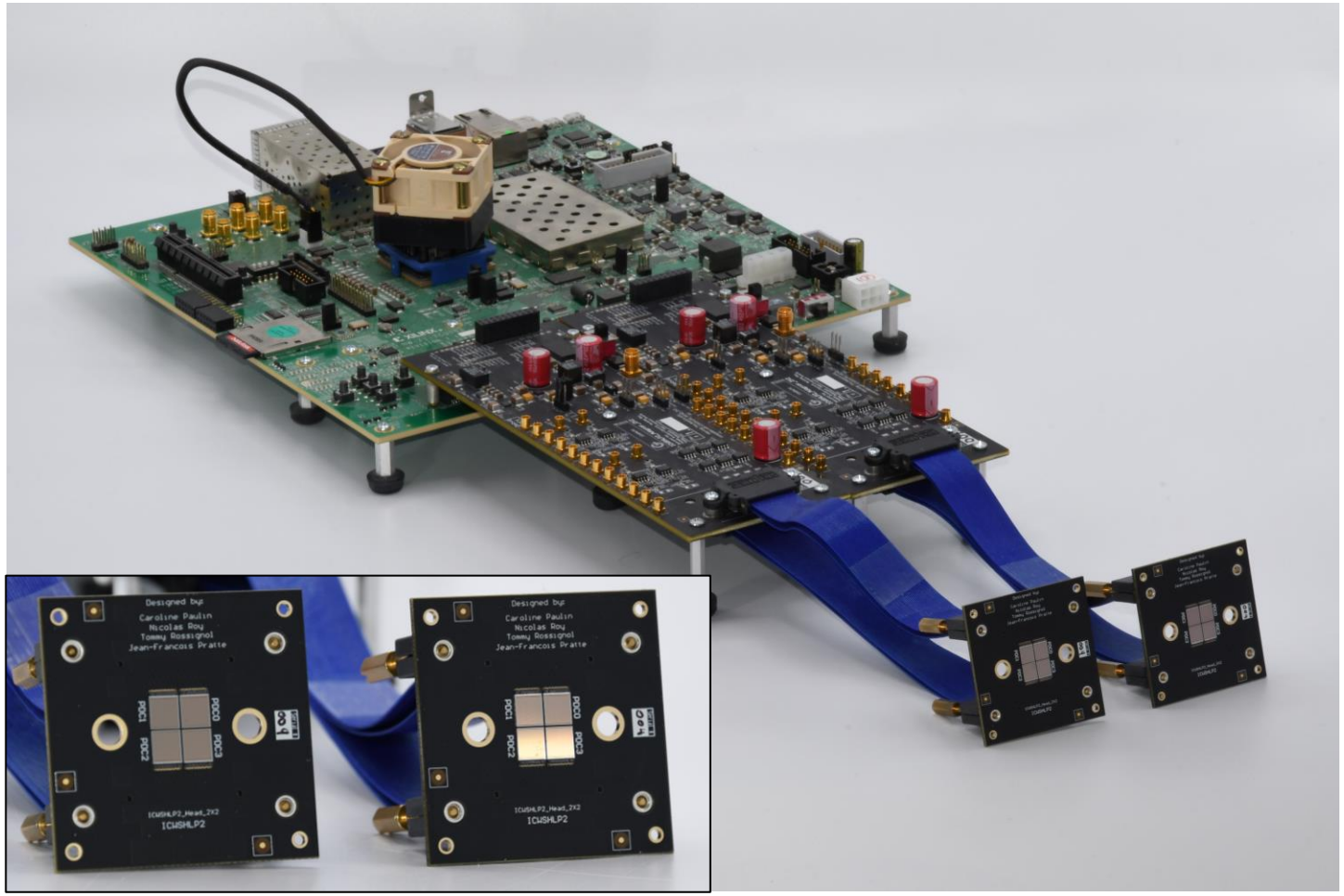
Powering those measurements: Our Test Platform

- Readout and control implemented in ZCU102 FPGA dev-board
- Open to share



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Conclusion

- Key milestones achieved in the past months
- Testing our first 3D integrated PDCs
  - Exciting times for us, but also for you!
- Hoping to share our test platform

- Upcoming tests and characterisation to guide further optimisation and maturity of our process
- Design of the precise timing PDC

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Sherbrooke: A team's work

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Jean-François Pratte
Serge Charlebois
Artur Turala
Frédéric Nolet
Frédéric Vachon
Gabriel Lessard
Guillaume Théberge-Dupuis
Jérémy Chenard
Jérôme Deshaies
Keven Deslandes
Nicolas Roy
Raffaele Aaron Giampaolo
Robin Scarpellini
Samuel Parent
Sean Prentice
Simon Carrier
Tommy Rossignol
Olivier Lepage

Collaborators

Fabrice Retiere (TRIUMF)
Lorenzo Fabris (ORNL)
Stéphane Martel (TDSI)
Simon Viel (Carleton)
Roger Lecompte (CIMS)
nEXO Collaboration
nEXO Canada
ARGO Collaboration

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Thank you

Backups

Available 3D Integrated Processes and Considerations

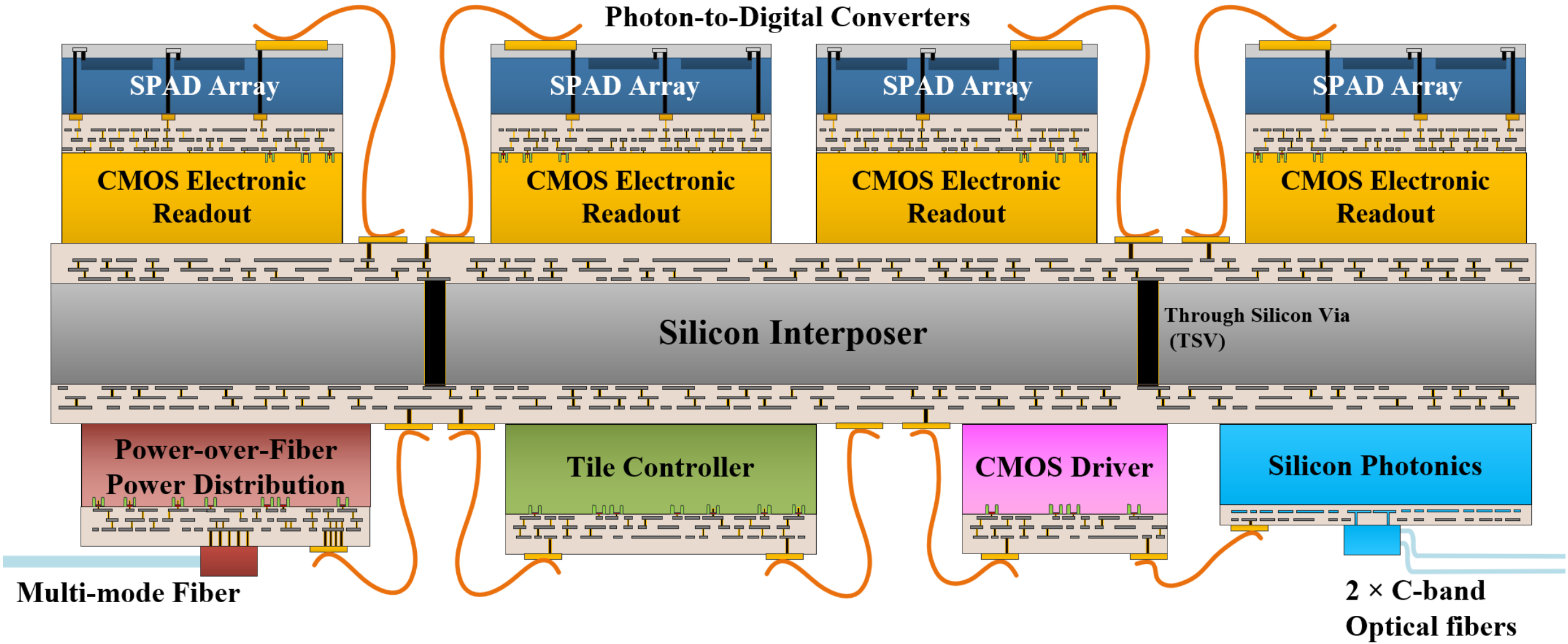
- It is all about the wavelengths of interest!
- Mismatch between what drives industry and what we need:

	Industry: Camera and LIDAR	Radiation instrumentation & Medical Imaging: scintillation light and charged particles
Wavelengths of interest	visible to near-infrared => BSI	ultraviolet to visible => FSI
Timing resolution	~300 of ps	down to < 10 ps
Pixel size	small (<10 µm) for density	large (50-100 µm) for greater fill factor
Integrated circuit technologies	sub-100 nm ($$$)	chosen for the purpose (aim at the best PDE, timing resolution and noise)

Costs of 3D PDCs – how can we evaluate it?

- CMOS layer (180 nm)
  - ~110k USD per mask set, 1,600 per wafers
  - 616 usable dies per wafer => 110k + ~3 USD/die (5x5mm^2)
- 65 nm: ~4x the cost of 180 nm but more area per wafer
- SPAD Layer, comparable to commercial SiPMs (price/area)
- 3D bonding technique: ???
- Factor in yield in this equation?
- Consider the price as both the SiPM tiles, their frontend and assembly. Is it that much more expensive?

Scaling Towards Large Scale: Photodetection Module



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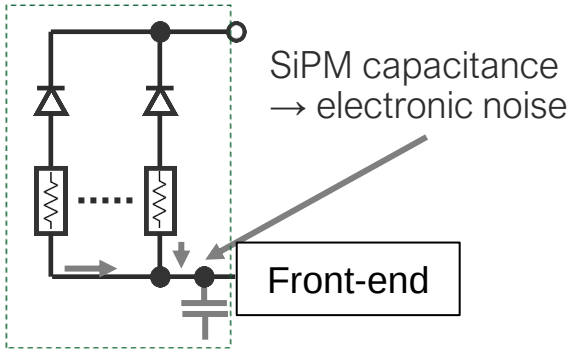
Power consumption in SiPM readout

Conventional SiPM

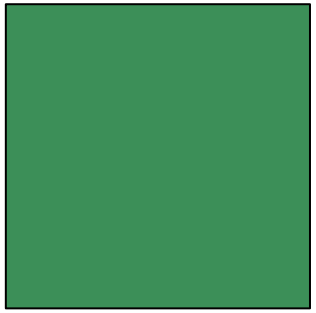


Preliminary study

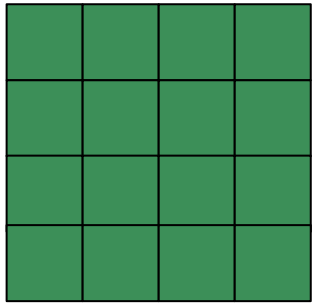
$$P \propto [C_{SiPM} + C_{In}]^2$$

$$P \propto \sum^{N_{seg}} \left[\frac{C_{SiPM}}{N_{seg}} + C_{In}(N)\right]^2$$

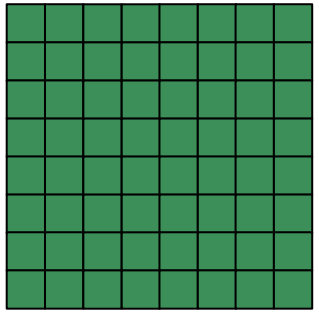
$$P \propto M \cdot DCR \cdot E_{trigger}$$



Single SiPM



N Segments



M Individual SPADs

Analog front-end (before digitization)

No analog front-end

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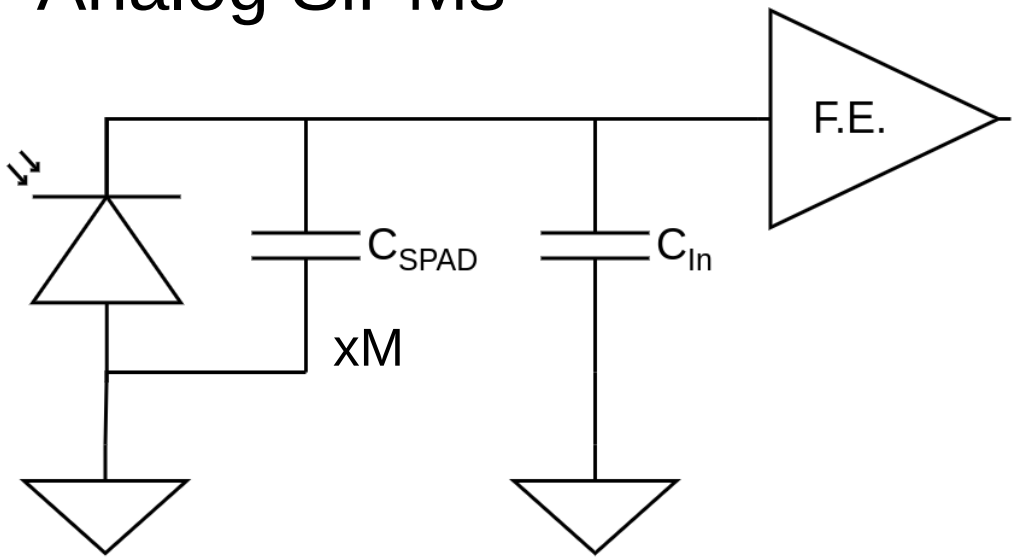
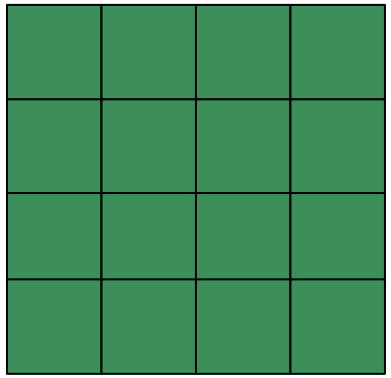
Other Approaches – SiPM Segmentation and Power Consumption

Analog SiPMs





Segmented

What is the optimal segmentation?

Single array:

$$P \propto [C_{SiPM} + C_{In}]^2$$

Segmented array:

$$P(N_{seg}) \propto \sum^{N_{seg}} \left[\frac{C_{SiPM}}{N_{seg}} + C_{In}\right]^2$$

How can C_{in} be optimised… ?

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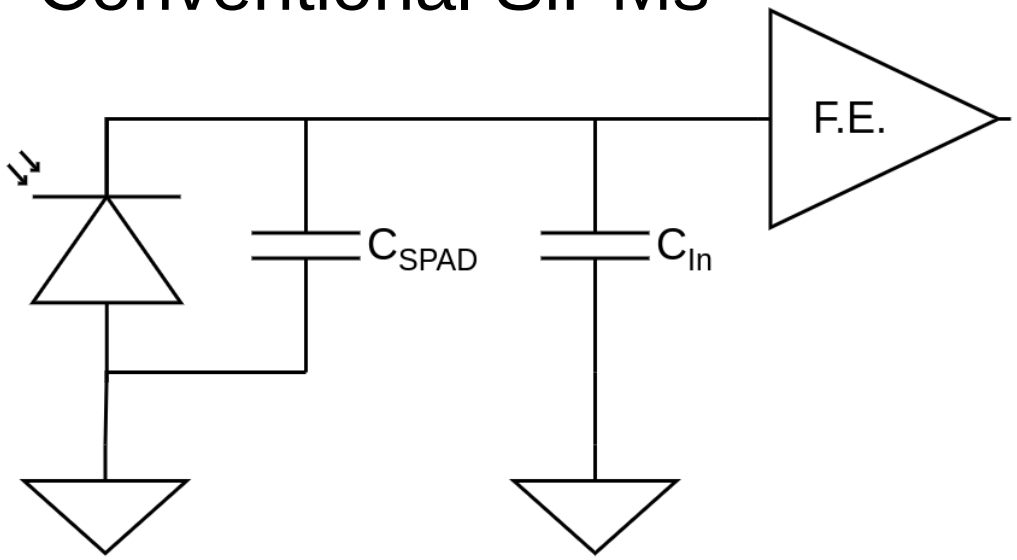
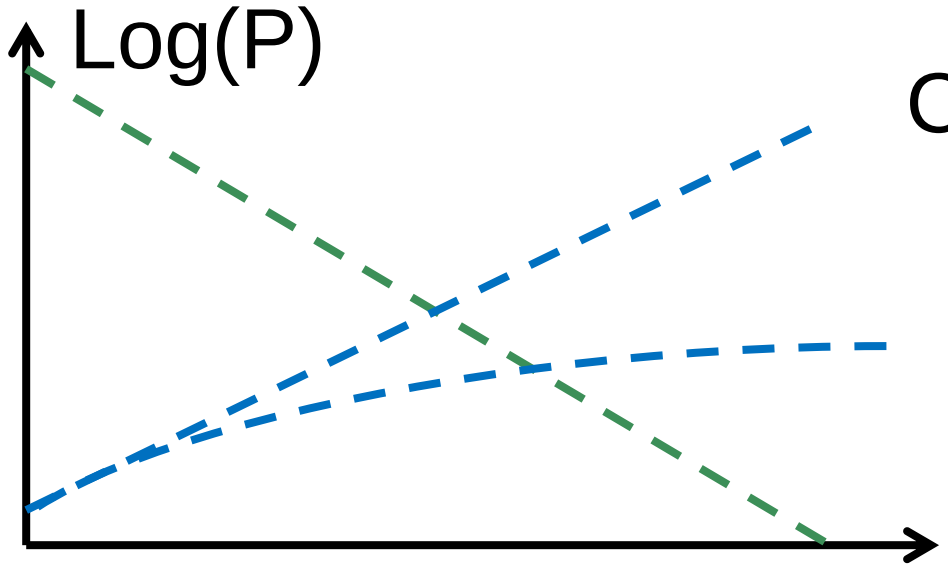
Other approaches – SiPM Segmentation

Conventional SiPMs





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How can C_{in} be optimised… ?

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Power consumption of 180

From T. Rossignol et al. [2]

$$P_{\text{total}} = P_{\text{static}} + P_{\text{events}} + P_{\text{clock}} + P_{\text{buf}}$$

P_{static}: 65 µW for 4m^2

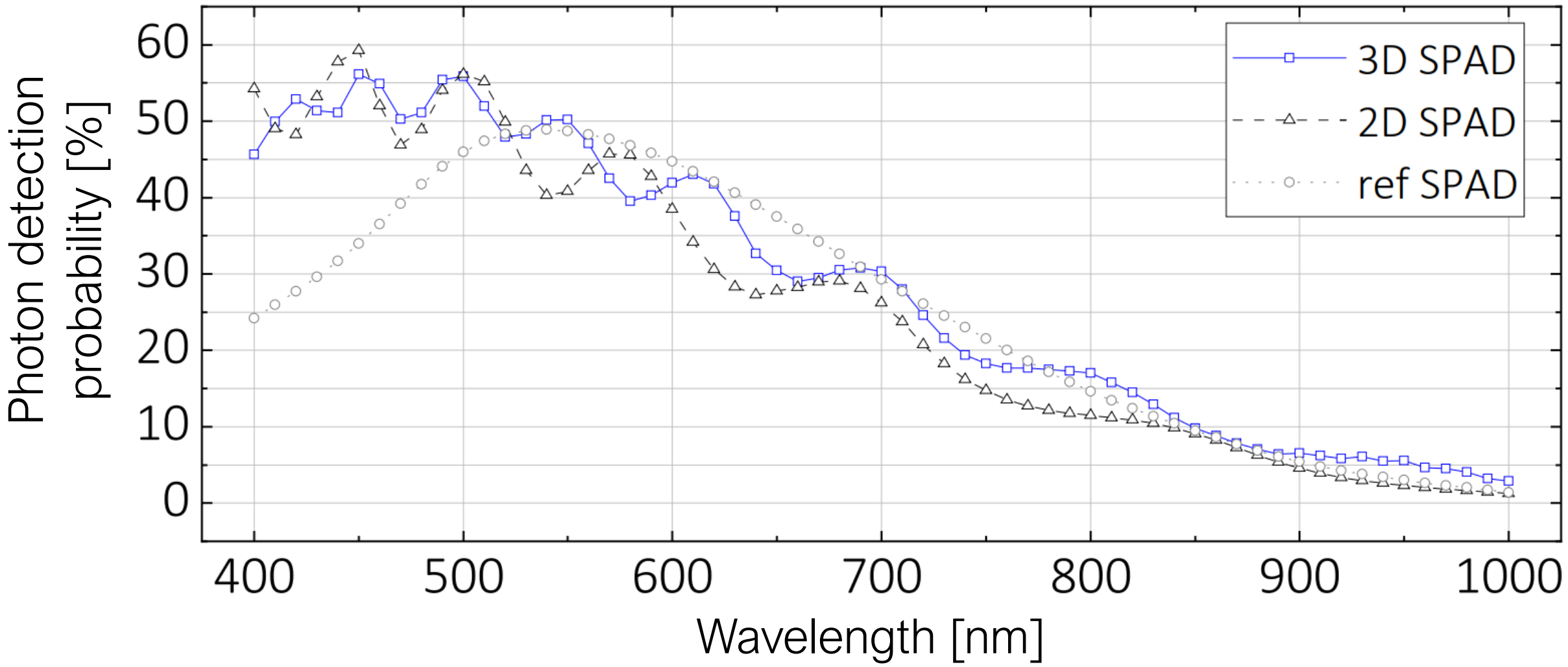
$$P_{\text{events}}\,(W) = 8.8 \times 10^{-12}\,(J) \times R_{\text{events (cps)}}$$

$$P_{\text{clock}}\,(W) = 1.8 \times 10^{-9}\,(J) \times R_{\text{acq}} \times N_{\text{clock cycles/acq}}$$

$$P_{\text{buf}}\,(W) = 85 \times 10^{-12}\,(J) \times R_{\text{acq}} \times N_{\text{bits/acq}}$$

For nEXO (DCR = 50 cps/mm^2) => 140 µW/PDC, 560 µW/cm^2

PDP



https://doi.org/10.1109/JEDS.2024.3359088

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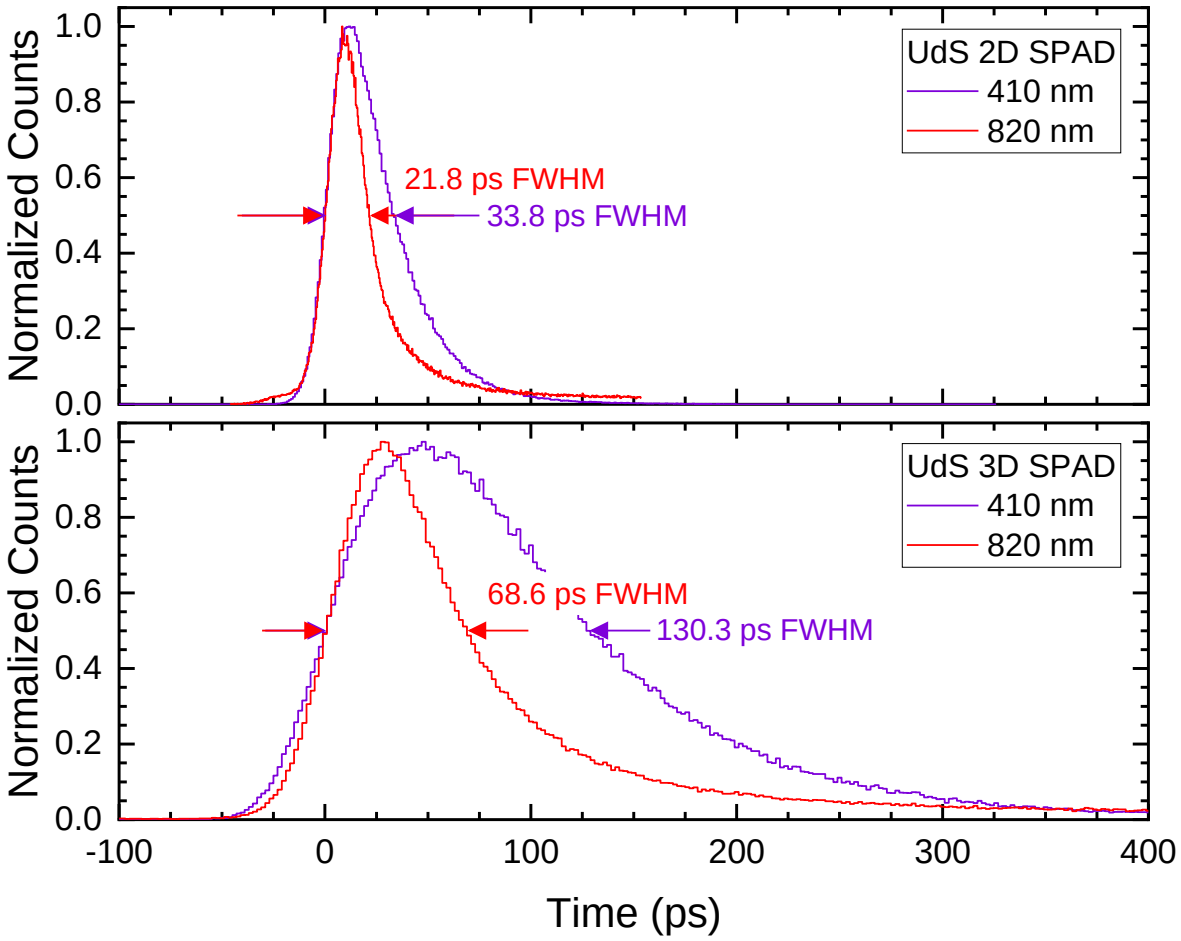
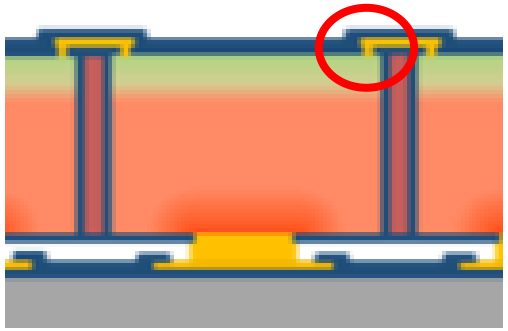
2D vs 3D Measurement: Single-Photon Timing Resolution



- The increased jitter of the 3D SPADs is linked to a flawed contact (non-ohmic and high valued)
  - Reduces the signal rising slope



- Process correction confirmed
  - New timing measurements to come

Single SPAD measurement (3D mechanical SPADS)

			103.8	89.6	459.0	64.7	25003.9			
	127.9	79.5	62.2	61.6	50.0	42.0	33989.3	63.1	75.1	
131.2	105.9	71.4	2901.6	43.6	43.4	36.8	41.6	51.3	84.8	96.1
116.0	94.3	14648.6	44.1	38.6	44.4	37.5	39.2	48.7	205.2	114.3
194.0	79.2	46.5	38.1	38.1	47.3	35.5	42.7	51.6	91.9	118.9
3944.2	2404.2	69.4	47.6	41.7	32.6	38.1	41.0	46.1	71.1	118.7
320.7	108.3	61.8	42.4	40.6	38.1	41.6	43.2	45.6	75.9	111.1
346.8	160.8	517.7	69.8	32183.7	58.3	45.1	48.3	70.2	106.9	148.6
	207.7	163.2	1654.5	101.7	116.7	136.7	83.9	141.5	230.5	
			119.5	219.7	164.9	645.8	203.8			

Dark count rate (cps)

			24.41	24.27	24.32	24.27	24.37			
	24.51	24.49	24.40	24.34	24.34	24.34	24.30	24.38	24.48	
24.46	24.34	24.43	24.41	24.38	24.38	24.30	24.32	24.32	24.20	24.29
24.48	24.37	24.45	24.41	24.43	24.35	24.26	24.49	24.41	24.18	24.04
24.45	24.45	24.45	24.40	24.40	24.23	24.21	24.18	24.23	24.05	24.04
24.34	24.43	24.46	24.48	24.32	24.32	24.32	24.30	24.16	24.12	24.09
24.23	24.46	24.45	24.43	24.32	24.24	24.23	24.24	24.30	24.09	24.13
24.41	24.26	24.35	24.32	24.27	24.12	24.26	24.35	24.23	24.18	24.27
	24.38	24.41	24.26	24.16	24.16	23.93	24.26	24.16	24.21	
			24.35	24.23	24.16	23.90	24.26			

Breakdown voltage (V)

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DCR distribution and screamers

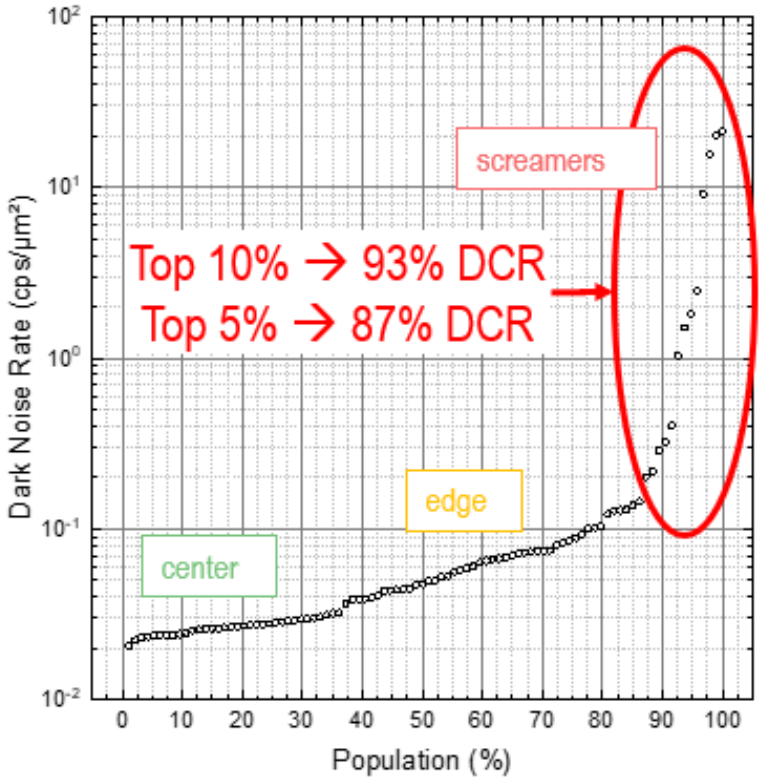
- Median DCR of ~0.05 cps/um2
- Outliers represent less than 10% of the population and are typical for SPAD (point defects) [1]
- Concentric distribution of the dark noise is caused by metal contacts misalignment during in-process issues (known solution underway).

Dark noise rate (cps/µm²)

			65E-3	56E-3	288E-3	41E-3	16E+0		
	80E-3	50E-3	39E-3	39E-3	31E-3	26E-3	21E+0	40E-3	47E-3
82E-3	66E-3	45E-3	2E+0	27E-3	27E-3	23E-3	26E-3	32E-3	53E-3	60E-3
73E-3	59E-3	9E+0	28E-3	24E-3	28E-3	23E-3	25E-3	30E-3	129E-3	72E-3
122E-3	50E-3	29E-3	24E-3	24E-3	30E-3	22E-3	27E-3	32E-3	58E-3	75E-3
2E+0	2E+0	44E-3	30E-3	26E-3	20E-3	24E-3	26E-3	29E-3	45E-3	74E-3
201E-3	68E-3	39E-3	27E-3	25E-3	24E-3	26E-3	27E-3	29E-3	48E-3	70E-3
217E-3	101E-3	324E-3	44E-3	20E+0	37E-3	28E-3	30E-3	44E-3	67E-3	93E-3
	130E-3	102E-3	1E+0	64E-3	73E-3	86E-3	53E-3	89E-3	144E-3	
			75E-3	138E-3	103E-3	405E-3	128E-3		

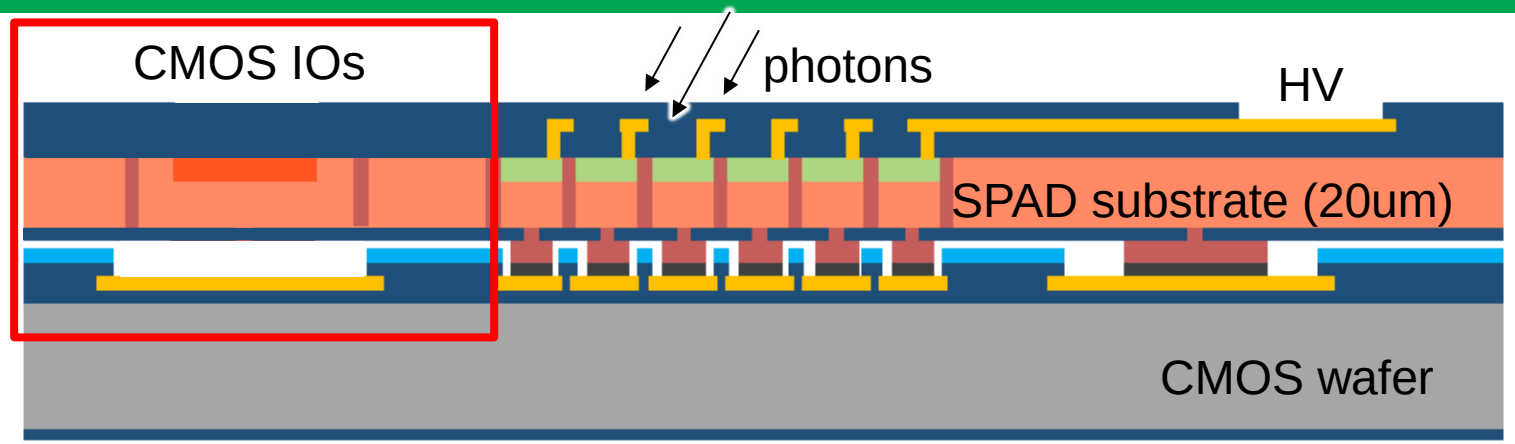
3D SPAD: V_{ov}=4.8V (20%) t_{ho} =1µs

Avg.	839E-3
Median	48.6E-3
Min	20.5E-3
Max	21.3E+0



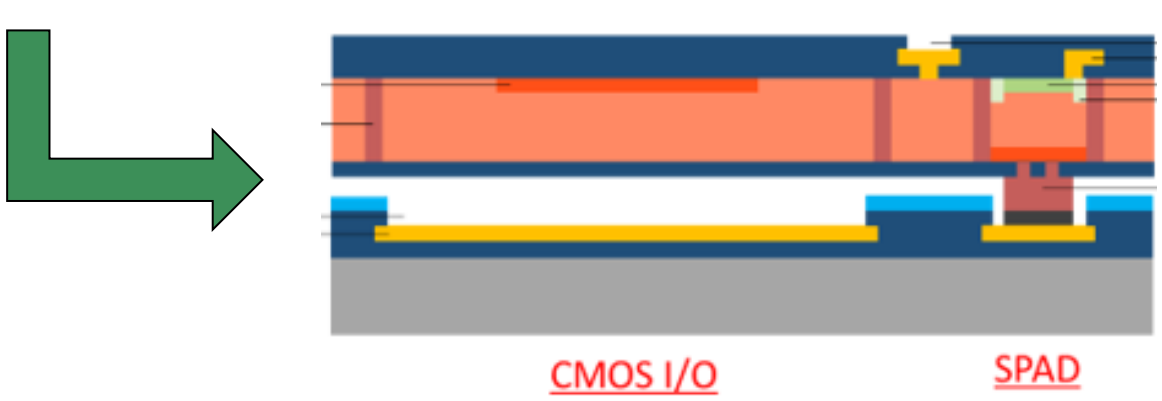
Giudice et al., High-rate photon counting and picosecond timing with silicon-spad based compact ctor modulesJournal of Modern Optics, 54(23):225–237, 2007

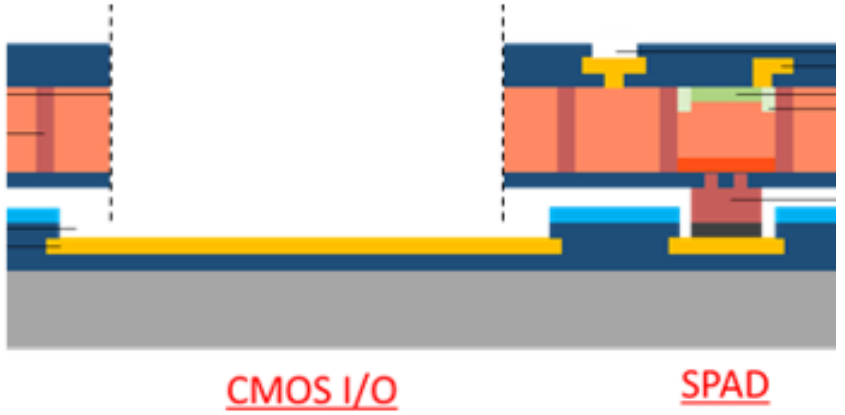
Our strategy for wafer-to-wafer bonding - contacts



Full-thickness opto-electrical isolation trenches

→ TSV-less architecture





Wirebond directly on CMOS

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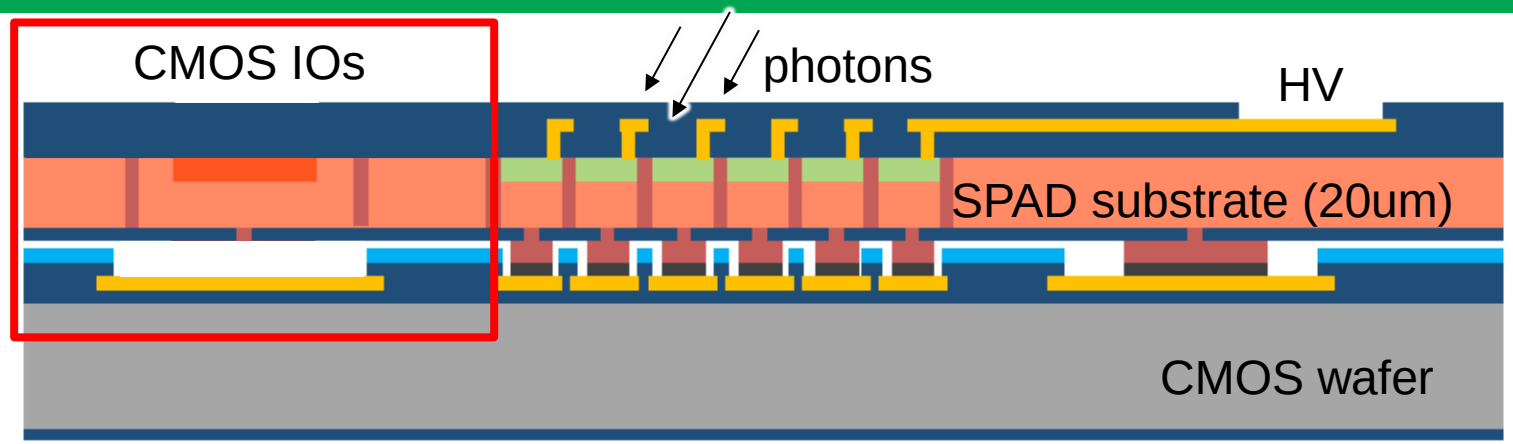
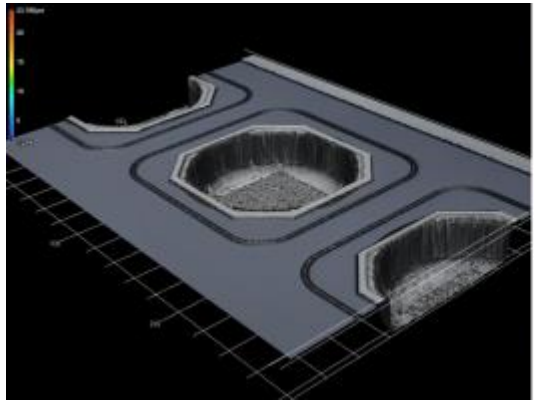
Our strategy for wafer-to-wafer bonding - contacts

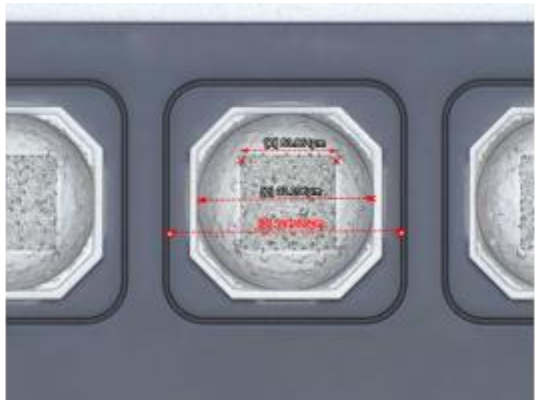


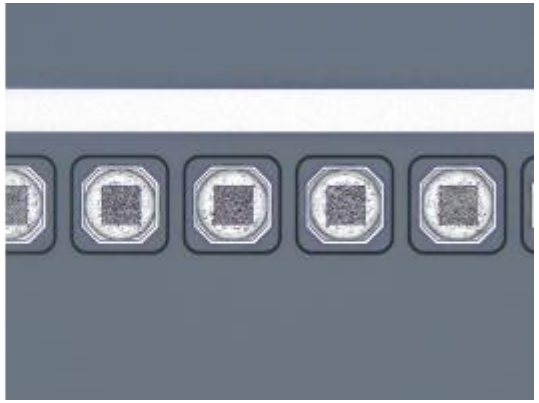
Full-thickness opto-electrical isolation trenches

→ TSV-less architecture

Currently done at the die-level







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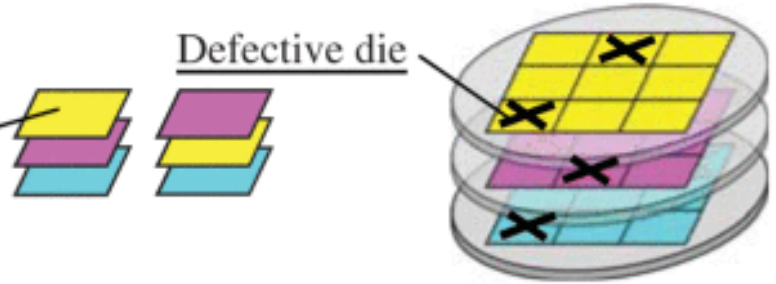
Multi-chip-to-wafer

Bonding Methods	*Die-to die*	*Wafer-to-wafer*	*Die-to-wafer*	*Advanced die-to-wafer*
				
Stacking procedure	Pick & place	Wafer bonding	Pick & place	Self-assembly & batch trasfer
High production throughput	No	Yes	Yes/No	Yes
High production yield	Yes	No	Yes	Yes
High flexibility in chip size	Yes	No	Yes	Yes
High feasibility for different material & device stack in layers	Yes	No	Yes	Yes
Applications	Packaging	DRAM (high-yield products)	Image sensor, logic, memory, MEMS, etc.	Image sensor, logic, memory, MEMS, etc.

Stmicros 3D40 Process

***Abstract*—We present a 10.17µm pitch 3D-stacked backside illuminated Single Photon Avalanche Diode (SPAD). The wafer stack features a fully custom top tier process which is highly optimized for optical performance and a 40nm bottom tier which enables dense and low-power signal processing, local to the pixel array. State-of-the-art pixel performance is presented with a specific focus on high-sensitivity, low power, and high-speed operation. With a minimum operating voltage of 19.1V (at 60°C) a PDE of 18.5% is obtained at 940nm, with a 2.5V excess bias (which rises to 22% at 3.5V), with low DCR and low Jitter. This is achieved while consuming only 70fC of charge per pulse. The combination of low breakdown voltage and low charge per pulse minimizes power consumption which is essential for array scaling and for enabling low-power portable applications. With the selected sensing circuit design, tailored for high frequency performance, 85Mcps Max Count Rate is achieved, with a 2.5V excess bias (rising to >110Mcps at 3.5V), significantly reducing the pressure on pixel pitch reduction to cope with high illumination levels.**

Keywords— SPAD pixel, 3D 40nm SPAD technology, Low Power, High Count Rate, LIDAR, portable applications.

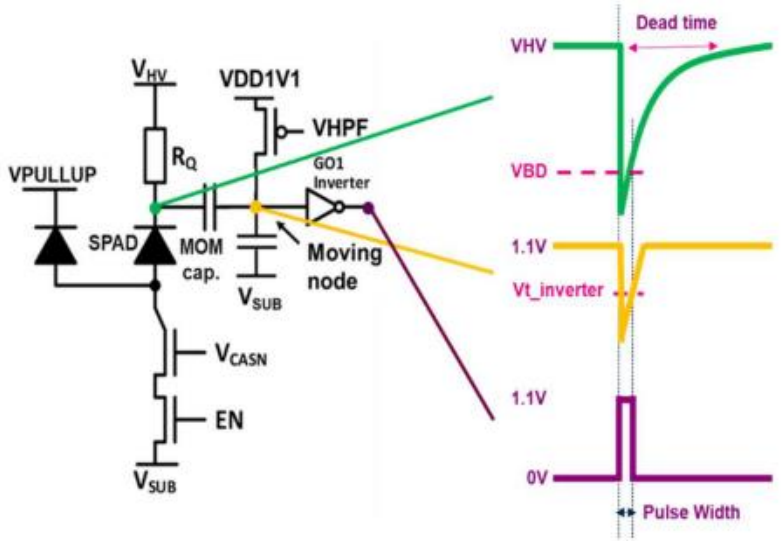


Fig. 7. Pixel schematics including the SPAD diode, the quenching resistor RQ, the Metal-Oxide-Metal coupling capacitor, the readout circuitry, and the disabling circuitry. Expected voltage swing observed at the SPAD cathode (green), the pulse shaping node (yellow) and after the inverter (purple).

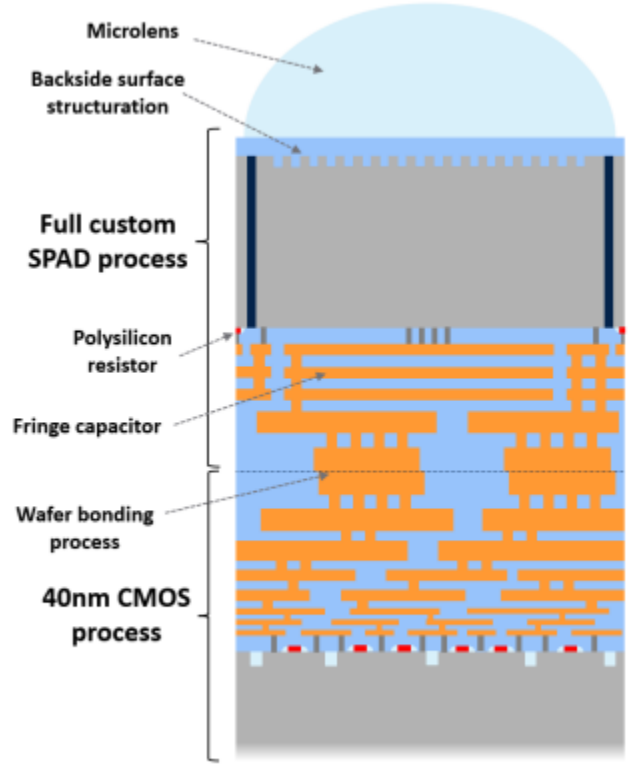


Fig. 1. Cross-section of our 3D-stacked backside illuminated SPAD pixel.

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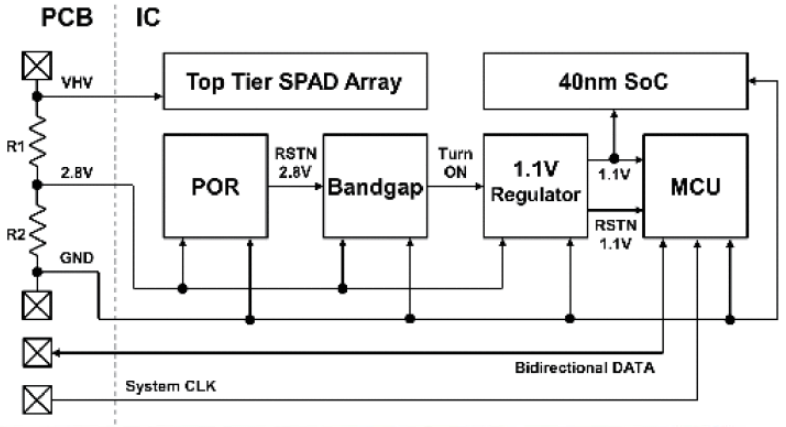
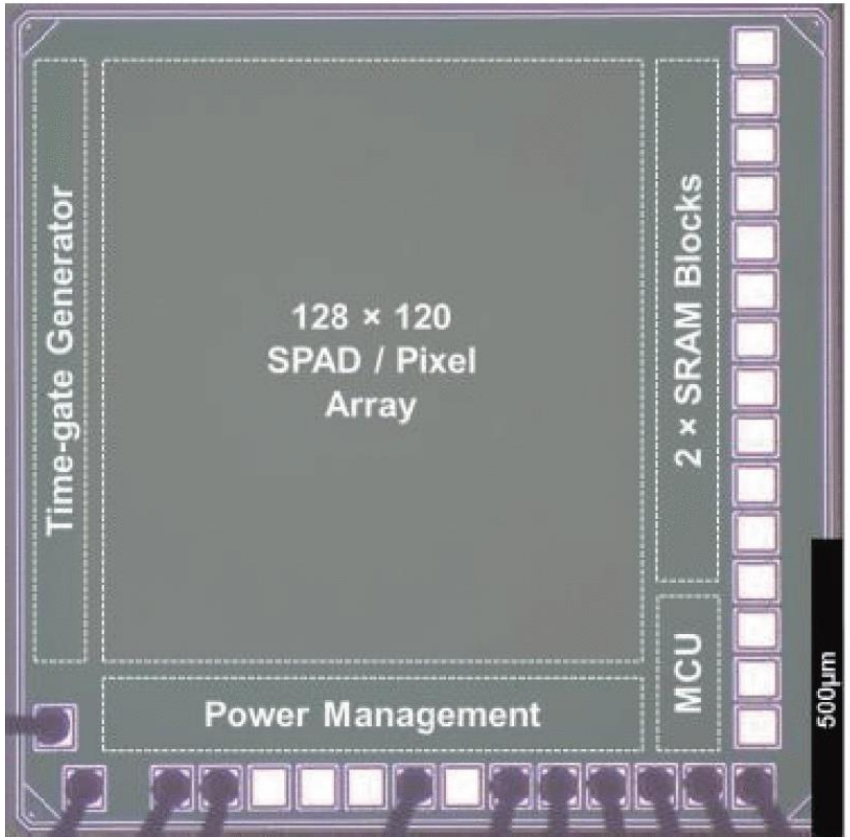
A 128 × 120 5-Wire 1.96mm² 40nm/90nm 3D Stacked SPAD Time Resolved Image Sensor SoC for Microendoscopy

- Using ST's 3D40 process
- Top Tier SPADs 90 nm
- Bottom Tier CMOS 40 nm
- 1.4 mm x 1.4 mm, 3D-integration integrated

- SPAD Layer
  - 8 µm pixels (BSI)
  - 45 % fill factor

- CMOS Layer
  - 390 ps gating resolution
  - Power consumption
    - 10 mW for Vdd (core); 100 mW for SPADs
  - Time resolved (390 ps)





https://ieeexplore.ieee.org/document/8777979

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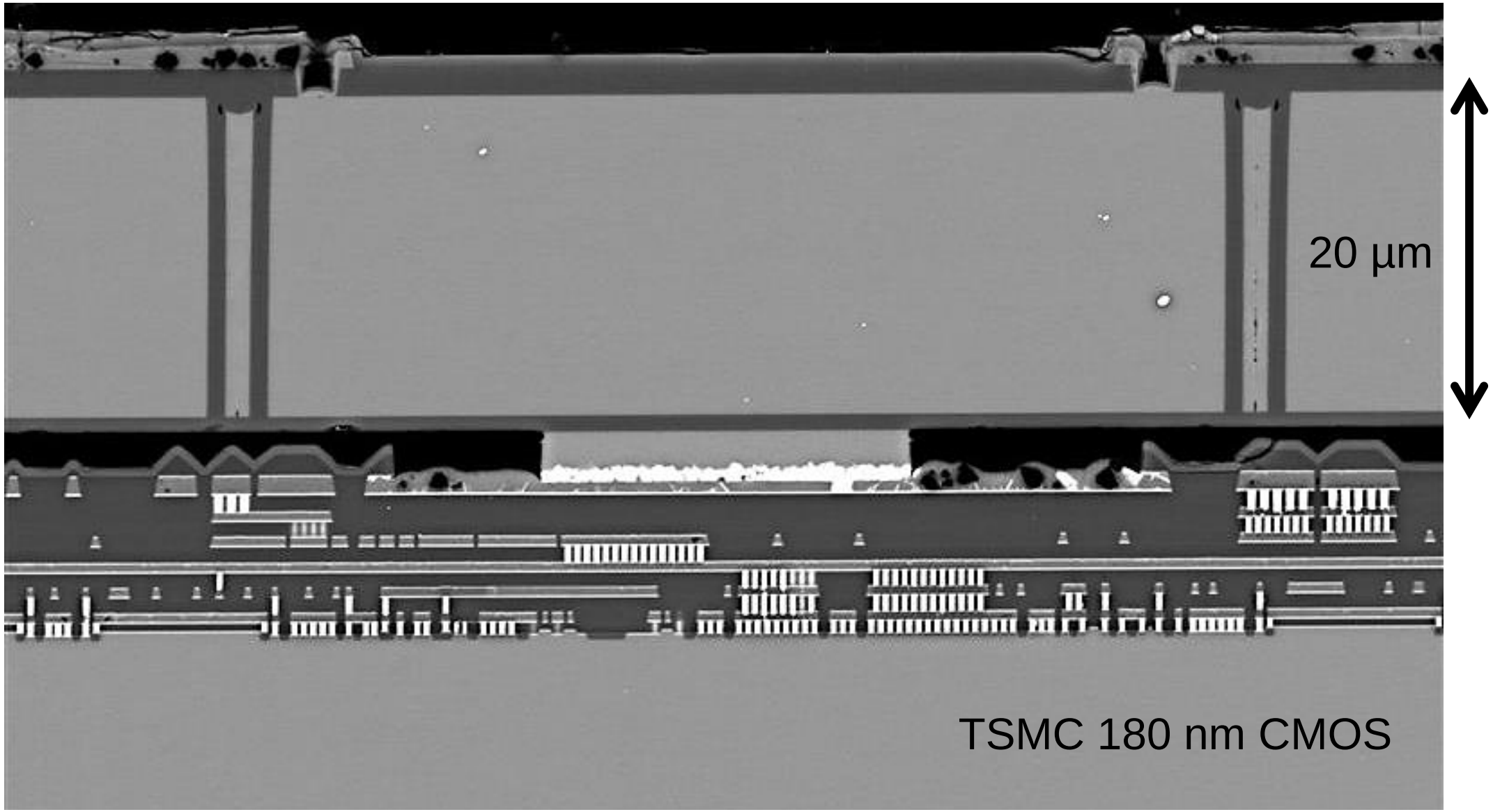
Side view of bonded SPAD



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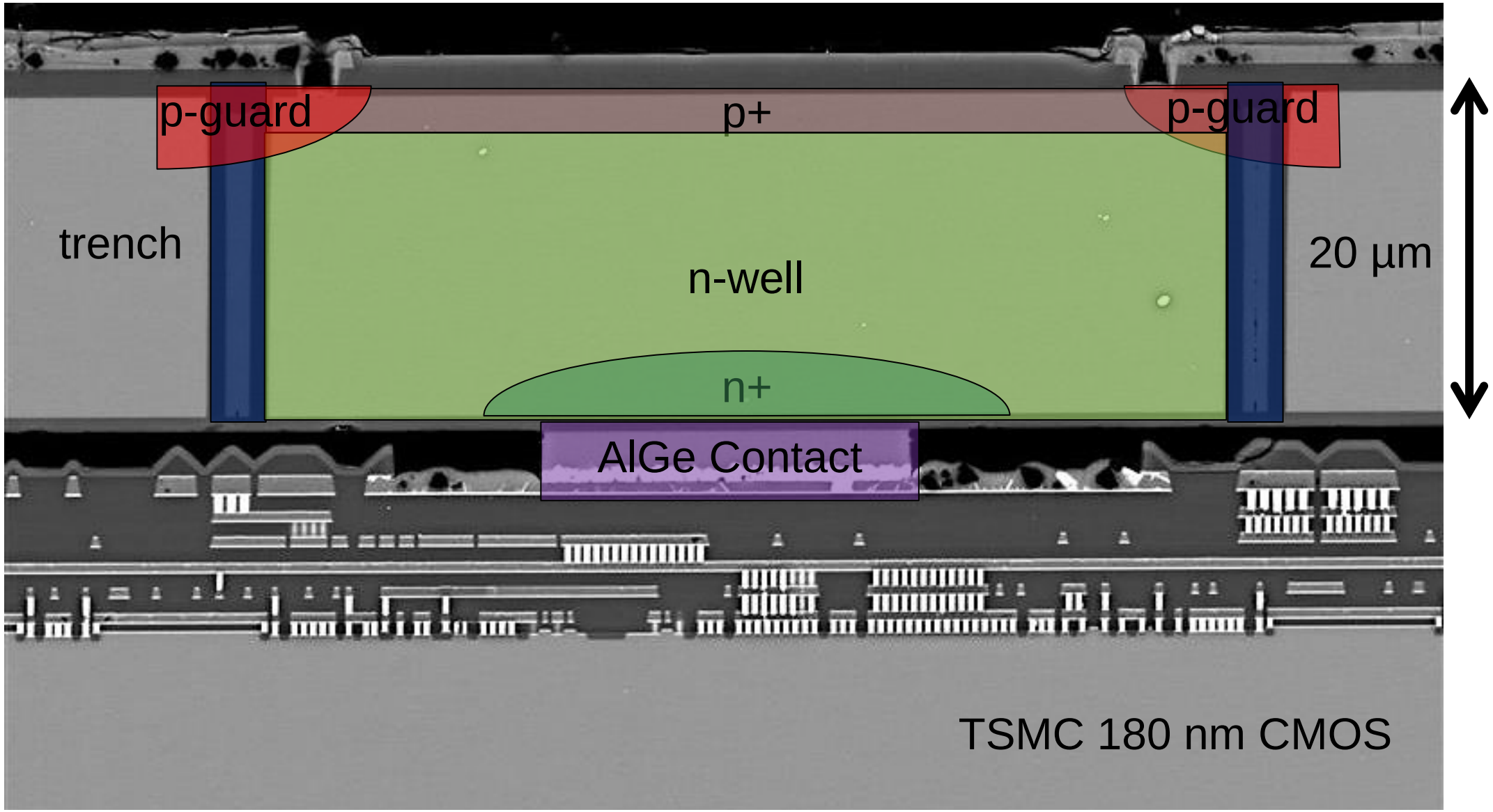
Side view of bonded SPAD



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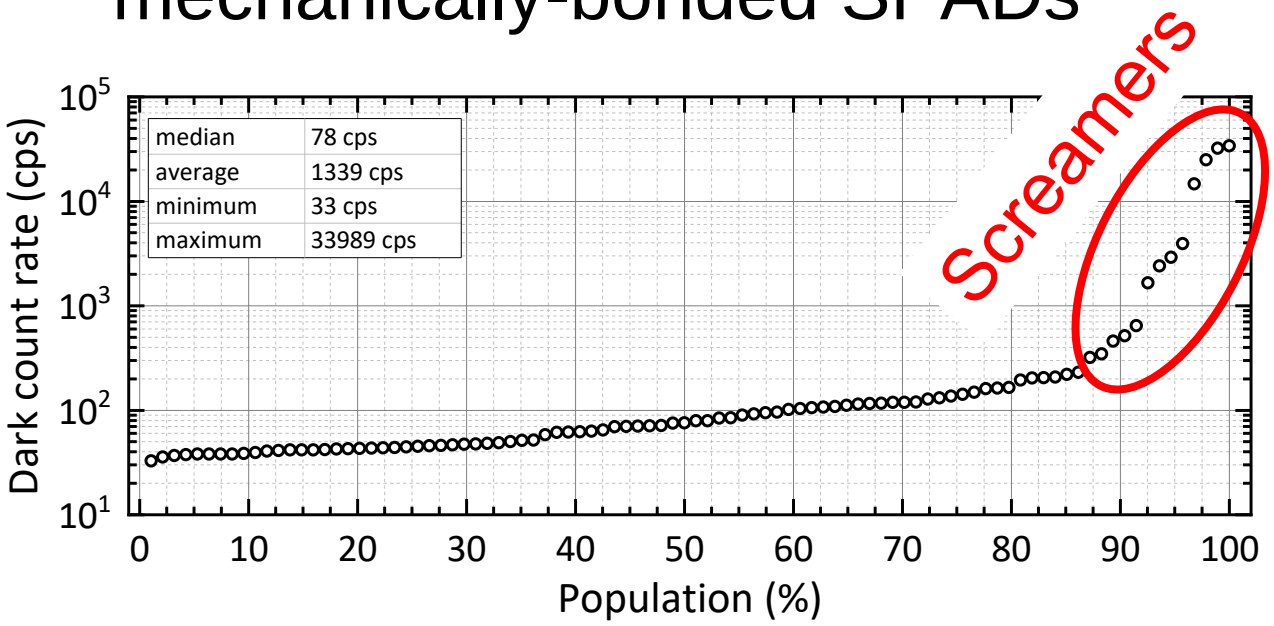
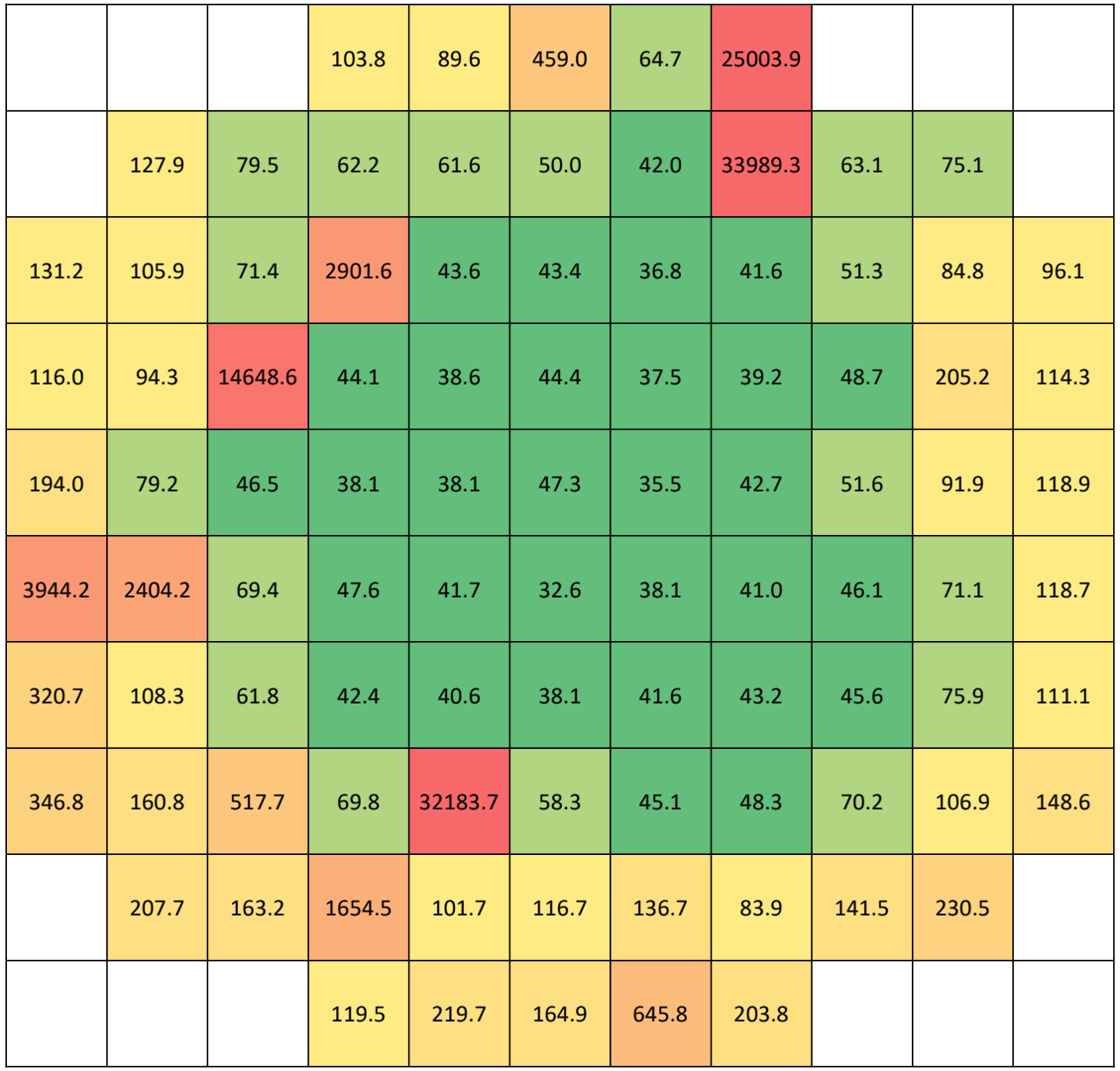
Status and results - SPADs

- Early stages of measurements on CMOS-bonded SPADs PCMs
- Expectations from 3D mechanically-bonded SPADs





DCR (cps)

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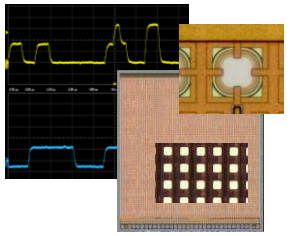
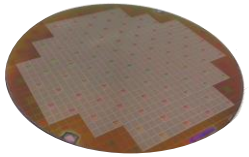
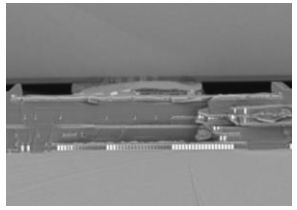
Our future roadmap and objectives



2D SPADs
and
Wafer level
bonding



1st 3D SPAD
wafer
(on fake CMOS)

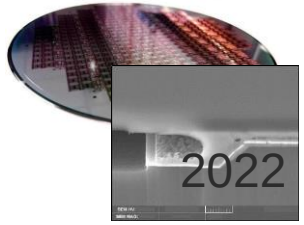


Complete
PDC

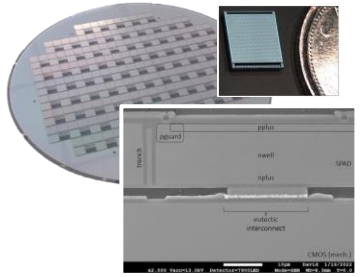
2018 — 2019 — 2020-21 — 2022 — 2022 — 2023 — 2024

Start
at TDSI

1st CMOS
readout



2nd CMOS
readout
wafer run



Bonding on
real CMOS
demonstrated

CMOS
180nm

Low power PDC optimization

System integration

Neutron detectors

Large cryogenic exp.

Spectral LIDAR

CMOS
65nm

Optimized SPAD layer

Die to wafer assembly process

CMOS readout singulated die run

Very low production capability - prototyping

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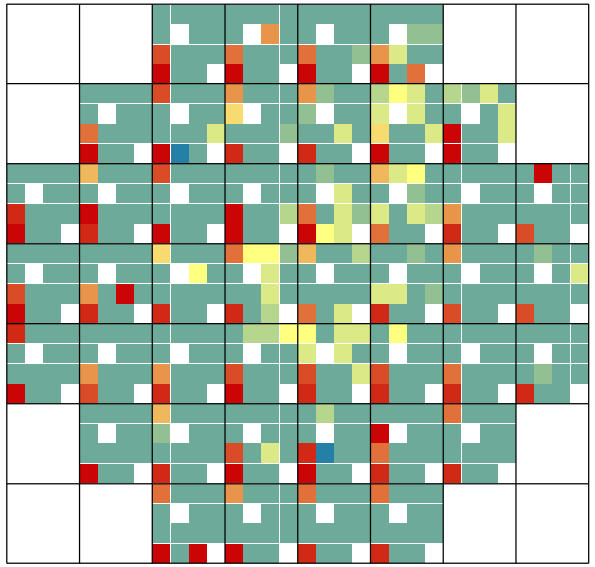
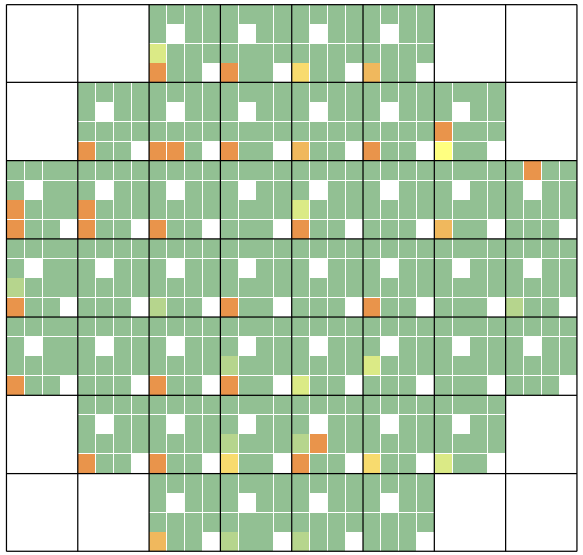
Status and results – CMOS/PDC

- Mapping whole wafer
- Testing various functionalities
- What makes for a known good die?
  - Power draw
  - Digital core «working »
  - Frontend working
- Yield optimisation

Core

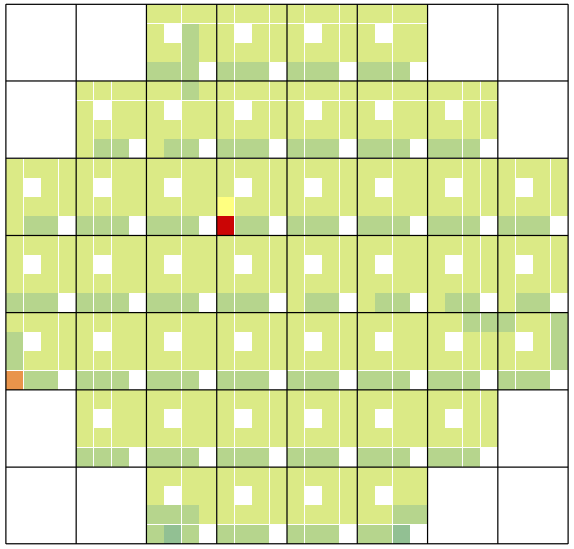


Frontend



Current draw from different supplies

IO



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