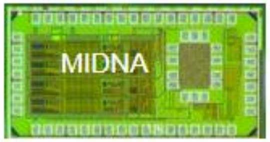
Overview of Fermilab ASIC Development in Photodetectors and Related Areas

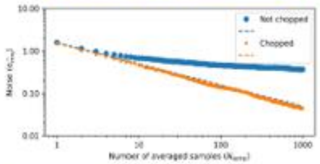
Paul Rubinov

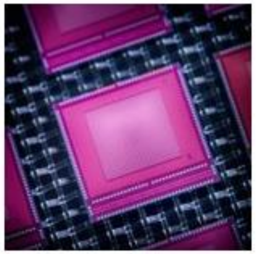
Fermilab Microelectronics

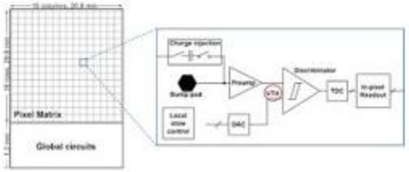
- ~ 25 designers + dedicated test engineers and support

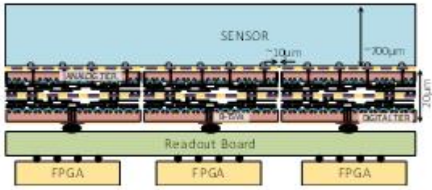
Ultra-Low Noise Sensing (Dark matter detectors)	Ultra-High Frame rates (Xray detectors)	Picosecond timing (HL LHC detectors)	Operation in extreme radiation/ cryogenic (HL LHC/ DUNE)	edgeless 3D ICs (HEP / BES light sources)



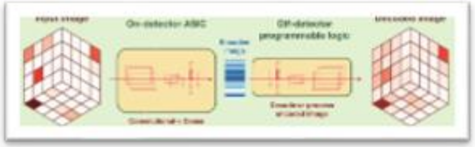


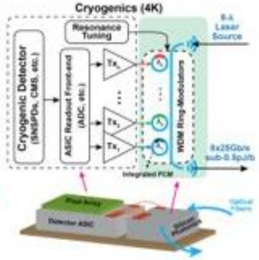






High speed cryogenic Data converters (with Microsoft)	Quantum Support Chips	AI-on-chip (ultra-fast data processing)	AI-in-pixel (minimizing data movement)	High-speed Photonic links (low power communications)





Slide from Farah Fahim

Microelectronics at Fermilab: focused on Extreme Environments

Cryogenic Radiation tolerant Ultra fast

Goal: develop the next generation of microelectronics for science

Essential for next generation HEP experiments

Design in advanced node technology has gotten increasingly complicated – ASIC life cycles have increased in both time and manufacturing costs

Challenge: maintain and expand core ME capabilities.

Plan, conduct, and maintain ME R&D and capability development program & link to the national ME ecosystem until the next HEP detector projects ramp up

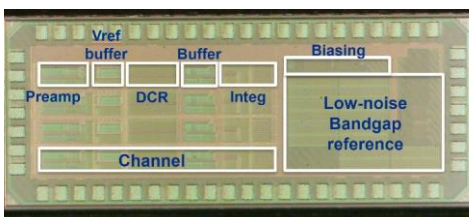
Opportunity: leverage CHIPS and Science Act funding for HEP microelectronics

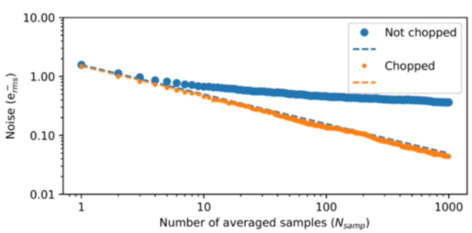
Leverage core capabilities for strong participation to CHIPS act programs to grow core competencies and expand workforce. Improve and add infrastructure

Skipper CCD and CCD-in-CMOS readout

Skipper CCD readout: MIDNA

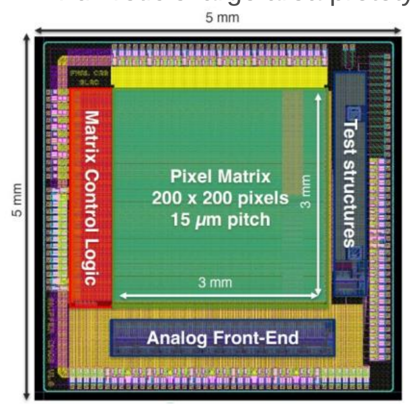
- State-of-the-art noise performance (~3e- noise performance)
- Cryogenic operation (100K)
- On-chip analog pile-up to reduce readout time
- 100x lower power, extremely small footprint, significantly reduced cost
- Excellent test performance





Skipper CCD-in-CMOS Sensor

- Collaboration with leading CMOS foundry (Tower Semiconductor) to develop Skipper-CCD in commercial CMOS process
- Prototyped ASIC has ~400 variations (pixel designs/process splits) to evaluate best design
- Testing underway, so far demonstrated detection, charge transfer, and skipping
- Full-reticle large area prototype to follow



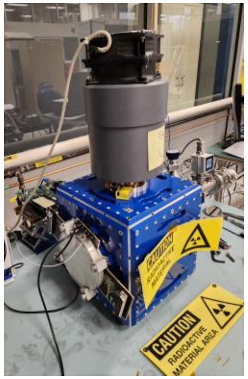
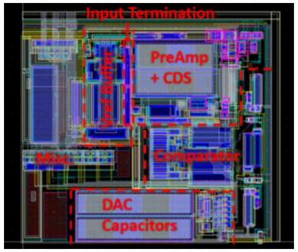


Image sensor ASIC

Fermilab SLAC CNEA Tower Semiconductor

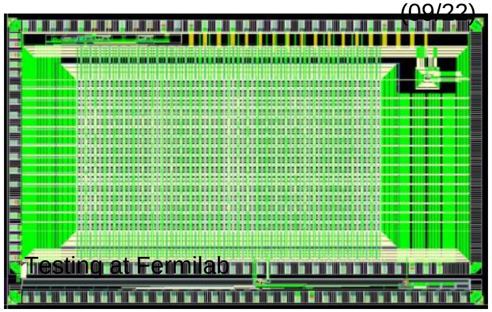
Highly-parallel readout ASIC for Skipper-on-CMOS

- Developed low-power in-pixel ADC for highly parallel readout (→ high frame rates)
- Per-pixel 10b ADC for massively parallel readout
- First two prototypes under test
- Full-reticle ASIC in 2023



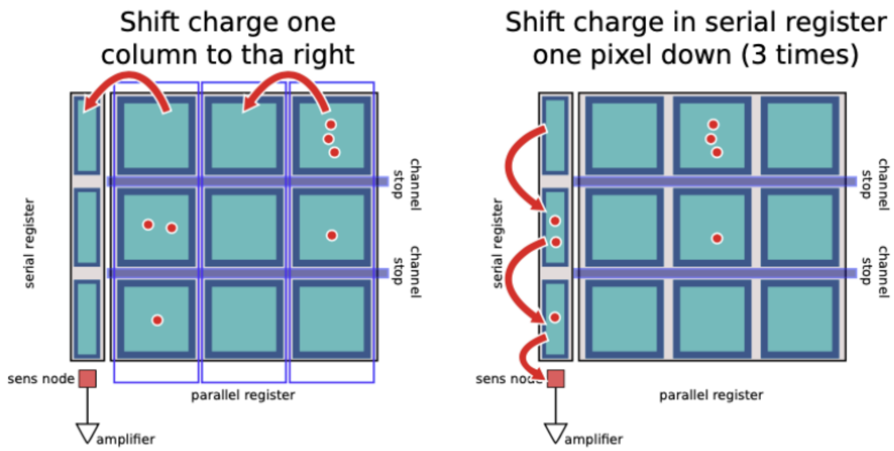
10b, 100KSPS
in-pixel ADC
(~30x30µm)

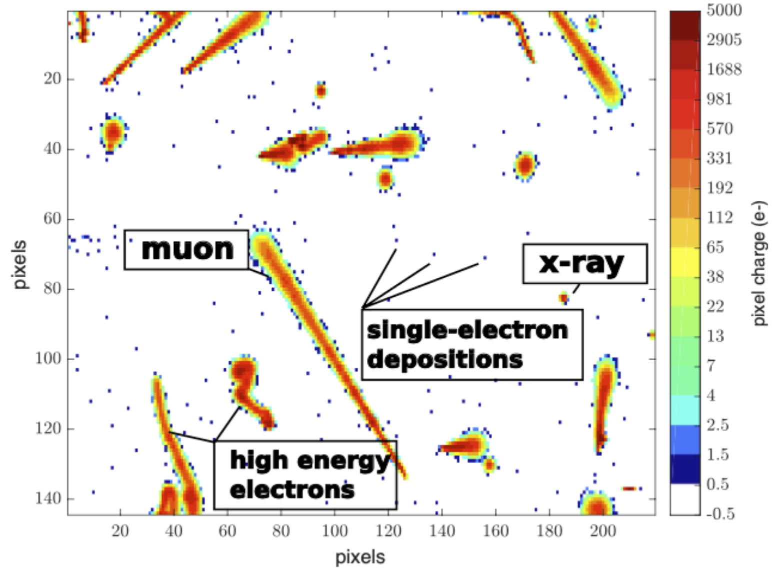
SPROCKET ASIC:
64x32 pixels
(09/22)

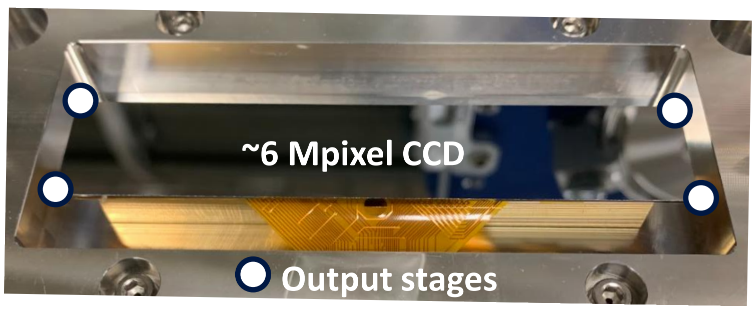


Skipper CCD

3x3 operation cartoon







More about Skipper-CCDs: doi.org/10.1002/asna.20230072 ,arXiv:1706.00028, 2107.00168, 2004.11378

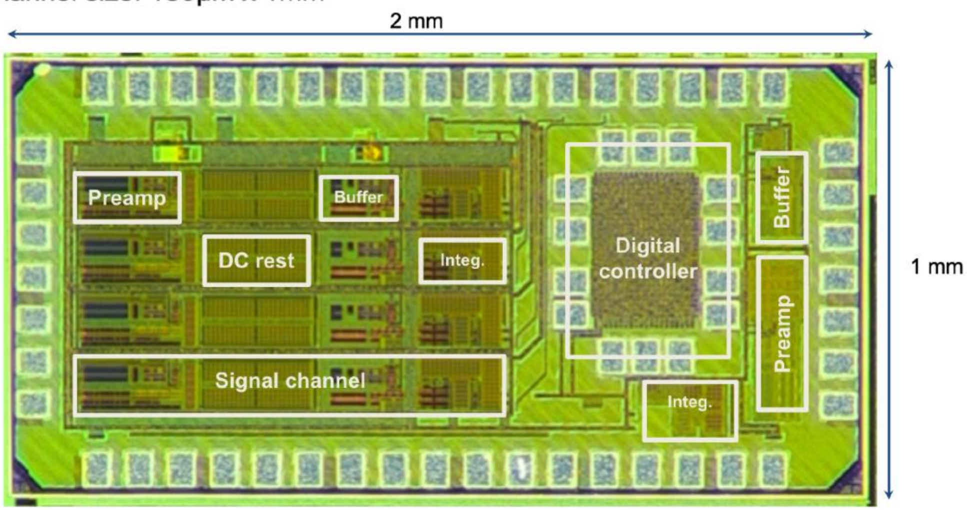
Cryogenic ASIC (~120K)

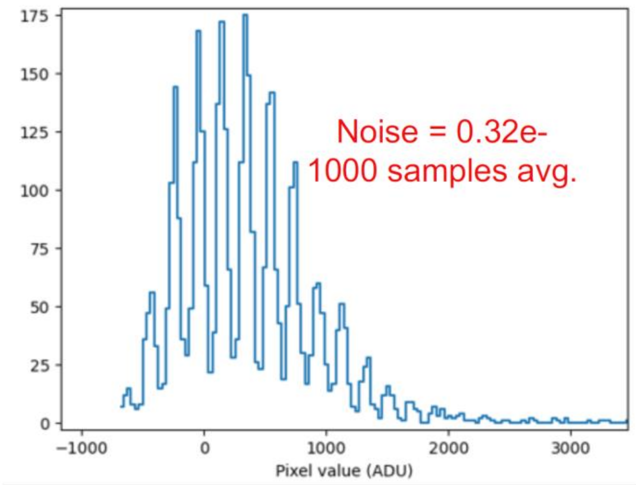
MIDNA: Low-Noise Skipper CCD Readout w/ Chopping Integrator

FNAL: Troy England, Hongzhi Sun, Davide Braga, Shaorui Li, Juan Estrada, Farah Fahim
CNEA: Fabricio Alcalde Bessia, Miguel Sofo Haro

- Midna1 demonstrated very low noise performance
- Midna2: implemented on-chip reference and buffers to further improve low-noise performance and isolate coupling between channels; improved integrator dynamic range to facilitate larger pile-up range for off-chip processing, and improved integrator sensitivity by further lowering the input offset.

Channel size: 150μm x 1mm





Top-Level Overview

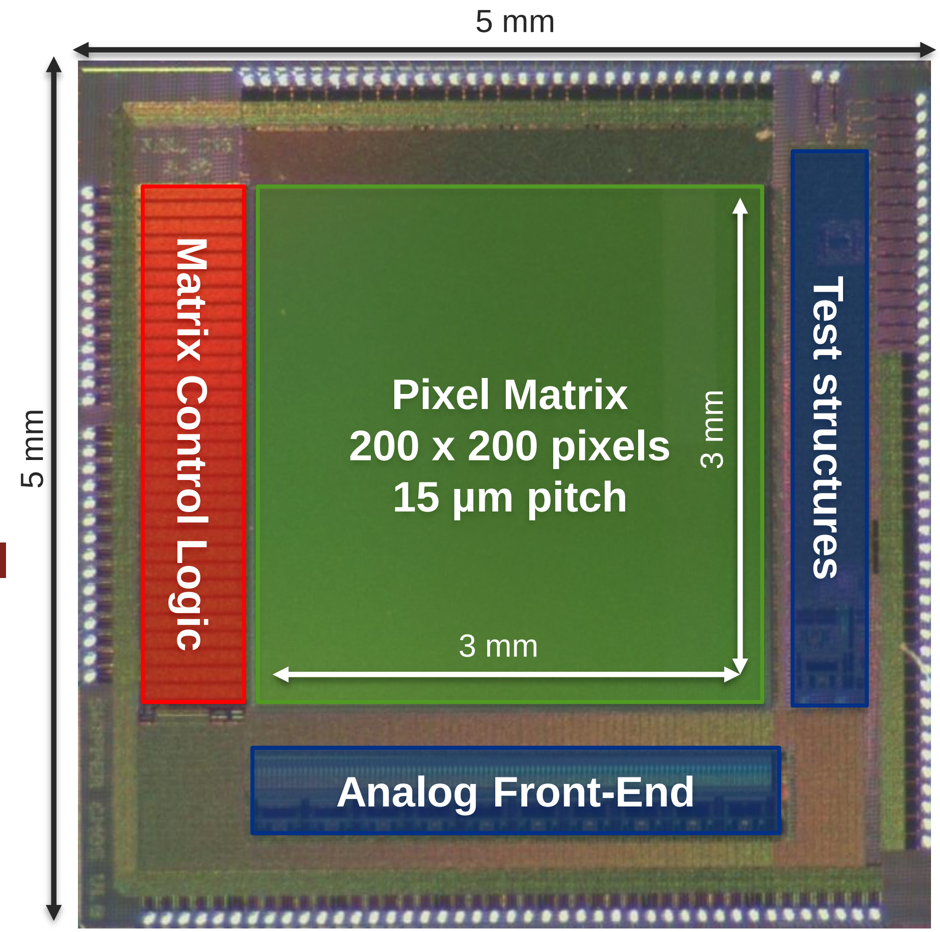
- MPW with front-side illumination
- Size: 5x5 mm^2
- Active area: 3x3 mm^2
- Pixel design compatible with Back-Side Illumination
- n-type channel detector

Collaboration Landscape:

1. Tower Semi: CMOS and Pixel Technology
2. Centro Atómico Bariloche: Pixel and Matrix testing
3. Fermilab: Front End Readout Design
4. SLAC: Digital blocks and top-level implementation
5. Fermilab, UNS: testing

Physics Applications

1. Low mass dark matter searches
2. Single electron trackers for dark sector searches
3. Soft x-ray spectroscopy
4. Astrophysics: deep measurements of dark energy and dark matter signatures
5. Single-photon quantum sensing



AFE Specification

- Achieve single-electron CMOS Imaging
- High dynamic range
- Microsecond readout time

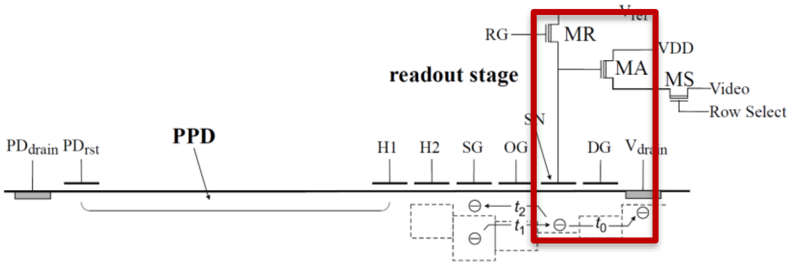
Pixel

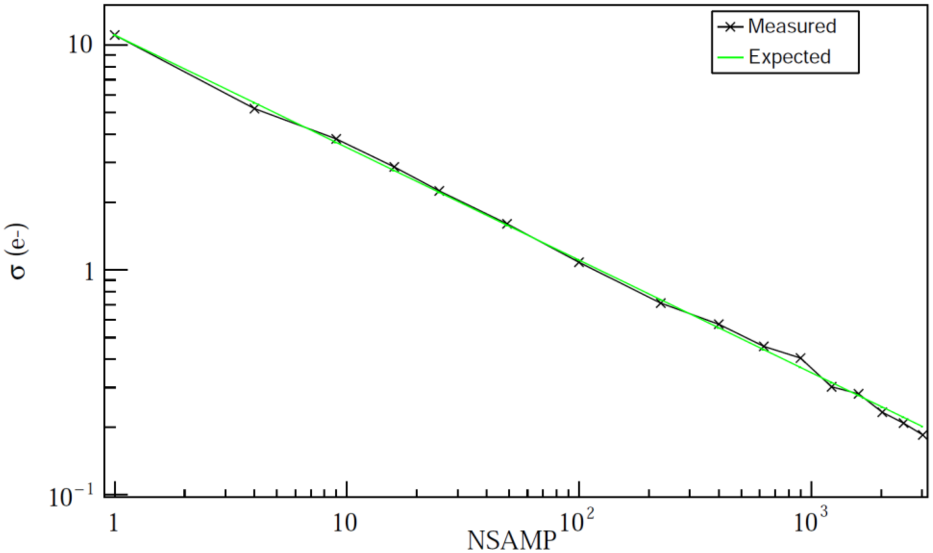
Variable	Value	Unit
Conversion Gain	115	µV/e-
Dynamic range	11000	e-
White Noise	<10e-9	V/√Hz
Fnc	>100	MHz
ENC (single Meas)	<1	e-

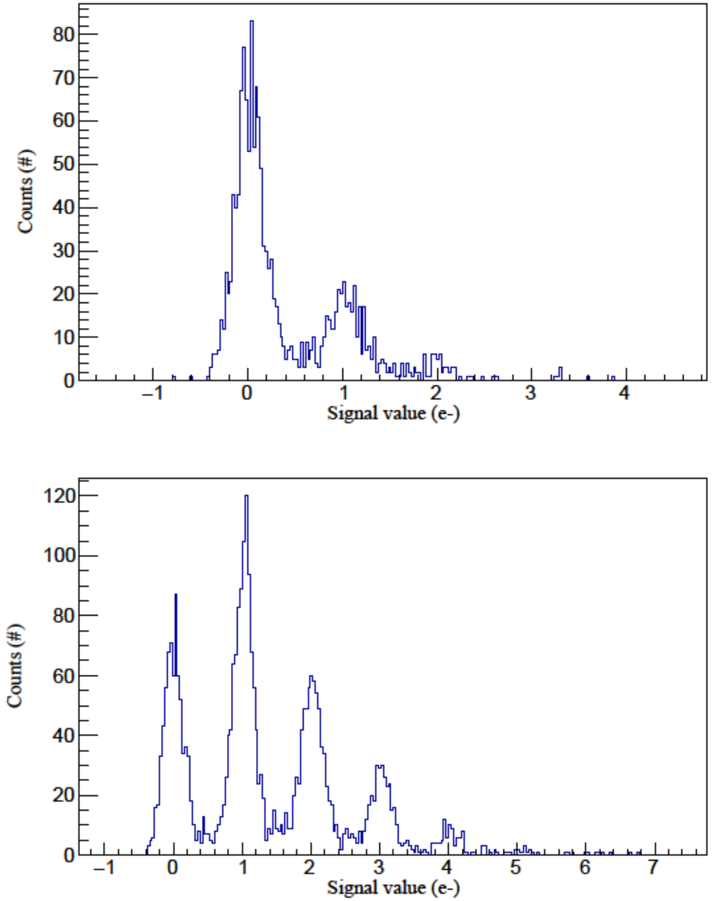
Analog Readout

Variable	Min	Target	Max	Unit
Input Amplitude	1		11000	e-
Input Amplitude	0.125		1375	mV
PGA gain (trimmable: 4-bit)	1		64	V/V
measurement time	1	10		µs
Temperature	-40	27		C
ENC (single measurement)		<2		e-

Understanding the operation of the output stage

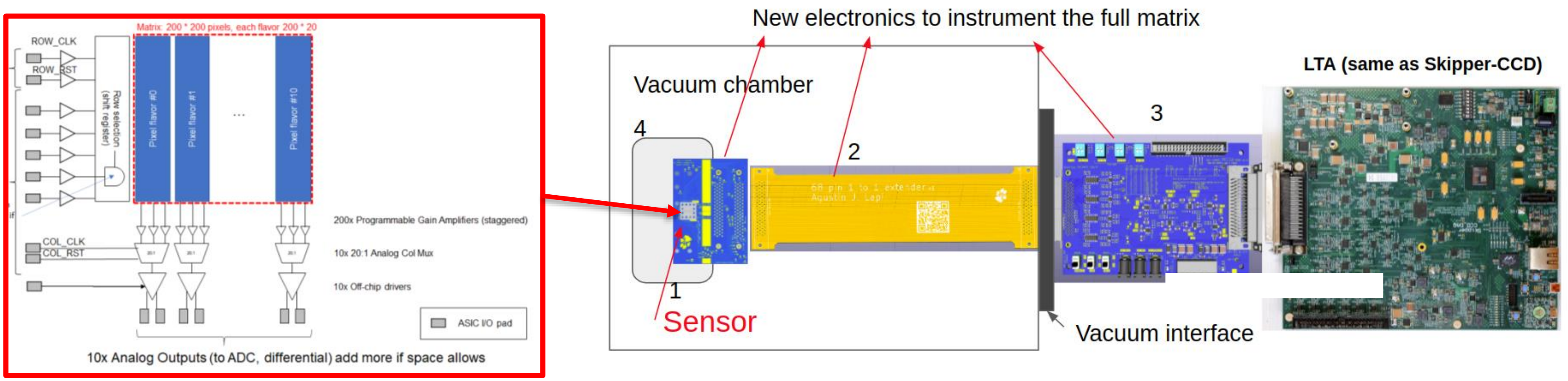






- Output stage characterization
- Demonstration of noise reduction
- Single sample noise s
- Measurements from the SF showing much lower noise. Some extra LF noise.

Instrumentation of the full matrix

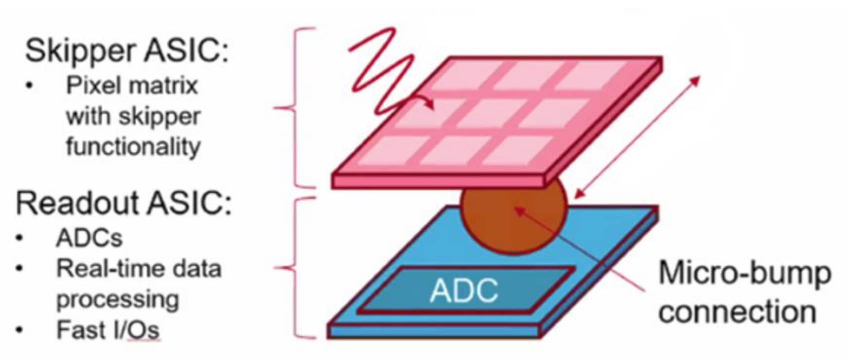


- ❑ New adaptor board sent for fabrication to instrument the full matrix
- ❑ Instrument the full matrix
- ❑ The full matrix has 20 different pixel architectures with small modifications in the pixel architecture
- ❑ **Architecture: 20 variants – 5 Splits: 400 pixel falvors**

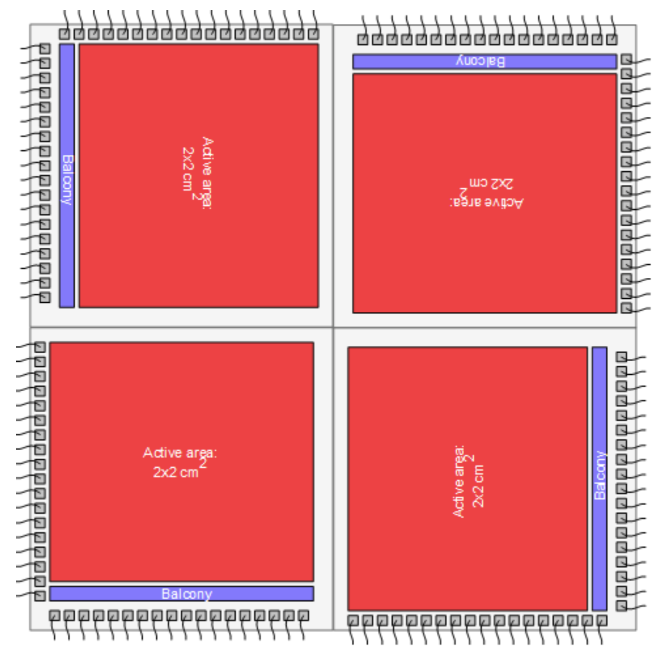
Skipper-in-CMOS: phase II

Goal of Skipper-in-CMOS phase II:
- Increase frame-rate to 1 kfps

Novel architecture with 3D integration:
- Increase parallelism of the system: x16 pixel cluster connected to an ADC
- Skipper-in-CMOS with back-side illumiation (BSI) bonded to readout ASIC (SPROCKET) on CMOS 65nm



Conceptual design of camera based on tiled, full-reticle Skipper-in-CMOS sensors

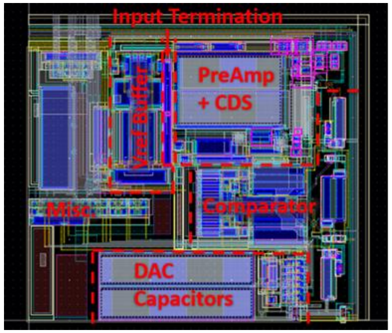


SPROCKET (Skipper-CCD Parallel Read-Out Circuit) readout ASIC

Readout ASIC for hybrid bonding with image sensor.

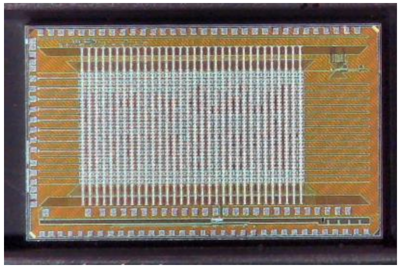
In-pixel readout front end includes a preamplifier, correlated double-sampling circuit, and 10b SAR ADC in ~30×30μm (60x60 μm including digital)

- **SPROCKET1 (Sep '22):** 64 x 32 pixel array with in-pixel ADC
- **SPROCKET2 (Dec '22):** second version including analog pile-up capability
- **SPROCKET3A (May '23):** Prototype of digital control + pattern generation
- **SPROCKET3 (Nov '23):** 320 x 64 pixel array, includes full functionality to be bump-bonded to CMOS image sensor
- **SPROCKET3-FR (Summer '24):** Full-reticle SPROCKET

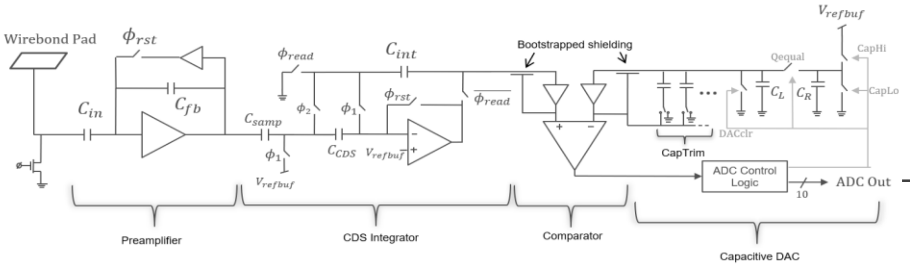


10b, 100KSPS in-pixel ADC (~30x30μm)

SPROCKET1 Analog Pixel Layout



SPROCKET1 Die Photo



Binary tree + serializer

SPROCKET2 front end with analog pile-up

Conclusions

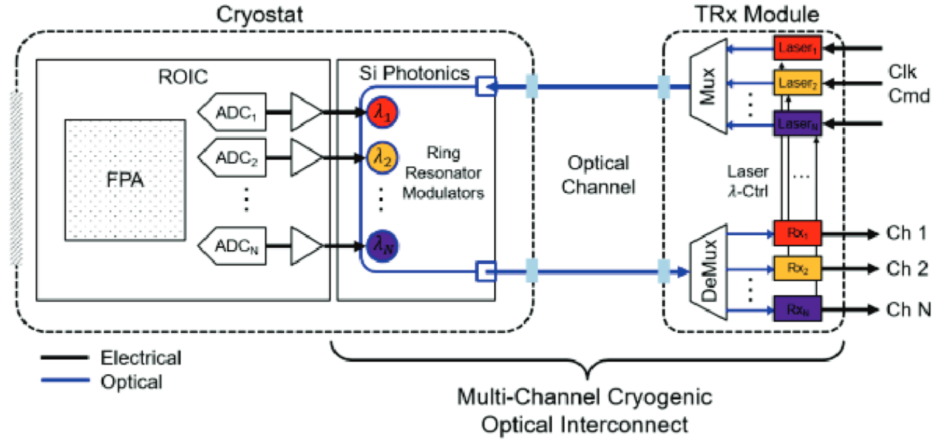
- The single photon counting capability of the pixel unit has been demonstrated.
- Extra optimization is required to get the best performance of the device.
- Most of this optimization will come from the instrumentation of the full matrix. Different pixels architectures.
- Test of the full matrix will start soon.
- A second version of BSI device is being designed.
- A fast readout ASIC for bump bonding to the sensor is being developed.

Silicon Photonics: A Critical Technology for Future Detectors

100x bandwidth, **100~1000x** lower heat load, **10~100x** channel density, EMI/cross-talk immunity.

Application Areas:

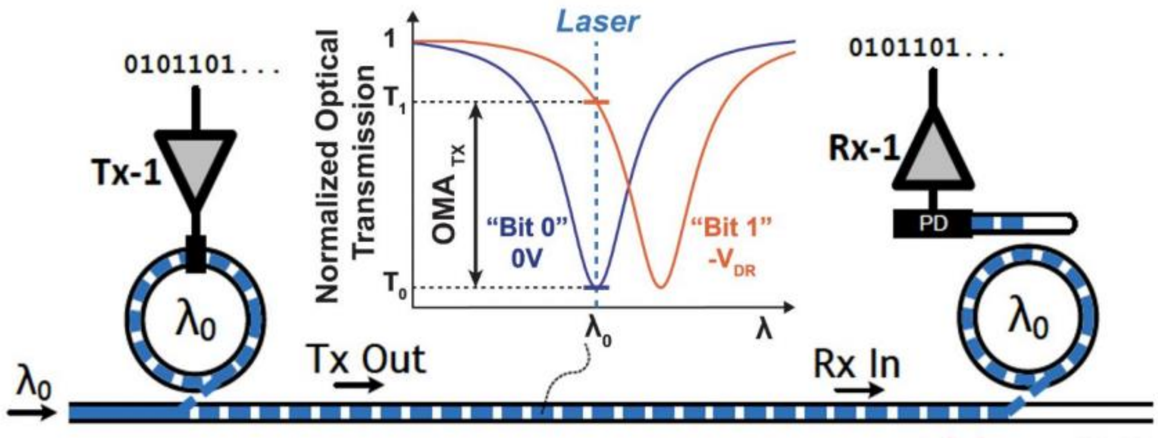
High-Bandwidth, Low-Power RT Readout	• FCC-ee, FCC-hh • High-rate X-ray Imagers
Cryogenic (100K, 4K) Readout	• Dune Mod. 3/4 • SNSPDs • Quantum / SC Readout
Radiation-Hard Readout	• LHC Phase 3

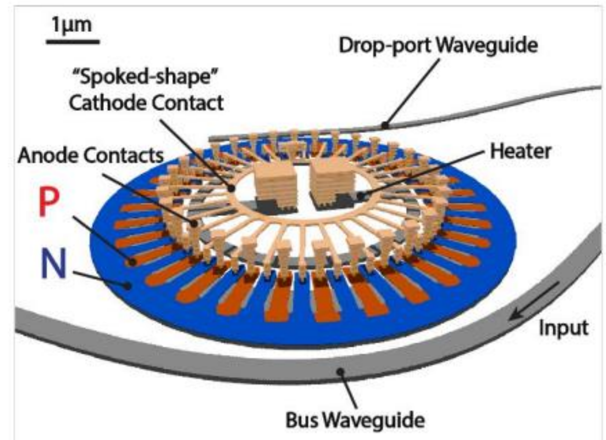


Quotes from ECFA Detector R&D Roadmap:
"Silicon photonics may be a **game-changing technology** in this context thanks to its good integration density and integration synergies with microelectronics." [7.3.2.3]

"Silicon photonics as the successor to actively modulated VCSEL-based links, facilitating **full-custom photonic integrated circuits (PICs) for HEP** (DRDT 7.4, DRDT 7.5)" [7.3.2.4]

Micro-Ring Modulators





The Potential:

- Extremely high bandwidth through WDM
- Low power (signaling mirror analogy)

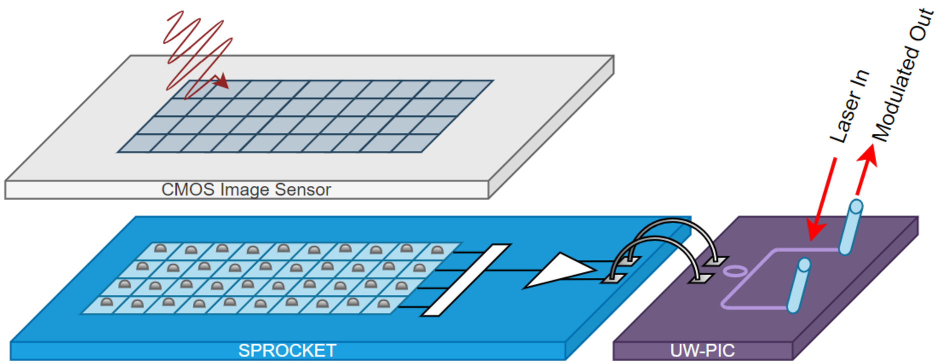
The Challenges:

- Improving cryogenic bandwidth
- Tuning cryogenic MRMs
- **Electronic/Photonic Co-design**

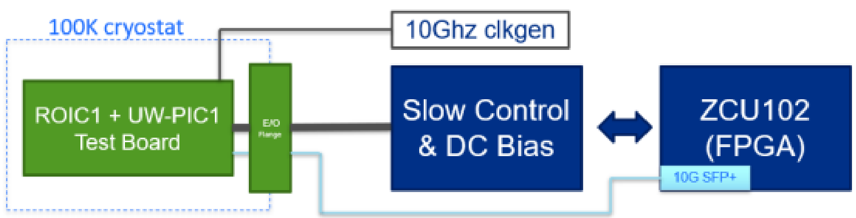
Fermilab

SParkDream (Silicon Photonics Demonstration at Fermilab)

Key Objective: Demonstrate the readout of a pixel detector ASIC using silicon photonics (10.24 Gb/s/chan) at both room and medium (100K) cryogenic temperature.



ROIC/PIC Integration (top)
Demonstration Block diagram (bottom)



We are here. → **Phase 0:** Design test software and hardware.

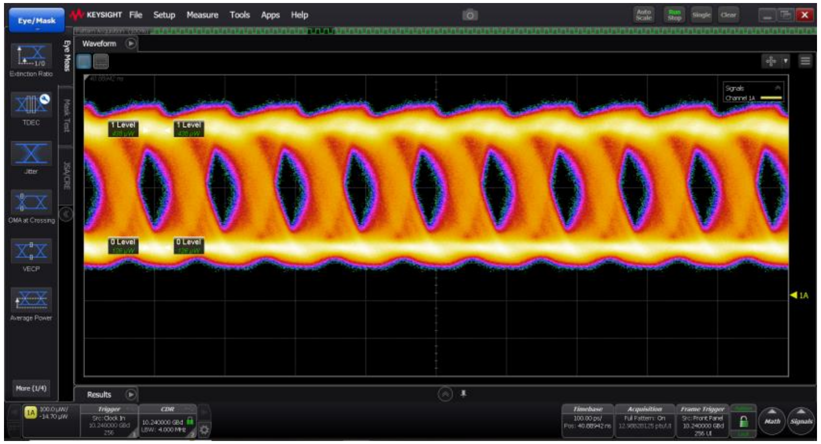
Q1 2025 — **Phase 1:** Demo Single-Channel Link @ RT + Cryo

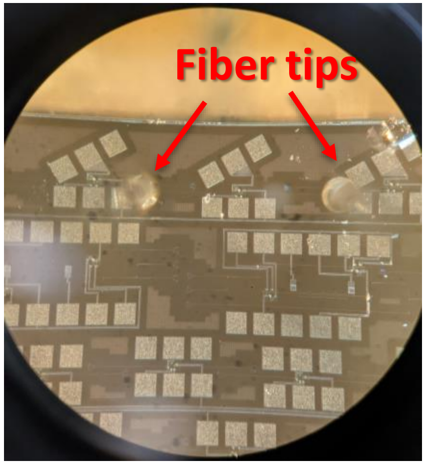
Q3 2025 — **Phase 2:** Demo Wavelength-Division Multiplexing (WDM)

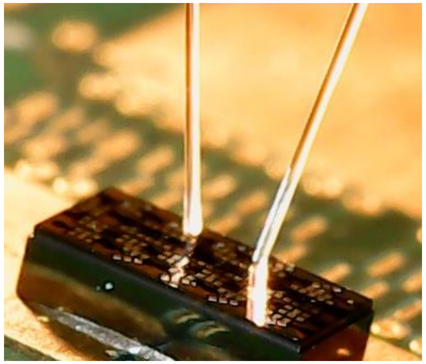
Future Work: Deep Cryo (4K), radiation hardness

SParkDream Initial Demonstrations in 2024

- Created a prototype link using a discrete optical transmitter with a driver based on the CERN lpGBT.
- Demonstrated a closed link at 10.24 Gb/s.
- Initial independent verification of ASIC and FPGA firmware.
- Prototyped micro-positioners and demonstrated successful alignment to photonic IC grating couplers.



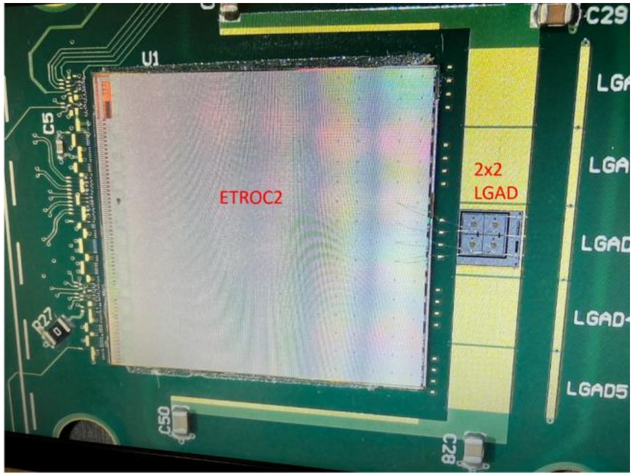




Fast Timing

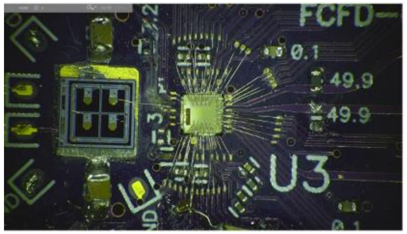
ETROC

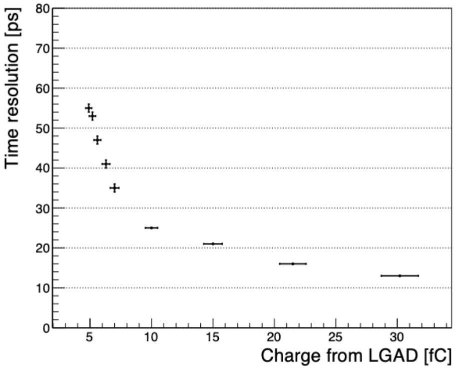
- LGAD readout ASIC for CMS Endcap Timing Layer
- 16x16 pixel, full reticle chip in 65nm
- ETROC2: full size, full functionality prototype currently being tested
- Per-pixel TDC with self calibration scheme to compensate for process variation, temperature, and power supply voltage
- Sensor+ASIC time resolution of 40ps



Constant Fraction Discriminator

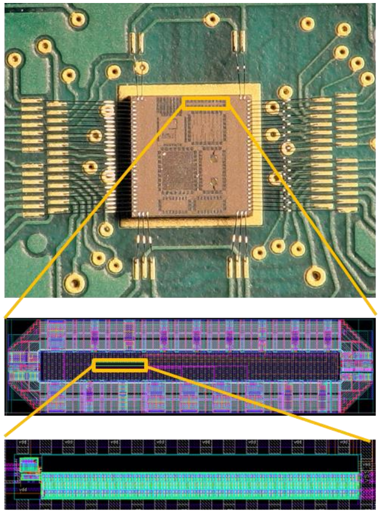
- 65nm CMOS
- does not require offline corrections or calibrations
- Achieves 15ps for 20fC signal





ASIC TDC

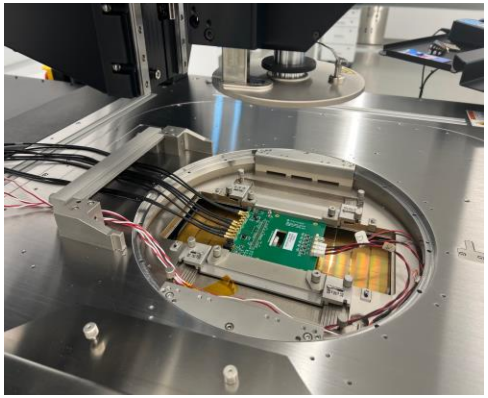
- Time-to-digital converter test structure for SNSPD readout
- Cryogenic operation (4K)
- 22nm CMOS
- Demonstrates better than 8ps timing resolution at 4K (300uW)

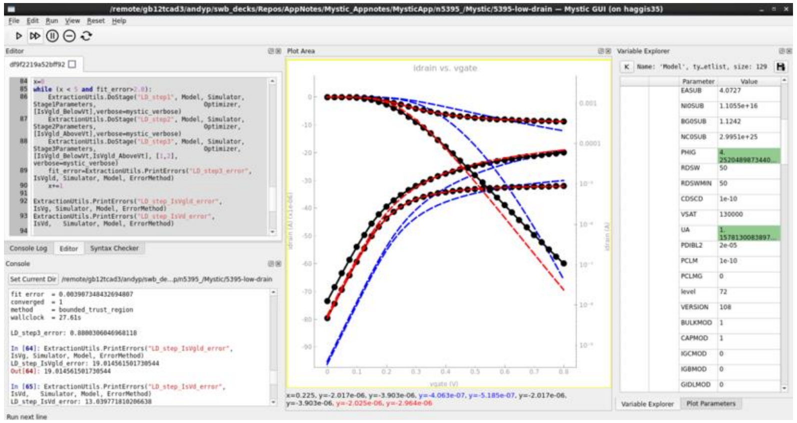


TDC block: 250x20μm

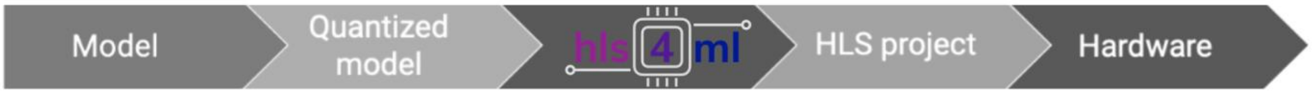
MODELING, TESTING AND CHARACTERIZATION

- Testing **infrastructure**: 12” wafer probing; cryogenic probing
- **Robotic testing** for mid-volume chip characterization
- Development of extreme environment **technology models** for cryogenic and rad-hard chips

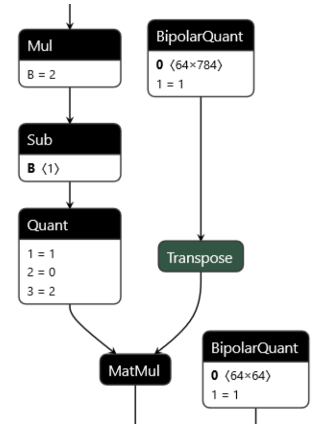


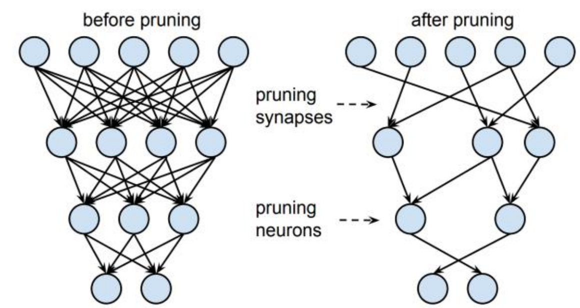


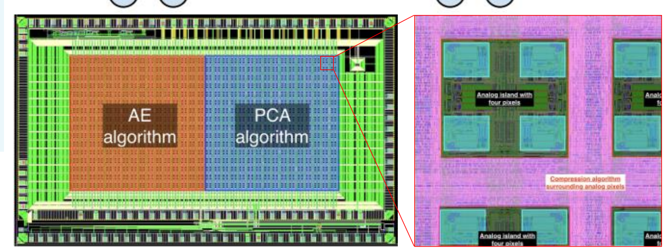
OPEN-SOURCE TOOLS & EDGE AI



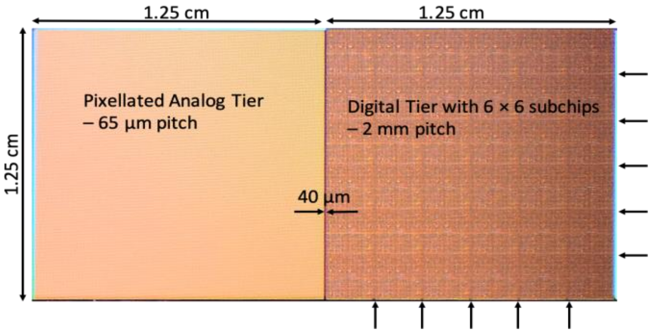
- Develop **efficient edge ML** algorithms
  - Quantization and sparsity, optimization techniques
  - Physics-inspired and robust inverse algorithms
- Build user-driven, **open-source workflows** for algorithm-hardware codesign
  - Democratizing powerful edge ML for a broad range of scientific applications and industry
  - Workforce development, multi-disciplinary collaborations, and education/demos/tutorials

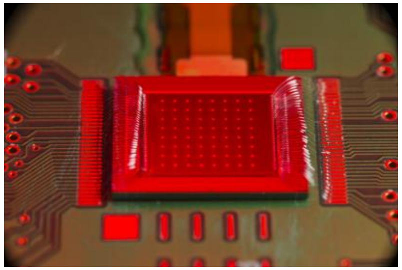




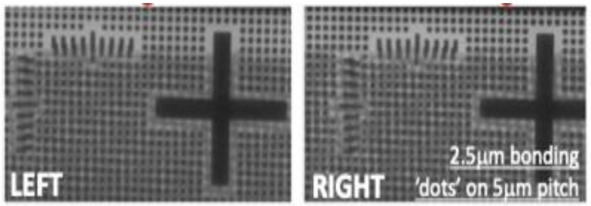


HETEROGENOUS SYSTEMS

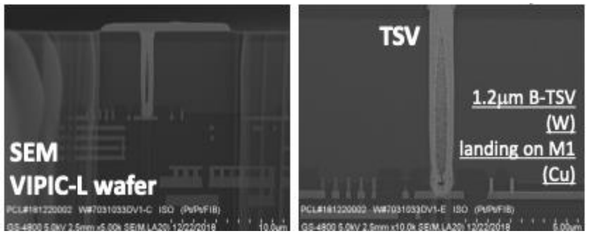


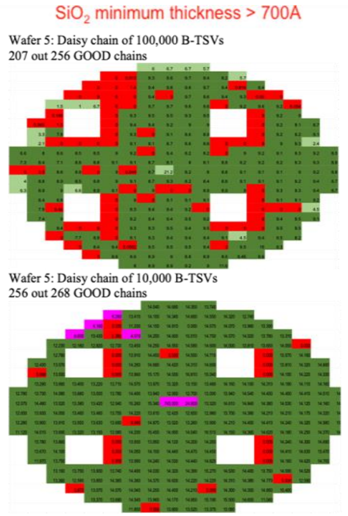


Face-to-face bonding



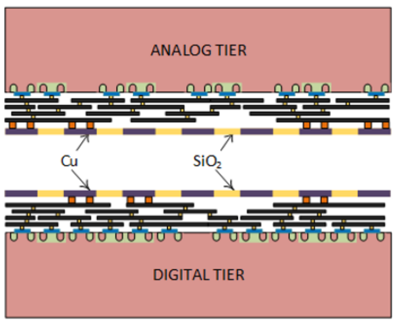
B-TSVs and back-metal



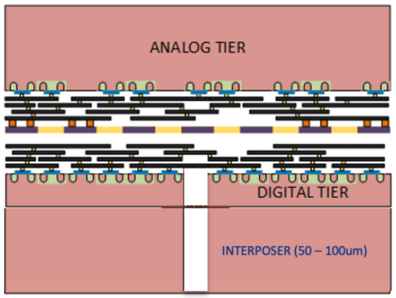


- Fermilab started investigating 3D integration in 2006
- **Evaluated various techniques setting the current industry standard for DBI bonding**
- Created 3D IC consortium with various university, lab and industry partners
- Support US manufacturing
- Enable next generation research on heterogenous multi-layer chip stacks

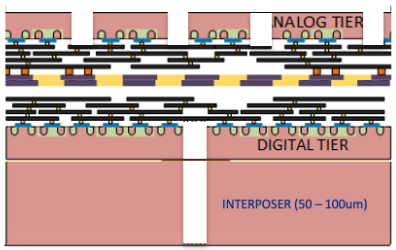
Establishing Chicago 3D Chips Codesign Community



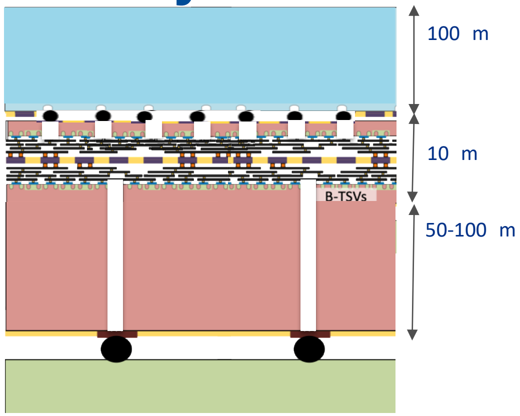
a. Face-2-Face wafer bonding



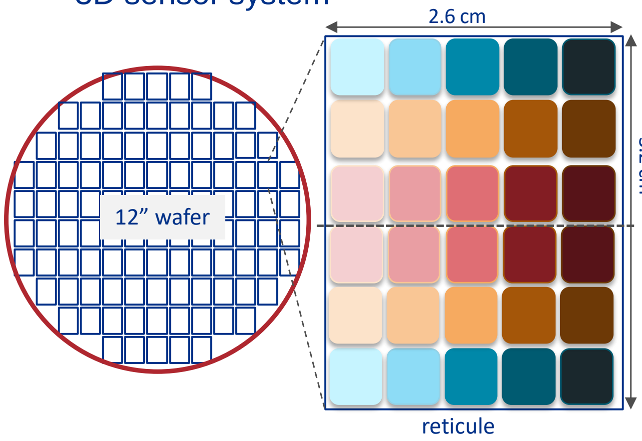
b. B-TSV insertion and bond to TSV interposer wafer



c. Thinned down top side and B-TSV insertion



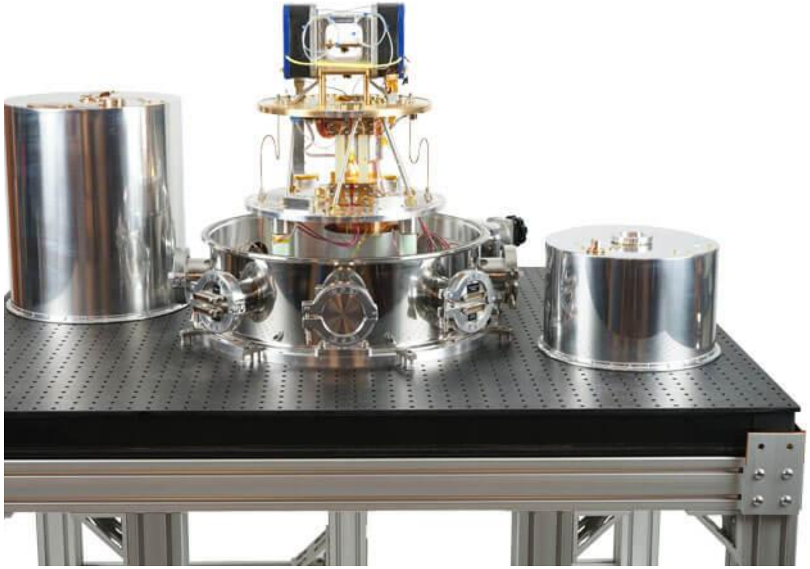
3D sensor system



- CREATING A COMMUNITY and RELEVANT PARTNERSHIPS
- Create open source ADK (Assembly Design Kits) and distribute to consortium members
- Fermilab assembles MPW work with (IMEC, MUSE and others)
- Currently have a multi party NDA with more than 80 institutions for HEP chips (IMEC-TSMC-CERN-Fermilab and others)

Utilize Fermilab's new Integrated Engineering Research Center

Significant investment in last few years



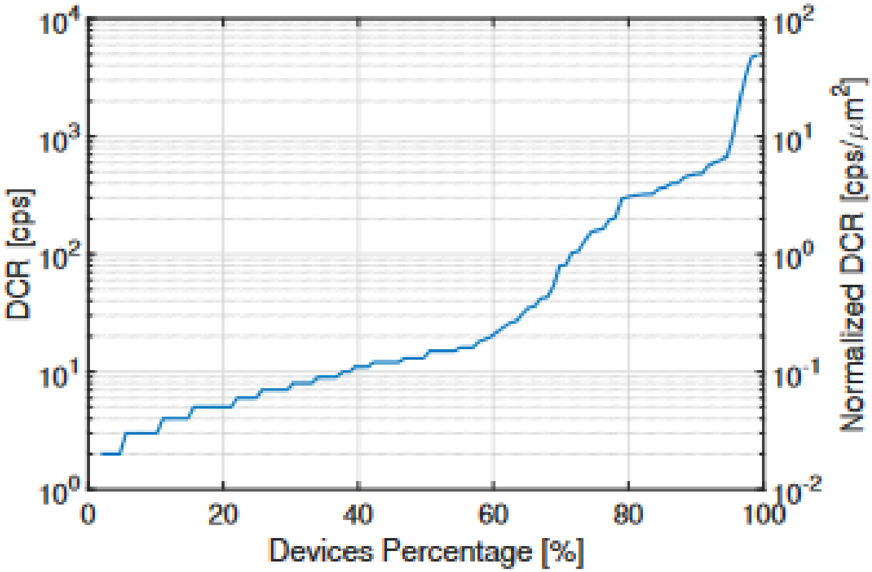
dSiPM for LAr

11/20/2024

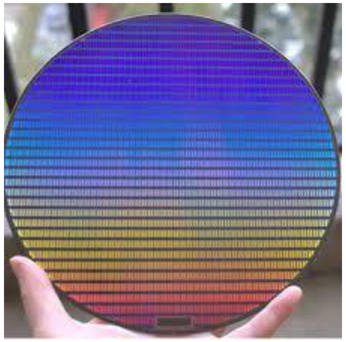
In partnership with:

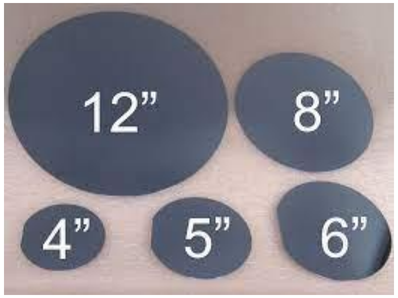
EPFL GlobalFoundries®

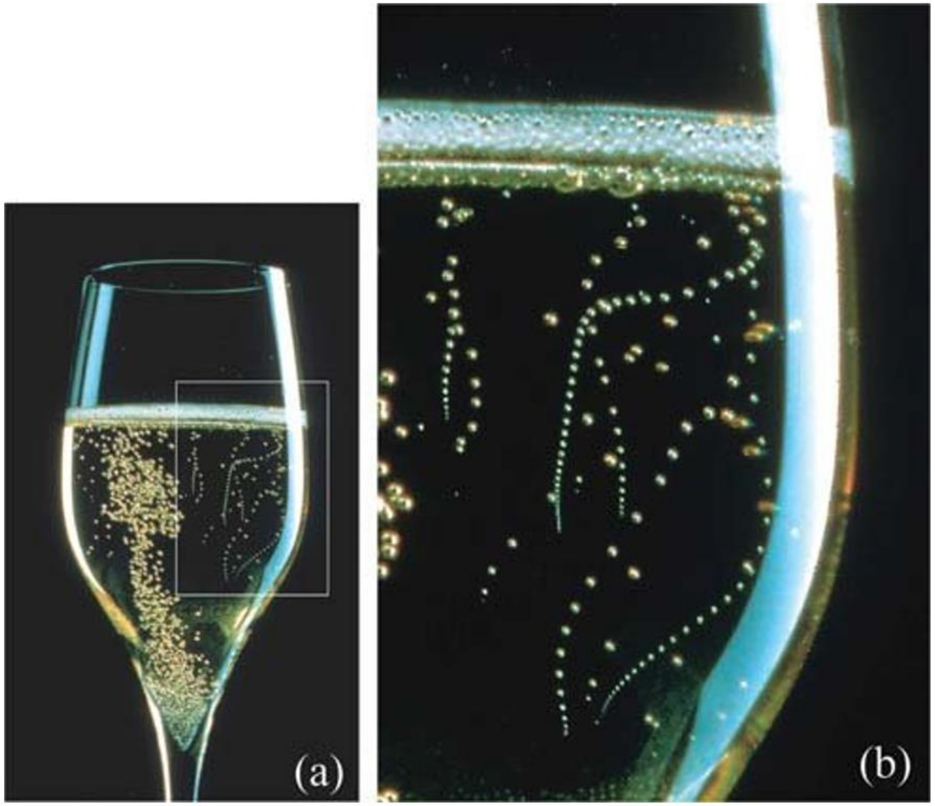
Motivation



From Francesco Gramuglia PhD Thesis



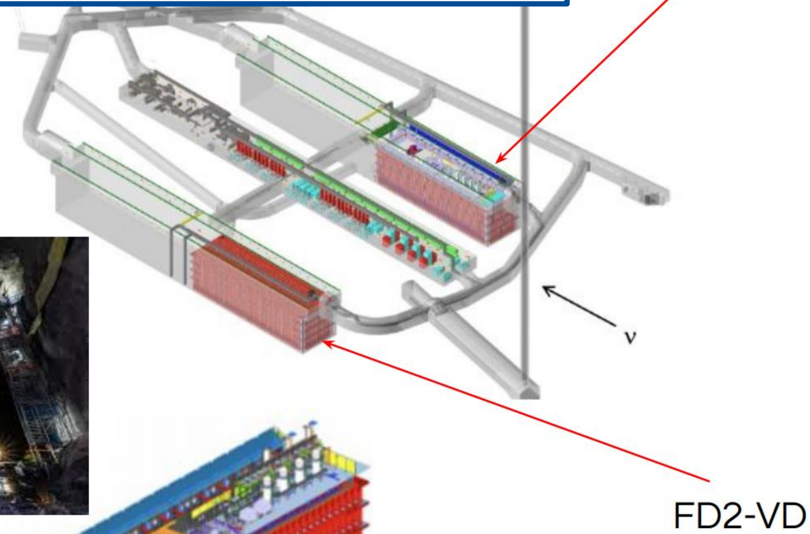


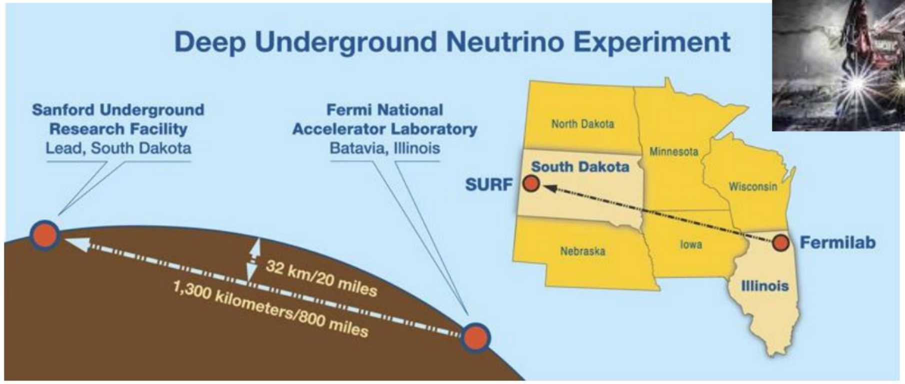


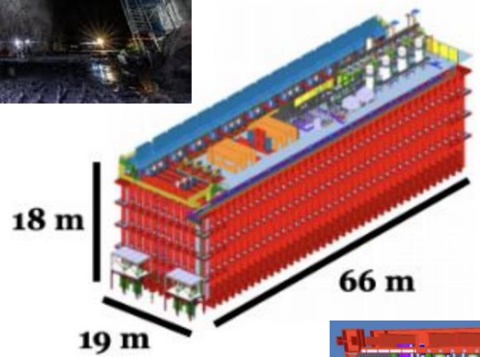
https://www.researchgate.net/publication/23412886_Recent_advances_in_the_science_of_Champagne_bubbles

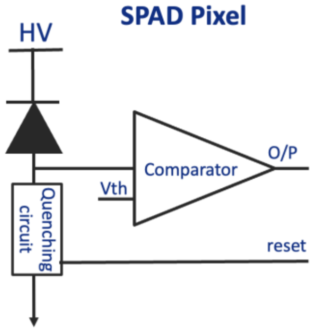
DUNE PDS overview

- **4 LArTPCs** of **17 kton** and **1.5 km** underground
- Phase I :
  - **FD1 - Horizontal Drift LArTPC**
  - **FD2 - Vertical Drift LArTPC**
- Phase II :
  - **FD3 and FD4:**
    - **Vertical drift**

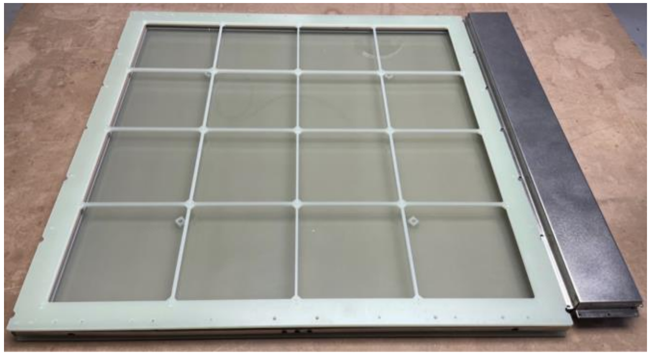




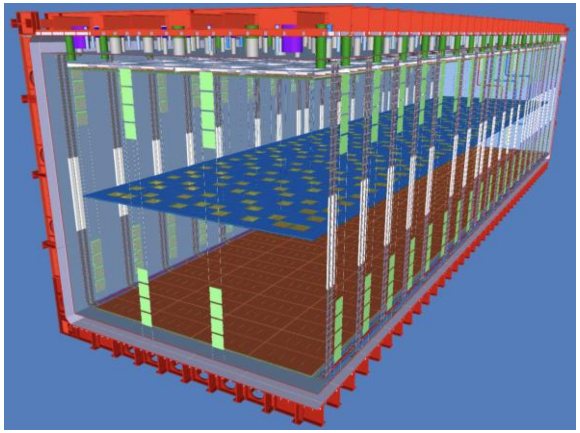




DigitalSiPM



SiPMs-Based Photodetection Unit

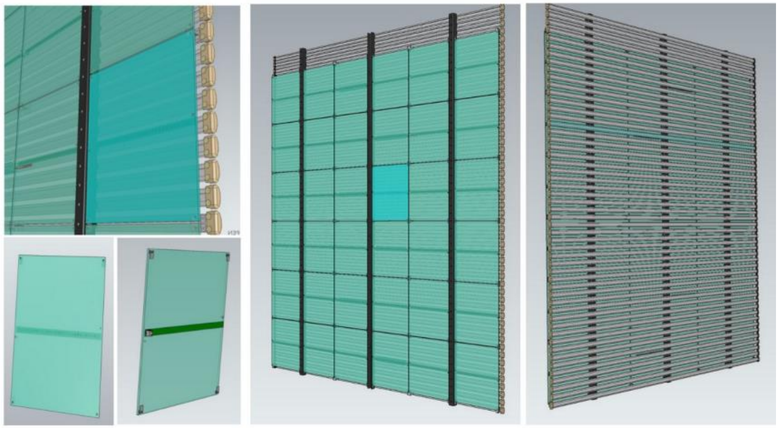


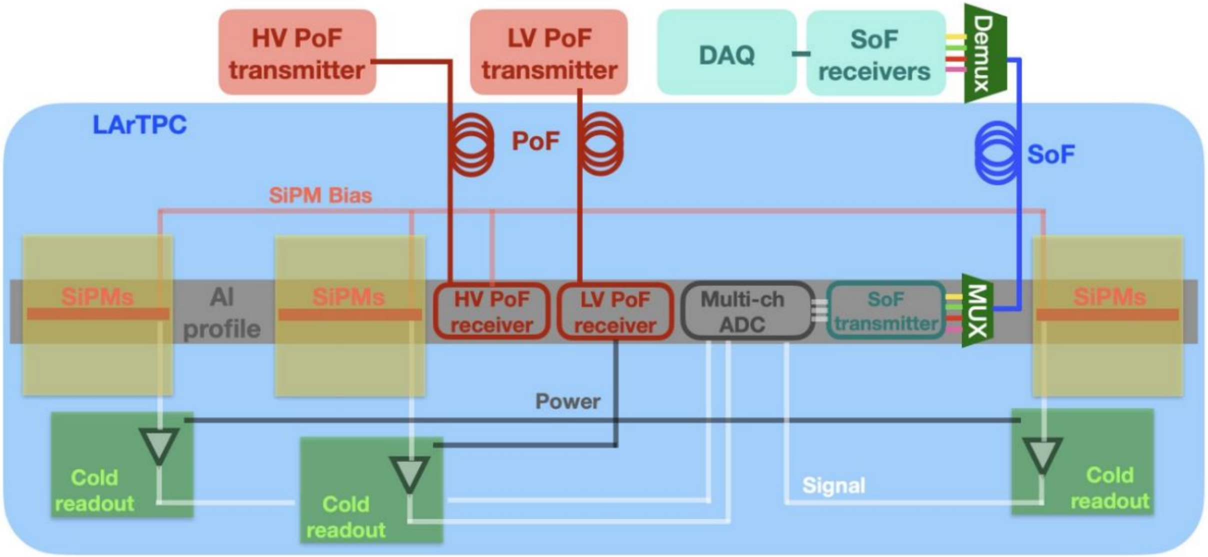
Large Area Photon Detector

Application Specific Si Photon detector

APEX: Aluminum profiles with embedded X-ARAPUCA

- Each row of 6 PD modules in an APEX panel is a electrically isolated system
- 1 PD module/9 profiles
  - 5th profile: mechanical fastening and electrical reference
    - C-shaped profile: Faraday cage shielding for CE readout boards for the 6 module on horizontal row
  - PoF transmitter and SoF receivers (driver and laser diode) to the PDs via fibers



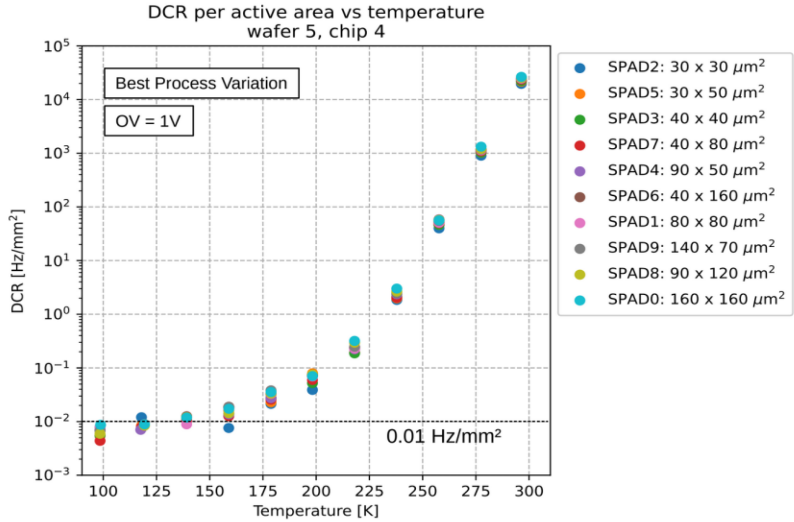


UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

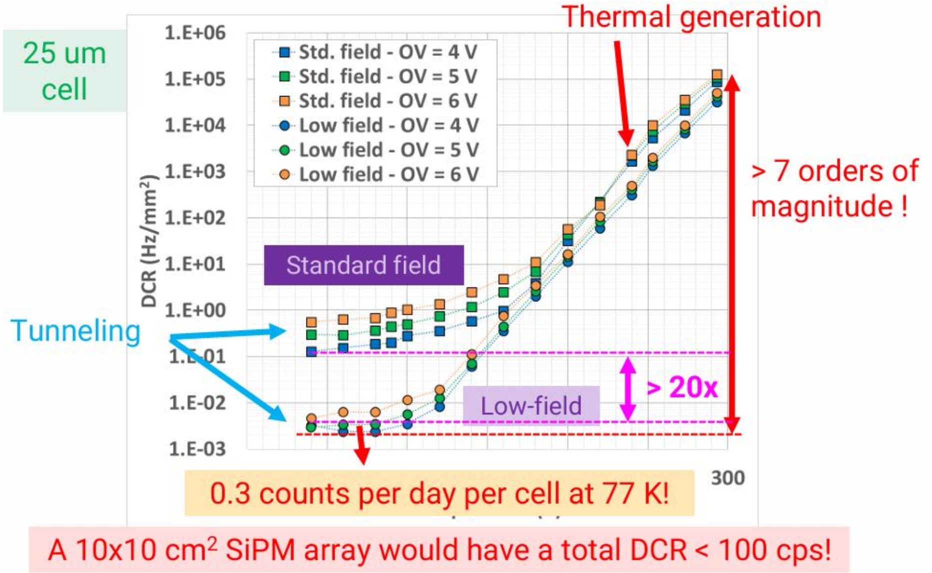
Schaltungstechnik und Simulation

CMOS based SPAD Arrays for light detection in rare event search experiments

LIDINE 2021, 17.09.2021
Michael Keller, Peter Fischer - Heidelberg University

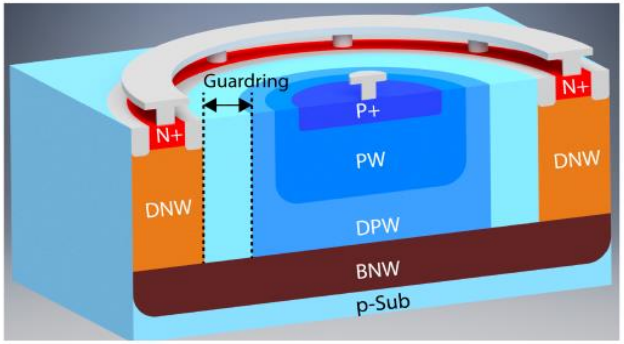


- DCR is <0.01 Hz/mm² @ 100K and 0.02 Hz/mm² @ LXe



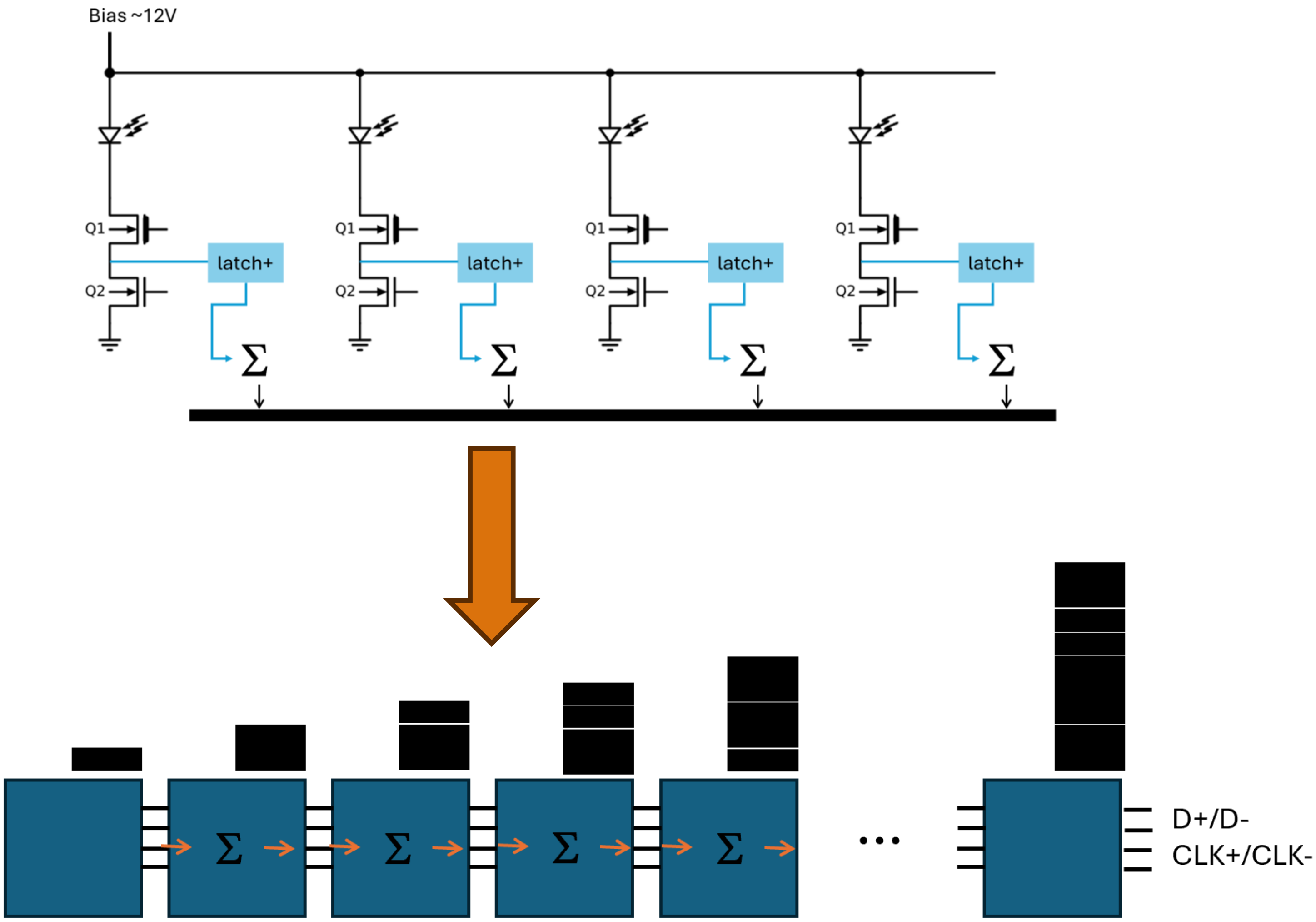
Reduction of Dark Count Rate at cryogenic temperature thanks to electric field engineering in FBK SiPMs.

Showing performance of FBK SiPM for use in DarkSide-20K. Shown by A. Golla, Chief Scientist of FBK at CERN Detector Seminar, April 2023.

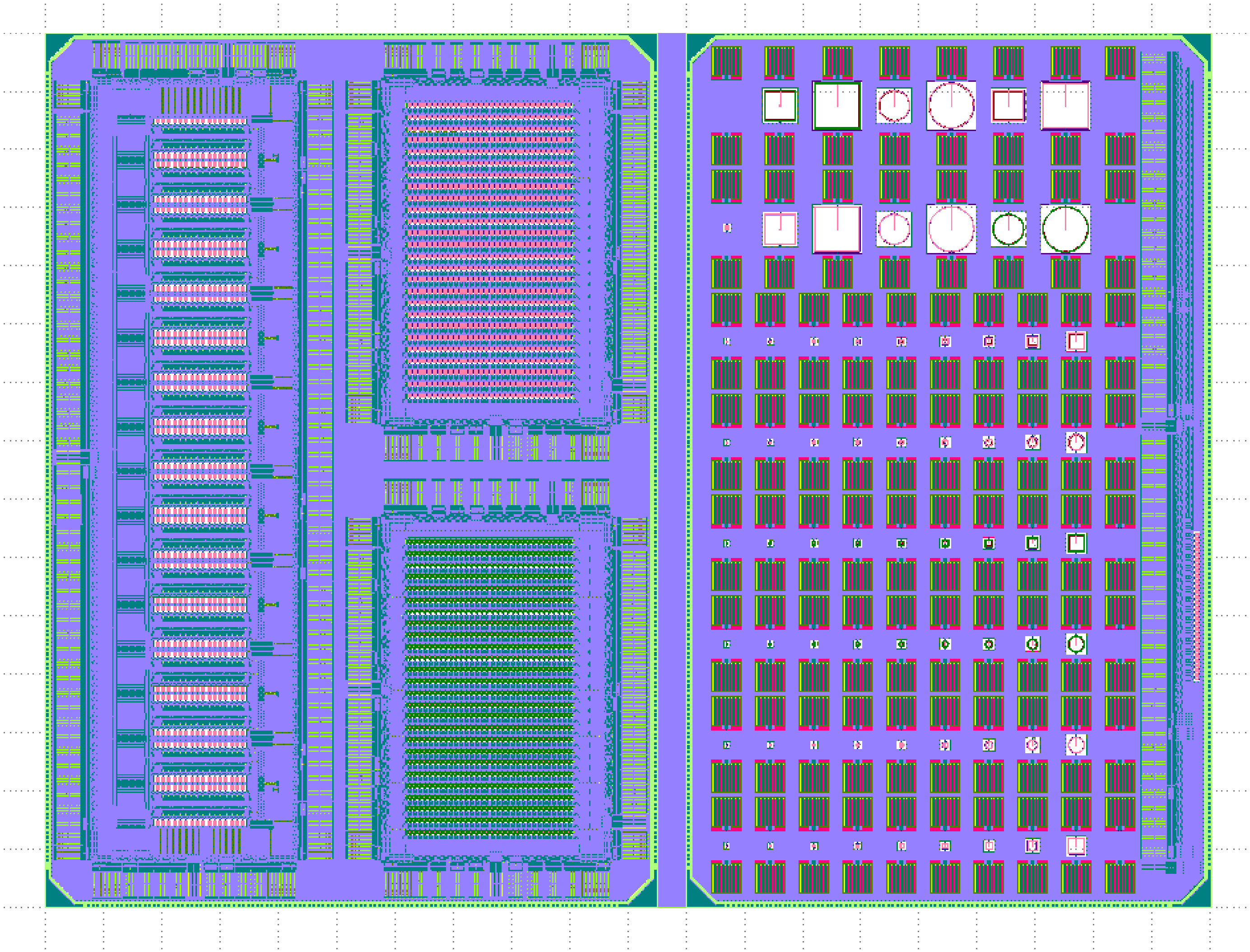


Cross section of a SPAD in the GF55nm process from PhD Thesis of F. Gramuglia (EPFL, 2022).

dSiPM idea: ”photon number digitizer, 1MSPS”



Layout



Conclusions

- Fermilab ASIC group is involved in a wide variety of developments:
  - Targeting cryogenic circuits in 65nm TSMC, 55nm GF, 22nm GF and more (including superconducting devices)
  - Targeting radiation hard circuits in 65nm TSMC, 28nm TSMC

- Our dSiPM effort is just getting started – first submission
  - dSiPM focusing on "photon counting at MSPS rate over large area"
  - Many test structures
  - Focusing on Liquid Noble Gas applications, but not exclusively
  - Focused on reducing dark count rate and afterpulsing
  - Building blocks for a APPLICATION SPECIFIC photon detector