

CAEN 2024 Sales Meeting and Training Week

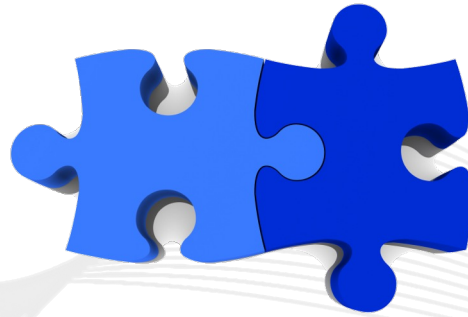


**Innovating Tomorrow:
Breakthroughs and Insights from
CAEN's Research and Development**

Tandem solutions : detector readout chains for every need

WAVEFORM DIGITIZERS

- General Purpose Instrument
- Specialized by FW and SW (high flexibility)
- Digital Pulse Processor
- High Data Throughput
- DPP - Open FPGA
- Need Front-End
- Rack-mount electronics
- Integration with other systems



FERS

- Based on ASIC chips
- Specialized by HW (the ASIC makes the specs)
- Analog Pulse Processor
- Low Data Throughput
- Full readout chain (directly connected to detectors)
- Distributed electronics
- Scalability
- Low cost per channel



FERS: all-in-one readout system based on FE ASICs

- Many research groups and spin-off companies develop **ASICs** for the readout of multi-detector systems in NP and HEP applications. Sometimes, they also develop the electronic boards housing the ASICs.
- The same ASICs may become interesting for other applications, but the electronics and the relevant software must be redesigned and adapted.
- **FERS** (Front End Readout System) aims to implement versatile modules facilitating the integration of ASICs, ensuring their adaptability across diverse applications through comprehensive hardware and software provision.
FERS can be used as a stand-alone evaluation board as well as a highly scalable solution.

Synergies



Off-the-shelf front-end ASIC for scientific instrumentation.

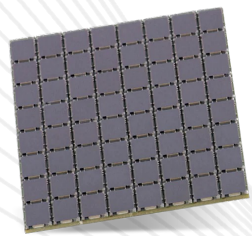


Design of Readout Electronics and Power Supply for NP and HEP



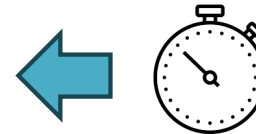
Building electronics around the ASICs

*make the ASICs
ready for the
application!*



Cabling &
Conditioning

Multi-board
Synchronization



Global Timing



Readout
Interfaces



Infrastructure
(power, clock, configuration...)

First born: A5202, 64 channel SiPM readout with Citiroc

HV Bias (on the bottom)

uC

+12V DC-IN

2 In + 2 Out

Eth/USB

TDlink:
Data+Sync

Detector
inputs

FE-ASIC

ADC

FPGA

DETECTOR SPECIFIC FRONT-END

COMMON INFRASTRUCTURE

FERS scalable architecture



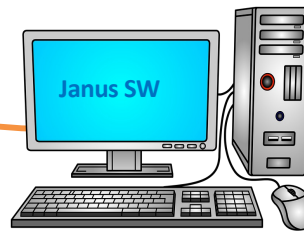
DT5215 Data Concentrator:

- 1 TDlink => up to 16 FERS
- 1 DT5215 => 128 FERS = 8k/16k ch.

Global Time



1/10G Eth
USB 3.0



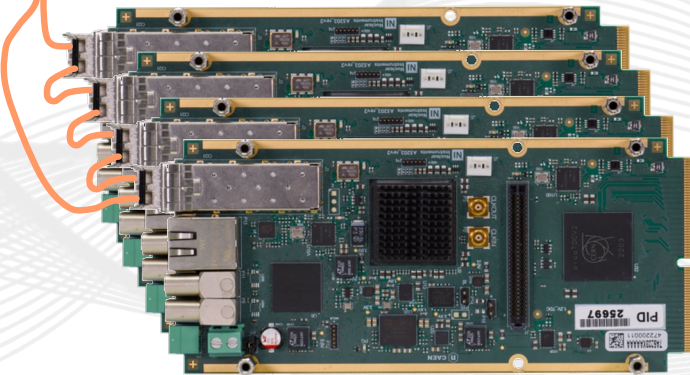
10/100M Eth
USB 2.0



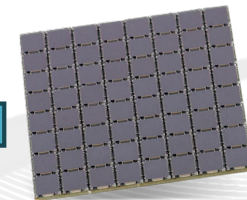
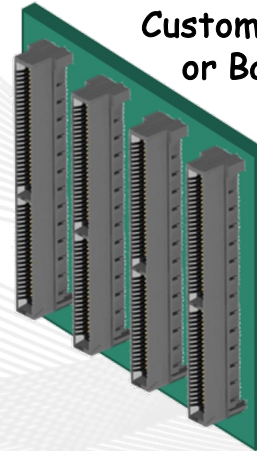
Desktop Evaluation Setup:
Low Cost, Plug & Play

Readout
+
Slow Control
+
Synchronization

3.125 Gb/s TDlink

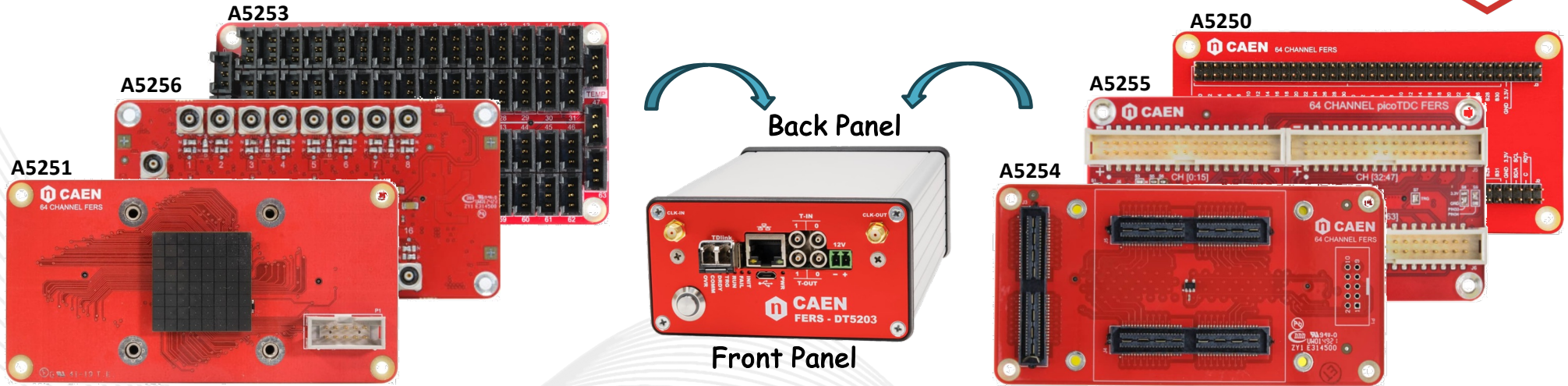


Custom Flange
or Backplane



Easy ASIC integration on FERS

Adapters and Extensions



Back Panel

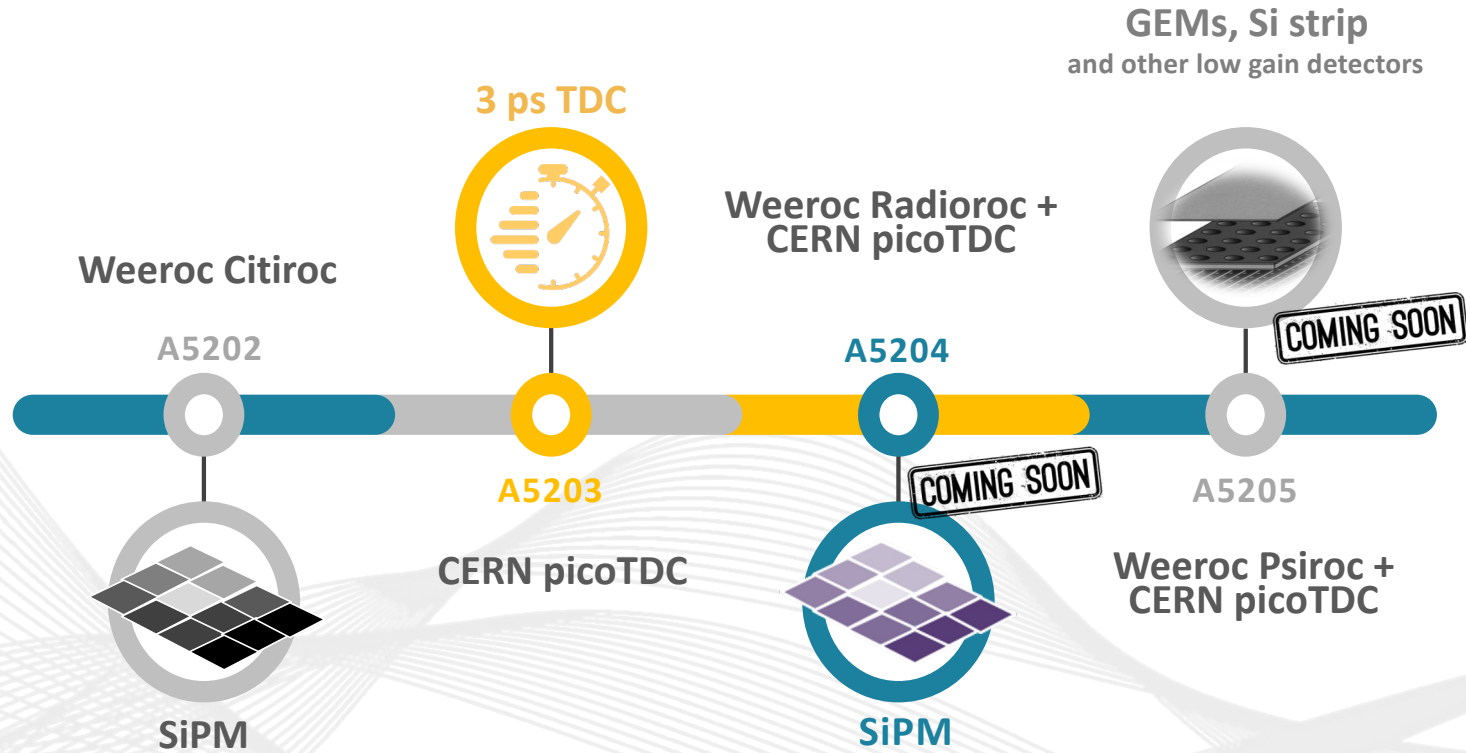
Front Panel

A5260: Remotization cable





FERS Roadmap

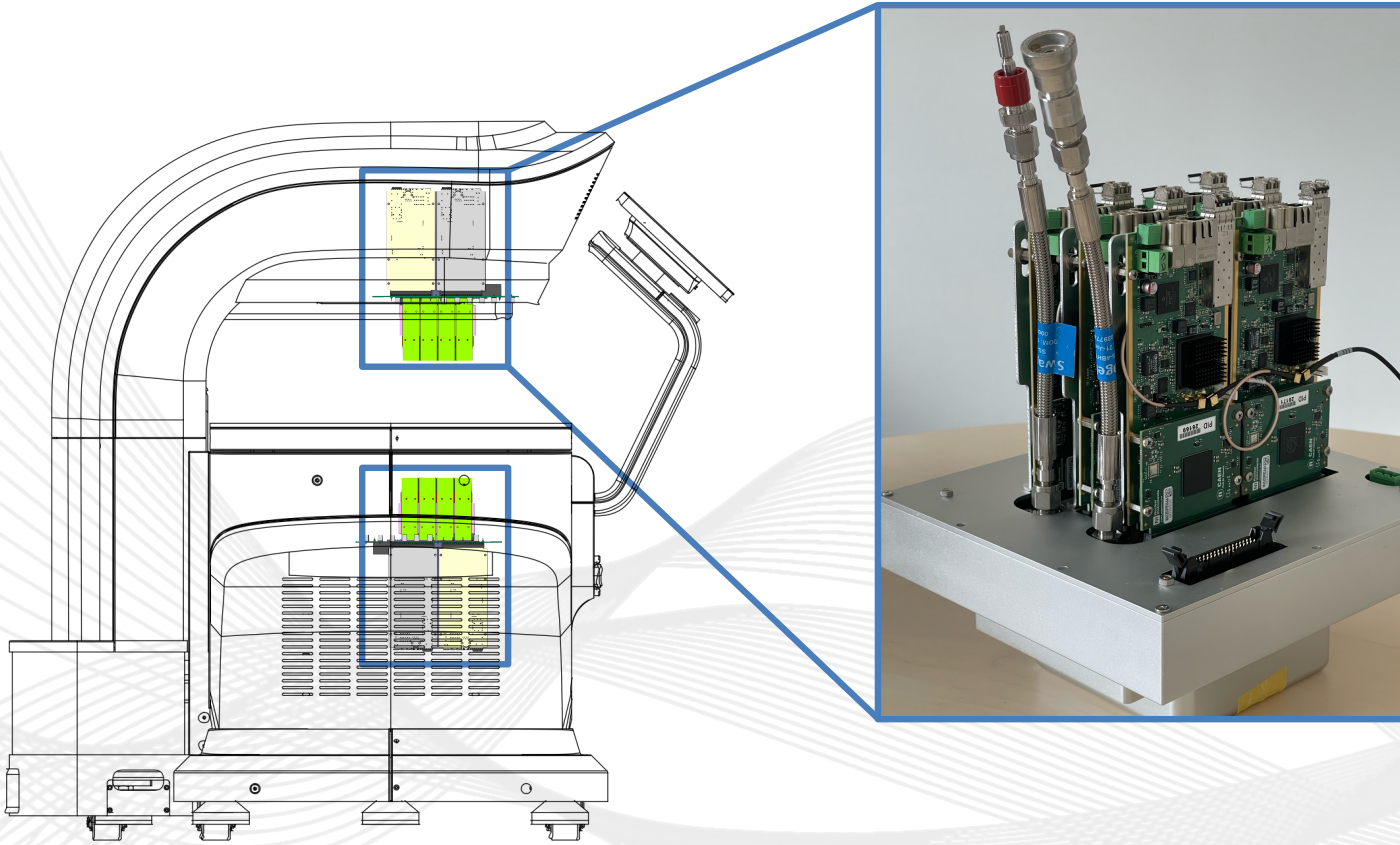




What's next

- **A5204:** 64 channel, **Radoroc + picoTDC** for SiPM readout. Under test right now. First board with new Weeroc package (same footprint for a series of chips)
- **A5205:** 64 channel, **Psiroc + picoTDC**. Designed to read low gain detectors, such as SSD, GEM, pin diodes. Psiroc can be an alternative to the VMM3 ASIC (already used in many applications). Linearized ToT allows for streaming readout (no common trigger, no dead-time) of both time and energy.
- **Poproc:** PMT and Multi-Anode PMT readout (positive and negative inputs). SiPMs have not replaced PMTs yet... there is still a demand for readout electronics.
- **NALU** ASICs for ultra-fast waveform digitizing. Digitizers based on SCA sit in an intermediate region between FERS and the traditional Waveform Digitizer: moderate bandwidth requirement, high channel density, embedded FE, DPP in FPGA, distributed electronics in small cards...
- White Rabbit on DT5215 Data Concentrator: HW should be compliant (to be verified). Need FW/SW development. Not a priority for now... unless there is a specific request.

picoTech ProVision PET scanner

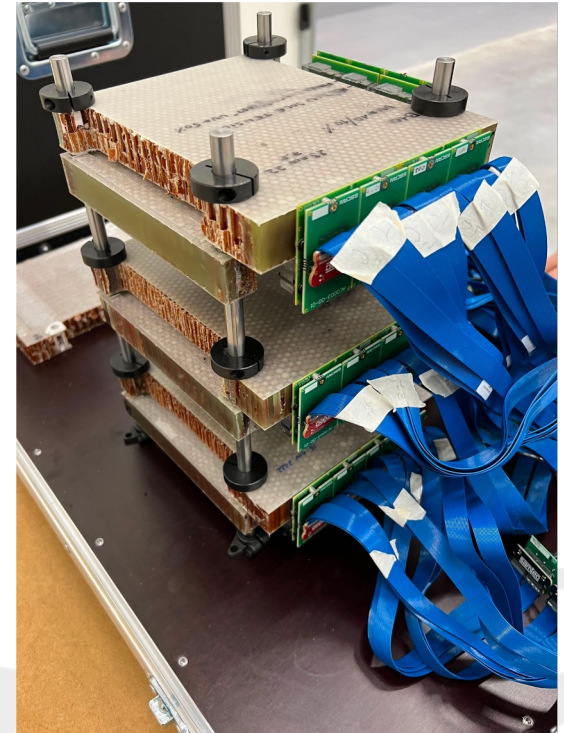
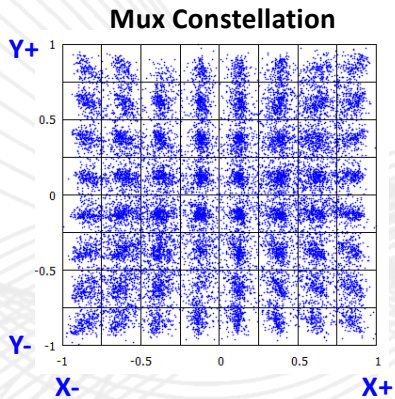


- 2x768 SiPM channels
- 2x6 A5203Bs (128 ch. TDC)
- 1 DT5215 Concentrator
- Precise timing and TOT measurement
- High throughput – almost zero deadtime
- ToT cut for Dark Count and noise suppression

Silent Border

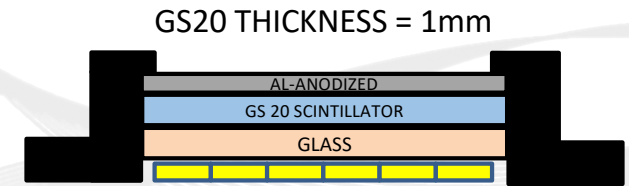
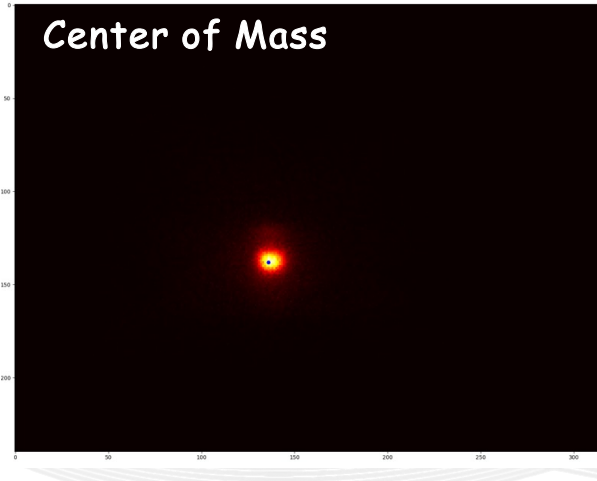
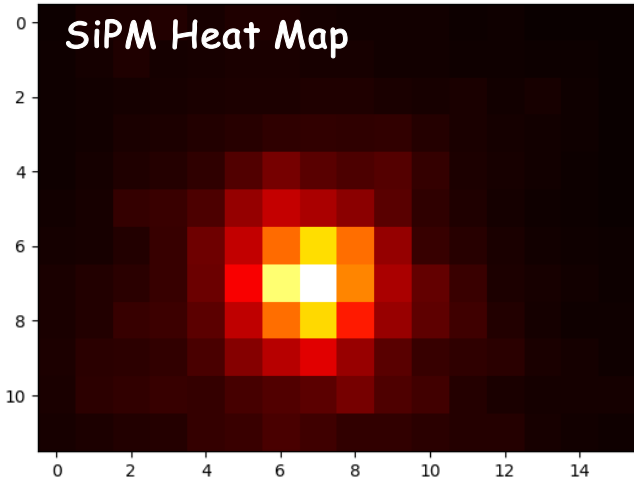
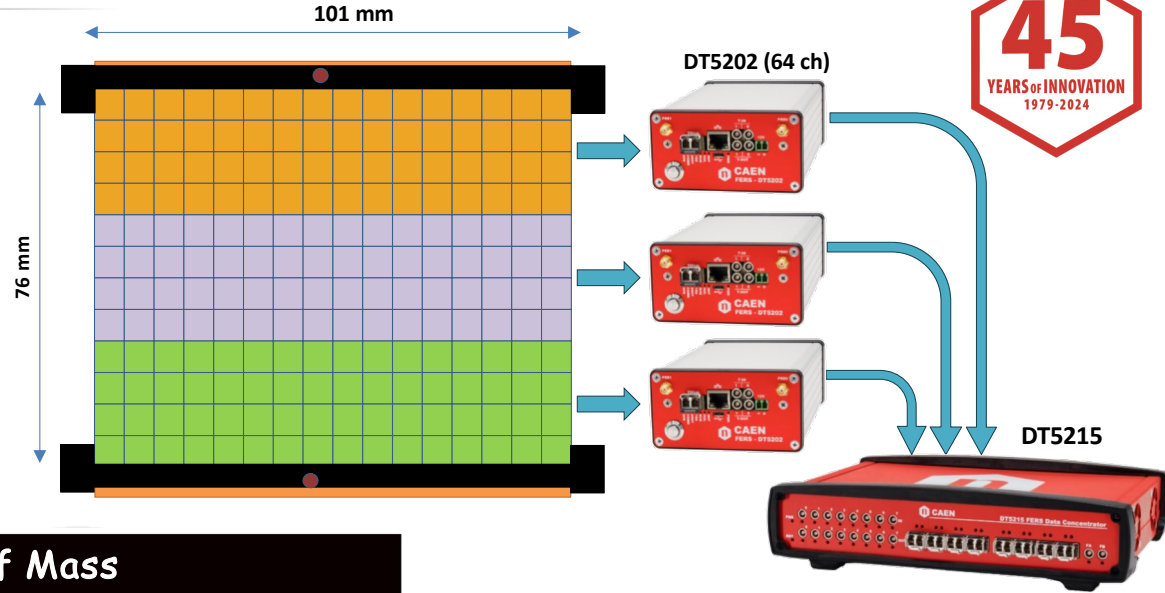
Cosmic Ray Tomograph for identification of hazardous and illegal goods hidden in Trucks and Sea Containers

- 221.184 Fibers + SiPMs
- 1 mux = 64 SiPMs = 4 FERS channels (X+, X-, Y+, Y-)
- 216 A5202 FERS units
- 3 DT5215 (Data Concentrator)



Neutron anger camera

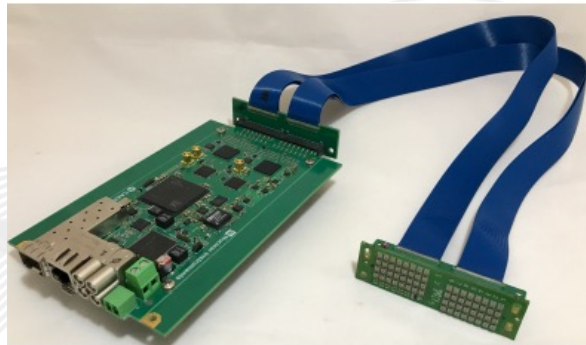
- Based on GS20 scintillators
- 6x6 mm SiPMs, 16x12 array (192 channels)
- 3 DT5203 + 1 DT5215 Concentrator
- Majority trigger implemented in FERS cards
- Gamma discrimination based on Energy Cut
- < 1 mm spatial resolution



IDEA: dual readout calorimeter

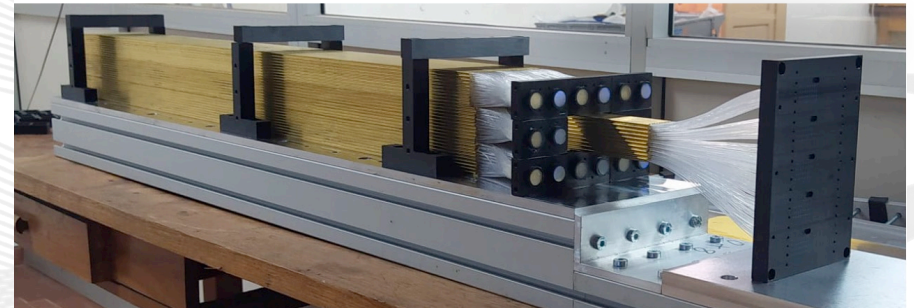
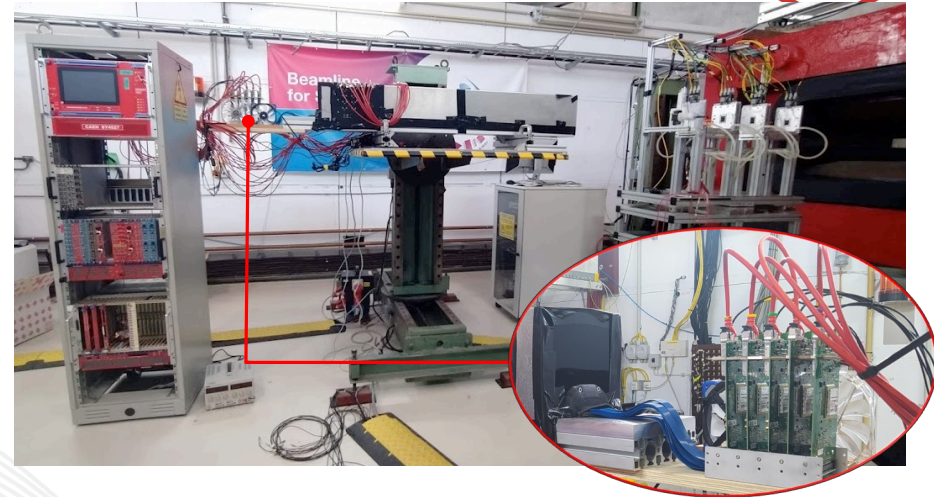
- Development and testing of **dual readout highly granular calorimeter**, exploiting SiPM technology and CAEN A5202 board.
- Successful qualification of a module on beam with EM shower containment @Desy (June 2021) and @CERN (August 2021)
- Plans to **scale-up the system** to handle more SiPMs for hadronic containment

- **320 SiPM = 5 A5202s**
- **No Concentrator**
- **Sync via LEMO cable**
- **Custom SiPM holder with remotization cable**



Courtesy of R. Santoro

<https://indico.ihep.ac.cn/event/14967/contribution/1/material/slides/0.pdf>





Conclusions and thoughts about FERS

- Many applications already done => good feedback so far!
- FERS is well suited for SiPMs with Weeroc chips. Chip footprint compatibility opens great opportunities for developing of a huge family of readout systems, covering SSD, GEM, PMT, Pin diodes and many others
- Resolution of picoTDC is excellent but needs discriminators (A5256: 16+1 ch fast discr => need a 64 ch version). Radioroc/Liroc: suitable FE for picoTDC? VME models to replace V1190/V1290?
- Use of **ToT** for Walk correction (get rid of CFD) and Energy reconstruction. An appealing dead-timeless, self-triggering, low-cost readout system! Difficult to calibrate (signal shape dependent). Work in progress for SAND experiment (5000 fast PMTs).
- Demand for Rad and magnetic field tolerance (to be tested). Cryogenic apps: ASIC on a separate card
- Janus software: open source, already used in many applications. SDK being released soon. Integration in MIDAS at Triumf. Root data converter at INFN-Pi => need our GitHub repository also for FERS!
- Concentrator: DT5215 is often overkilled. A downsized version in A4818 or A5818 would be appreciated.
- What is the boundary between V27xx and A52xx? TDLINK in digitizers? SCA on FERS? Unified Software?