EPF

An Open-Source RISC-V-based GPGPU Accelerator for Machine Learning-based Edge Computing Applications





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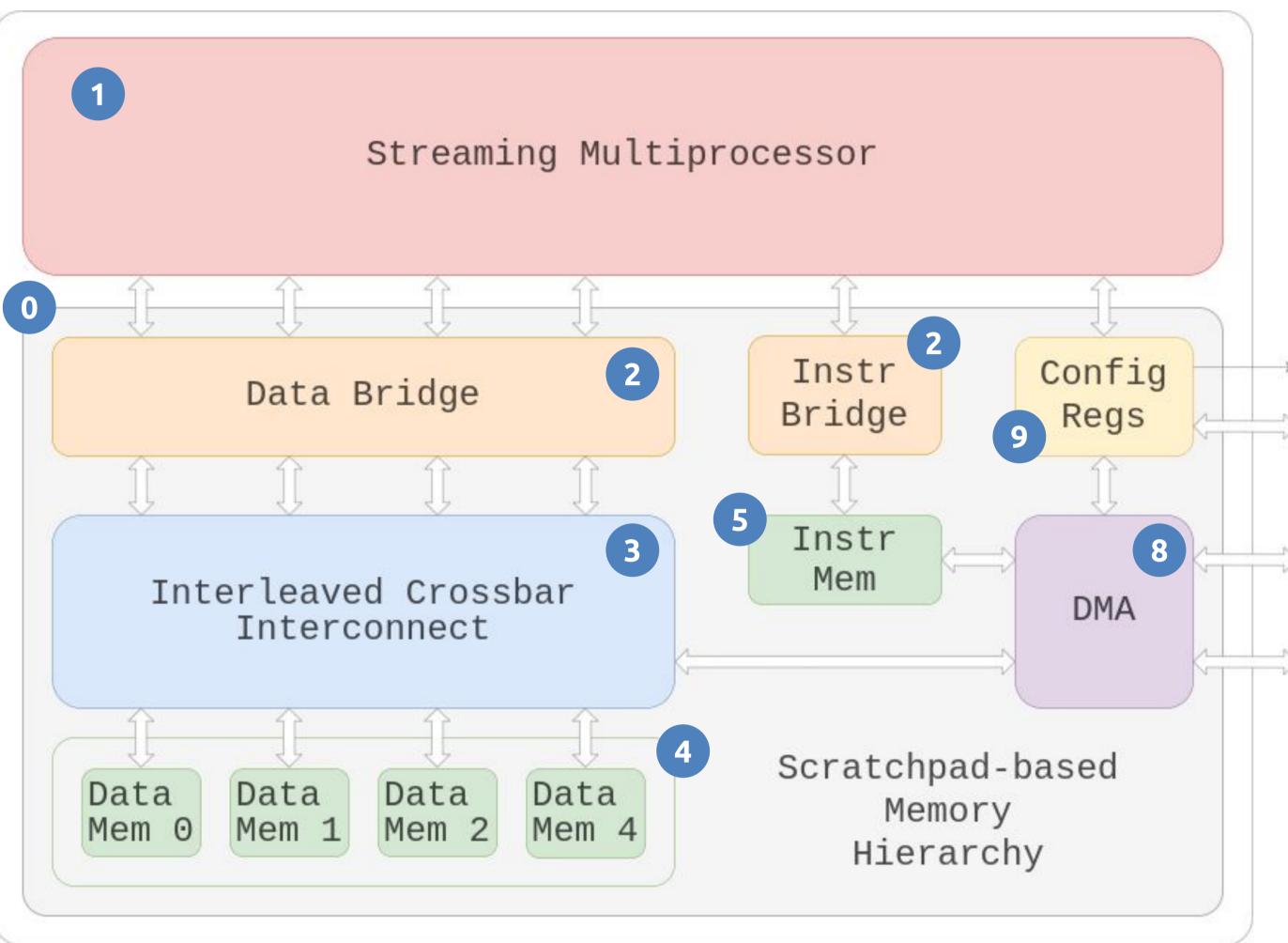


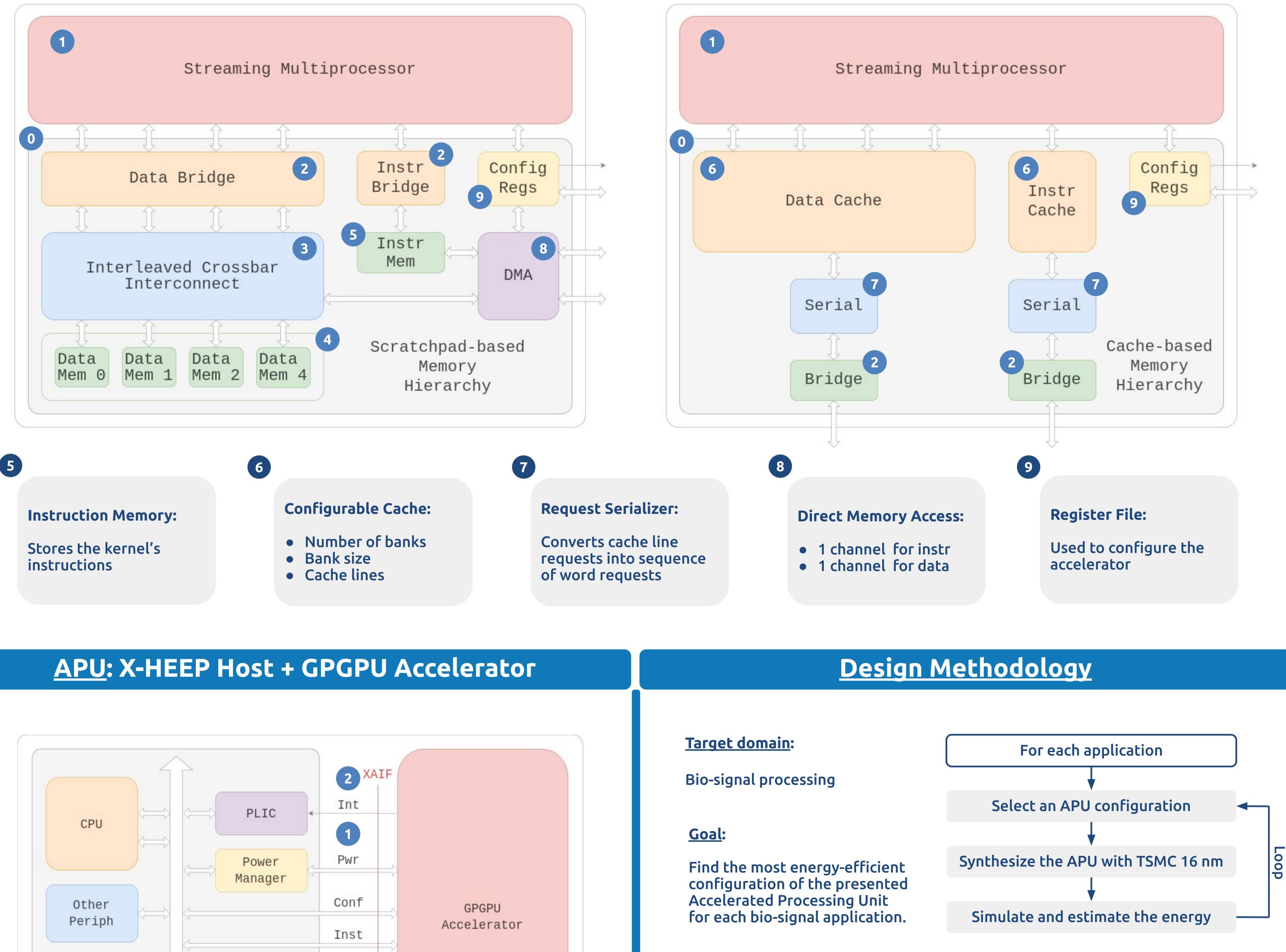
<u>GPGPU Accelerator</u>: Scratchpad-based and Cache-based Architectures

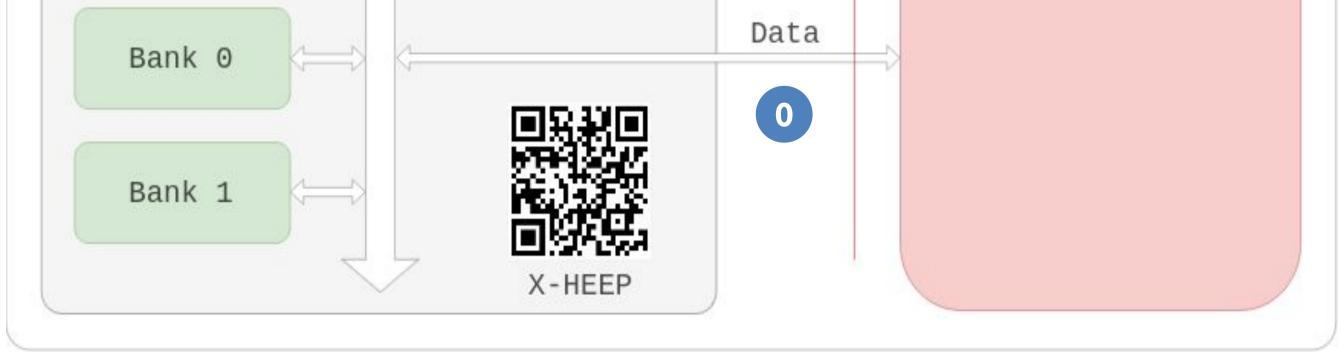
0		1	2	3	4
	figurable Memory archy:	Configurable RISC-V GPGPU Core:	Protocol Bridge: Converts from the	Bus Interconnect: Interleaved fully	Data Memory:
	cratchpad-based ache-based	 Number of threads Number of warps 	MEM to the OBI protocol used by	connected crossbar to enable parallel access to	Stores the kernel's data

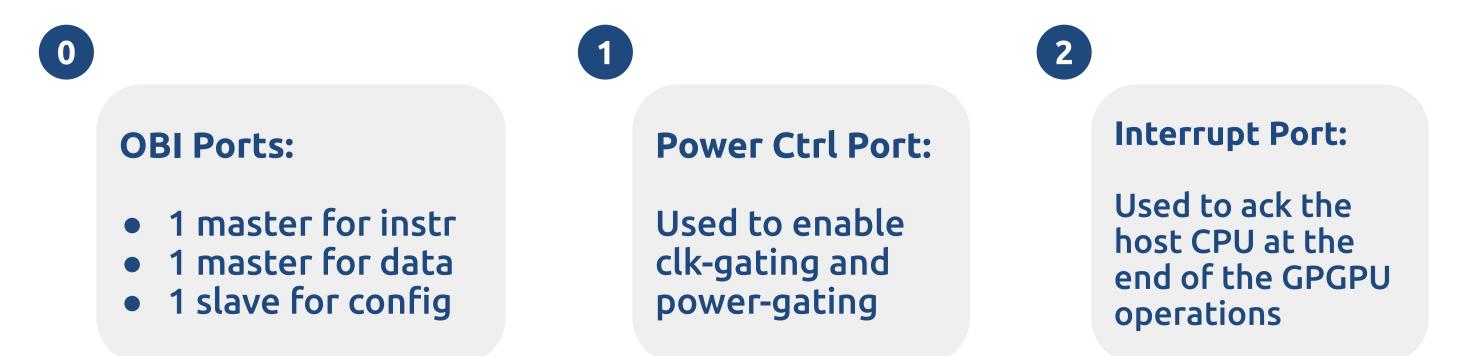
• Floating-point unit

X-HEEP host











- We present the first open-source and configurable GPGPU accelerator specifically designed for ultra-low-power wearable devices.
- We integrate the presented GPGPU accelerator with our in-house-designed X-HEEP host microcontroller to realize an APU for exploring CPU/GPGPU interactions.
- We propose a design methodology to select the most energy-efficient configuration of the presented APU for each bio-signal application.