Enhancing the L0 Muon Trigger: project goals and needs

SMARTHEP Edge Machine Learning school (23-27 Sept 2024, CERN)

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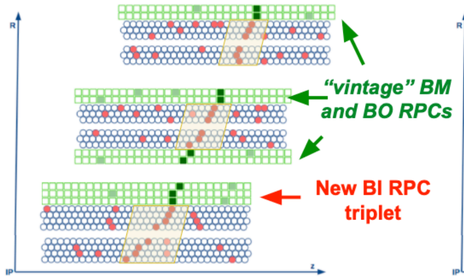
Enhancing the L0 Muon Trigger

L0 MDT trigger: improve the robustness of L0 muon trigger system against the potential loss of performance due to aging RPC detectors and to improve acceptance coverage

Hit Extraction

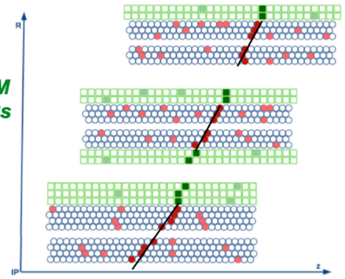
RPCs provide seeds to identify MDT hits from a muon & set up segment fitting step



Pattern recognition algorithms to identify regions of interest with only MDT hits

Segment Fitting

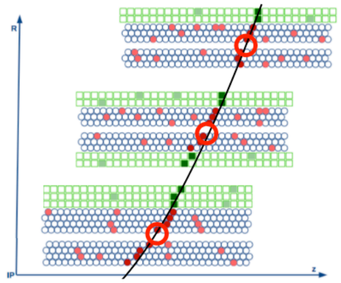
RPCs provide timing to calibrate hits and derive segments



Timing of the muons to determine bunch crossing with Tile or only MDTs

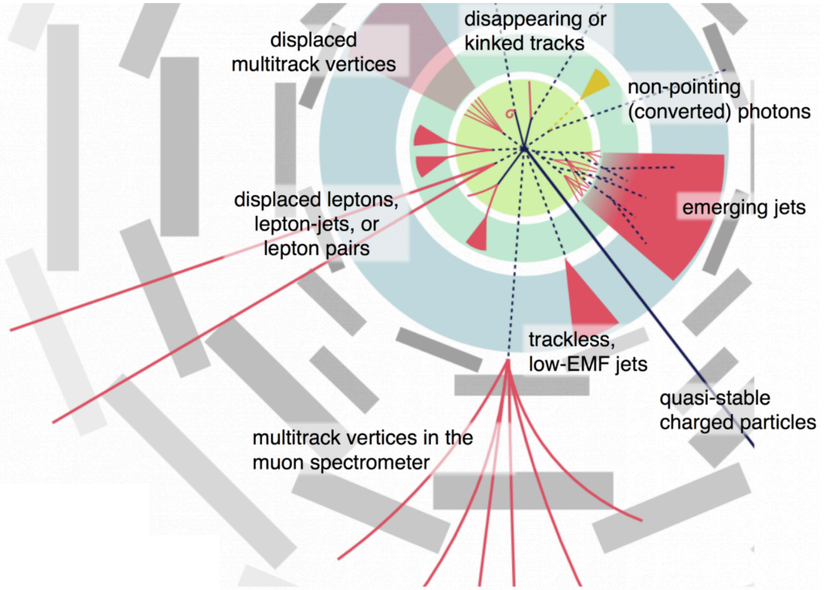
Momentum Estimation

RPCs provide second coordinate for the p_T estimate since the B-field is non-uniform



Momentum estimation without a second coordinate from RPCs

Exotic signatures: additional trigger strategies for non-pointing signatures from decay of long-lived exotic particles



Implement novel trigger strategies in firmware

Starting from displaced muons, but also interested in closeby muons, high multiplicity signatures, slow moving or highly ionizing particles

Plenty of room for innovative ML algorithms!

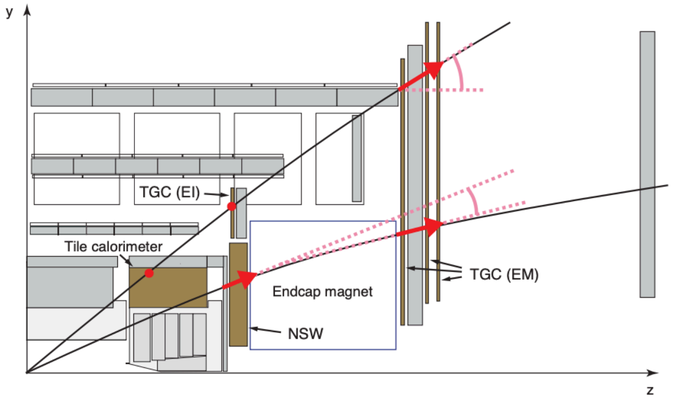
Enhancing the L0 Muon Trigger

Goal is to be forward-thinking and use ML in FPGAs

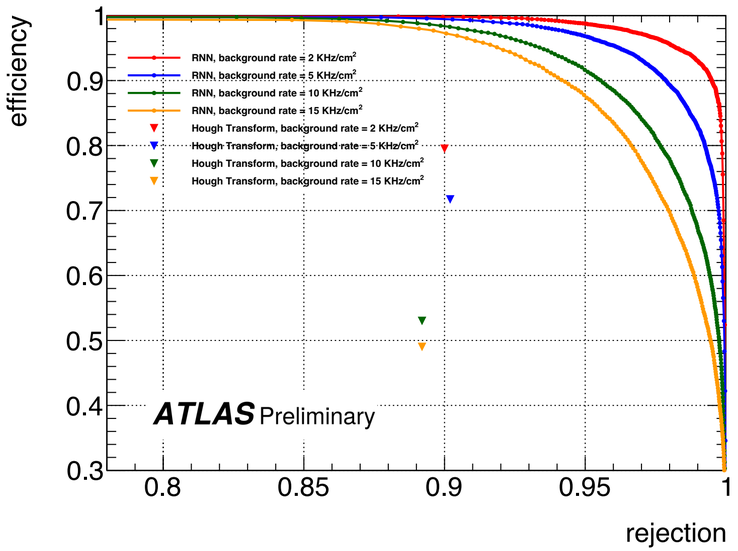
- Study different algorithms/approaches for L0 Muon triggers in case of loss of RPC performance or coverage

Studies on muon detectors toy model simulation for segment reconstruction show promising results

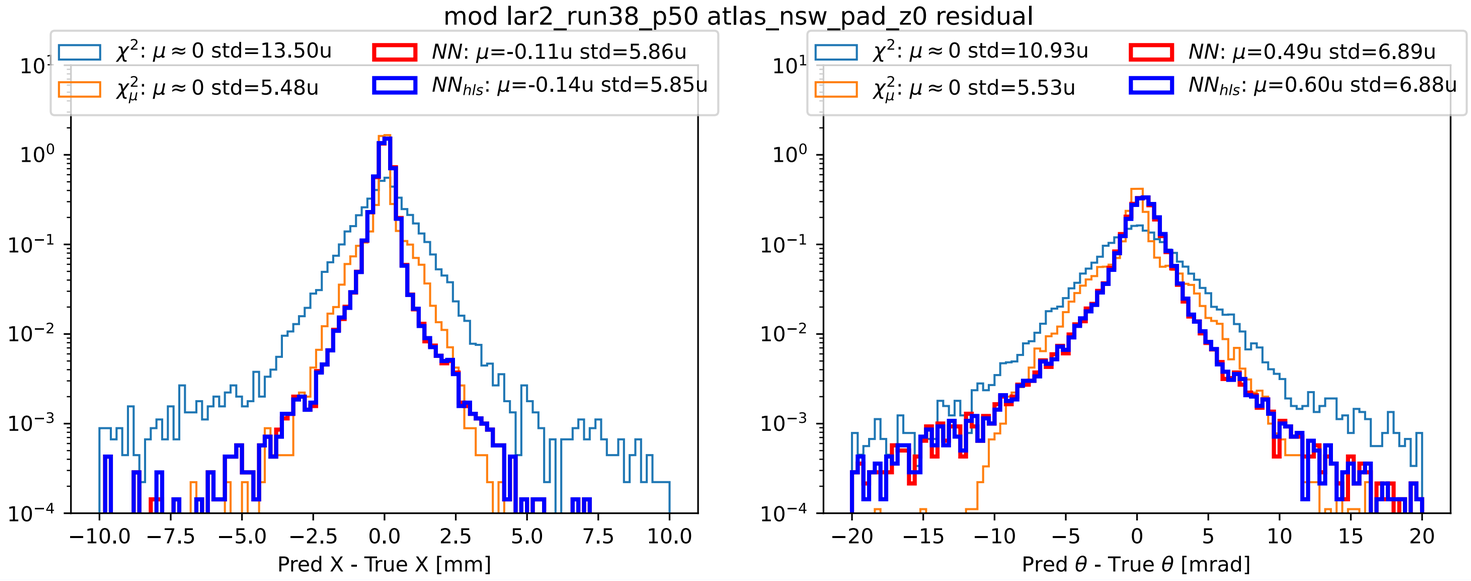
- Starting from toy model simulations based on ATLAS muon subsystem →layers of detectors identifying the crossing position of a passing muon
- For muon p_T we need to measure the particle bending ⟶ must determine both segment position and angle



RNN for track hit identification



CNN for segment position and angle regression



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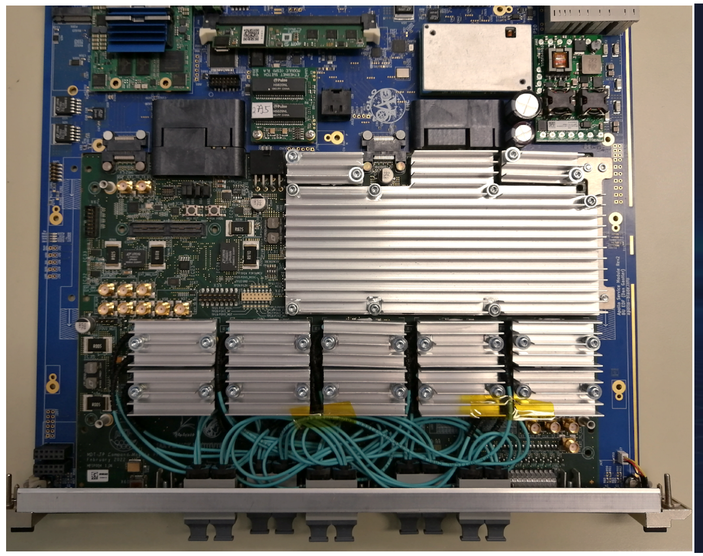
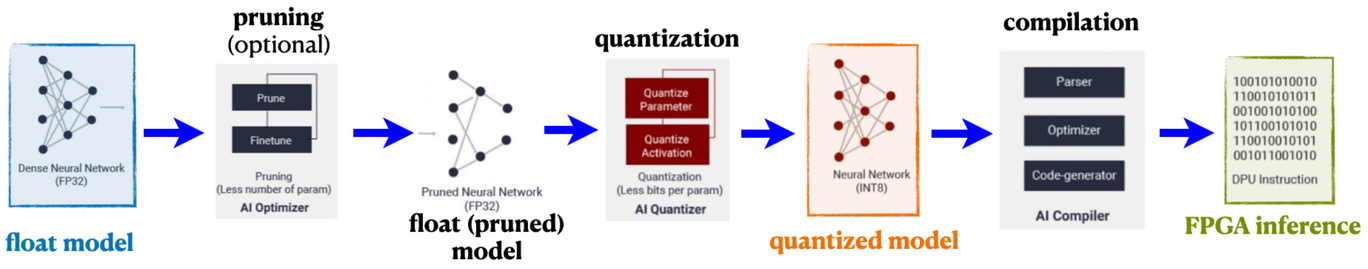


FPGA implementation

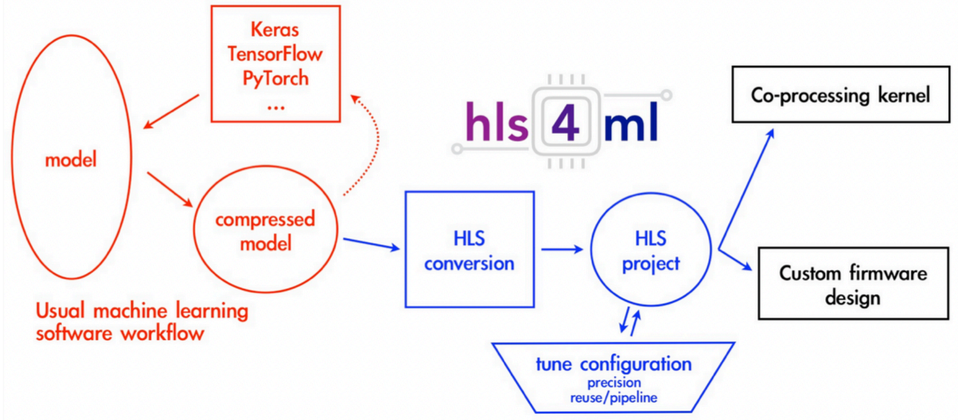
- Can target the current L0 Muon trigger hardware (Xilinx VU13P FPGA) using HLS4ML
- Explore potential improvements using different hardware

Use already existing frameworks developed for ML inference on FPGA such as:

VITIS-AI



HLS4ML



AMD development platform for optimized deployment of deep learning models on FPGA