DRD7 Collaboration Proposal

Electronics and On-Detector Processing

Francois Vasey, CERN

on behalf of the DRD7 Steering Committee*

DRDC Plenary meeting, 3 June 2024

*Jerome Baudot, Marcus French, Ruud Kluit, Angelo Rivetti, Frank Simon, Francois Vasey

Gratefully acknowledging the very significant contribution of Dave Newbold until Sep 2023

CERN

EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS
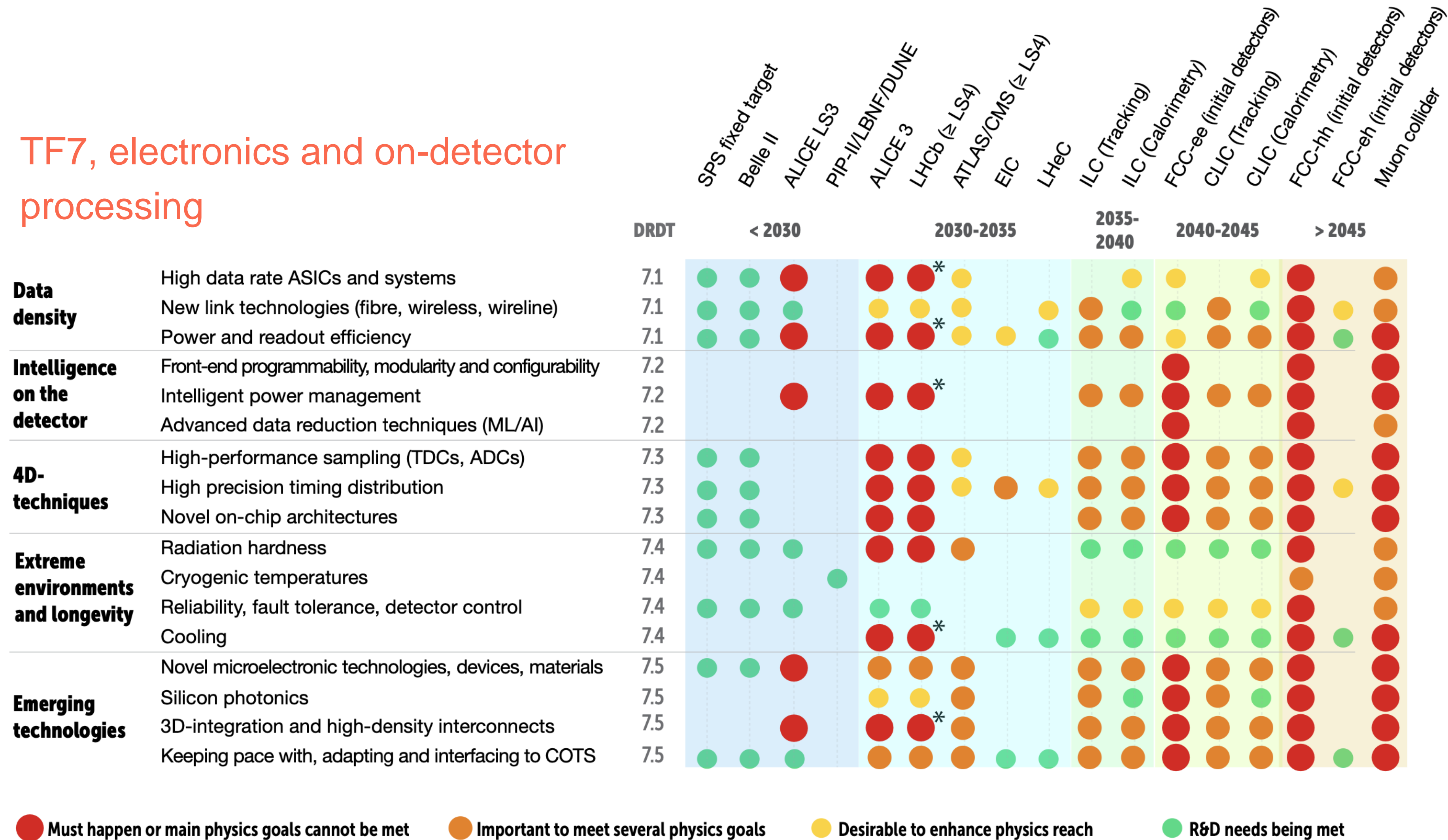
Outline

- Motivation & History

- DRD7 Collaboration Structure

  - Implementing the Structure: Transition out of the Proposal Phase

- Scientific and Technical Goals

- Connections to other DRDs and Summary

Motivation and History

Motivation

Responding to the ECFA Detector R&D Roadmap of TF7

TF7, electronics and on-detector processing

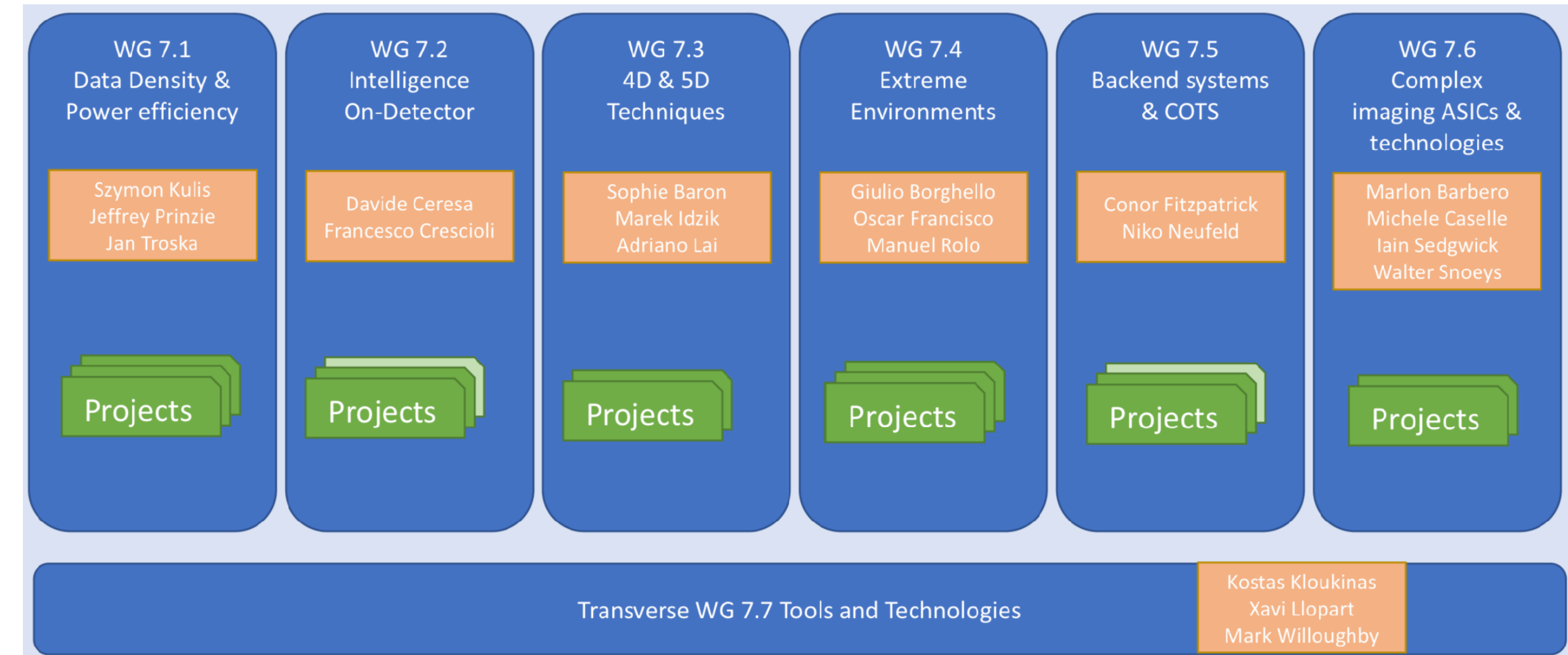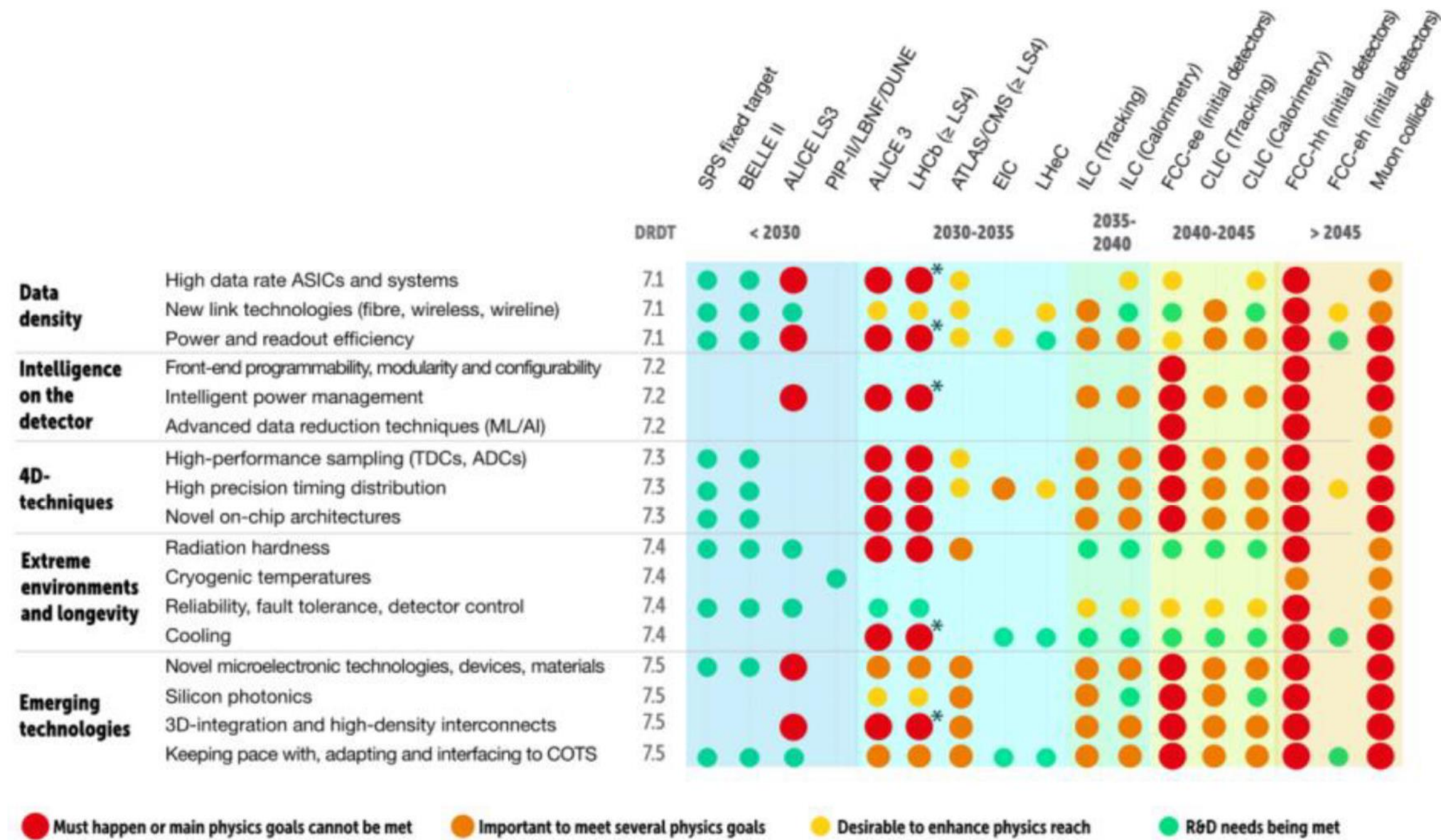|		DRDT	SPS fixed target	Belle II	ALICE LS3	PIP-II/LBNF/DUNE	ALICE 3	LHCb (≥ LS4)	ATLAS/CMS (≥ LS4)	EIC	LHeC	ILC (Tracking)	ILC (Calorimetry)	FCC-ee (initial detectors)	CLIC (Tracking)	CLIC (Calorimetry)	FCC-hh (initial detectors)	FCC-eh (initial detectors)	Muon collider
			< 2030				2030-2035					2035-2040		2040-2045			> 2045		
Data density	High data rate ASICs and systems	7.1	🟢	🟢	🔴		🔴	🔴*	🟡	🟡		🟡	🟡	🟠		🟠	🔴		🟠
	New link technologies (fibre, wireless, wireline)	7.1	🟢	🟢	🟢		🟡	🟡	🟡		🟡	🟠	🟢	🟢	🟠	🟠	🔴	🟡	🟠
	Power and readout efficiency	7.1	🟢	🟢	🔴		🔴	🔴*	🟡		🟢	🟠	🟠	🟠	🟠	🟠	🔴	🟢	🔴
Intelligence on the detector	Front-end programmability, modularity and configurability	7.2												🔴			🔴		🔴
	Intelligent power management	7.2			🔴		🔴	🔴*				🟠	🟠	🔴	🟠	🟠	🔴		🔴
	Advanced data reduction techniques (ML/AI)	7.2												🔴			🔴		🔴
4D-techniques	High-performance sampling (TDCs, ADCs)	7.3	🟢	🟢			🔴	🔴	🟡			🟠	🟠	🔴	🟠	🟠	🔴		🔴
	High precision timing distribution	7.3					🔴	🔴	🟡	🟠	🟡	🟠	🟠	🔴	🟠	🟠	🔴	🟡	🔴
	Novel on-chip architectures	7.3	🟢				🔴	🔴				🟠	🟠	🔴	🟠	🟠	🔴		🔴
Extreme environments and longevity	Radiation hardness	7.4	🟢	🟢		🟢	🔴	🔴	🟠			🟢	🟢	🟢	🟢	🟢	🔴		🟠
	Cryogenic temperatures	7.4				🟢											🔴		🟠
	Reliability, fault tolerance, detector control	7.4	🟢	🟢	🟢		🟢	🟢				🟡	🟡	🟠	🟡	🟡	🔴		🔴
	Cooling	7.4					🔴	🔴*		🟢		🟢		🟢	🟢	🟢	🔴	🟢	🔴
Emerging technologies	Novel microelectronic technologies, devices, materials	7.5	🟢	🟢	🔴		🟠	🟠	🟠			🟠	🟠	🔴	🟠	🟠	🔴		🔴
	Silicon photonics	7.5					🟡	🟡	🟠			🟠	🟢	🔴	🟢	🟢	🔴		🔴
	3D-integration and high-density interconnects	7.5			🔴		🔴	🔴*				🟠	🟠	🔴	🟠	🟠	🔴		🔴
	Keeping pace with, adapting and interfacing to COTS	7.5	🟢	🟢	🟢		🟠	🟠	🟠	🟢		🟠	🟢	🔴	🟠	🟠	🔴	🟢	🔴

- Significant R&D needs in many areas already for near - mid-term projects.

- NB: Phase IIb LS4 upgrades have to reach TDR stage by ~2026

🔴 **Must happen or main physics goals cannot be met**   🟠 **Important to meet several physics goals**   🟡 **Desirable to enhance physics reach**   🟢 **R&D needs being met**
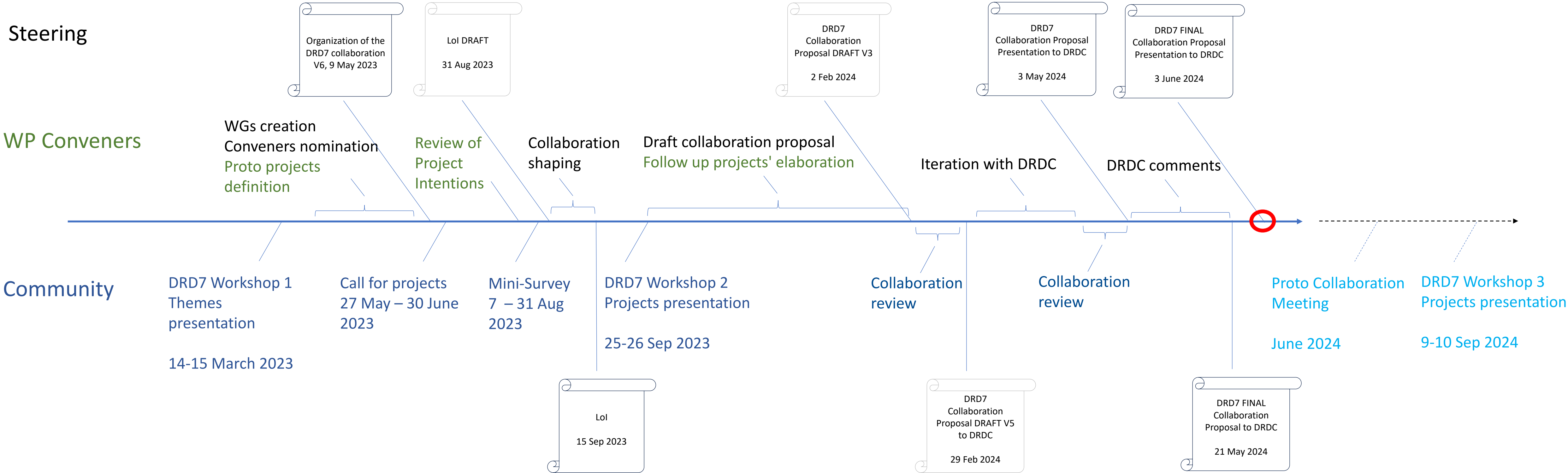
* LHCb Velo

From Roadmap to DRD7

DRDTs to WPs and Projects

- Seen a rich and interesting R&D program that addresses all *Detector R&D Themes* identified in the ECFA Detector R&D Roadmap
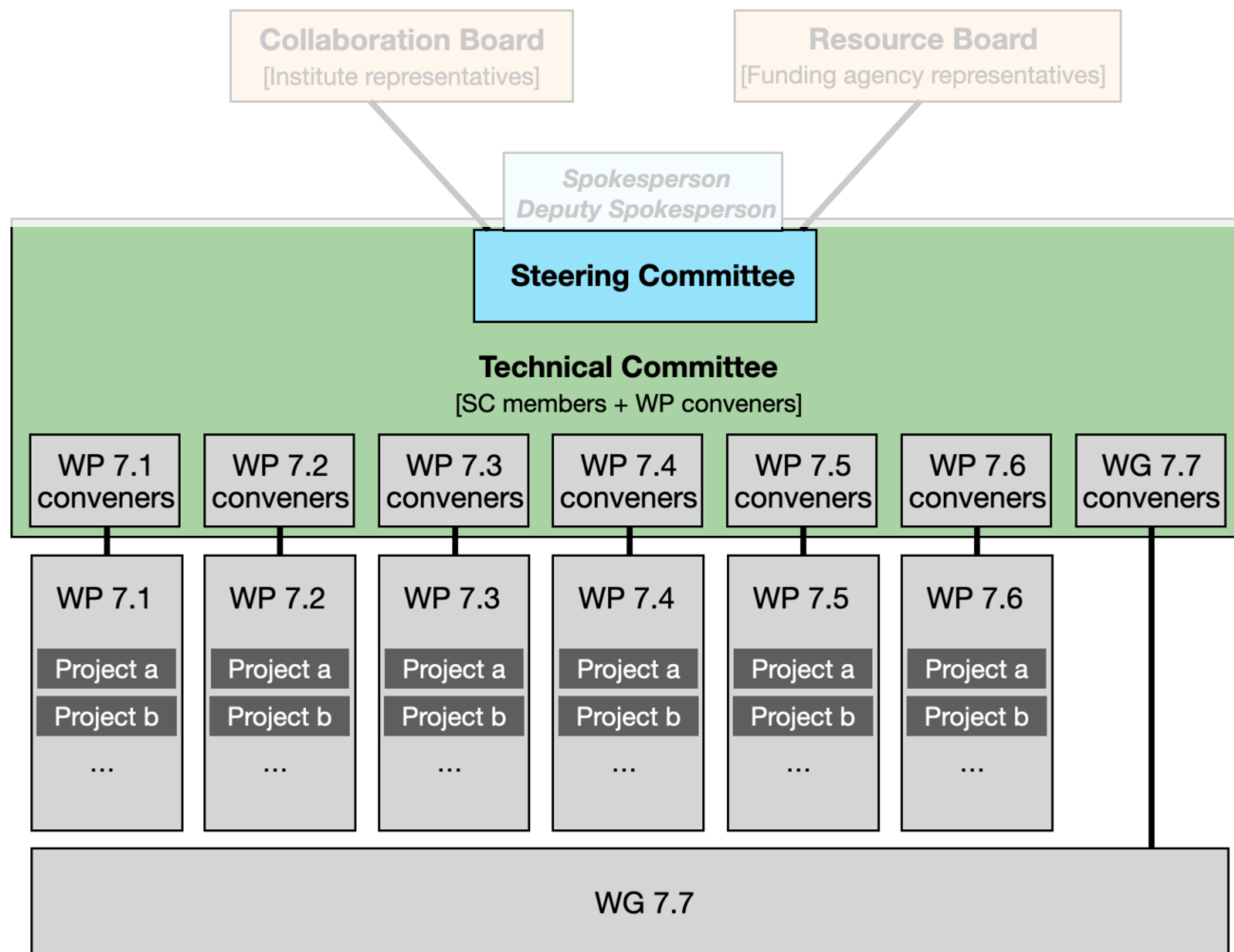
History

Steering

Organization of the
DRD7 collaboration
V6, 9 May 2023

LoI DRAFT

31 Aug 2023

DRD7
Collaboration
Proposal DRAFT V3

2 Feb 2024

DRD7
Collaboration Proposal
Presentation to DRDC

3 May 2024

DRD7 FINAL
Collaboration Proposal
Presentation to DRDC

3 June 2024

WP Conveners

WGs creation
Conveners nomination
Proto projects
definition

Review of
Project
Intentions

Collaboration
shaping

Draft collaboration proposal
Follow up projects' elaboration

Iteration with DRDC

DRDC comments

Community

DRD7 Workshop 1
Themes
presentation

14-15 March 2023

Call for projects
27 May – 30 June
2023

Mini-Survey
7 – 31 Aug
2023

DRD7 Workshop 2
Projects presentation

25-26 Sep 2023

Collaboration
review

Collaboration
review

Proto Collaboration
Meeting

June 2024

DRD7 Workshop 3
Projects presentation

9-10 Sep 2024

LoI

15 Sep 2023

DRD7
Collaboration
Proposal DRAFT V5
to DRDC

29 Feb 2024

DRD7 FINAL
Collaboration
Proposal to DRDC

21 May 2024

DRD7 Structure

The Collaboration Structure

Adapted to the Community

NB: Nomenclature may still to be adjusted to achieve uniformity across DRDs

- R&D in electronics often revolves around major laboratories that can provide a backbone of expertise (in particular engineering) and resources (production, expensive hardware). Reflected in composition of **Steering Committee** as central executive body.

- Research activities defined bottom-up by institutes coming together in **Projects**, grouped thematically in **Work Packages**. WP conveners as coordinators, facilitators of information exchange within WG, within DRD7, and with observing parties from other backgrounds and other DRDs.

The Collaboration Board

Composition of the Collaboration

- One representative per contributing institution

- Chaired by a chairperson, elected from CB members

- Appoints SC members, endorses Spokesperson, Co-Spokesperson and WP/WG Conveners nominated by SC

- 68 institutions from 19 countries (incl. CERN)

  Member institutes are institutes that are active in at least one project
  (e.g. with a concrete FTE commitment)

  11 institutes from non-CERN-member-states (1-CA, 1-JP, 2-KR, 7-US)

  Several additional institutes have shown interest in projects, but have not yet formally joined. These institutes are invited to subscribe to the observers list, and will be informed about events related to the WG subscribed to, and about general DRD7 events.

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	University of Manchester	conor.fitzpatrick@cern.ch
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	Ohio State University	gan.1@osu.edu
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The Steering Committee

The Central Executive Body of DRD7

- Current structure: 6 members. Chaired by two co-chairs elected from within the committee.
- Has evolved out of R&D roadmap TF7 membership by ad-hoc appointments.
  Primary motivation for current composition: Representation of major national communities / centers, diversity of expertise, ensuring continuity with roadmap recommendations.
- After proposal phase: Chaired by Spokesperson and Deputy Spokesperson - nominated from within the committee, endorsed by Collaboration Board. Expect 4 - 8 members of SC.

Current composition:

- Frank Simon [KIT] (co-chair)
- Francois Vasey [CERN] (co-chair)
- Jerome Baudot [IPHC Strasbourg]
- Marcus French [STFC RAL]
- Ruud Kluit [NIKHEF]
- Angelo Rivetti [INFN TO]

Main roles:

- Oversees activities and progress of WPs
- Prepares annual report and workshop
- Nominates Spokesperson, Deputy Spokesperson, WP Conveners

Together with WP Conveners: ***Technical Committee***

- Progress tracking and reviewing of projects
- Proposal of new Projects to Collaboration Board
- Oversight of DRD7 presentations and publications
  (detailed procedures to be worked out)

The Work Packages

Addressing Roadmap DRDTs, hosting Projects

		DRDT
Data density	High data rate ASICs and systems	7.1
	New link technologies (fibre, wireless, wireline)	7.1
	Power and readout efficiency	7.1
Intelligence on the detector	Front-end programmability, modularity and configurability	7.2
	Intelligent power management	7.2 ↻
	Advanced data reduction techniques (ML/AI)	7.2 ↻
4D-techniques	High-performance sampling (TDCs, ADCs)	7.3
	High precision timing distribution	7.3
	Novel on-chip architectures	7.3 ↻
Extreme environments and longevity	Radiation hardness	7.4
	Cryogenic temperatures	7.4
	Reliability, fault tolerance, detector control	7.4 ↻
	Cooling	7.4
Emerging technologies	Novel microelectronic technologies, devices, materials	7.5
	Silicon photonics	7.5
	3D-integration and high-density interconnects	7.5
	Keeping pace with, adapting and interfacing to COTS	7.5

- WP 7.1 - Data Density and Power Efficiency
- WP 7.2 - Intelligence on the Detector
- WP 7.3 - 4D and 5D Techniques
- WP 7.4 - Extreme Environments
- WP 7.5 - Backend Systems and commercial off-the-shelf Components
- WP 7.6 - Complex imaging ASICs and Technologies

↻ topics currently not explicitly addressed by projects

WG 7.7

Tools and Technologies

- With slight remapping of activities to maximize synergies within working groups
- Complex monolithic sensors / ASICs added in area of emerging technologies (overlap with DRD3 resolved)
- Backend systems & COTS as an independent topic
- Transverse WG on Tools and Technologies (WG7.7)

The WP/WG Conveners

Coordinating the Execution of the Scientific Program

- WP 7.1 - Data Density and Power Efficiency
  Szymon Kulis [CERN], Jeffrey Prinzie [KU Leuven], Jan Troska [CERN]

- WP 7.2 - Intelligence on the Detector
  Davide Ceresa [CERN], Francesco Crescioli [LPNHE]

- WP 7.3 - 4D and 5D Techniques
  Sophie Baron [CERN], Marek Idzik [Krakow]

- WP 7.4 - Extreme Environments
  Giulio Borghello [CERN], Manuel Da Rocha Rolo [INFN TO], Oscar Augusto De Aguiar Francisco [Manchester]

- WP 7.5 - Backend Systems and commercial off-the-shelf Components
  Conor Fitzpatrick [Manchester], Niko Neufeld [CERN]

- WP 7.6 - Complex imaging ASICs and Technologies
  Marlon Barbero [CPPM], Michele Caselle [KIT], Ian Sedgwick [STFC RAL], Walter Snoeys [CERN]

- WG 7.7 - Tools and Technologies
  Kostas Kloukinas [CERN], Xavi Llopart Cudie [CERN], Mark Willoughby [STFC RAL]

Ad-hoc appointments, based on expertise, coverage of community, involvement in relevant R&D projects.

Transition out of Proposal Phase

Next Steps after Approval

- Following approval - establish central collaboration bodies:
  - First meeting of the Collaboration Board; election of chair.
  - Call for nominations of Steering Committee members - expect majority of current SC members would be willing to serve for at least one more year.
  - Election of Steering Committee members by Collaboration Board.
  - Steering Committee will propose WG/WP Conveners, to be endorsed by Collaboration Board. Expect that majority of current WG/WP Conveners would be willing to serve for at least one more year. Steering Committee will propose Spokesperson and Deputy Spokesperson for endorsement.
- Expected terms of office:
  - 3 years for SC members, renewable once.
    Desirable to rotate and renew the committee: 2 new members per year.
  - 1 year for Spokesperson and Deputy, renewable.
- Once all collaboration bodies are established and legitimized, the yearly rolling replacement of Steering Committee members (elected by CB) will enter into effect, ensuring both broad community representation and continuity.

Scientific and Technical Goals

WorkPackages & Projects

High-Level Overview

WP7.1	PROJECTS
Data density and power efficiency	7.1a Silicon Photonics transceiver development 7.1b Powering next generation detector systems 7.1c Wireless Data And Power Transmission (WADAPT)
WP7.2	*
Intelligence on the detector	7.2b Radiation tolerant RISC-V SoC 7.2c Virtual electronic system prototyping
WP7.3	
4D and 5D techniques	7.3a High performance TDC and ADC blocks at ultra-low power 7.3b1 Strategies for characterizing and calibrating sources impacting time measurements 7.3b2 Timing distribution techniques

More channels
More bits
Less power

Programmability, modularity, configurability
System-level optimization

High resolution in position, time and energy
System-level optimization

- For each project: Milestones and deliverables defined - currently 2024 - 2026, with perspectives beyond for most projects
- Summary table for each project in the appendix of this presentation

* Project 7.2a (e-FPGA) postponed, pending consolidation of resources

WorkPackages & Projects

High-Level Overview

WP7.4

Extreme environments

7.4a Device modelling and development of cryogenic CMOS PDKs and IP

7.4b Radiation resistance of advanced CMOS nodes

7.4c Cooling and cooling plates *Possible overlap with DRD8 to be clarified*

Harsh environments

Dense heat generation and critical extraction

WP7.5

Backend systems and COTS components

7.5a DAQOverflow

7.5b From FE to BE with 100GbE

DAQ platforms survey and benchmarking

Reference implementations

Simplified backends

WP7.6

Complex imaging ASICs and technologies

7.6a Common access to selected imaging technologies

7.6b Shared access to 3D integration

Collaborative effort on complex technologies

Common access framework

IP blocks

- For each project: Milestones and deliverables defined - currently 2024 - 2026, with perspectives beyond for most projects
- Summary table for each project in the appendix of this presentation

Work Packages - Resource Overview

High-Level Overview

	FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
total 7.1	38,5	35,7	33,8	31,3	17,5	21,8	23,6	15,4	883,0	760,0	460,0	535,0	648,0	928,0	978,0	505,0
total 7.2	9,7	9,2	8,7	8,5	7,2	8,2	8,2	8,2	20,0	50,0	50,0	100,0	5,0	20,0	40,0	20,0
total 7.3	16,2	15,5	13,4	6,6	8,0	11,0	13,6	11,1	682,5	637,5	465,0	10,0	300,0	435,0	590,0	545,0
total 7.4	18,4	14,6	11,7	5,5	6,5	13,5	17,8	15,3	274,0	302,0	60,0	70,0	245,0	461,0	731,0	585,0
total 7.5	10,6	10,3	8,3	1,0	5,3	7,3	8,8	7,5	70,5	65,5	33,0	0,0	133,0	218,0	203,0	80,0
total 7.6	27,0	27,0	27,0	26,5	9,5	9,5	9,5	9,5	454,6	1093,3	623,3	988,3	68,0	68,0	68,0	68,0
Grand Total	**120,4**	**112,3**	**102,9**	**79,4**	**54,0**	**71,3**	**81,5**	**67,0**	**2384,6**	**2908,3**	**1691,3**	**1703,3**	**1399,0**	**2130,0**	**2610,0**	**1803,0**

~335 MY	~200 MY	~7 MCHF	*~6 MCHF*
68 institutes		19 countries	

NB: By construction the plans beyond 2026 are less well defined, with several projects expected to end. Results in reduced resource estimates.

Resource estimates will evolve as results of grant applications become available, and as new projects materialize. Tables will be consolidated by the 3rd DRD7 workshop

Transverse WG 7.7: Tools and Technologies

Enabling ASIC Development in State-of-the-Art Technologies

- Development of ASICs in modern deep submicron technologies is a major endeavour, requiring a wide skillset that many small design groups cannot deliver alone - resource requirements, legal complexity, … Is resulting in increased risk of design failure.

- To respond to these difficulties, a Hub-based structure for ASICs developments in the HEP community is proposed. WG 7.7 will create a task force to develop the implementation of such a structure.

- *Hub concept*: A limited number of regional collaboration and coordination centers (hubs), with CERN as the lead focus. Overall goal:

  - To establish and maintain access, for the DRD community, to state-of-the art microelectronics technologies and EDA software tools

  - To ensure a professional approach to prototyping and production fabrication cycles by delivering best practice in design, verification and foundry submission,

  - To facilitate collaborative work across distributed design teams establishing the necessary infrastructure for IP block sharing, and

  - To ensure that projects follow rigorous project review and submission processes to manage risks and control changes in projects.

Connections to other DRDs, Summary

Connections to other DRDs

- Electronics is of importance in (nearly) all detector R&D projects:
  Development of specific electronics covering direct needs of R&D projects handled in respective DRDs.

- Contacts defined by other DRDs will interface with DRD7 where appropriate:
  - DRD1: Marco Bregant and Sorin Martoiu
  - DRD2: Elena Gramellini
  - DRD3: Jerome Baudot, Eva Vilella
  - DRD4: David Gascon
  - DRD6: Christophe de la Taille
  - Regular meetings with DRD7 Technical Committee may be established if required

- DRD7 will focus on low TRL developments, targeting in priority disruptive, transformative, far-reaching goals.

- Forums in each DRD7 WP will be an opportunity for interested parties in other DRDs to participate and contribute to discussions on important DRD7 topics.

Summary

- DRD7 is projects-based. It puts the technical content at the forefront, and supports it with an as lightweight as possible structure.

- It covers most priorities highlighted by the roadmap, confirming the desire of the collaboration to address in common the strategic challenges in electronics for detectors.

- It creates a transverse WG on tools and technologies, with a mandate to propose an implementation model for a hub-based structure for ASIC developments.

- It is agile, with projects formed bottom up, and a rolling renewal of the governance. Calls for new projects will take place yearly.

- The central Collaboration event is expected to be a yearly DRD7 workshop, which will coincide with the collaboration board meeting. The next DRD7 workshop will take place on 9-10 Sep 2024.

- WPs will organise additional, more focused events, including forums open to observers wishing to be kept informed of progress without committing to collaborate.

- 2024-2026 will be a learning phase, and tuning will take place as/if necessary, as decided by the CB.

Appendix: Project Summaries

7.1a Silicon Photonics Transceiver Development

This project aims to develop high-speed optical transceivers based on Silicon Photonics technology for use in a wide range of future particle physics applications from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors.

Project Name	Silicon Photonics Transceiver Development (WP7.1a)
Project Description	Develop high-speed optical transceivers based on Silicon Photonics technology. Duration 4-5 years.
Innovative/strategic vision	First opportunity to design and operate custom optical data transmission systems in HEP detectors.
Performance Target	100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link operating at a BER of 10^{-12}. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy and power consumption of 250 mW. Cryogenic temperature operation for some lower-speed variants.
Milestones and Deliverables	**M7.1a.1** (M12) Cryogenic test of SiPh PIC **M7.1a.2** (M12) Submission of Ring Modulator Driver **D7.1a.1** (M12) Delivery of WDM test PIC **M7.1a.3** (M24) Radiation test of WDM PIC **D7.1a.2** (M24) Delivery of packaged WDM PIC **M7.1a.4** (M30) Submission of photodiode TIA **M7.1a.5** (M36) System test of WDM PIC with Driver
Multi-disciplinary, cross-WP content	Silicon Photonics combines data-density, timing distribution, Back-end, as well as 2.5/3D integration, with the need for foundry access to specialist processes.
Contributors	CA: Sherbrooke CERN DE: DESY, KIT, Wuppertal ES: IGFAE UK: Birmingham, Imperial IT: INFN Milano, INFN Pisa, Sant'Anna, Uni. Trento US: Argonne, Fermilab
Available resources	25.7 FTE/yr 440k/yr
Addt'l resource need	8 FTE/yr 250k/yr

7.1b Powering Next Generation Detector Systems

This project aims to develop power distribution schemes and their voltage/current regulators and converters for use in a wide range of future particle physics applications, from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors and beyond (future collider experiments)

Project Name	Powering Next Generation Detector Systems (WP7.1b)
Project Description	Develop power distribution schemes and their voltage/current regulators. Duration 4-5 years.
Innovative/strategic vision	Develop very efficient converters (at least 90% at high load, 10A), and at unprecedented radiation hardness up to 1×10^{16} particles/cm^2 and 10 MGy . New technologies as CMOS High voltage 0.18um will be used along with new Gallium Nitride (GaN).
Performance Target	High-efficiency (at least 90% at high load) converters for serial and parallel powering schemes for high voltage conversion and around 75% for fully integrated DCDC in 28nm technology. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy
Milestones and Deliverables, see Appendix B.1.2 for details of activities.	**M7.1b.2** (M12) Test results on first prototypes of a linear regulator and a resonant converter in 28nm technology **M7.1b.1,3,4,5** (M24) Tests on parallel and serial GaN DCDC converter prototypes with custom air core inductors **D7.1b.1,3,4,6** (M36) Delivery of a report on high voltage (48V) DC-DC converter for serial and parallel powering schemes
Multi-disciplinary, cross-WP content	Power distribution scheme combines connection with Back-end power supplies and integration of the on-chip regulation in the front-end ASICs (Pixel, strips and monolithic)
Contributors	AT: TU Graz CERN DE: FH Dortmund, RWTH Aachen University EE: Tallinn University of Technology (TalTech) ES: ITAINNOVA IT: INFN Milan, University of Udine (UNIUD), University of Milan (UNIMI)
Available resources	5.2 FTE/yr 87k/yr
Addt'l resource need	5.4 FTE/yr 101k/yr

7.1c Wireless Data and Power Transmission

This project aims to develop wireless technology based on a millimeter wave (mmw) transceiver IC as well as on Free Space Optics to connect neighboring detector layers, providing increased data rates, high power efficiency and high density of data links, with the aim of reducing mass and power consumption.

Project Name	WADAPT (WP7.1c)
Project Description	Develop millimeter wave Wireless technology together with Free Space Optics technology to connect neighboring detector layers with the aim of reducing mass and power consumption. Wireless power transmission will also be explored.
Innova-tive/strategic vision	First attempt to provide a promising alternative to cables and optical links that would revolutionize the detector design. Removing partly or totally cables would be a major advance in reducing the amount of spurious matter spoiling the measurement of the particle parameters. In addition wireless technology allows efficient partitioning of detectors in topological regions of interest, with the possibility of adding intelligence on the detector to perform four-dimensional reconstruction of the tracks and vertices online.
Performance Target	Radial wireless readout for pixel detectors. Data from detector front-end modules can be serialized as channels up to 10 Gb/s and be aggregated across detector layers (25 to 100 Gb/s). Commercially available technology has demonstrated radiation hardness amply sufficient for envisaged lepton colliders. Radiation hard transceivers will be developed in order to match radiation levels expected at future hadron colliders, maximum fluence at HL-LHC is 2×10^{16} particles/cm^2 and at FCC-hh is 6×10^{16} particles/cm^2.
Milestones and Deliverables	**M7.1c.1,2,3** (M12,24,36) Intermediate annual reports **D7.1c.4** (M24) Delivery of report summarising a proof of principle demonstration of multi-hop RF data transmission using commercial ICs **D7.1c.7** (M24) Delivery of a design of an optimized RF transceiver IC **D7.1c.10** (M36) Delivery of a test report demonstrating FSO data transmission, integration, radiation hardness **M7.1c.4** (M36) Demonstrators made available and training organized.
Multi-disciplinary, cross-WP content	mmw technology and FSO technology will as much as possible aim at developing common tools as common interfaces and common test benches in order to ease performance comparison in a given context and provide the users with adapted solutions. After proof of principle, the ultimate goal would be to generalize the use of wireless data-links to other detectors, with the potential of adding on-detector intelligence. This is however beyond the scope of this 3-years project and further system and implementation analysis will then be required. Some collaborations with group developing radiation hard ICs, 4D and monolothic techniques could be envisaged.
Contributors	FR: CEA-Leti, LPSC IL: Tel-Aviv IT: INFN Pisa, Scuola Superiore Sant'Anna KR: GWNU SE: Uppsala US: Ohio State University
Available resources	5 FTE /yr; 174k /yr
Add. resource need	7.5 FTE /yr; 500k /yr

7.2b Radiation Tolerant RISC-V System-On-Chip

The project aims to develop a radiation-hardened System-On-Chip (SoC) based on the RISC-V ISA standard.

Project Name	Radiation Tolerant RISC-V System-On-Chip (WP7.2b)
Project Description	Develop a radiation-hardened SoC based on the RISC-V ISA standard according to the roadmap defined in M7.2b.1. Topics: 1- SoC architectures 2- Radiation Tolerance design methodology, 3- Verification methodology, 4- SoC generator toolchain. Duration 5-6 years.
Innovative/strategic vision	Develop a technology and a design platform to anticipate and adapt the challenges and opportunities of the future Electronic systems and IC design.
Performance Target	The following targets will be defined in M7.2b.2: Processing Speed Power Consumption Radiation Tolerance Memory and Storage Communication Interfaces Scalability and Flexibility Verification and Testing
Milestones and Deliverables	**M7.2b.1** (M12) Rad-Tol RISC-V SoC roadmap **M7.2b.2** (M24) SoC architectures proposal **D7.2b.3** (M36) Delivery of Rad-Tol SoC building block test chip
Multi-disciplinary, cross-WP content	Electronics Engineering - Digital Design Computer Science - Embedded Systems Systems Engineering - Integration and Testing
Contributors	DE: FH Dortmund BE: KU Leuven CERN UK: UKRI-STFC RAL UK: Royal Holloway University Of London UK: University of Warwick UK: University of Bristol US: Fermilab
Available resources	6.15 FTE/year 40 kEUR/year
Addt'l resource need	7.9 FTE/year 21.7 kEUR/year

7.2c Virtual Electronic System Prototyping

The project aims to develop a simulation of the readout chain of a particle detector at a high level modelling the essential components and processes that occur from the moment particles interact with the detector to the digital readout of the collected data.

Project Name	Virtual Electronic System Prototyping (WP7.2c)
Project Description	Develop frameworks for high-level simulation of particle detectors. **Topics:** **1-** Signal generation in detector elements **2-** Digitization and Signal Processing **3-** Data readout architecture Topics 1. and 3. aim to create independent frameworks that can be used as a single toolchain. Topic 2. will be better defined during the project and might converge in one of the two frameworks or represent a third framework of the chain. Duration 3-4 years.
Innovative/strategic vision	Develop a toolchain for virtual prototyping to: **1-** model detector at high-level **2-** perform architectural studies **3-** provide a reference model for the verification
Performance Target	**Topic 1:** Cluster multiplicity: 1-10 Position resolution: $<10\ \mu m$ Time resolution: 10 ps to 100 ns **Topic 2:** to be defined in M7.2c.2 **Topic 3:** Accuracy: Event/Cycle-level Speed: hundred thousand transactions per second Scalability: readout components library Verification: integrate in verification environment User-Friendly: docs & support for user-only roles
Milestones and Deliverables	**D7.2c.1** (M12) Delivery of a release of the PixESL framework **M7.2c.2** (M12) Target/methodology for Topic 2 **M7.2c.3** (M18) Model Common interface ASIC **D7.2c.4** (M24) Delivery of a release of the detector simulation tool-chain.
Multi-disciplinary, cross-WP content	**Detector Technologies:** support various detector technologies **Particle Physics Models:** integration of comprehensive particle physics models **Geometric Configurations:** ability to define and customize the geometry **Data Formats:** support for common data formats **Monte Carlo Techniques:** implementation of Monte Carlo methods for simulating particle interactions and energy depositions, **Electronics Simulation:** accurate modeling of the readout electronics **Readout Architectures:** support triggered and data-driven systems
Contributors	CERN FR: IPHC Strasbourg *USER:* PSI (CH), UK Cons., INFN Cagliari (IT)
Available resources	3.0 FTE/year 0 kEUR/year
Addt'l resource need	0.0 FTE/year 0 kEUR/year

7.3a High performance TDC and ADC blocks at ultra-low power

This project aims to develop ultra-low power high performance TDC and ADC blocks for use in a wide range of future particle physics experiments.

Project Name	High performance TDC and ADC blocks at ultra-low power (WP7.3a)
Project Description	Development of high performance, ultra-low power TDC and ADC blocks. Duration 3 years. A further extension is planned after 3 years.
Innovative/strategic vision	Develop high-performance, ultra-low power TDC and ADC blocks in advanced CMOS technologies, ready to be deployed as key components of SoC readout ASICs for a variety of future particle detectors.
Performance Target	High resolution ($\sim$ 10ps) TDC and medium-high resolution (10-14 bits) fast sampling (>40 MSps) ADC blocks. High performance, especially ultra-low power consumption, should be confirmed with a very good Figure of Merit, compared to the state-of-the-art solutions obtained using the same CMOS technology and characterized by similar parameters
Milestones and Deliverables	**M7.3a.1** (M12) Report on design of ADCs and related blocks **M7.3a.2** (M12) Report on design of TDCs and related blocks **M7.3a.3** (M24) Progress report on development of ADCs and related blocks **M7.3a.4** (M24) Progress report on development of TDCs and related blocks **D7.3a.1** (M36) Delivery of prototype ASICs of ADCs and related blocks **D7.3a.2** (M36) Delivery of prototype ASICs of TDCs and related blocks.
Multi-disciplinary, cross-WP content	TDCs and ADCs are common blocks of readout ASICs for wide range of detector systems.
Contributors	AT: TU Graz ES: ICCUB FR: CEA IRFU, CPPM, IP2I, OMEGA KR: DGIST PL: AGH US: SLAC
Available resources	7.3 FTE/yr 500k/yr
Addt'l resource need	7.3 FTE/yr 280k/yr

7.3b1 Strategies for characterizing and calibrating sources impacting time measurements

This project aims to study and propose generic data-driven calibration strategies for the time measurements in detectors requiring high precision timing. These include simulation, impact studies and data-based calibration strategies of phase variations in all or part of the detector timing distribution tree (for example jumps due to resets in the electronics system and or temperature dependent phase drift), as well as the calibration of the front-end TDC timewalk and non-linearities.

Project Name	Strategies for characterizing and calibrating sources impacting time measurements (WP7.3b1)
Project Description	Generic data-driven impact studies and calibration strategies of phase variations for timing detectors. Duration 3 years.
Innovative/strategic vision	First opportunity to have a common strategy between the different experiments for data-driven timing studies.
Performance Target	Design of a protocol of measurement. Development of simulation tools in the different experiments. Definition of common figures of merit. Measurement of the properties in test facilities to compare with the predictions. Design of calibration chain inside the different experiments.
Milestones and Deliverables	**D7.3b1.1** (M12) Delivery of a report summarising common metrics and description of the effects for simulation **M7.3b1.1** (M24) Implementation of measurements on realistic DAQ chain **D7.3b1.2** (M36) Delivery of a report summarising the items (hardware or software) to be improved for the next generation of experiments.
Multi-disciplinary, cross-WP content	Concerns all state-of-the-art timing detectors and therefore requires a unified approach which is proposed by this project. Reciprocal reports with DRD7.3a & 7.3b2
Contributors	CERN: ATLAS HGTD, CMS HGCAL FR: Université Clermont Auvergne. CNRS-IN2P3, LPCA (ATLAS HGTD) US: Boston University (CMS ETL)
Available resources	1.5 FTE/yr (ATLAS & CMS core funds) 0 kEUR[1]
Addt'l resource need	0 FTE 0 kEUR[1]

[1] The teams will have full access to simulation processors, detector simulation data & test-benches

7.3b2 Timing Distribution Techniques

This project aims to study and propose strategies to optimize and assess ultimate precision and determinism of timing distribution systems for future detectors. The precision target of upcoming timing detectors is now enforcing new figures of merit to be taken into account in addition to the traditional random jitter, such as clock phase stability and determinism (at picosecond level). Such metrics are systems- and COTS-specific and need to be carefully assessed. In addition, generic solutions shall be provided to mitigate the various kinds of instabilities brought by the selected components. This project will be carried out in tight collaboration with its counterpart project based on simulation (7.3b1): Strategies for characterizing and calibrating sources impacting time measurements.

Project Name	Timing Distribution Techniques (WP7.3b2)
Project Description	Bench-marking of the performance of COTS- or custom-based solutions to assess achievable timing precision and determinism. Investigation of generic solutions to mitigate the observed limitations.
Innovative/strategic vision	Common effort of the community to explore limits of COTS and reach ambitious timing precision not targeted by commercially available solutions
Performance Target	Develop and compare implementations on different COTS and custom platforms. Studies and implementation of FPGA-agnostic or ground-breaking solutions to improve phase stability.
Milestones and Deliverables	**M7.3b2.1** (M12) Specification for a light-weight timing and synchronization protocol also capable of passing fixed latency messages **D7.3b2.2** (M18) Deliver a report comparing the phase determinism of various FPGAs (PolarFire, Agilex, Versal) and potential mitigation mechanisms **D7.3b2.3** (M18) Delivery of first demonstrators of the light-weight protocol, and of a generic deterministic link based on AMD FPGAs and DDMTD + DCPS ASICs from University of Minnesota **M7.3b2.2** (M18) Submission of a unique chip for Phase Monitoring and Phase Shifting (PMPS) **D7.3b2.4** (M24) Delivery of a report on White Rabbit for 4D detectors and for Agilex FPGA **D7.3b2.5** (M36) Delivery of a report summarising a proof of concept demonstration of a FPGA-Agnostic Cascaded Link (FACL) with PMPS ASIC.
Multi-disciplinary, cross-WP content	Distribution is critical and universal to all detectors requiring timing. DRD7.3b1 and 7.3b2 will feed each other with simulation and assessed figures
Contributors	CERN: HPTD team ES: CIEMAT, ITAINNOVA, CSIC (IFCA & IMB-CNM) FR: IN2P3 (CPPM, IJCLab) UK: Bristol University NL: Nikhef USA: The University of Minnesota
Available resources	18.7 FTE over 3 years 310 kEUR over 3 years
Addt'l resource need	10.6 FTE over 3 years 485 kEUR over 3 years

7.4a Device modelling and Development of Cryogenic CMOS PDKs and IP

The project will focus on cryogenic device modelling from selected CMOS technology nodes, the development of "cold" Process Design Kits (PDKs) and mixed-signal CMOS IP blocks and mixed-signal demonstrator chips for cryogenic operation.

Project Name	Device modelling and Development of Cryogenic CMOS PDKs and IP (WP7.4a)
Project Description	Device modelling from selected CMOS technology nodes, development of "cold" Process Design Kits (PDKs), design and characterisation of mixed-signal CMOS IP blocks and demonstrator chips for photon detection in (LAr, LXe) noble liquid experiments, quantum computing interface and sensing.
Innovative/strategic vision	The aggregation of the international research teams will create the critical mass needed for the construction of infrastructures and tools, needed for device characterisation and modelling , towards the development of cold PDKs and cold-IP blocks. These will be made available to a wider community working towards the construction of frontier particle and photon cryogenic detectors.
Performance Target	cold PDK for a deep sub-micron CMOS technology, with temperature corners at 165-87-77-4K, cold IP blocks demonstrated on board of a multi-channel mixed-mode demonstrator chip.
Milestones and Deliverables	**D7.4a.1** (M9) Deliever a specification and requirements document for a full-chip demonstrator. **M7.4a.2** (M18) Cold-PDK for TSMC28nm complete **M7.4a.3** (M26) Tapeout of full-demonstrator chip **D7.4a.4** (M38) Deliver a report of full-demonstrator silicon chip characterisation.
Multi-disciplinary, cross-WP content	The availability of reliable device models and PDKs for advanced CMOS technology nodes, qualified for operation at cryogenic temperatures, will pave the way for the development of cryo-qualified CMOS IP blocks suitable for integration on complex mixed-signal ASICs for DRD2 and DRD5.
Contributors	Graz University of Technology (Austria) University of Sherbrooke (Canada) Forschungszentrum Jülich (Germany) INFN (Italy) KEK (Japan) ICCUB, University of Barcelona (Spain) EPFL (Switzerland) RHUL (UK) University of Oxford (UK) Fermilab (US)
Available resources	5.4 FTE/yr 46k/yr
Addt'l resource need	6.3 FTE/yr 184k/yr

7.4b Radiation Resistance of Advanced CMOS Nodes

This project investigates the radiation response of CMOS technologies from the 28nm node onward for use in the next generations of ASICs for particle detectors.

Project Name	Radiation Resistance of Advanced CMOS Nodes (WP7.4b)
Project Description	This project aims to evaluate the radiation response (total ionizing dose TID, single event effects SEE, and displacement damage DD) of commercial CMOS technologies more advanced than the 65nm node for use in the next generations of ASICs for particle detectors. Duration 4-5 years.
Innovative/strategic vision	Understanding the effects of radiation on CMOS technologies is essential for the design of ASICs used in particle detectors. This project represents a first and crucial step in evaluating the performance of advanced CMOS nodes for the unique environment of particle detectors.
Performance Target	Deepen the knowledge of the radiation response of 40nm and 28nm technologies and begin to study finFETs technologies.
Milestones and Deliverables	**D7.4b.1** (M12) Deliver a 28nm CMOS front-end (FE) circuits for pixel sensors prototype; TID test of IP-blocks in 28nm node **D7.4b.2** (M18) Deliver a chip in 28nm CMOS including matrices of FE channels for readout of pixel sensors **M7.4b.3** (M24) Radiation test of FE structures; Design and testing of rad-hard memory elements in 28nm node **D7.4b.4** (M36) Deliver a prototype in FinFET technology including IP blocks for pixel readout circuits.
Multi-disciplinary, cross-WP content	In order to ensure the success of projects involving ASIC design for particle detectors, it is imperative to consider the radiation resistance of the technologies used. On the other hand, the definition of radiation qualification would greatly benefit from the input of the designer. For example, ASICs developed in WP7.3a must be radiation tolerant and could also serve as valuable test vehicles to evaluate radiation effects.
Contributors	CERN AT: TU Graz IT: INFN Pavia, Uni. Bergamo, Uni. Padova, Uni. Pavia FR: CPPM
Available resources	3.2 FTE/yr 104k/yr
Addt'l resource need	2.4 FTE/yr 105k/yr

7.4c Cooling and cooling plates

This project focuses on the development of the next generation of cooling plates for front-end electronics and sensors based on different materials/techniques. The main goal is to explore manufacturing techniques while improving electronics integration with a cost-effective solution.

Note that depending on the evolution of the forming DRD8 Collaboration, some cooling-related projects may be best integrated in DRD8. This will be fine tuned in due-time to best match the needs of the projects.

Project Name	Cooling and cooling plates (WP7.4c)
Project Description	Development of the general purpose next generation of microchannels cooling structures to deliver excellent cooling performance, minimal material budget, and better electronics integration. Duration about 2+ years.
Innovative/strategic vision	Better integration of electronics features to the cooling plates especially in dense electronics applications. Better scalability considering alternative manufacturing techniques (more cost-effective). Thermal performance numerical simulation tools for new applications.
Performance Target	Different topics will explore different combinations of the following parameters: power dissipation (up to $2W/cm^2$), material budget ($\leq 0.5\%X_0$), integration and/or cost. Different experiments will be able to profit from the portfolio created and optimize those solutions for their final application. The progress will be tracked via public reports in the form of presentations, public notes and/or papers.
Milestones and Deliverables	**D7.4c.3** (M15) Deliver a feasibility public note or paper (topic 3) **M7.4c.6** (M24) 3D printing public note or paper (topic 4) **D7.4c.5** (M27) Deliver a report summarising fluidic and thermal tests of demonstrators public note or paper (topic 1) **M7.4c.7** (M36) Bi-phase CO2 Thermo-fluidic models developed for microchannel, nuclear and annular flows, and thermal heat exchanger characterization and interconnection (topic 2).
Multi-disciplinary, cross-WP content	Communication with DRD8 (Mechanics) and DRD3 (Semiconductor detectors) via liaisons and workshops (e. g.: Forum on tracking mechanics) and 7.6b project (common access 3D and advanced integration) within the DRD7.
Contributors	CA: Sherbrooke CERN DE: DESY ES: IMB-CNM, IFIC-Valencia UK: Manchester FR: CPPM, LAPP, LEGI, LPNHE, LPSC
Available resources	7.7 FTE/yr (First year), 102k/yr (First year)
Addt'l resource need	7.0/yr (Largest, on 2026), 275k/yr (Largest, on 2026)

7.5a DAQOverflow

The DAQOverflow project aims to provide a benchmark of heterogeneous COTs architectures alongside a open-access, repository-hosted infrastructure and set of commonly used tools and algorithms that will keep pace with evolving COTs technologies (GPU, CPU and FPGA coprocessor farms) for the purpose of cost- and performance considered near-detector, near-real-time backend processing for HEP experiments.

Project Name	DAQOverflow (WP7.5a)
Project Description	Benchmarking of heterogeneous COTs architectures and development of TDAQ tools and algorithms distributed via a common repository that are up-to-date with evolving COTs technologies for cost- and performance-considered near-detector/real-time backend processing.
Innovative/strategic vision	Identify experiment-agnostic common TDAQ activities, define generic benchmarks to allow easy comparison of cost/energy efficiency for various compute architectures for the purposes of backend/trigger processing. Make generic algorithms / tools available for various architectures as a repository of 'best practice'.
Performance Target	Cost- and performance-evaluated figures of merit (cost/energy per unit of work), mutil-disciplinary deliverables (kept up-to-date for newer generations of hardware) and distributed reference implementations and examples through a documented common repository of firmware and software. The target after three years is a community-driven, growing project of development with appropriate funding mechanism from the work package and interested users to re-benchmark for new hardwares/technologies when needed.
Milestones and Deliverables	**D7.5a.1** (M9) Delivery of first reference implementations of workflows on simpler platforms **D7.5a.2** (M12) Delivery of a repository and documentation with format agreed upon, reference implementations hosted **D7.5a.3** (M24) Delivery of reference implementations of workflows for a full suite of ASIC/CPU/GPU delivered **D7.5a.4** (M30) Delivery of the benchmarking for full suite, documented and published **D7.5a.5** (M33) Delivery of any followup benchmarks using improved algorithms on existing hardware and first benchmarks on next-gen hardware **D7.5a.6** (M36) Delivery of any comparative performance studies between previous and current generation hardware published.
Multi-disciplinary, cross-WP content	Commodity TDAQ hardware is cross-experiment in nature. The outcomes will be transverse to much of the DRD program for specific DAQ considerations.
Contributors	Instituto de Física Corpuscular (IFIC) Valencia, University College London, University of Birmingham, University of Bristol, Rutherford Appleton Laboratory, University of Geneva, Universidad de Oviedo, University of Manchester
Available resources	∼ 6.5 FTE/yr ∼ 30kEUR/yr
Addt'l resource need	∼ 2.5 FTE/yr ∼ 125kEUR/yr

7.5b From Front-End to Back-End with 100GbE

The perspective of future HEP experiments with lower radiation levels than typically seen at LHC opens the door to increasing the complexity of Front-End electronics, implementing for example RISC-V based processors and SoC in the Front-End. In this context, high throughput 100GbE-based data readout link can reasonably be envisaged. This is a new paradigm which will be investigated in this DRD7.5 Project. It will be tightly linked to other Working Groups like DRD7.2/RISC-V or DRD7.1/links activities.

Project Name	From Front-End to Back-End with 100GbE (WP7.5b)
Project Description	Develop full 100Gb Ethernet-based solutions for Data Readout links from Front-End to DAQ.
Innovative/strategic vision	Lower radiation levels and higher data throughput in future detectors open the door to envisage and investigate 100GbE-based data readout links.
Performance Target	Design and performance comparison between network demonstrators of 100GbE networks based on specific protocol designs, configurations of COTS and potentially customized switches.
Milestones and Deliverables	**M7.5b.1** (M12) Delivery of a report on generic implementation of standard 100GbE on current custom Back-End boards **D7.5b.1** (M12) Delivery of a demonstrator of a FEC-based asymmetric 100GbE link with lpGBT **M7.5b.2** (M18) Specifications for a Macrocell for potential future 100GbEFront-End ASICs **D7.5b.2** (M18) Delivery of smart switch specifications (document) and prototype, including a paper submission and a gitlab repository - Theme 2 **D7.5b.3** (M24) Delivery of demonstrators of a full 100GbE system **D7.5b.4** (M24) Delivery of first prototype test ASIC including protocol IPs and test report. **M7.5b.3** (M36) Full report with conclusion on feasibility of 100GbE-based readout links for Front-End of future detectors
Multi-disciplinary, cross-WP content	Universal across HEP for detectors requiring high/concentrated data readout bandwidth. Tightly linked to other WP like DRD7.2/RISC-V or DRD7.1/links activities
Contributors	CERN FR: CPPM CNRS/IN2P3 NL: Nikhef UK: Bristol University,[1] Imperial College, Rutherford Lab US: Brookhaven National Lab[1]
Available resources	9.7 FTE over 3 years 70k over 3 years
Addt'l resource need	14 FTE over 3 years 185k over 3 years

[1] The participation of this institute in the project depends on the success of the request for funds made at the end of 2023.

7.6a Common Access to Selected Imaging Technologies

This project aims to provide common access to advanced imaging technologies through the organization of common fabrication runs. These are initially envisaged for the TowerJazz 180 nm, TPSCo 65 nm ISC, and the LFoundry 110 nm CMOS imaging technologies. These will be accessible for different clients in the community, among which the other DRDs like DRD3, experiments and projects in HEP. Assembly of the reticle for the different runs is foreseen, as well as design support for the PDK, development of special design rules, TCAD support for sensor optimization and interfacing to the foundry. IP development is also foreseen to accelerate and streamline the design effort. Continuation of this common access beyond the initial three years is expected. Synergy with the 7.6b 3D development will be explored possibly with already existing chips or chiplets. Full 3D-stacked runs, offered in all three technologies, may possibly be pursued later.

Project Name	Common Access to Selected Imaging Technologies (WP7.6a)
Project Description	Provide common access and centralized support for selected CMOS imaging technologies, including specific IP development to accelerate the design effort. Duration 3 years, expected to be extended.
Innovative/strategic vision	Potential of monolithic technologies, confirmed by successful ALICE ITS2 tracker and the widespread community interest. Efficient and affordable technology access requires concentration of the resources in the community.
Performance Target	Organize common runs and efficient and cost-effective access to selected technologies.
Milestones and Deliverables	**TPSCo 65 nm ISC:** **M7.6a.1a** (M12) Completion of IP specifications **M7.6a.2a** (M18) First version of IP complete **D7.6a.1a** (M24) Delivery of a report summarising a foundry submission Q4 2025 **M7.6a.3a** (M36) Documentation of IP for common use **TJ 180 nm (submissions subject to demand):** **M7.6a.1b** (M12) Completion of IP specifications **M7.6a.2b** (M18) First version of IP complete **D7.6a.1b** (M24) Delivery of a report summarising a foundry submission Q4 2025 **M7.6a.3b** (M36) Documentation of IP for common use **LF110 nm:** **D7.6a.1c** (M24) Delivery of a report summarising a foundry submission Q4 2025 **D7.6a.2c** (M36) Delivery of a report summarising a foundry submission Q2 2026
Multi-disciplinary, cross-WP content	Concerns several detectors types, calorimeters, tracking, etc. Serves other DRDs like DRD3 and DRD6, experiments and projects in HEP. Strong connection with 7.6b (e.g. 3D integration of chiplets). Requires expertise in analog and digital IC design, device design and technology, and significant testing effort.
Contributors	CH: CERN FR: IN2P3: CPPM, IPHC, IP2I + others IT: INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI) NL: NIKHEF NO: UiB, UiO and USN UK: STFC US: TBC, SLAC already doing effort
Available resources	TPSCo 65nm 12 FTE/yr 290k/yr TJ 180 nm 1.5 FTE/yr 20k/yr LF 110 nm is 8 FTE/yr 100 k/yr
Addt'l resource need	6.5FTE/yr 410k/yr (TBD)

7.6b Shared Access to 3D Integration

This project aims to develop essential technologies for both 2.5D and 3D integration that can be quickly transposed to wafer-to-wafer 3D integration for a wide range of future particle physics applications, ranging from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors. Synergy with the 7.6a will be explored by employing either already existing chips or dedicated test structures. Furthermore, 3D-integration technologies are evolving quickly in industry. Therefore, exploring concrete connections with industrial partners is a key mission of the project.

Project Name	Shared Access to 3D Integration (WP7.6b)
Project Description	Develop advanced chiplet and 3D integration technologies, including the integration of SiPh chips on detector, by in-house infrastructures and third-party vendors. Initial duration of 3 years with potential for further prolongation beyond.
Innovative/strategic vision	Potential of silicon interposer and chiplet technologies. In-house infrastructure for quick production of prototypes/demonstrators and test vehicles, by employing bump-bonding and detector packaging technologies already available. To establish a concrete connection with the industrial partners.
Performance Target	Shared competences/experiences and infrastructures/processes. Build up and maintain the capability for a quickly transposed to 3D integration. Keeping a cost-effective access to selected technologies.
Milestones and Deliverables	**M7.6b.1** (M18) Establish TSVs process on Si interposer and dummy wafers **M7.6b.2** (M24) Establish RDL process on Si dummy structures **D7.6b.1** (M30) Delivery of report summarasing the integration of SiPh on detector by 2.5D interposer/chiplet technologies **D7.6b.2** (M30) Delivery of a report on W2W bonding by industrial partners **D7.6b.3** (M36) Deliver documentation of the process for the common use.
Multi-disciplinary, cross-WP content	Strong connection with 7.1 for the integration of SiPh chip and optical fiber on detector module. Strong connection with 7.6a (e.g. 3D integration/chiplets).
Contributors	CA: Sherbrooke DE: MPG-HLL, FH Dortm. KIT NO: Norwegian Institutes (Uni. of Bergen (UiB), Uni. of Oslo (UiO), and Uni. of Southeast Norway (USN)) US: Fermilab (TBC)
Available resources	5.5 FTE/yr 390k/yr
Addt'l resource need	3 FTE/yr 68 k/yr

7.7 Tools and technologies

The efficient delivery of the common technical goals in the area of electronics, and the strategic recommendations of the Road-map both demand that the community collectively conform to a portfolio of practices, standards and tools to enable professional and efficient collaboration.

This need is particularly acute for micro-electronics technologies, where the complexity and cost of development are extremely high and continue to increase for every new generation. The issue has been highlighted in recent years where several critical path ASIC developments for experiments have not delivered as expected. This has delayed upgrades and escalated costs with systems often requiring multiple additional foundry cycles. The particle physics community need to address this and ensure as far as is practicable that production ASIC developments deliver solutions that are robust and ready for manufacture whilst also harnessing the full potential of the wider community.

With the current deep submicron technologies, ASIC development is now a major endeavour requiring a wide skillset that many small design groups cannot deliver alone. This has left many projects exposed to greater risk of design failures than in the past. Given the number of projects and the breadth of the R&D programme taking shape under the auspices of the DRD collaborations, taking such a risk in the future is now unaffordable and unacceptable: for new large and complex ASIC developments, smaller groups will need to partner with experienced centres that possess, or have access to, the necessary expertise and tools to ensure successful submissions.

The access to semiconductor technologies that is required for future projects is also subject to strict legal control measures that are rigorously enforced by both the semiconductor manufacturers and the EDA software tool providers in a way that's intended to protect their business interests. These controls, along with strict end-use restrictions, export controls and taxation issues further complicate the situation. While these restrictions have not prevented ASIC design collaborative work and IP sharing with the right agreements in place, the community will benefit from making this process as lightweight and efficient as possible for the future.

In response to the above concerns, and in order to manage ASIC-related design risks in our distributed community, the Steering Committee invites Conveners of WG7.7 to create and steer a task force that will propose an **implementation solution for a Hub-based structure for ASICs developments in the HEP community**.

The Terms Of Reference for the task force will be:

- To establish and maintain access, for the DRD community, to state-of-the art microelectronics technologies and EDA software tools through regional collaboration and coordination (the Hubs)

- To ensure a professional approach to prototyping and production fabrication cycles by delivering best practice in design, verification and foundry submission

- To facilitate collaborative work across distributed design teams establishing the necessary infrastructure for IP block sharing, and

- To ensure that projects follow rigorous project review and submission processes to manage risks and control changes in projects

The ambition will be to be as inclusive as possible, the scope of the EDA tool provision will build on the successful Europractice model. It's extension will be evaluated on a case-by-case basis taking into account existing agreements and other possible restrictions.