STFC Early-Stage research and development scheme: Intention to submit (ItS)

To apply for the STFC Early-stage research and development scheme, all applicants are required to complete the below pro forma and submit it to **KEGroup@stfc.ac.uk**

Please title the email **Early-Stage research and development scheme ItS**

Any applications received which have not submitted this this version of the form will not be accepted.

These ItS will be assessed internally by a sift panel who will determine if the project is eligible for the scheme. They will determine if

- the applicant and lead institution meets the STFC criteria for holding a grant.
- the project TRL is suitable for the scheme
- the project has been developed from STFC science and fits within the STFC remit
- the project is of potential benefit to the PPAN community and/or the wider UK community

Applicant details

Lead applicant name:	Richard Bates
Lead applicant e-mail:	Richard.bates@glasgow.ac.uk
Lead institution:	Glasgow University

If the project is planned as part of a larger collaboration, please state the names and affiliations of all partner organisations	Richard Plackett richard.plackett@physics.ox.ac.uk – Oxford University Mark Williams mark.williams@cern.ch – Edinburgh University Alexander.Oh@manchester.ac.uk Alexander.Oh@manchester.ac.uk – Manchester University Andrew Stephen Chisholm Andrew.Chisholm@cern.ch – Birmingham University Giulio Villani - STFC UKRI giulio.villani@stfc.ac.uk – RAL PPD
Project details	
Please state the proposed title of the project:	Hybrid pixel detectors with Picosecond timing with micrometre position resolution

Please mark with an X the relevant box, stating the remit area you work in

Quantum Science	Particle physics	Astronomy	Particle astrophysics	Solar and planetary science	Nuclear Physics	Accelerator science	Supporting Computing science	Other (please state)
	X							

Please mark with an X the relevant box, stating the remit area the project is looking to target

Quantum Science	Particle physics	Astronomy	Particle astrophysics	Solar and planetary science	Nuclear Physics	Accelerator science	Supporting Computing science	Other (please state)

	X				X			

Please provide a brief (less than 300 words) overview of the project, including high level aims and objectives
Future PP experiments will push the luminosity envelop to extract the maximum useful data. However, track multiplicity increases with luminosity and the ability to unambiguously reconstruct tracks fails. This limitation is overcome by uniquely associating a timestamp to tracks which enables spatially overlapping tracks to be differentiated temporally, known as 4D tracking. 4D tracking requires silicon devices with 10 ps timing resolution simultaneously with single figure micrometre position resolution. Such timing resolutions are obtained by minimising jitter noise via increasing the signal to noise ratio and signal slew rate. This can be realised using a detector with internal gain produced by impact ionisation operated at a bias where the signal to noise ratio is maximal. Low Gain Avalanche Detectors (LGAD) are such a device. The project investigators developed LGADs with mm pitches for the High Granularity timing Detector system with Teledyne e2v and developed LGADs with Micron Semiconductor Ltd targeting a pixel pitch of 50 μm. Both companies produced LGADs with the required gain. However, the work demonstrated small pixel devices are non-trivial due to the device's high-field management architecture resulting in unity gain for pixel pitches smaller than 100 μm. The aim of the project is to develop small pitch pixel LGADs coupled to state-of-the-art pixel chips and tested in CERN beamtests. The project will move the TRL of the small pixel LGAD from TRL3 to TRL6. The aim will be reached by fulfilling these objectives: 1: TCAD design of the devices using process simulation to investigate different designs to manage high field configurations for small pixel pitches 2: Fabrication of the most two positive designs 3: Lab testing diode arrays 4: Assembly of pixel modules: including RAL 28nm CMOS LGAD chip. 5: Lab testing pixel modules 6: Beam testing pixel modules Project aligns with the DRD3 collaboration aims.

Science and Technology Facilities Council

Please provide a brief (less than 300 words) overview of • who the project will benefit • how the project has been developed from STFC science and technology


Science and
Technology
Facilities Council