CMOS Pixel Sensors designed for the ALICE-ITS Upgrade

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  - ⋇ specifications and architecture
  - ⋇ changes w.r.t. STAR-PXL sensor
- *Work plan*
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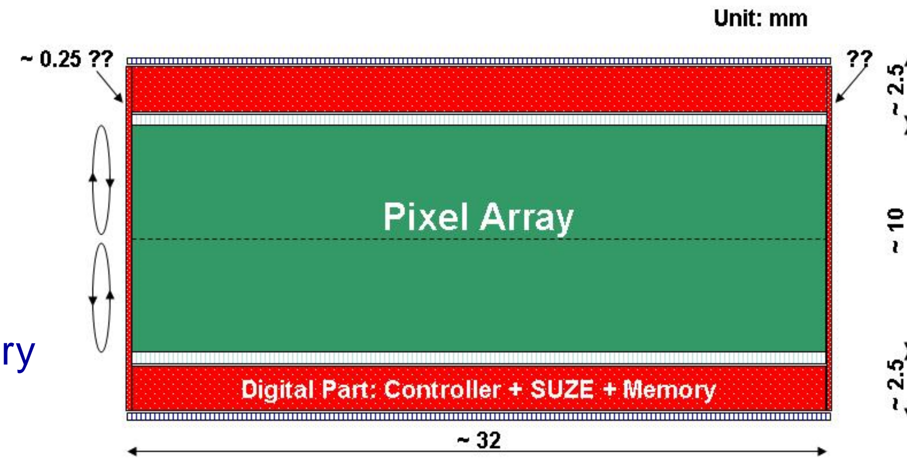
  - ⋇ tentative work plan
- *Ladder concepts*
- *Summary*

MISTRAL : Main Characteristics

- **MISTRAL** $\equiv$ **MI**MOSA **S**ensor for the inner **TR**acker of **AL**ICE

- **Adapted to "standard" running including TPC**

- **Derived from ULTIMATE (STAR - PXL) :**
  - ⋇ in-pixel pre-amp + cDS
  - ⋇ column parallel read-out ($\equiv$ rolling shutter)
  - ⋇ each column ended with discri. $\triangleright$ binary charge encoding
  - ⋇ zero-suppression & output buffers integrated at chip periphery
  - ⋇ JTAG programmable
  - ⋇ thinned to 50 μm

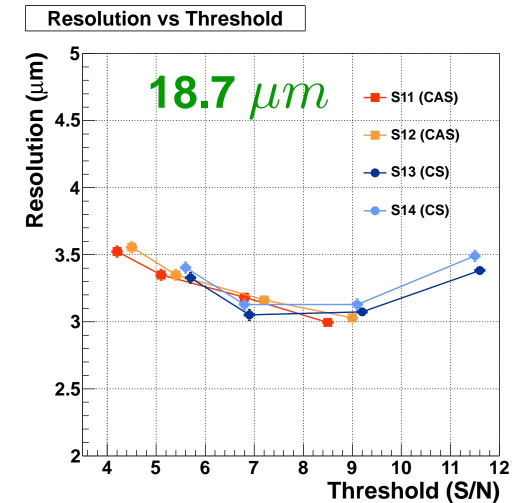


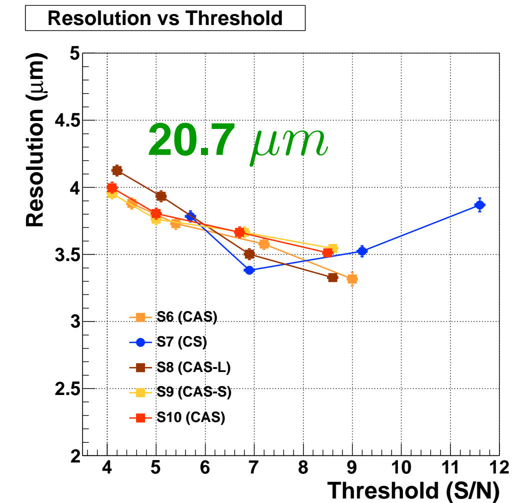
- **Differences w.r.t. ULTIMATE :**
  - ⋇ 0.18 μm triple-well HR-epi techno. (instead of 0.35 μm double-well hR-epi)
  - ⋇ $\sim$ 1$\times$3 cm^2 large sensitive area (instead of 2$\times$2 cm^2)
  - ⋇ double-sided read-out (instead of single-sided)
  - ⋇ 1 or 2 output pairs at $\gtrsim$ 200 MHz (instead of 1 output pair at 160 MHz)
  - ⋇ two $\lesssim$ 200 μm wide raw sequencers (instead of one 350 μm wide sequencer)
    - $\triangleright$ potentially : raw sequencers moved to bottom (requires $\sim$ 6 ML $\Rrightarrow$ longer design)

MISTRAL : M.I.P. Detection Characteristics

- **Detection related characteristics :**

Pixel dimensions	$\sigma_{R\phi,z}$	t_{integ}	P_{diss}
20 $\times$ 20 μm^2	3.5–4 μm	40–50 μs	$\lesssim$ 250(400) mW/cm^2
20 $\times$ 40 μm^2	5–6 μm	20–25 μs	$\lesssim$ 250(400) mW/cm^2
STAR : 20.7 $\times$ 20.7 μm^2	$\sim$ 3.5 μm	$<$ 200 μs	$\lesssim$ 150(200) mW/cm^2





- **Radiation tolerance at +30°C** (not yet established) **:**
  - ⋇ several MRad
  - ⋇ $\gtrsim 2\times10^{13} n_{eq}$/cm^2

MISTRAL : Moving to 0.18 μm CMOS Technology

- **Evolve towards feature size $<<$ 0.35 μm :**
  - ⋇ μ**circuits :** smaller transistors, more Metal Layers, ...
  - ⋇ **sensing :** triple well, depleted sensitive volume, ...
- **Benefits :**
  - ⋇ faster read-out $\Rrightarrow$ improved time resolution
  - ⋇ higher μcircuit density $\Rrightarrow$ higher data reduction capability
  - ⋇ thinner gates, depletion $\Rrightarrow$ improved radiation tolerance
- **Image Sensor process of Tower/Jazz Semi-Conductor :**
  - ⋇ visited on May 16th in Israël
  - ⋇ attractive features of technology (and founder):
    - ◇ optimised sensing systems available and tunable (?) $\Rrightarrow$ enhanced SNR
    - ◇ high-resistivity epitaxy (1 - 5 $k\Omega \cdot cm$) $\Rrightarrow$ enhanced SNR
    - ◇ stitching $\Rrightarrow$ multireticule surface sensor
    - ◇ 6 ML, deep P-well, etc.
    - ◇ $\geq$ 8 Multi-Project-Wafer runs per year $\rightarrowtail$ Shuttle Nr 62 on 24.10.11
- **Synergies :**
  - ⋇ CBM - MVD sensor
  - ⋇ SuperB vertex detector: in-pixel μs time-stamping architecture fits in 50$\times$50 μm^2 pixel

MISTRAL : Chip Submission Plans

- **Chip submission flow :**

  ⋇ Q4/2011 : MIMOSA-32 ▷ prototype for technology exploration

  ⋇ Q2/2012 :

  - ◇ MIMOSA-22THR ▷ prototype with 128 columns (of 128-256 pixels) ended with discriminators
  - ◇ SUZE-02 ▷ prototype with latch-up free zero-suppression μcircuit and output buffers

  ⋇ Q2/2013 : MISTRAL-1 ▷ full size prototype combining MIMOSA-22THR with SUZE-02 designs

  ⋇ Q2/2014 : MISTRAL-2 ▷ final sensor $\equiv$ optimised MISTRAL-1 design

- **Still pending :**

  ⋇ building blocks vs radiation tolerance : do we need ELT, latch-up free design, etc. ?????

  ⋇ optimisation of data transfer μcircuitry ???

  ⋇ integration of trigger ????

MISTRAL : Human Resources

- **Manpower for chip design :**

Chip	Purpose	run type	IPHC FTE	"Missing" FTE
MIMOSA-32	*techno. explor.*	*multi-project*	*2*	$\gtrsim$ *1 ???*
MIMOSA-22THR	*col. // archi.*	*multi-project*	*2-3*	–
SUZE-02	*0-supp. & buffers*	*multi-project*	*0.3*	$\sim$ *2-3 ???*
MISTRAL-1	*techno. explor.*	*engineering*	*3-4*	$\gtrsim$ *0.5 ???*
MISTRAL-2	*design optimis.*	*engineering*	*3-4*	$\gtrsim$ *0.5 ???*

- **Manpower for sensor tests :**
  - ⋇ functionnality tests : designers
  - ⋇ particle detection characterisation in lab and at CERN : $\gtrsim$ 1-2 FTEs missing
  - ⋇ radiation tolerance tests : $\sim$ 2 FTEs welcome
- **Manpower for chip steering and DAQ :** Missing
- **Synergies :**
  - ⋇ building blocks : SuperB
  - ⋇ techno. properties (e.g. radiation tolerance, charge collection) : SuperB, CBM, etc.

Besides/Beyond MISTRAL

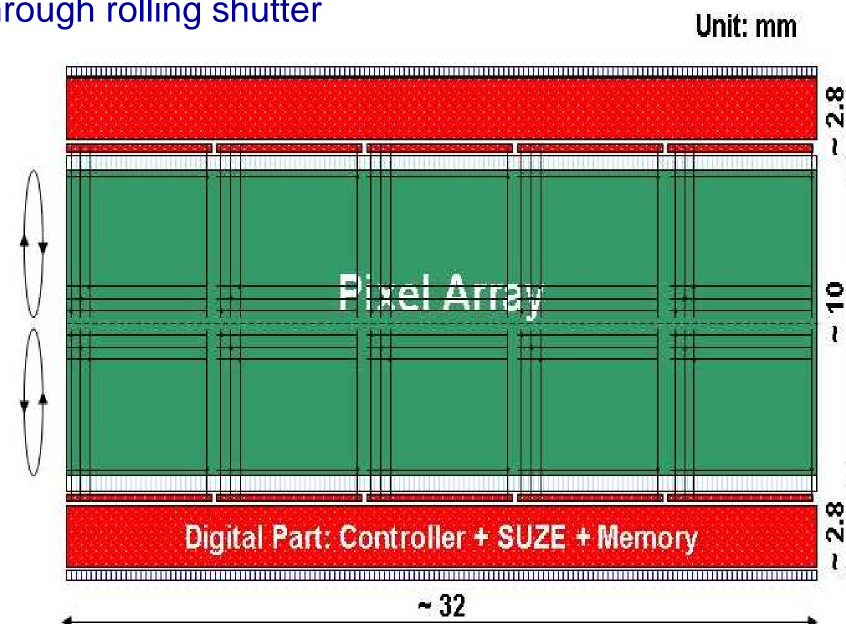
- **Motivations :**
  - ⋇ baseline improvements (e.g. CCE, SNR)
  - ⋇ extended running conditions or physics goals (e.g. read-out speed)

- **Baseline improvements $\equiv$ keep baseline architecture :**
  - ⋇ use of technology features improving charge collection or noise performance
  - ⋇ full use of $\geq$ 6 ML (e.g. row sequencer at bottom)
  - ⋇ etc.

- **Extended running conditions $\Rrightarrow$ modify baseline architecture :**
  - ⋇ 2 different architectures ;
    - ◇ parallel rolling shutter (PRS) architecture
    - ◇ high-density in-pixel (HDIP) functionnalities
  - ⋇ **Each option explores a different optimisation of speed $\star$ resolution $\star$ power :**
    - ◇ PRS $\Rrightarrow$ slower but more precise and dissipating less power
    - ◇ HDIP $\Rrightarrow$ faster and more selective but less precise and dissipating more power

Besides/Beyond MISTRAL

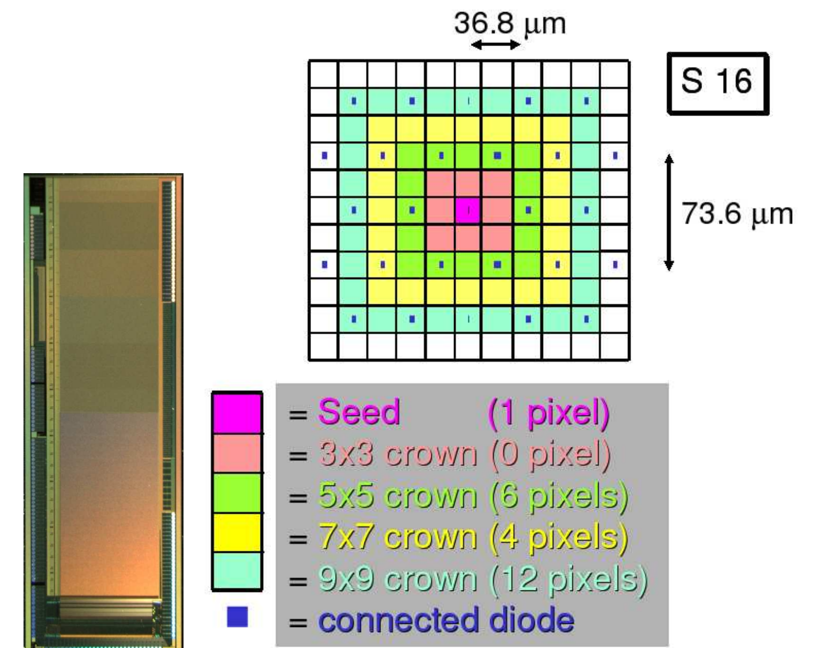
- **Parallel rolling shutter (still ”in birth”):**
  - ⋇ subdivide sensitive area into $\sim 2 \times 8$ sub-arrays read out independently through rolling shutter
  - ⋇ enlarge the pixel and use in-pixel p-type T
  - ⋇ implement in-pixel 2-bit ADC to keep spatial resolution $\sim$ 5-6 μm ($\Rrightarrow$ raw r.o. time $\times$ 2 !)
  - ⋇ approach expected to improve read-out time by factor $\gtrsim 4 \Rrightarrow$ $t_{integ} \gtrsim 5\ \mu s$
  - ⋇ alleviates increase of power dissipation
  - ⋇ drawback : larger pitch $\Rrightarrow$ reduced NI radiation tolerance



- **HDIP architecture :**
  - ⋇ in-pixel pre-amp $\oplus$ shaper $\oplus$ discriminator $\oplus$ time stamping
  - ⋇ faster than parallel rolling shutter $\rightarrowtail$ is it needed ?
  - ⋇ would benefit from expertise and designs of several ALICE groups (and from SuperB devt)
  - ⋇ easier to transfer to HPS in case of insufficient radiation tolerance of CMOS pixel
  - ⋇ drawbacks: more power consumption & worst impact param. resol. (”large” pitch (50 μm)

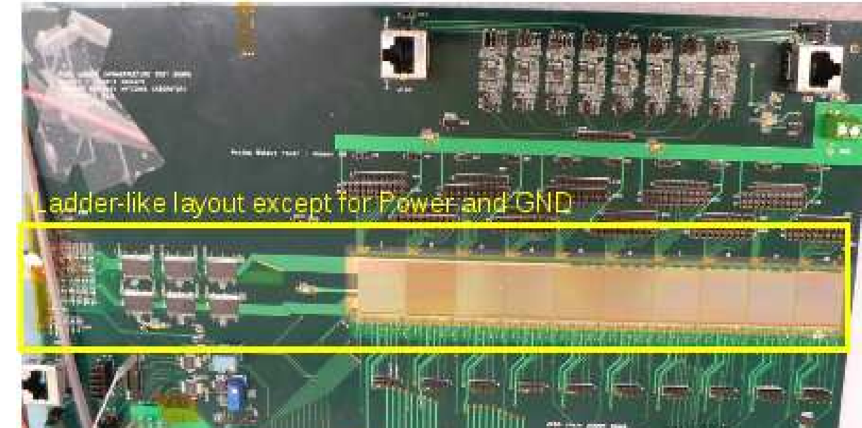
Towards a Large Pitch

- **Large pitch : Motivations**
  - ⋇ trackers require $\sigma_{sp} \gtrsim 10\ \mu m$
  - ⋇ calorimeters require O(100×100) μm^2 cells
    - ⇛ minimise number of pixels for the sake of power dissipation, integration time and data flow
- **Large pitch : Limitations**
  - ⋇ DANGER: increasing distance inbetween neighbouring diodes
    - ⇛ particles traversing sensor "far" from sensing diodes may not be detected because of e^- recombination
  - ⋇ "fragile" detection efficiency, exposed to losses due to irradiation, high temperature operation & slow read-out
- **Elongated pixels : Test results**
  - ⋇ elongated pixels allow minimising the drawbacks of large pitch
  - ⋇ concept evaluated with MIMOSA-22AHR prototype, composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⋇ m.i.p. detection performances assessed at CERN-SPS (T ∼ 15°C)
    - —∘ $\epsilon_{det} \sim$ 99.8 %
    - —∘ $\sigma_{sp} \sim$ 5-6 μm (binary charge encoding)
- **Square pixels : prototype under fabrication**
  - ⋇ MIMOSA-29 being fabricated on high-res epitaxy
  - ⋇ pixels of $\leq 80 \times 80\ \mu m^2$

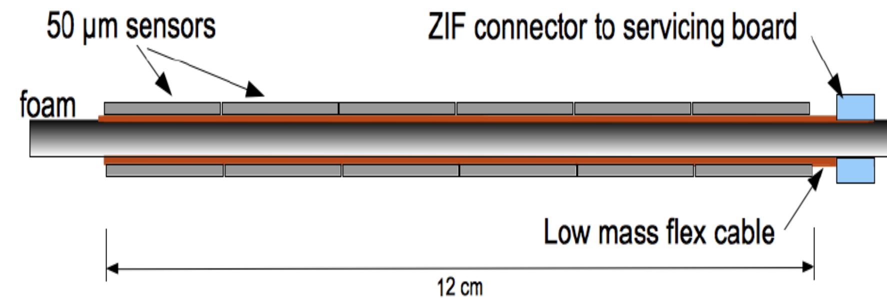


Sensor Integration in Ultra Light Devices

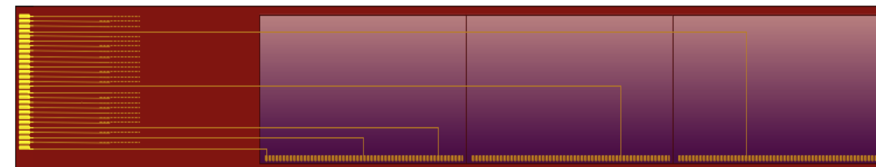
- "Useful" sensor thickness $\lesssim 30\ \mu m$ $\Rrightarrow$ *opens new possibilities w.r.t. thicker sensors*
  - ▷ *coarse thickness of sensors (e.g. EUDET BT) is 50 μm*



- **STAR-PXL ladder** (room temperature, single-end supported)**:**
  - ⋇ total material budget $\simeq$ 0.37 % X_0 :
    - ○ 50 μm thin sensors $\simeq$ 0.05 % X_0
    - ○ flexible cable $\simeq$ 0.07 % X_0
    - ○ mechanical support $\simeq$ 0.2 % X_0
    - ○ adhesive, etc. $\simeq$ 0.05 % X_0



- **Double-sided ladders with $\sim$ 0.2-0.3 % X_0 :**
  - $\Rrightarrow$ manifold bonus : compactness, alignment, redundancy, pointing accuracy (shallow angle), fake hit rejection, etc.



- **Unsupported & flexible ladders with $\lesssim$ 0.15 % X_0**
  - $\Rrightarrow$ 30-50 μm thin CMOS sensors mounted on thin cable & embedded in thin polyimide $\rightarrowtail$ suited to beam pipe ?

SUMMARY

- A baseline CMOS pixel sensor adapted to the specifications of L0 + ... is likely to be achievable by 2014, based on the ULTIMATE/MIMOSA-28 chip realised for the STAR-PXL :
  - ⋇ 0.18 μm CMOS technology
  - ⋇ $\sim$ 20$\times$20 μm^2 or 20$\times$40 μm^2 pixels $\Rrightarrow$ 40-50 or 20-25 μs r.o. time
  - ⋇ e.g. 2$\times$1500 columns of 256 pixels $\Rrightarrow$ 1$\times$3 cm^2 sensitive area
  - ⋇ room temperature operation (air flow)
- 2011 steps :
  - ⋇ understand and validate 0.18 μm technology (radiation tolerance, TJ sensing elements, ELT !!!)
  - ⋇ identify all human resources needed for sensor design (e.g. latch-up free digital circuitry ?)
  - ⋇ identify all resources needed for services (end of ladder steering & read-out)
  - ⋇ start designing binary output prototype
  - ⋇ identify and structure synergies with other projects (e.g. CBM)
- Besides baseline :
  - ⋇ develop focused improvements of baseline design (exploit $\geq$ 6 ML, TJ sensing diode)
  - ⋇ develop alternative, more effective, design $\Rrightarrow$ 2 options :
    - ◇ parallel rolling shutter (power economic) and hybrid pixel like (selective)
    - ◇ need input from WG-1/2 to optimise specifications
    - ◇ need to define which elementary structures to explore in multi-project run of Q4(2011)

0.18 μ Image Sensor Technology

- **Epitaxial layer :**
  - ⋇ high-resistivity p-type :
    - ⊸ controled high-resistivity : 300 $\Omega \cdot cm$
    - ⊸ uncontroled high-resistivity : 1–5 $k\Omega \cdot cm$, measurements for each wafer (mean, min, max)
  - ⋇ thickness: 12–18 μm (adjustable ?)

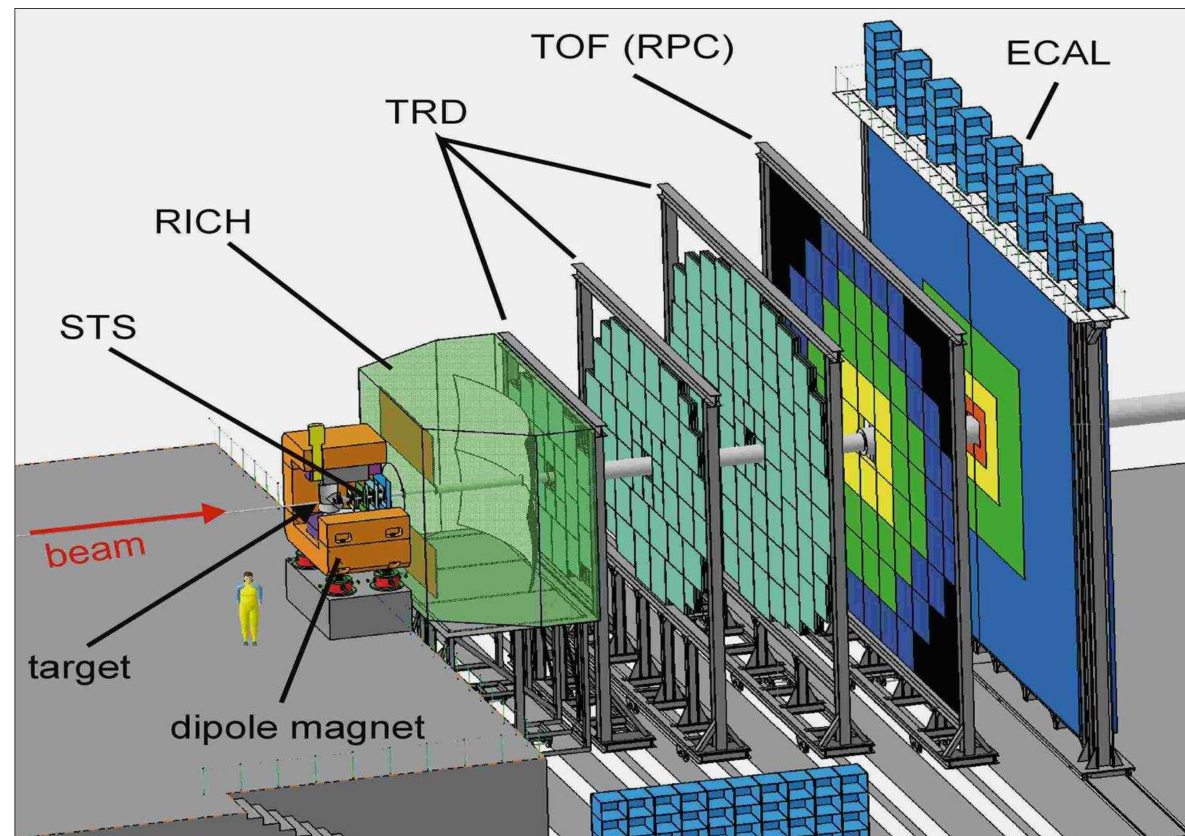
- **Sensing diode :**
  - ⋇ 2 optimised sensing systems designed by foundry, claimed to be much superiot to n-wells
    - ⤚ founder willing to support their implementation in MISTRAL design
  - ⋇ involvement of founder in design is part of the contract (business plan)

- **Radiation tolerance :**
  - ⋇ founder interested in assessments of the technology radiation tolerance
  - ⋇ ”radiation tolerant” chips fab. by founder will be sent to CERN-IPHC for radiation tolerant study
  - ⋇ possibility of ordering rad. tol. (digital) IPs to founder customer (SLU free NROM) ?

- **Fabrication :**
  - ⋇ $\geq$ 8 MPW runs per year ⤚ 50 kUSD for minimal surface (25 mm^2)
  - ⋇ MPW runs in *Image Sensor* process can include ”special” features (high-res epi, 6 ML, etc.)
  - ⋇ founder works on full project basis, including agreed set of MPW and engineering runs
  - ⋇ need of high-res epi wafers requires special request $\Rrightarrow$ ordre well in advance

Application of CMOS Sensors to the CBM Experiment

- **Cold Baryonic Matter (CBM) experiment at FAIR:**
  - ⋇ Micro-Vertex Detector (MVD) made of 2 or 3 stations located behind fixed target
  - ⋇ double-sided stations equipped with CMOS pixel sensors)
  - ⋇ **operation a negative temperature in vacuum**
  - ⋇ each station accounts for $\lesssim$ 0.5 % X_0
  - ⋇ sensor architecture close to ILC version

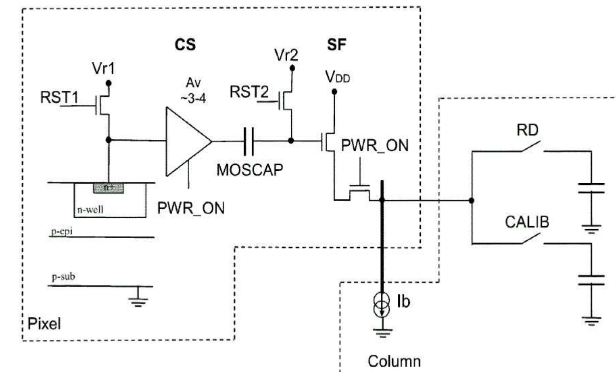


- **Most demanding requirements :**
  - ⋇ ultimately ($\sim$ 2020): 3D sensors
    $\lesssim$ 10 μs, $>$ 10^{14} n_{eq}/cm^2, $\gtrsim$ 30 MRad
  - ⋇ intermediate steps: 2D sensors
    $\lesssim$ 30-40 μs, $>$ 10^{13} n_{eq}/cm^2, $\gtrsim$ 3 MRad
  - ⋇ 1st sensor for SIS-100 (data taking $\gtrsim$ 2016)

Pixel Array of ILD-VTX Sensor

- **Main sensing and read-out micro-circuit elements :**
  - ⋇ charge collection on sensing diode
  - ⋇ sensed charge conversion into signal (voltage)
  - ⋇ pre-amplification
  - ⋇ average noise (pedestal) subtraction (clamping)

    ▷▷▷ single pixel consumption $\simeq$ 0.2 mW (3.3 V)

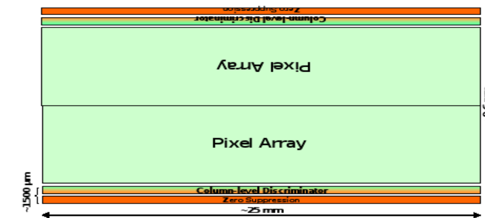


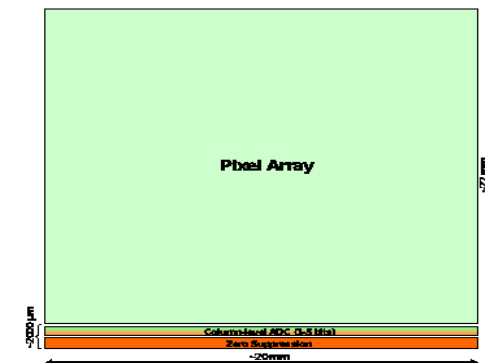
- **Power consumption of pixel array** (0.35 μm process) **:**
  - ⋇ **inner layers :**
    - ○ $\sim$ 1300 columns of 16 μm wide pixels
    - ○ two-sided read-out $\Rrightarrow$ 2600 columns/sensor

      ▷▷▷ $\sim$ 520 mW/sensor

  - ⋇ **outer layers :**
    - ○ $\sim$ 600 columns of 35 μm wide pixels
    - ○ single-sided read-out $\Rrightarrow$ 600 columns/sensor

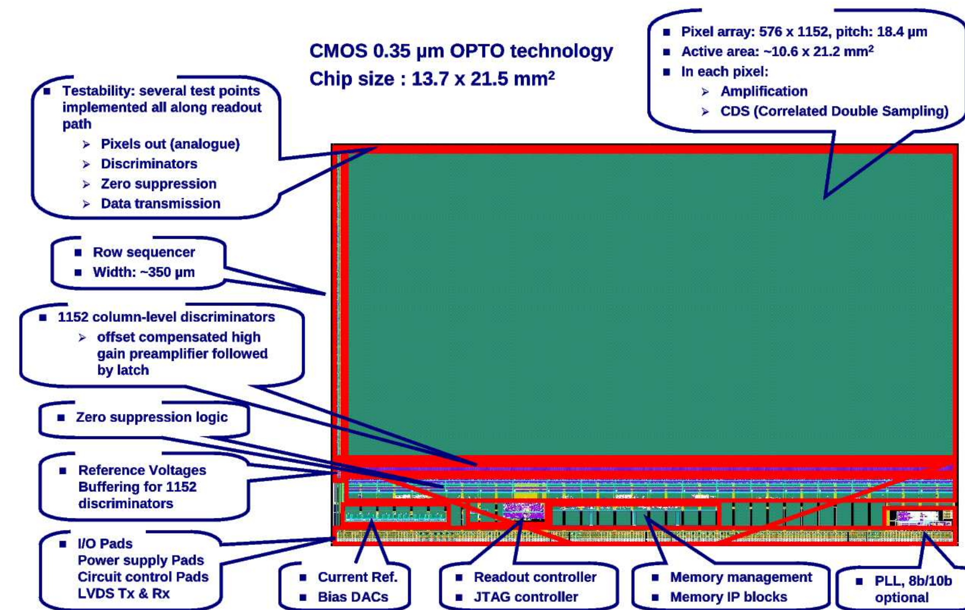
      ▷▷▷ $\sim$ 120 mW/sensor





Peripheral Circuitry of ILD-VTX Sensor

- **Main peripheral circuitry elements :**
  - ⋇ discriminators / ADCs : 300 / 500 μW/col.
  - ⋇ bias DACs (discri. & ADC thresholds, V_{ref}, etc.) : O(1) mW/DAC
  - ⋇ digital circuitry (zero-supp., sequencers, etc.) : $\sim$ 150 μW/col.
  - ⋇ memories (output buffers) : O(1) mW/Mbps
  - ⋇ signal transmission (LVDS) : O(10) mW/channel



- **Power consumption of peripheral circuitry** (0.35 μm process) **:**
  - ⋇ discriminators / ADCs : 800 / 300 mW (in/out)
  - ⋇ bias DACs (discri. & ADC thresholds, V_{ref}, etc.) : 50 / 20 mW (in/out)
  - ⋇ digital circuitry (zero-suppression, sequencers, etc.) : 400 / 100 mW (in/out)
  - ⋇ memories (output buffers) : 200 / 50 mW (in/out)
  - ⋇ signal transmission (LVDS) : 200 / 50 mW (in/out)
    - ▷▷▷ **inner layers :** $\sim$ 1650 mW/sensor
    - ▷▷▷ **outer layers :** $\sim$ 500 mW/sensor