MONOLITHIC AND HYBRID TECHNOLOGIES FOR PIXEL DETECTORS

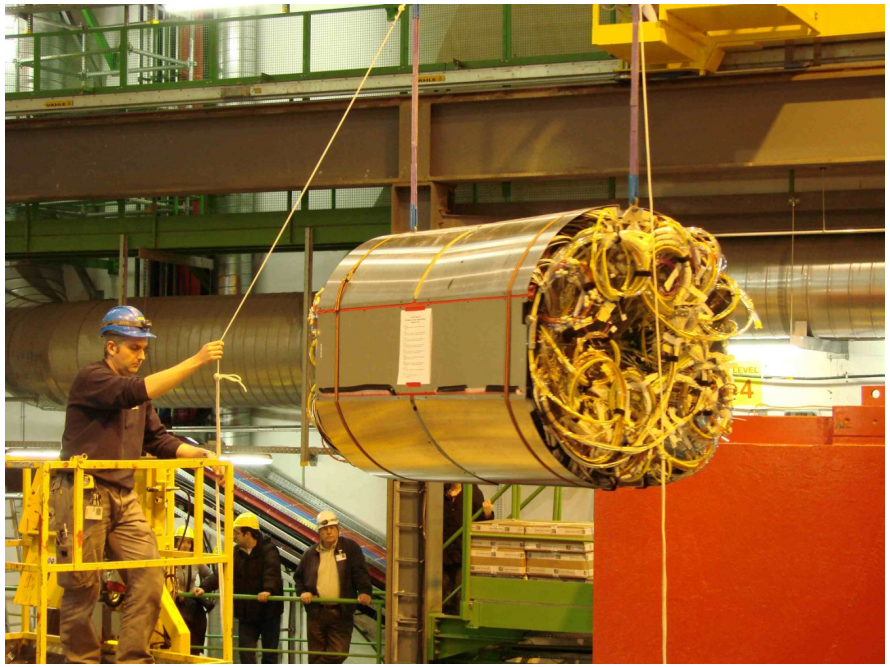
P. Riedler, A. Rivetti

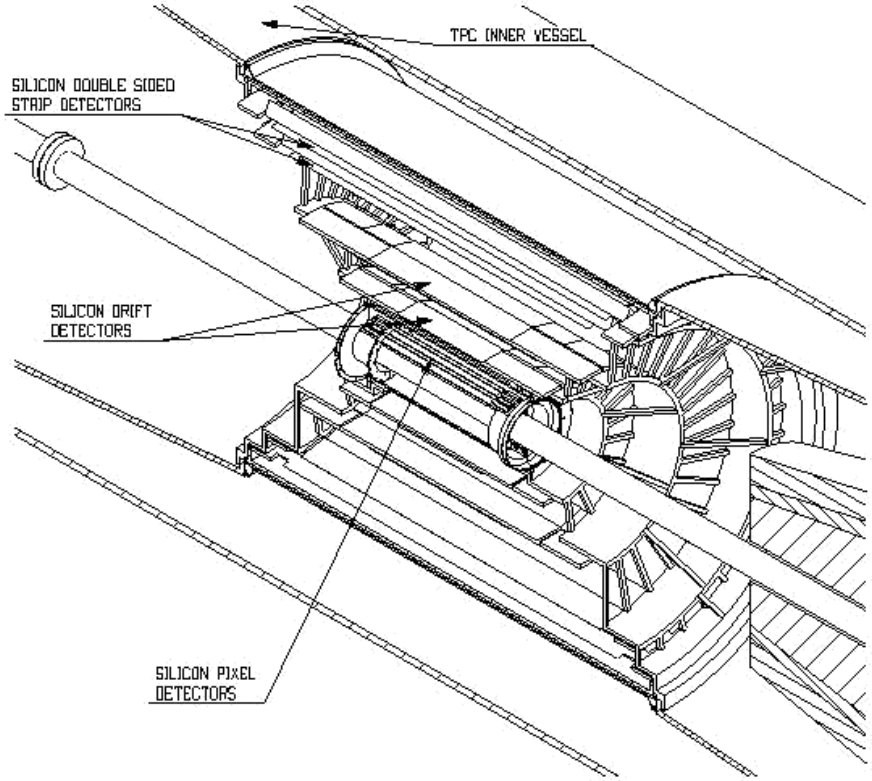
Overview

- Introduction
- Monolithic and hybrid technologies
  - MISTRAL >> see presentation by MARC
  - INMAPS
  - Hybrid sensor developments
- Material budget
  - Thinning
  - TSVs
- Readout developments
- Testing plans

Introduction

- The current ITS consists of 6 silicon layers (2 pixels, 2 drift, 2 strips) and covers radii from 3.6 cm to 43 cm

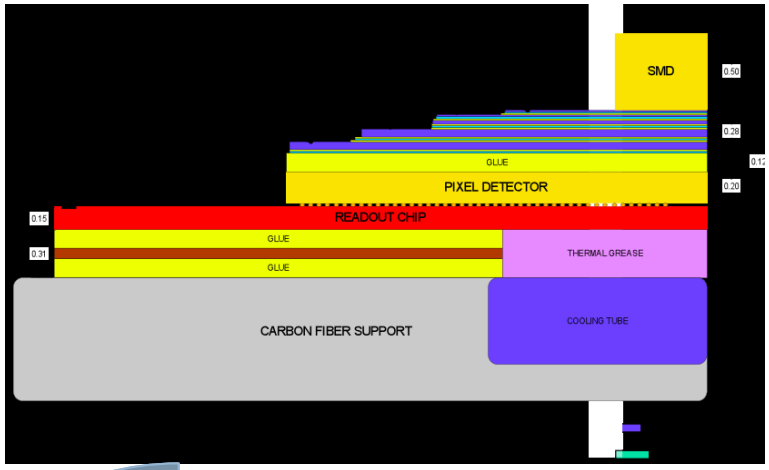




ITS Upgrade

- Key technical topics:
  - Get **closer to the interaction point**
    - Currently: 29 mm beampipe radius >> ~**20-22 mm**
  - Reduce the **material budget** (esp. innermost layers)
    - Currently: ~1.14% per pixel layer >> **0.3-0.5% X_0**
  - Reduce **pixel size**
    - Currently: 50 µm x 425 µm >> **20-30 um in r-phi (possibly z)**
  - **Trigger capability** (L2 ~ 100us): topological trigger, fast-OR and fastSUM at L0/L1(1.2 us/7.7 us)
  - **Increased acceptance**

Material Budget



ALICE SPD: 1.14% X_0 per layer

2 main contributors:
silicon (0.38%) and bus (~0.48%)

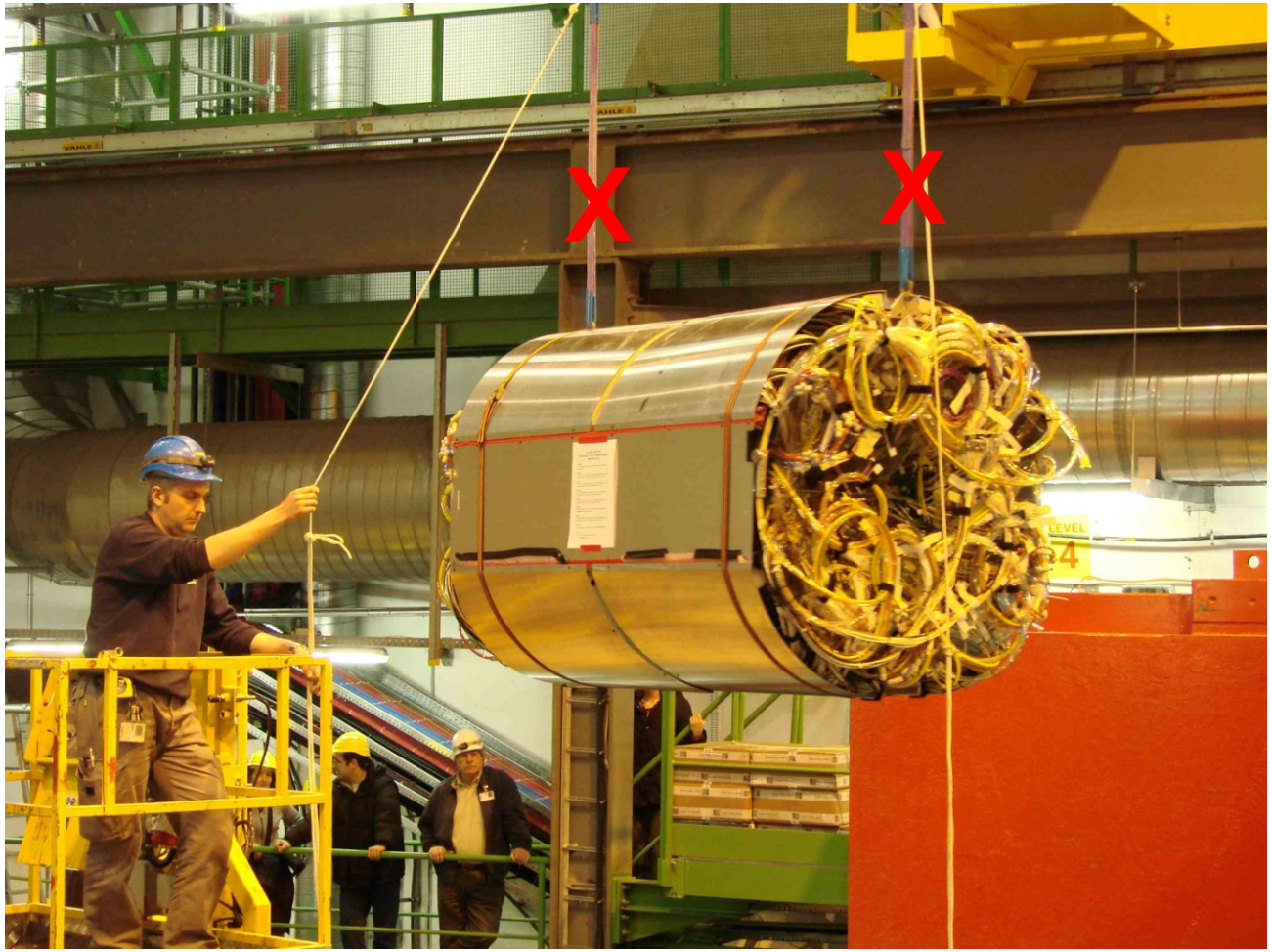
ITS Upgrade:

0.5 % X_0 as upper limit for the innermost layers

Target: 0.3-0.5% X_0

Improvement of a factor ~2-3 !

Material Budget



Configurations

- Two options under study, e.g.:
  - Replace the existing pixel layers and add a layer0
  - "all-new" ITS consisting of pixels and strips
- Activities two-folded:
  - 1. Study best possible configuration >> see talks by Romualdo, Diego, Arturo, Stefan, Giuseppe
  - 2. Identify technological options >> next slides

Pixel Upgrade

- Strategy: **follow hybrid and monolithic developments,** collect information and participate in prototyping >> prepare proposal by summer 2011
- Main considerations:
  - **Hybrid solution:**
    - Cost of flip chip bonding
    - Material budget
  - **Monolithic solution:**
    - Speed considerations
    - Radiation tolerance

Monolithic pixel technologies

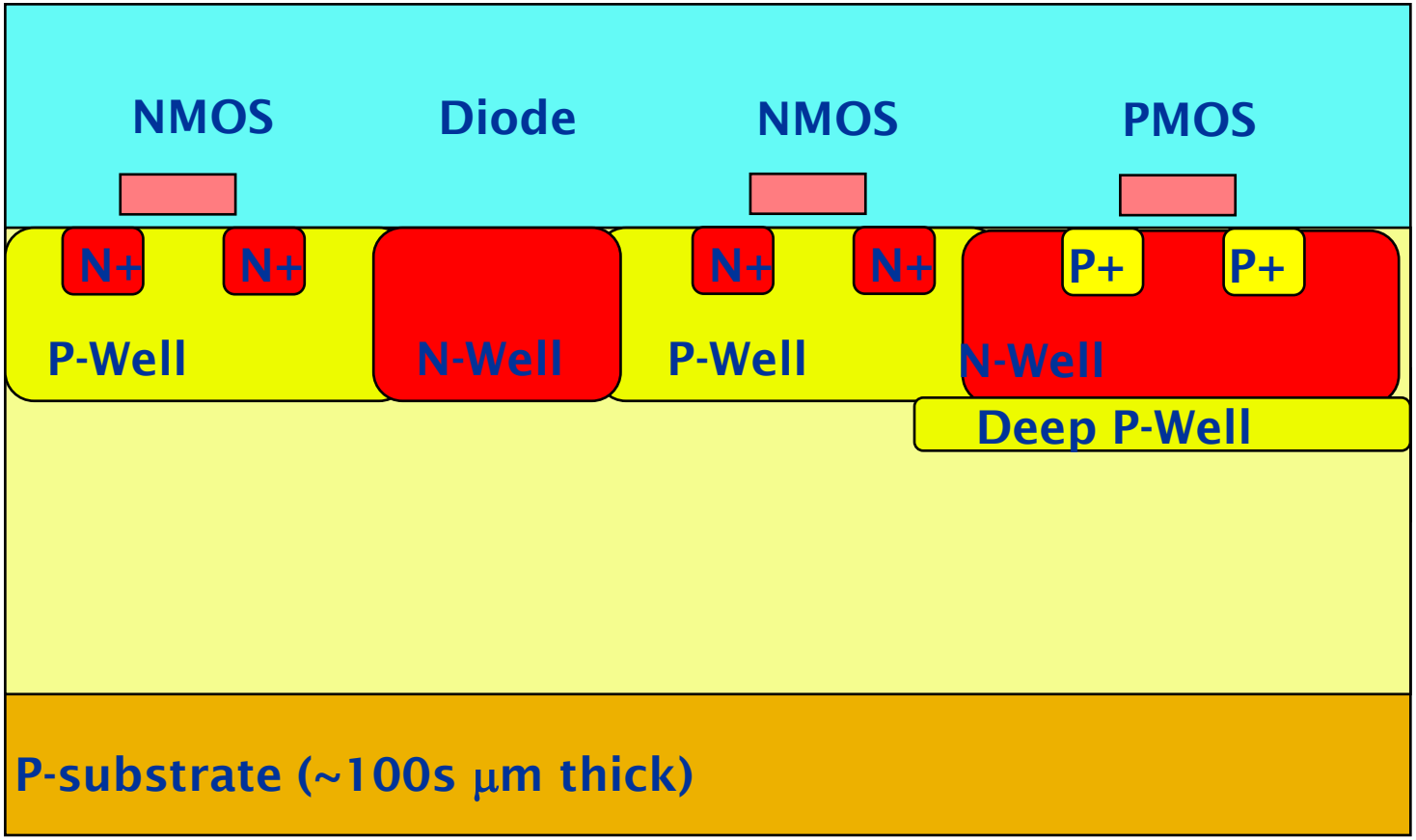
Several monolithic developments:

- MISTRAL – MIMOSA based design specific for ALICE >> see talk by Marc
- INMAPS
- LePix

Science & Technology Facilities Council
Technology

The INMAPS process

0.18 um CMOS process



Standard CMOS with additional deep P-well implant.

Quadruple well technology.

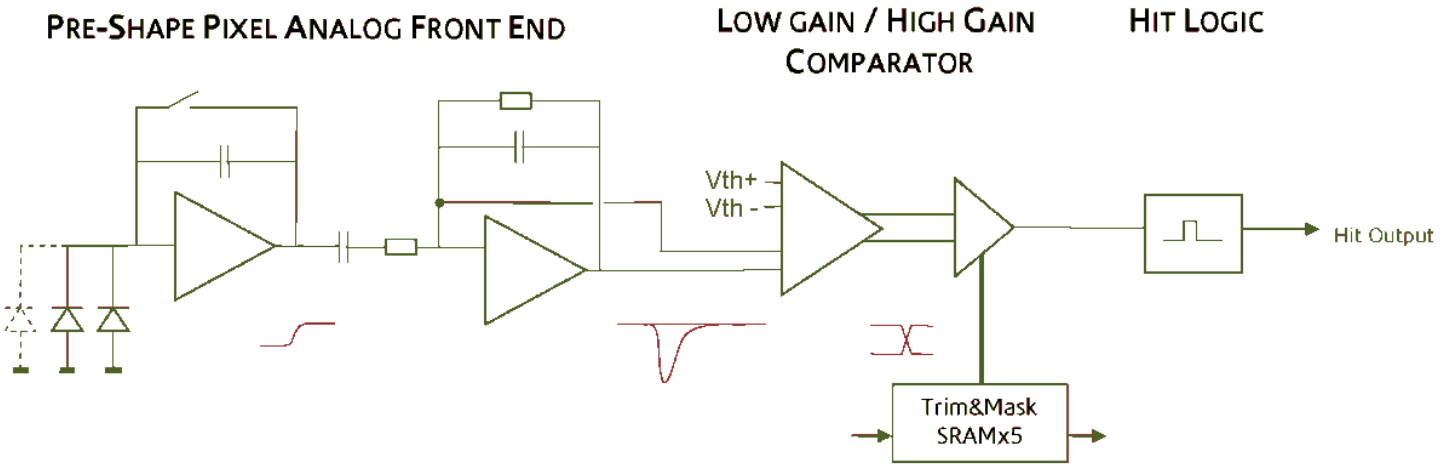
100% efficiency and CMOS electronics in the pixel.

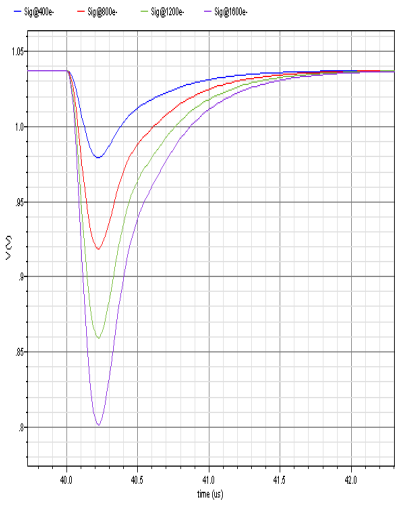
Optimise charge collection and readout electronics separately!

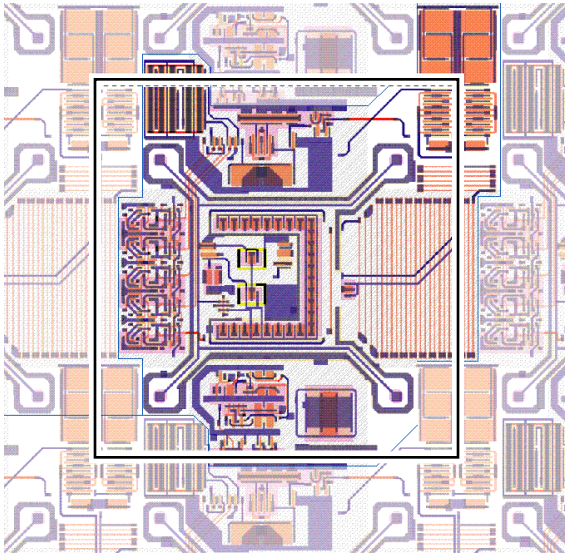
Science & Technology Facilities Council
Technology

TPAC. Sensor for the ILC ECAL (CALICE)

- preShape
- Gain 94μV/e
- Noise 23e-
- Power 8.9μW
- 150ns "hit" pulse wired to row logic
- Shaped pulses return to baseline







50 μm pixel
Over 150 transistors, N and PMOS

R. Turchetta/RAL

TPAC tests for WG3

- Received test cards and TPAC chips from colleagues at RAL/UK
- 0.18 um CMOS process from TOWER/JAZZ >> talk by Marc
- Setting up system at CERN to carry out irradiation tests on different TPAC circuits:
  - Epi 12 um and 18 um
  - HR and standard resistivity
  - With and without deep p-well

Cedric Mansuy/CERN

2) TPAC boards:

Fig: Main board

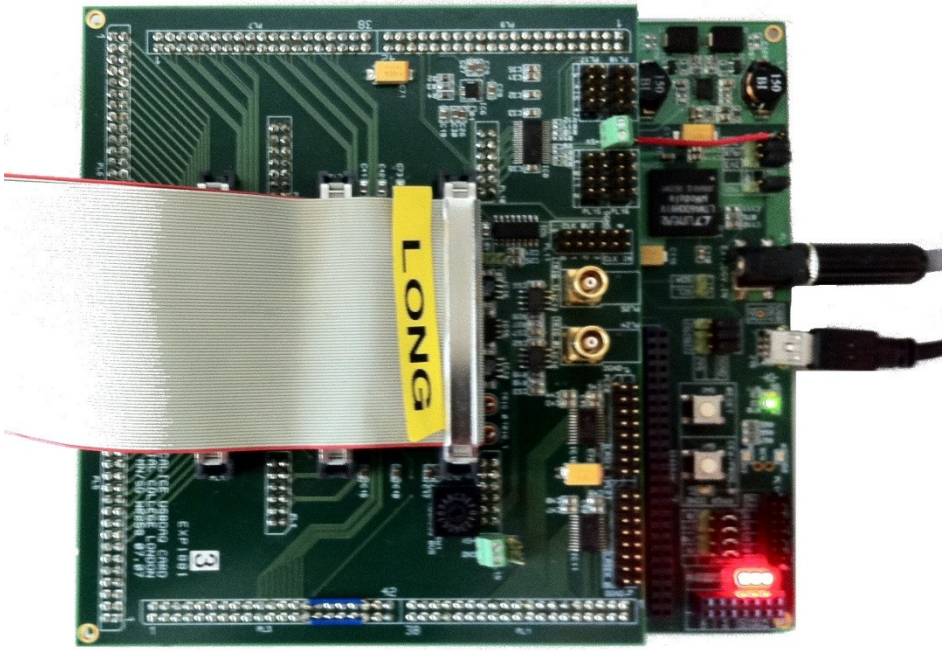
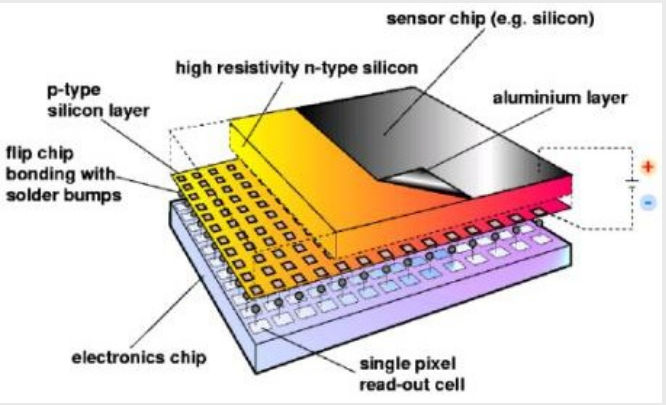
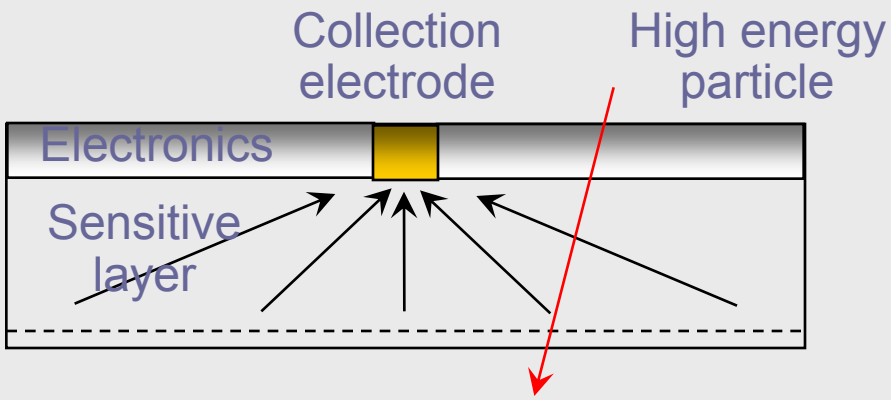


Fig: DAC board

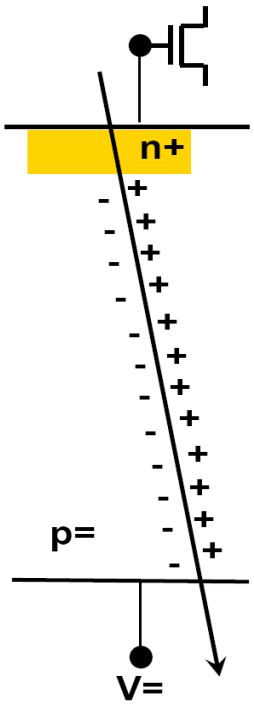
LePIX: monolithic detectors in advanced CMOS

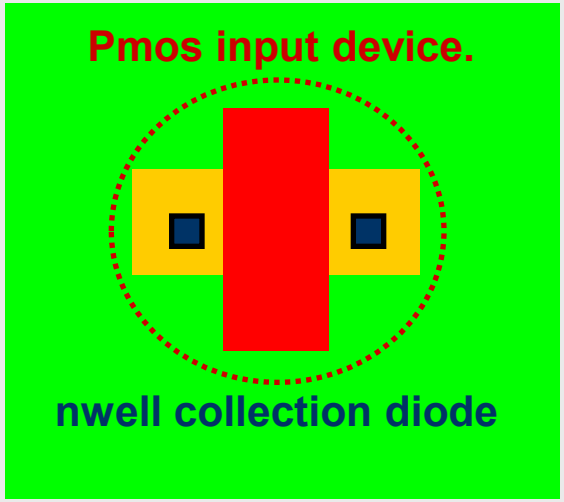




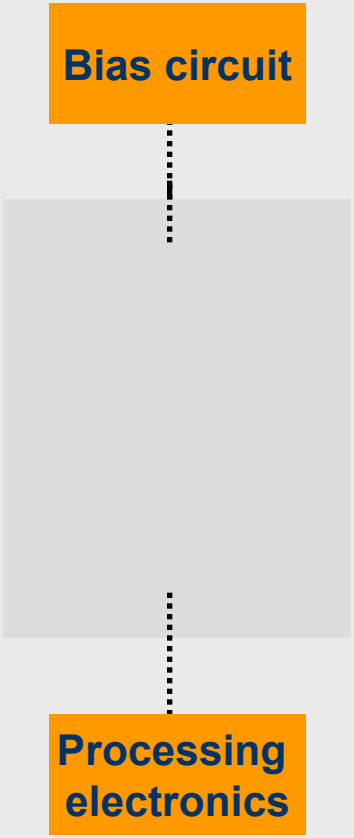
- Scope:
  - Develop monolithic pixel detectors integrating readout and detecting elements by porting standard 90 nm CMOS to wafers with moderate resistivity.
  - Reverse bias of up to 100 V to collect signal charge by drift
- Key Priorities:
  - Develop and optimize the sensor
  - Design low power (~ 1uW/pixel or less) front end electronics using low detector capacitance
  - Assessment of radiation tolerance
  - Assessment of crosstalk between circuit and detecting elements (may require special digital circuitry
- Need to carry development to a large matrix for correct evaluation

CIRCUIT ARCHITECTURE





- Charge to voltage conversion on the sensor capacitance
- For 30 μm depletion and 10fF capacitance: 38 mV for 1 mip.



- ✓ Only one PMOS transistor in the pixel (or maybe very few…)
- ✓ Each pixel is permanently connected to its front-end electronics located at the border of the matrix.
- ✓ Each pixel has one or two dedicated lines: need of ultra fine pitch lithography => 90 nm CMOS.

LePix

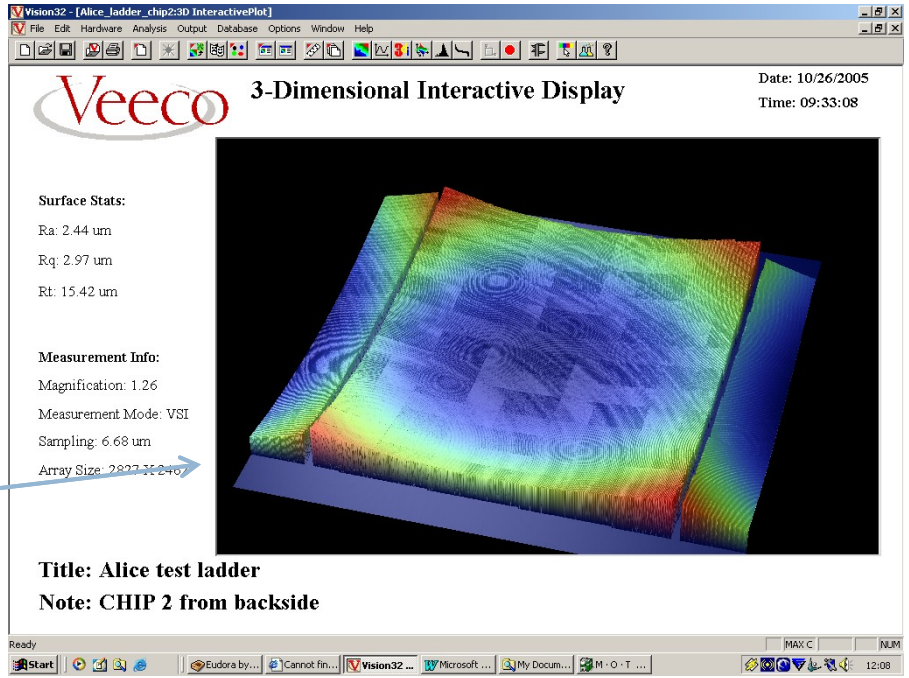
- The LePix approach may allow to have significantly thicker detection layers (30 um or more) with respect to what is achieved with other monolithic techniques.
- High resistivity wafers have been sent to fabrication and results are expected by the summer

Thinning

- Reduce the silicon contribution as much as is feasible/"sensible" given the targets
- Hybrid vs. Monolithic:
  - Target thickness for ASICS: 50 um
    - ~0.05% X_0
  - Different "weight" of the problem:
    - Monolithic: bowed chips will be more difficult to integrate into a module plane
    - Hybrid: Too high bow of chips can result in a disconnection of bump bonds >> loss of channels

Thinning

- Current ALICE chips: 150 um thinned during bump bonding process
- thickness reduction will make inherent stresses come out stronger
- first experience during the ALICE production
- Thinning process needs to be well studied and tuned to produce coherent results



S. Vahanen, VTT

Thinning – first studies in 2011

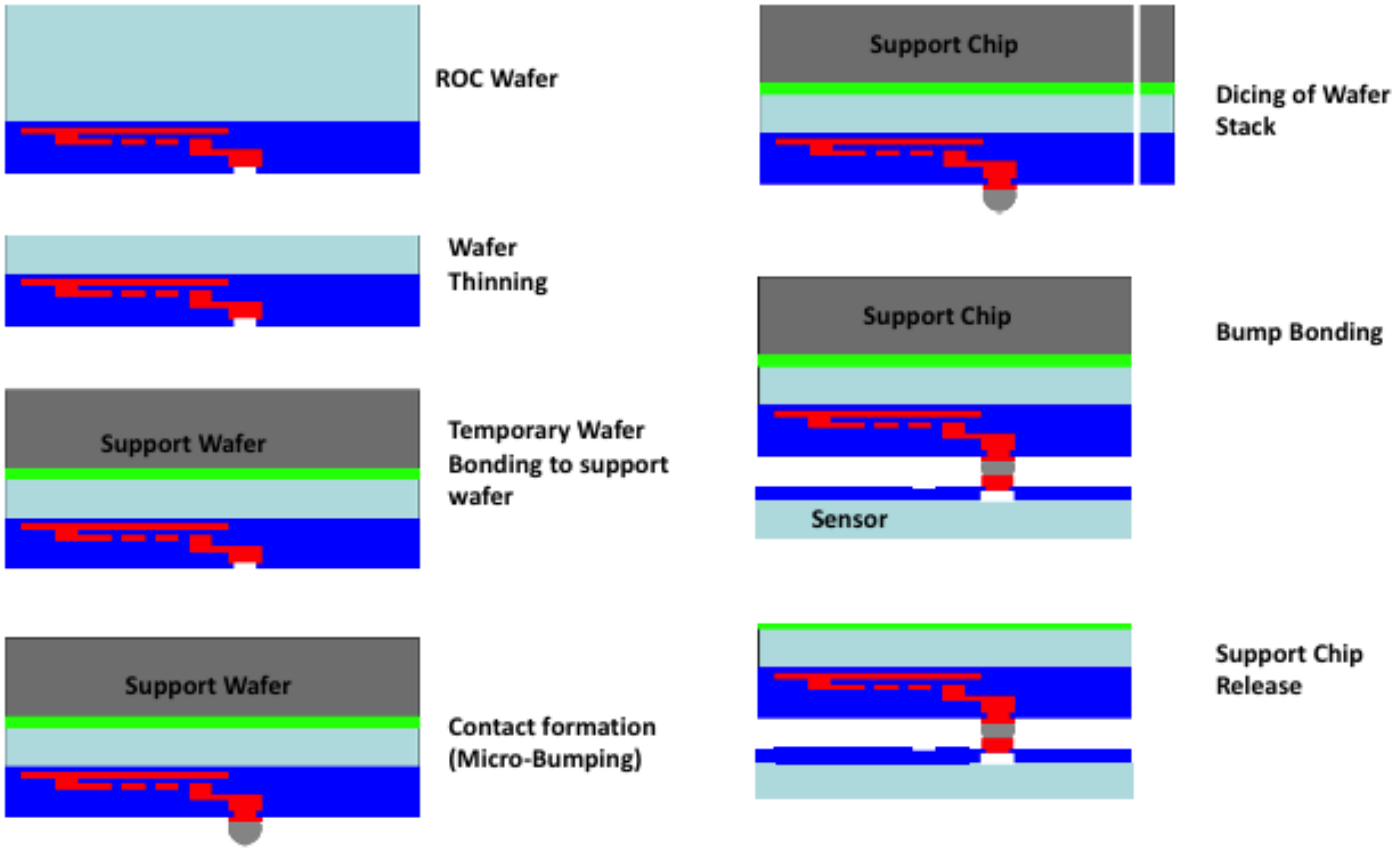
Study using dummy components with IZM Berlin

- Hybrid detector dummy components based on ALICE layout (sensors, chips), synergy with NA62 Gigatracker with similar requirements
- Specific IZM process for thinning:
- Sensor wafers (200 um) in processing, ASIC wafers ready in ~4 weeks
- First components back by end July 2011

	Si sensor [µm]	X_0 [%]	ASIC [µm]	X_0 [%]	X_0 total [%]
First R&D step	200	0.22	50	0.05	0.27
Target	100	0.11	50	0.05	0.16

Thin Chip Assembly – Temporary Support Approach

Process Flow



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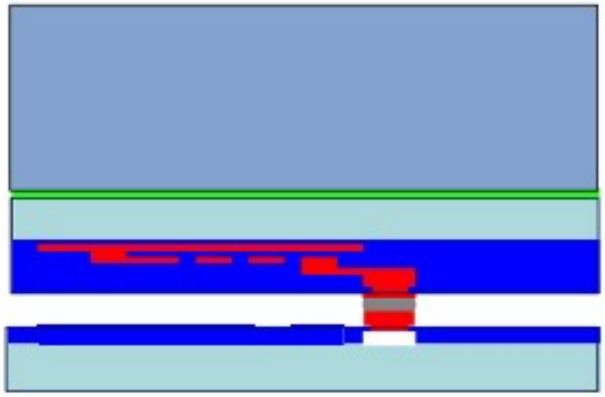
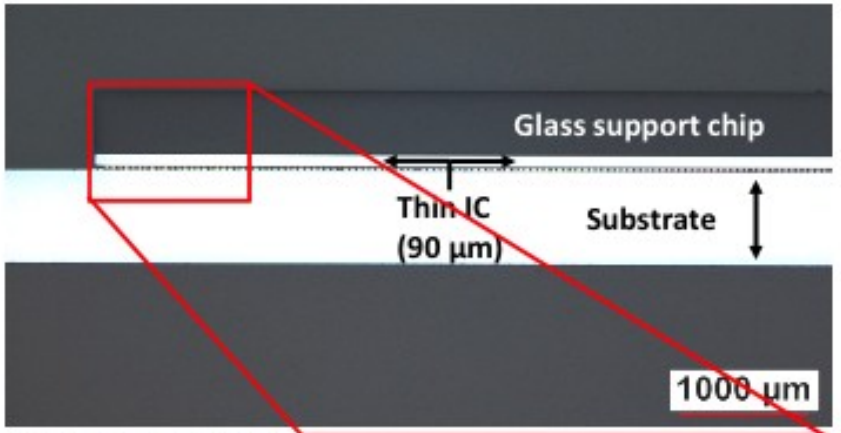
Fraunhofer IZM

Thin Chip Assembly – Temporary Support Approach

Laser Debonding using UV-Release Glue

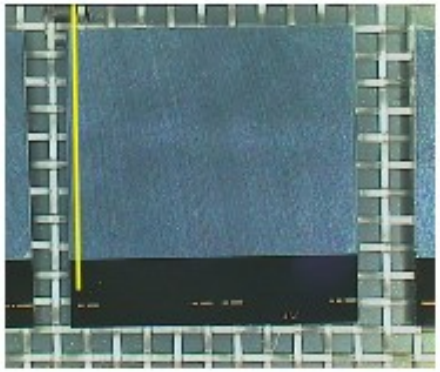
1. Step: Flip Chip Assembly of Chipstack

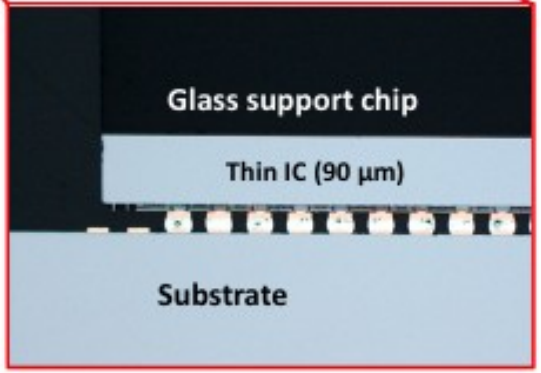




Left:
Chip after bump bonding
size 14x11 mm² (2x1 FE-I3)

Right:
Cross section of the first bump row
(yellow line)





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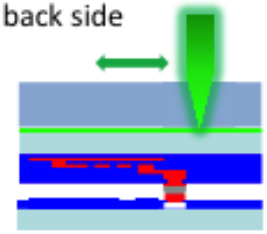
Thin Chip Assembly – Temporary Support Approach

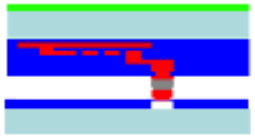
Laser Debonding using UV-Release Glue

2. Step: Support Chip Release

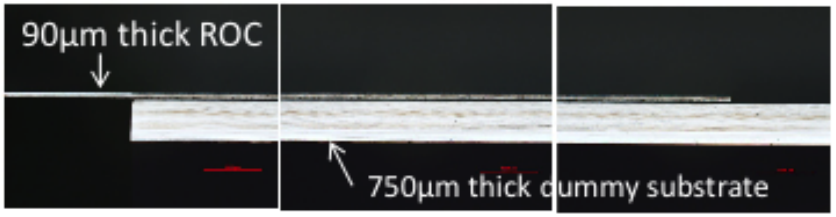
1. Laser scanning of back side

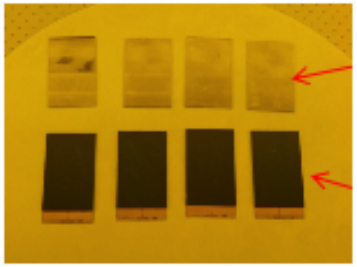


2. Carrier chip release



Side few on 14 x 11 cm² (Double ROC ATLAS FE-I2 reticle) dummy module after carrier chip release





Released glass carrier chip

Thin chip module (ROC side down)

14 x 22 cm² (Quad ROC ATLAS FE-I2 reticles) dummy modules after carrier chip release

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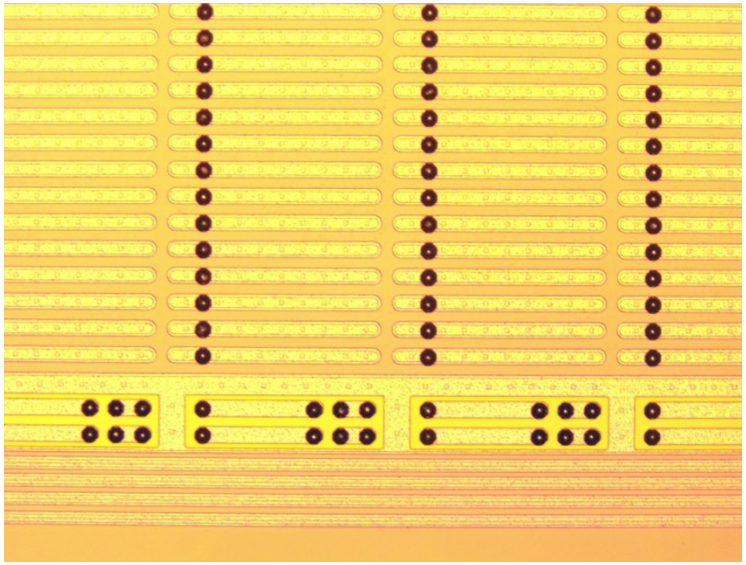
Hybrid Sensor

- Reduce hybrid sensor thickness (currently 200 um, lowest thickness in LHC experiments) in trade-off with the signal
- Target: 100 um
- First trials in 2010:
  - Use epitaxial sensor wafers (low-R carrier wafer "integrated") and thin away the support wafer
  - Run with FBK/Trento in 2010, processed 5 wafers with 100 um epi layer using standard ALICE layout (50 um x 425 um)

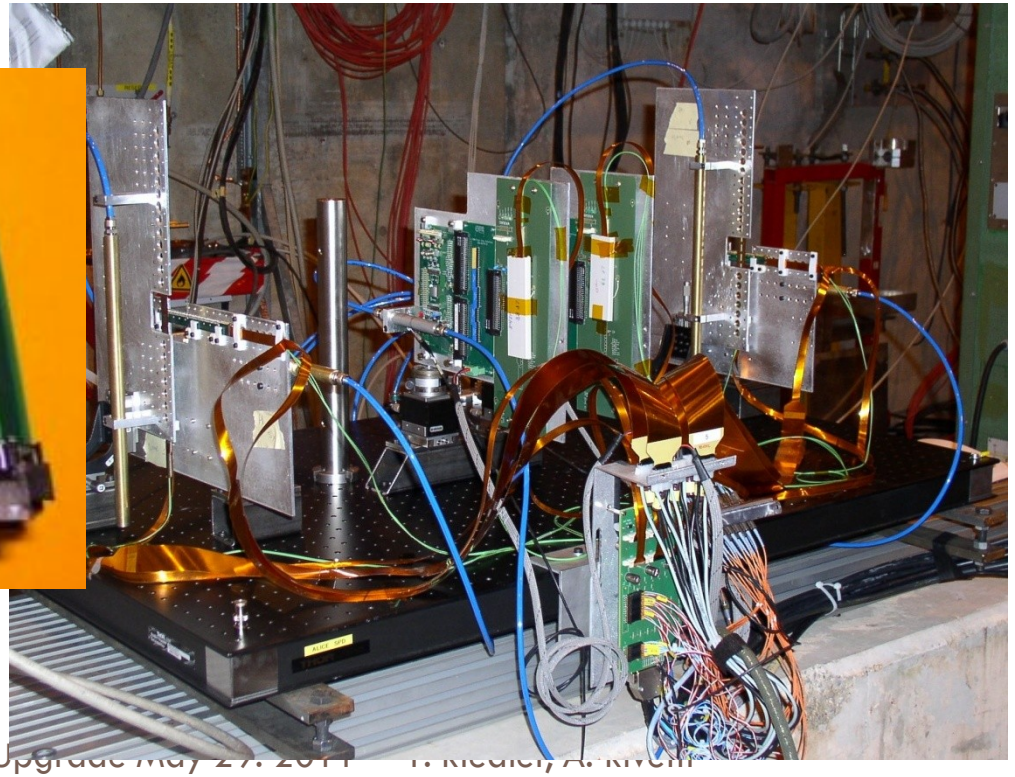
Hybrid Sensor

- 3 wafers processed at VTT
  - Successful thinning and back side patterning
  - overall sensor thickness: 105-115 µm (i.e. epi layer + ≈10 µm)
- 5 singles flip-chip bonded to the current ALICE pixel front-end chip
  - electrical tests: ~30 nA at 20V at RT, min. threshold ~ 1500 el., ~30 missing pixels

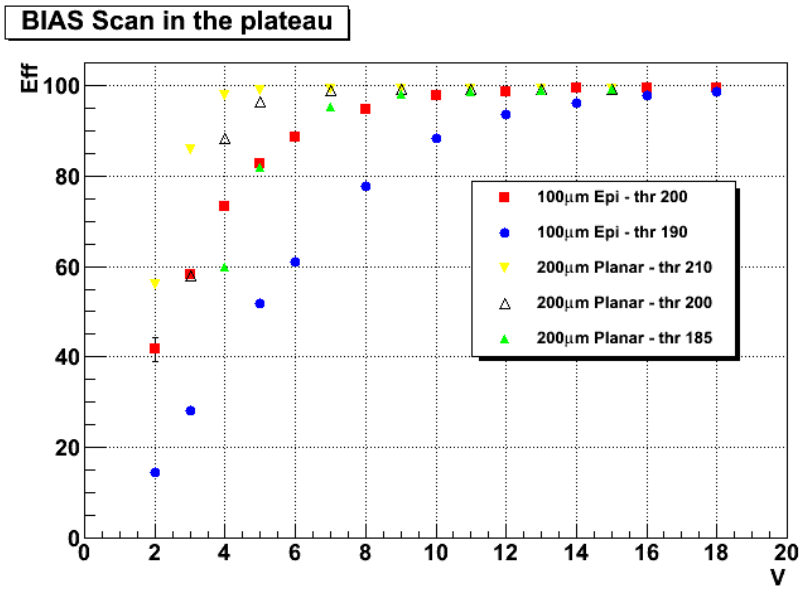


Hybrid Sensor

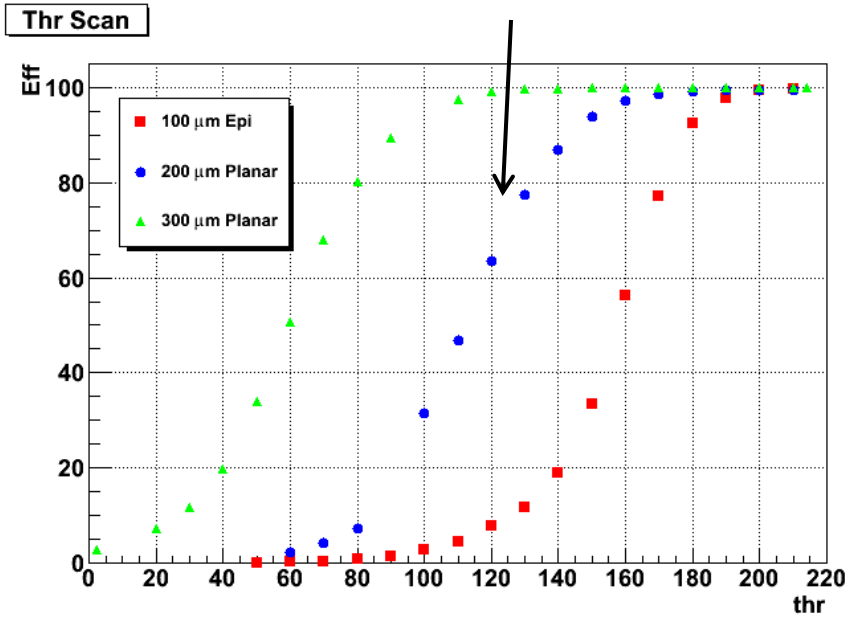
- Beamtest in November 2010 at CERN with epi sensors (and also 3D sensors)

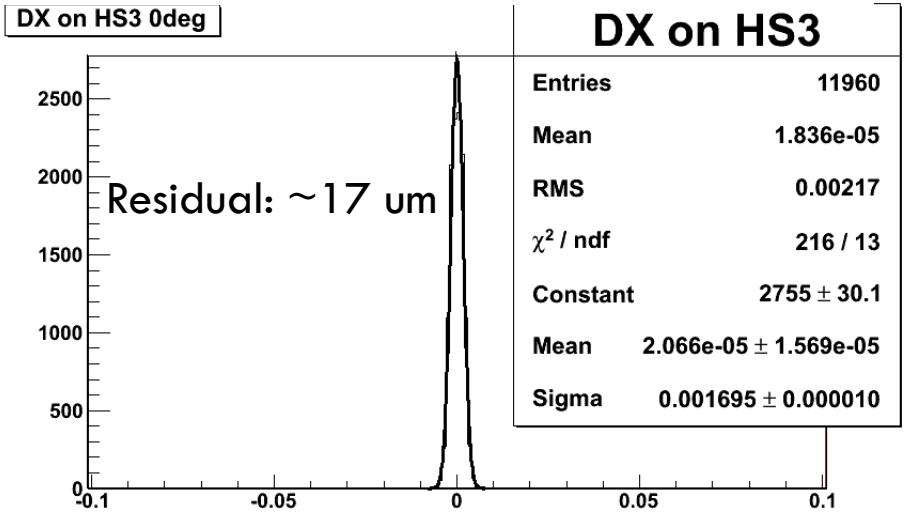


Hybrid Sensor



Current ALICE sensor

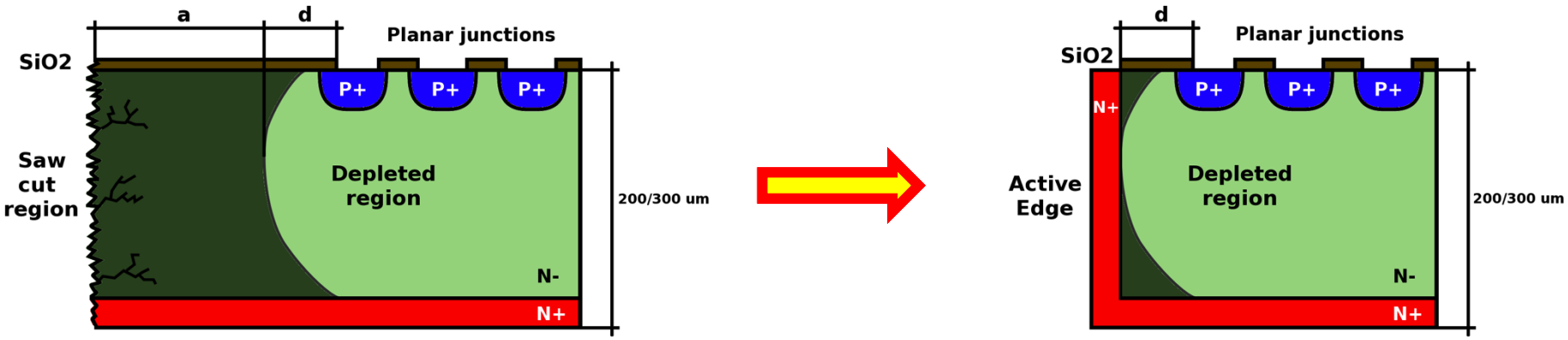




Thr (DAC)	Thr (el.)
200	3000
190	3600
180	4200
170	4800

Hybrid Sensors

- Next step: edgeless epi sensors (R&D with FBK/Trento)

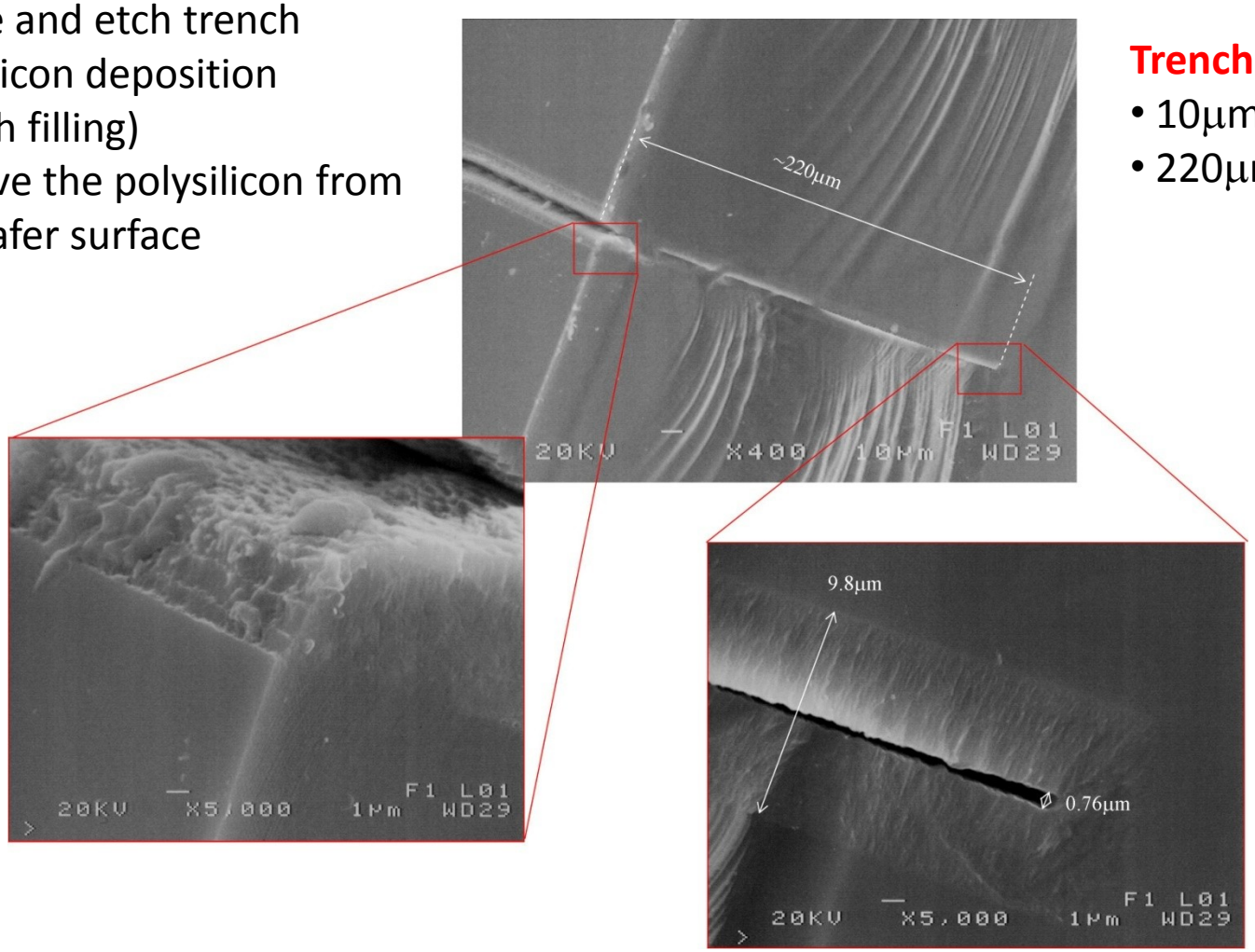


TECHNOLOGY : POLYSILICON TRENCH FILLING

M. Boscardin

Process

- Define and etch trench
- Polysilicon deposition (trench filling)
- Remove the polysilicon from the wafer surface



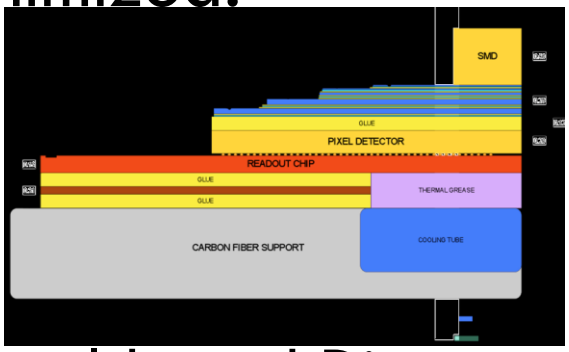
Trench :

- 10µm wide
- 220µm deep

More material budget

- The two main contributors to the current pixel in terms of material are silicon (see previous slides) and the **interconnection bus (0.48% X_0)**

- Several points where this can be minimized:
  - ASIC architecture >> next slide
  - "Novel" I/O for the front-end
    - TSVs for hybrids, ball-grid arrays, ..
  - Design of the bus >> see talk by Romualdo and Diego



Gianluca Aglieri Rinella/CERN

Reduction of power layers thicknesses

- Reduction of chip analog and digital consumptions
- Minimum thickness constrained by maximum bias drop compatible with chip bias specification
- Possible way to improve:
  - Segment the power and ground layers in parallel stripes, one per chip
  - Make stripes with uniform resistance by layout: widths of the bias stripes proportional to the length from power input
  - Equal voltage drops on each bias stripe
  - Thickness can be reduced at the price of larger (but equal) drops on the bias layers. All chips can be biased with uniform voltages

Other Developments

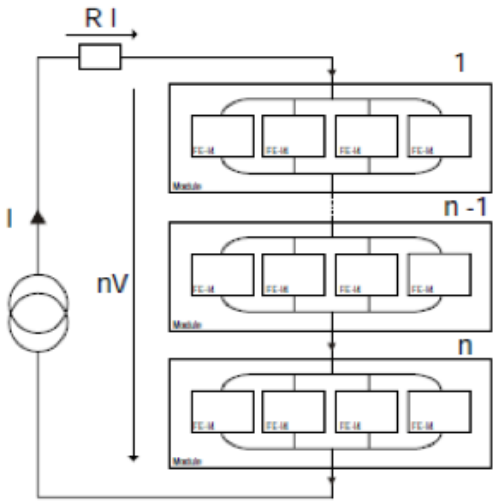


Figure 1. Schematical design of a SP scheme. The current is reduced by a factor n, where n is the number of modules in the chain, with respect to a parallel powering scheme where the same number of modules is powered by a constant voltage.

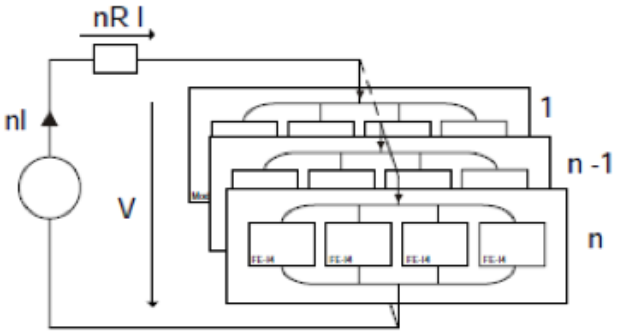
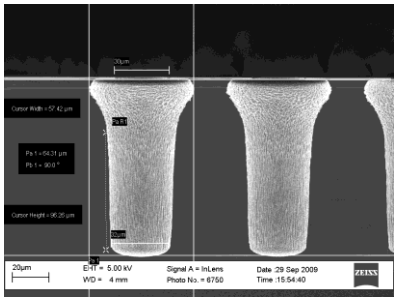


Figure 2. Schematical design of a parallel powering scheme.

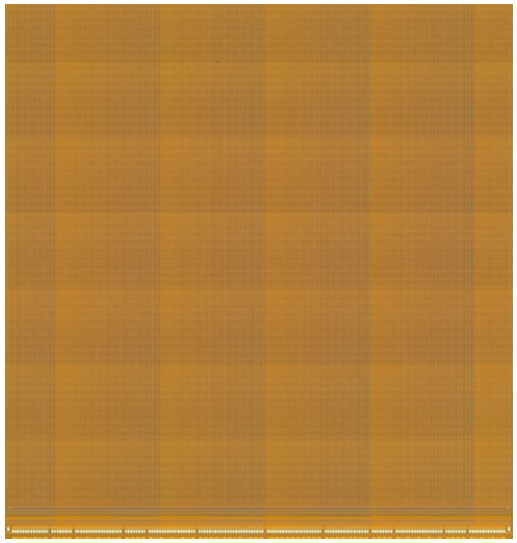
L. Gonella et al,: A serial powering scheme for the ATLAS pixel detector at sLHC JINST 2010, 5 C12002

Through Silicon Vias (TSV)

- Contribute to activity at CERN organized by Medipix Collaboration
- Medipix3 chip designed for TSV



TSVs etched by VTT on dummy wafer with 100 µm pitch



Dicing lanes near to matrix

All IO logic and pads contained within one strip of 800µm width

All IO´s have TSV landing pads in place

Permits 4-side butting

94% sensitive area

M. Cambpell, T. Tick
AIDA meeting, May 2011

Through Silicon Vias (TSV)

- Proposal from CEA-LETI
- Use 10 Medipix3 wafers
  - Front-side UBM deposition
  - Wafer thinning to 100 um
  - Drilling of TSV to M1 and electrical isolation of M1
  - Deposition and etching of back side connect layer
  - UBM deposition on back side
- First results autumn 2011

M. Cambpell, T. Tick
AIDA meeting, May 2011

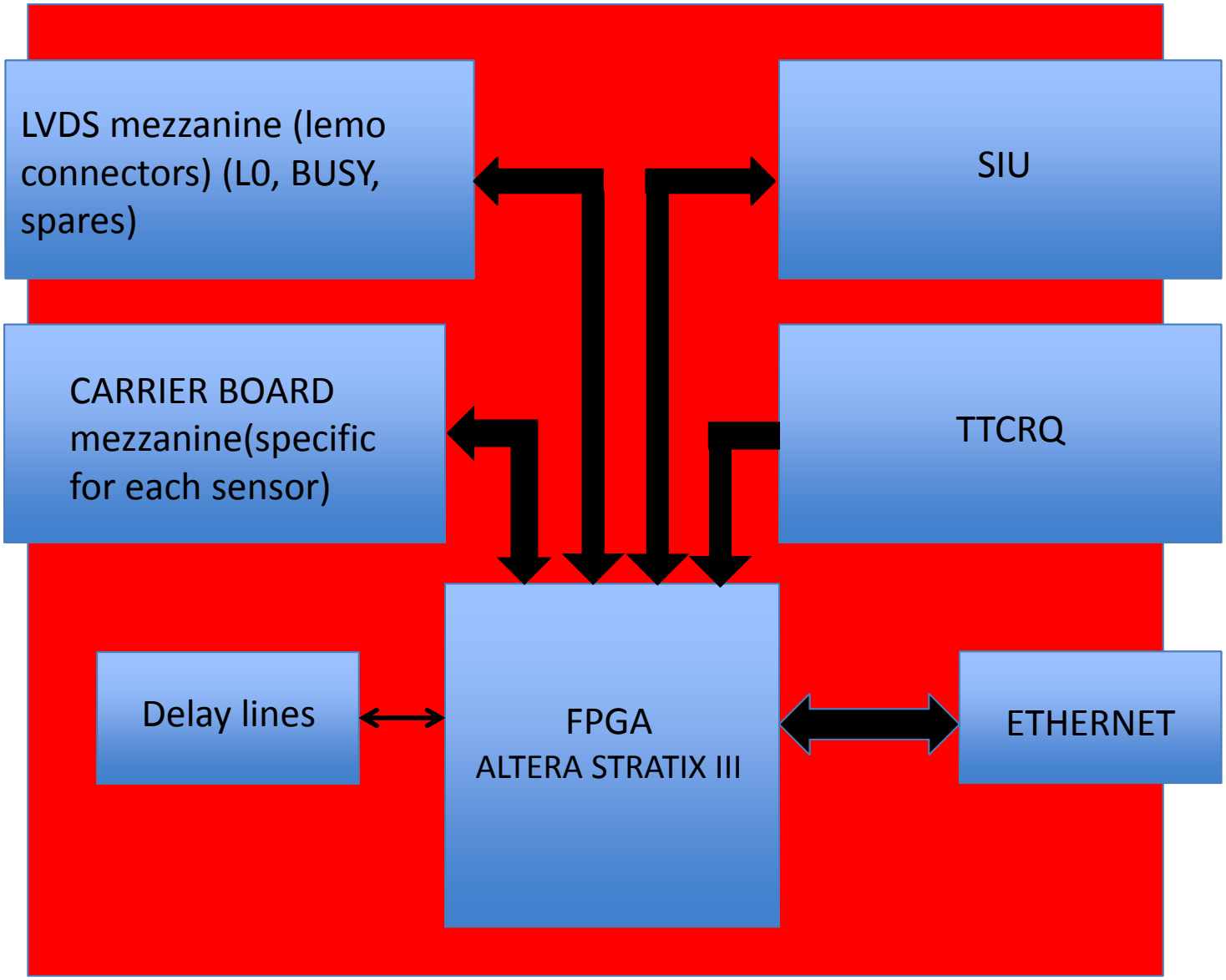
Readout Developments

Gianluca Usai/Cagliari

- Development of a pixel readout system for lab and testbeams
- Based on developments done for ZDC in ALICE
- Develop and implement interfaces on mezzanine cards to create fully versatile system for different frontend chips
- Maintain full compatibility with ALICE DAQ
- First prototypes in development (>>July 2011)

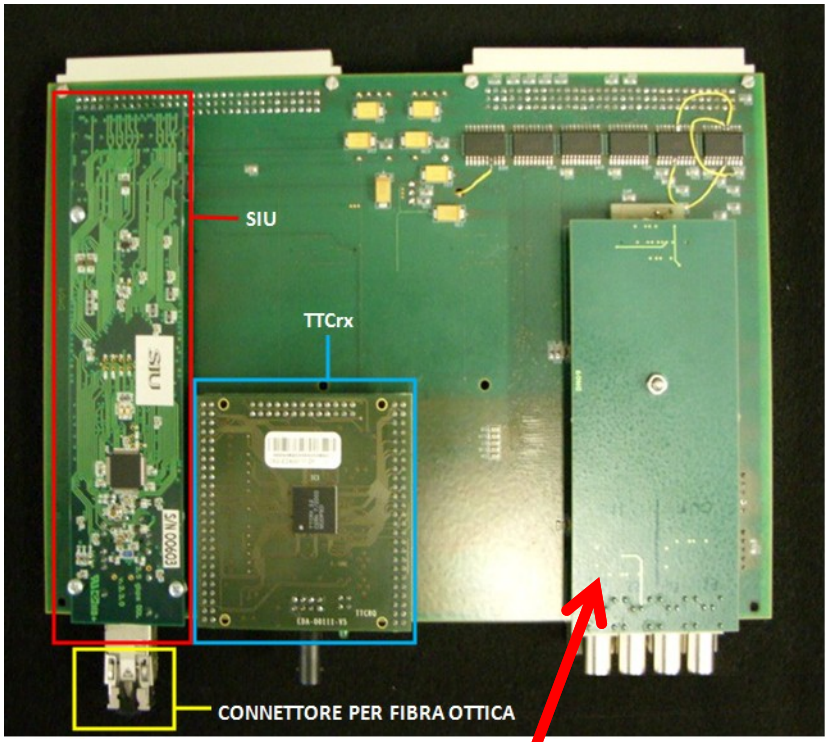
Interfaces implemented on mezzanine cards

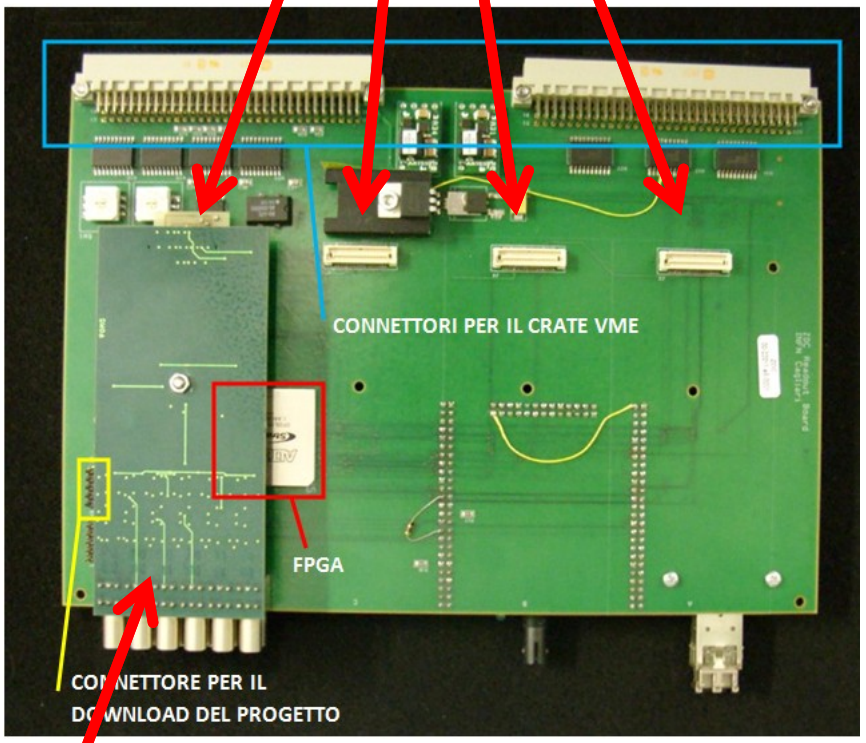
Gianluca Usai/Cagliari



Gianluca Usai/Cagliari

4 mezznine connectors available on this side

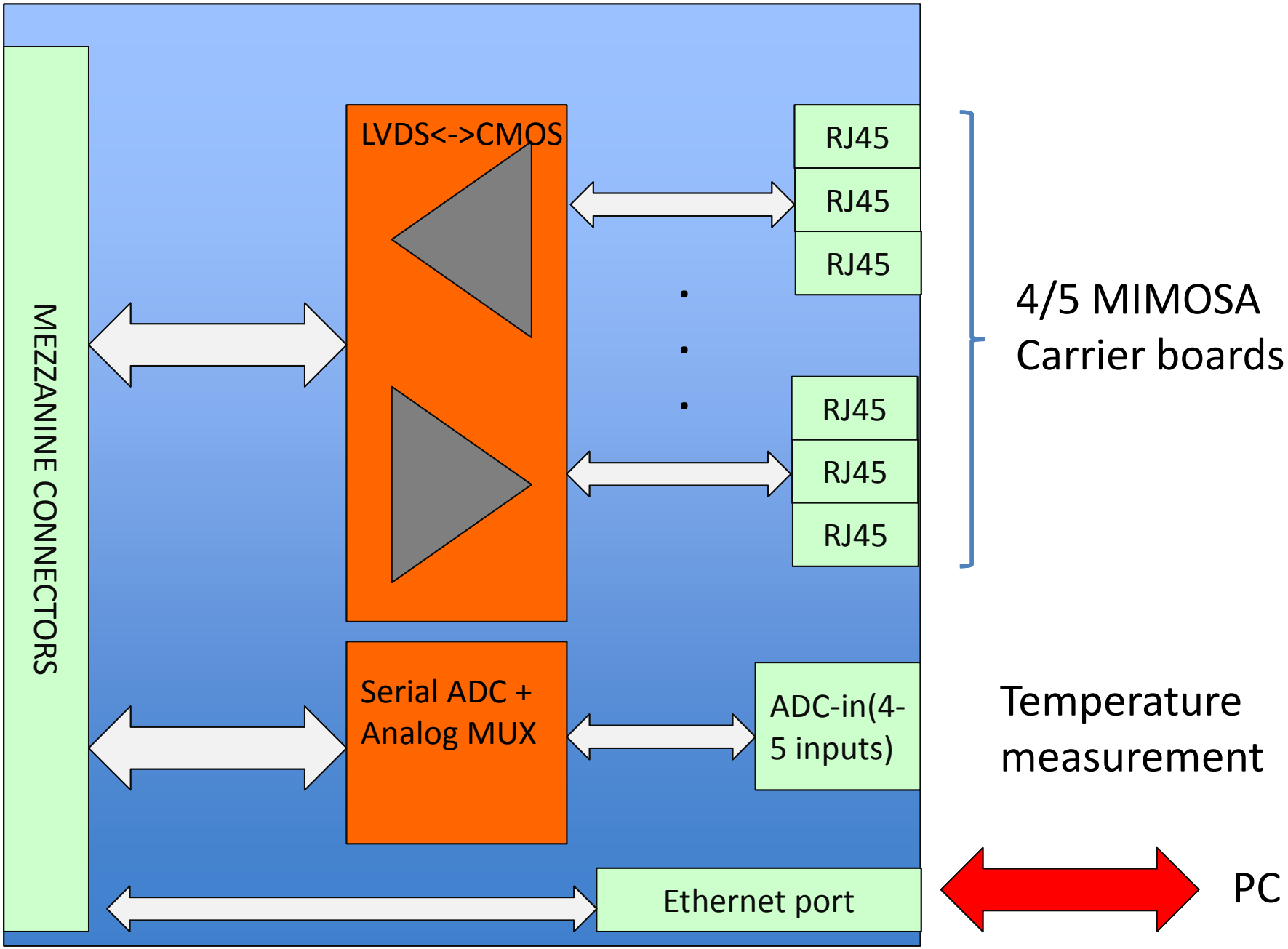




NIN mezzanine

LVDS mezzanine
(can be moved on the othe side
in place of the NIM
Mezzanine)

Interface mezzanine that interface with the mimosa chip carrier boards



Testing Plans 2011

- TPAC study and irradiation tests
  - X-ray irradiation (setup at CERN)
  - Hadron irradiation (various facilities accessible)
  - SEU tests (e.g. in Louvain)
- Testbeam in autumn 2011
  - Test of monolithic sensors
  - Test of edgeless epi hybrid pixels with thin chips
- Evaluation of thin dummies and later thin assemblies
  - SEM, pull tests, radiography, metrology measurements