TECHNOLOGIES FOR STRIP DETECTOR ITS UPGRADE - 29.5.2011

G. Contin

Outline

- Aims of the strip upgrade
- The present ALICE strip detector (SSD)
- Proposal for a new sensor design
- Ideas for the detector layout
- Micro-cables for interconnections
- ASIC specifications and development
- Plans for assembly tests

Aims of the strip upgrade

- Cover a large area on the outer (2-4) ITS-upgrade layers
  A. 2 layers (present SDD) ~ 1.3 m^2
  B. 4 layers (present SDD &SSD) ~ (1.3 + 5) m^2
- Manage higher multiplicity with low occupancy
  - even at small radius (15 cm) to replace SDD
- Provide tracking information with good resolution
  - Spatial resolution: at least 20 μm ($r\varphi$), 800 μm (z) as the present SSD
  - Connect tracks to TPC
- Provide dE/dx for an improved PID
  - over a dynamic range 0-15 Mip (for light nuclei & low mom. part.)
  - with 0.1 Mip resolution (to separate different particle types on a wide P_t range)

The present ALICE strip detector

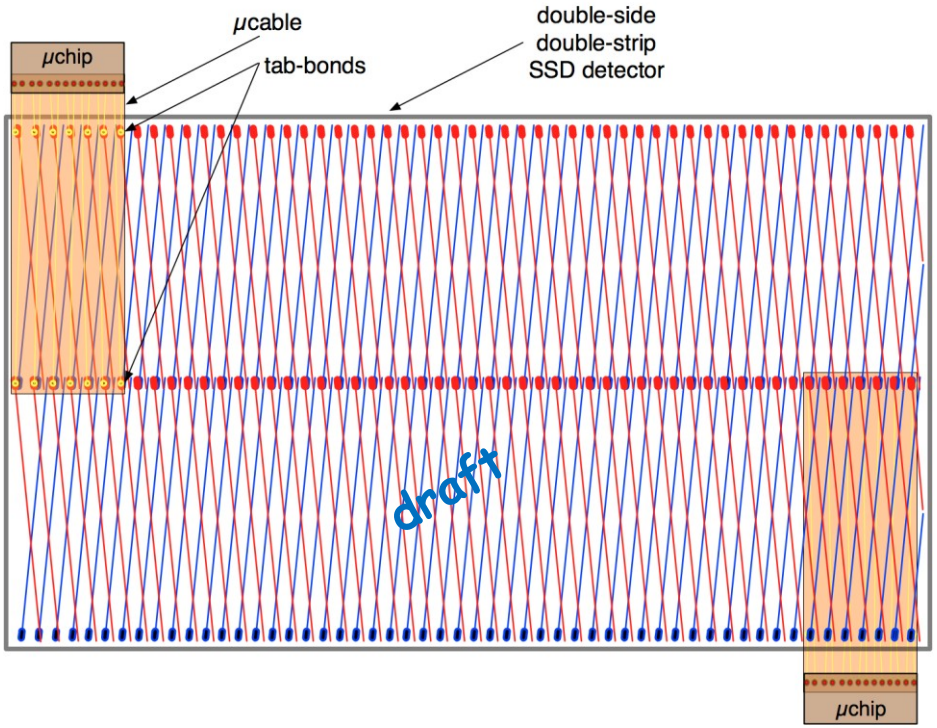
- The SSD detector
  - Overall dimensions: L x d ~ 1 m x 1 m A = (2.2 + 2.8) m^2
    - Layer 5: r = 38 cm ± z = 43.1 cm
    - Layer 6: r = 43 cm ± z = 48.9 cm
  - Acceptance coverage $|\eta| < 0.9$
  - 144 *half-ladders* - 1698 *modules* - 2.6 M *channels*
- The sensor
  - Layout: 300 µm thick, double-sided, 768 strip/side, 35 mrad stereo angle
  - Sensor area: 0.0028 m^2
  - Achieved spatial resolution: 20 µm ($r\varphi$) - 800 µm (z)
- The Front-End chip
  - HAL25 mixed analogue/digital ASIC designed in 0.25 CMOS process
  - 128 channels with preamp, shaper, storage capacitor
  - Input dynamic range: ± 14 MIP with good linearity
  - 1.4 – 2.2 µs adjustable peaking time
  - Signal sampled by external Hold and read-out through analogue multiplexer
  - Serialized samples are then AC decoupled to multiplexer/buffer and driven to ADC

R&D for the ALICE strip upgrade

- Start from the present strip technology which is optimized for the present experimental conditions
- Improve the strip system to meet the new ITS upgrade requirements (*occupancy, acquisition rate, time resolution, extended PID, data format, ...*)
- Benefit from the past experience to get better reliability and uniformity of components

Strip sensor layout

- The new strip sensor layout is being designed (Trieste group)
  - decrease the strip **length from ~40mm to 20mm**
  - cell size ~ -50%
  - C_{strip} ~ -50%
  - 2 x # of channels
  - same cluster size

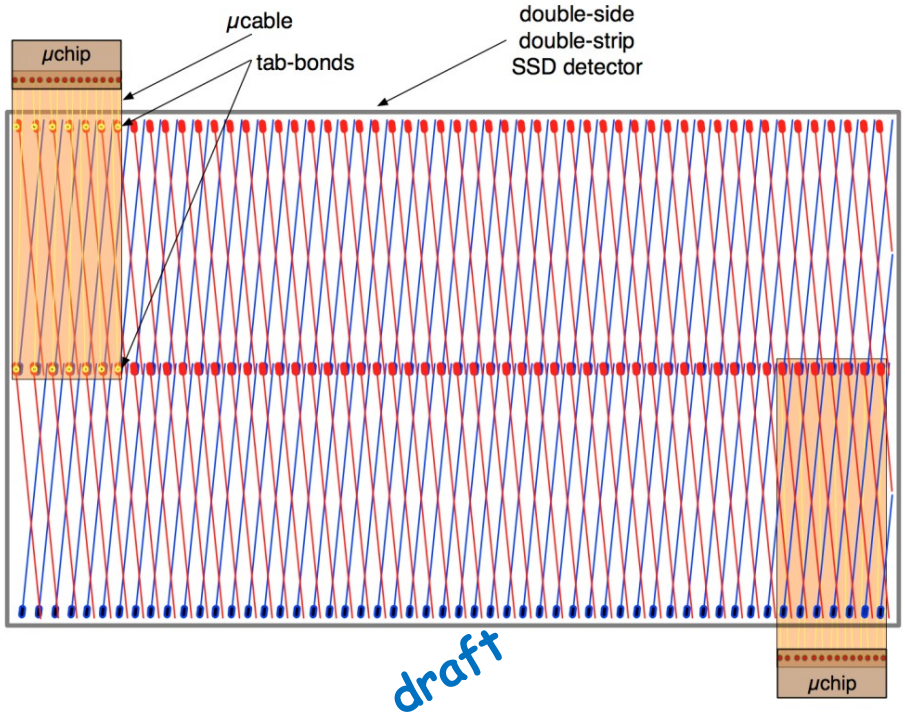


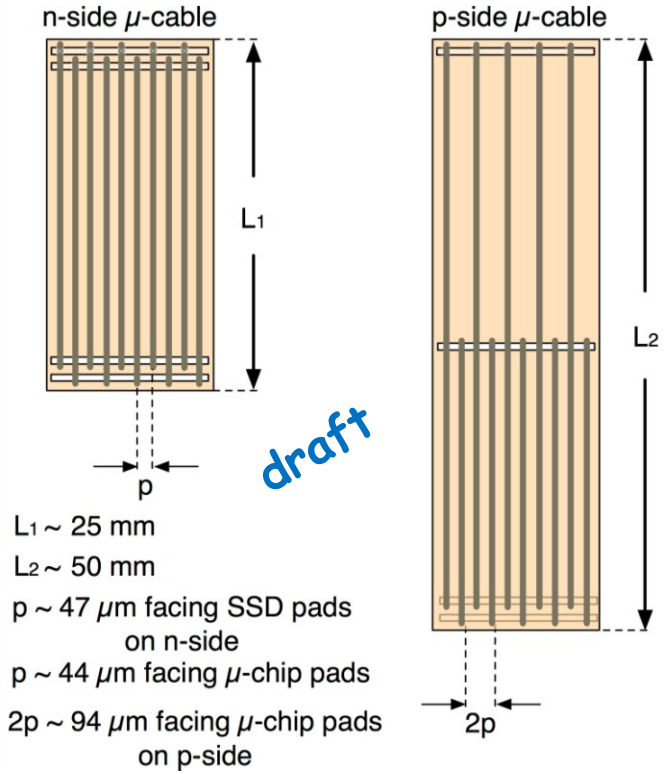
- **2 rows of strips per sensor side**

  occupancy: - 50%
  > ambiguity resolution
  < capacitive noise
  > S/N ratio
  ~ spatial resolution
  < 2 x power consumption

Strip μcables design proposals

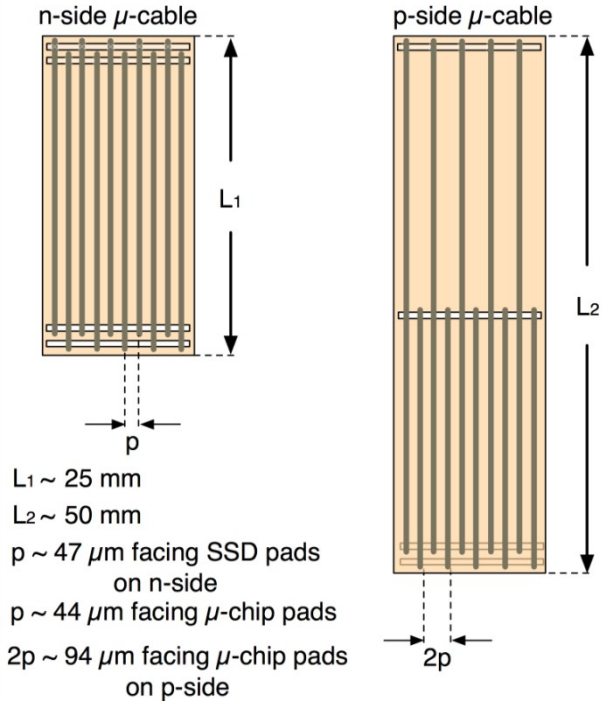
- Double no. of channels requires a new Al-polymide μcable design

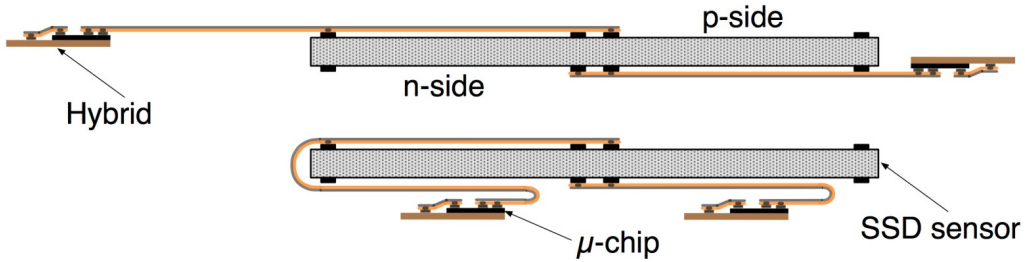




SSD micro-cables

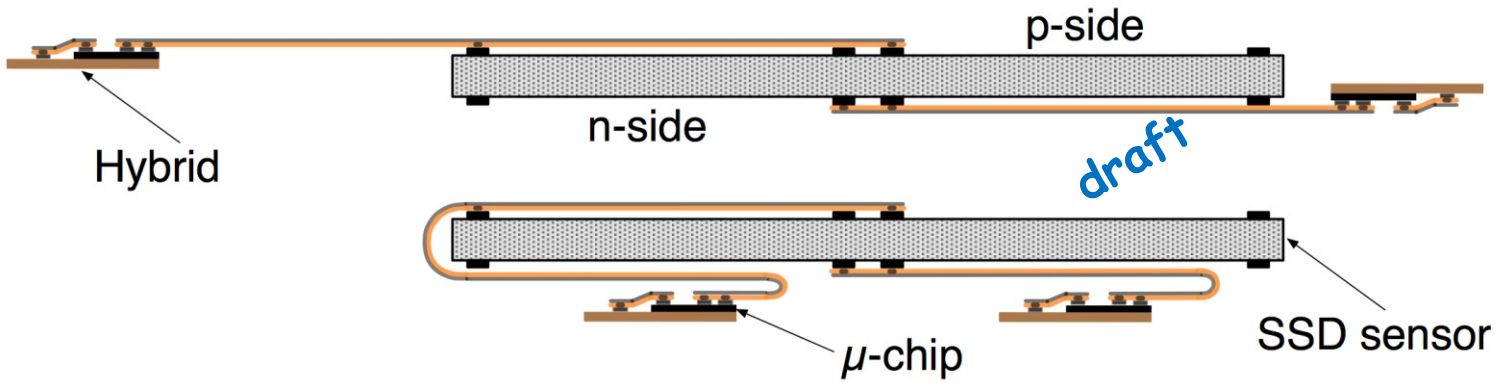
- Specifications:
  - Kapton-Aluminum micro-cables (by Kharkov)
  - Thickness: 10 μm + 14 μm
  - Pitch: 44 μm (chip) / 47.5 μm (sensor)
  - Length: ~ 25 mm / ~ 50 mm
- Assembly and folding
  - TAB bonding technique
  - Bonding windows facing sensor/chip
  - different hybrid layouts for P/N side



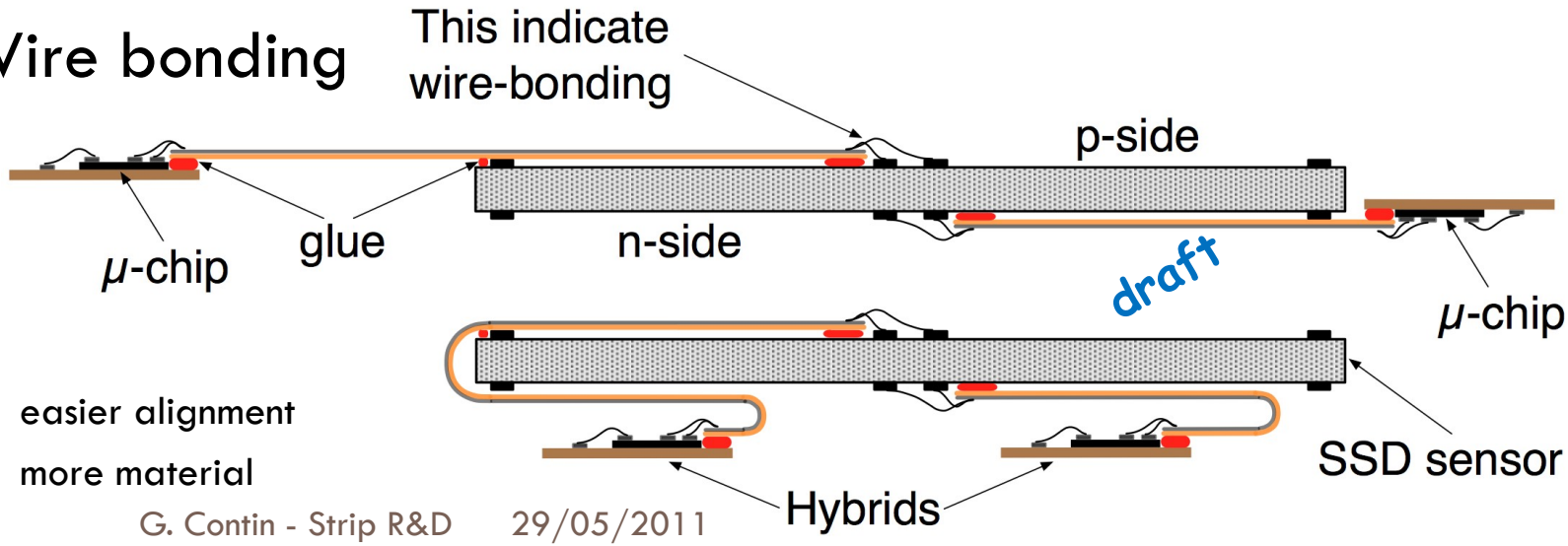


Options for bonding and layout

- TAB bonding technique: allows chip tests, less material, safe folding



- Wire bonding



  - easier alignment
  - more material

SSD interconnections

- TAB bonding: ultrasonic bonding of traces directly on pads
  - Advantages *(wrt wire bonding)*:
    - allows chip tests before assembly
    - less material
    - better planarity for a safer folding
  - Drawbacks for 50 um pitch:
    - narrow traces
    - risk of shorts
- Careful **test** of bonding procedure is required
  - a wafer of dummy chips already sent to Kharkov group:
    - *ALICE128-dummy*: right input pitch as reference for the production of micro-cables prototypes
  - dummy strip sensor mask (new layout) is being designed @ Trieste
  - dummy sensor production foreseen @ FBK-IRST *(by end of summer)*
  - first bonding tests @ Kharkov & Trieste *(by end of 2011)*

ASIC development

- Investigating for available solutions for strip ASIC front-end chip: contacts with UK and CERN Groups
- Specification definition in progress:

ASIC specs	HAL25 (Present SSD)	Upgrade target
CMOS technology	0.25 µm	**0.13 µm** (?)
Input pitch	80 µm	~44 µm On 2 staggered rows (?)
ASIC size	3.65 x 11.90 mm^2	5-6 x 6 mm^2 (?)
Dynamic range	1MeV ~290000 e-	**≳1.3MeV (15 Mip)** ~360000 e-
Charge resolution	~1 keV ~290 e-	**~1 keV (0.1 Mip)** ~290 e-
Noise (ENC for 5 pF load cap.)	< 300 e-	**< 300 e-**

ASIC specifications

ASIC specs	HAL25 (Present SSD)	Upgrade target
Peaking time	1.4 – 2.2 μs	≤1 μs
Readout & Format	Serial, analogue	**Digital** (?)
ADC	Off-detector	On chip (?)
Common Mode correction	Off-detector	On chip (?)
Power dissipation per channel [μW]	<1ms> : 265 - 360 Readout: 680 - 759 Acquisition: 290 – 355	**Less than present**
# channels per chip	128	128
Total # of channels	2.6 M	~1 – 5 M (?)
Expected Dose/Hadron Fluence (10 years)	//	30 kRad (TID) $6*10^{11}$ cm $^{-2}$ (hadron fluence in 1MeV n)

Summary

- The aims of the strip upgrade are well defined
- Clear ideas for the detector layout
- Strip sensor design in progress
- Solutions for interconnections being studied
- Front-end ASIC:
  - specs definition ongoing
  - looking for partners to develop the chip
- Tests with dummy components are planned to evaluate the assembly feasibility

Thank you for your attention…