



Status and efficiency of the 400 kW Solid-State Power Amplifier at 352 MHz for the European Spallation Source (ESS)

PRESENTED BY BRUNO LAGOGUEZ ON BEHALF OF THE PROJECT TEAM

2024-09-25

Agenda



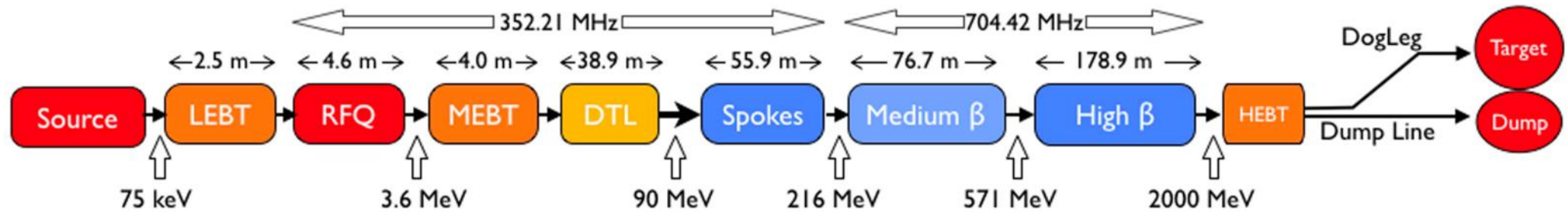
1. Background and Project Motivation
2. Technical Background
3. Planning and Direction
4. Efficiency consideration
5. Work in Progress and Summary



Background and Project Motivation



Background and Project Motivation



Spoke Power Stations

- 26 Stations in total
- 52 high power, high frequency tetrodes
- Power stations have suffered with a variety of reliability and technical challenges
- Many technical challenges have been resolved however the use of tetrodes, with a single supplier, is still considered a significant risk

Risk reduction

ESS initially picked klystrons as an alternative however this was changed to SSPA technology
Key motivators:

- New klystron development needed
- Risk of single supplier
- Power and frequency is in range of SSPA
- Review of commercial (technical and cost), in house development and continuation of Uppsala development carried out

ESS SSPA station goals:

High Level Goals:

Build on and extend technical solution developed at Uppsala

Cost effective (< 3 EUR/W)

Designed for high availability

Achieve a scalable design for high volume production

Key Technical Goals

400 kW capable for ESS pulse parameters

Designed to be a plug compatible with existing Spoke power stations

Compatible with exiting footprint and support structures.

Uppsala University

- Uppsala has worked on SSPA technology development for approx. 10 years.
- Received funding for part of the hardware of the first 400 kW unit.

ESS Approved funding for Technology Demonstrator

- Project timeline 2 years



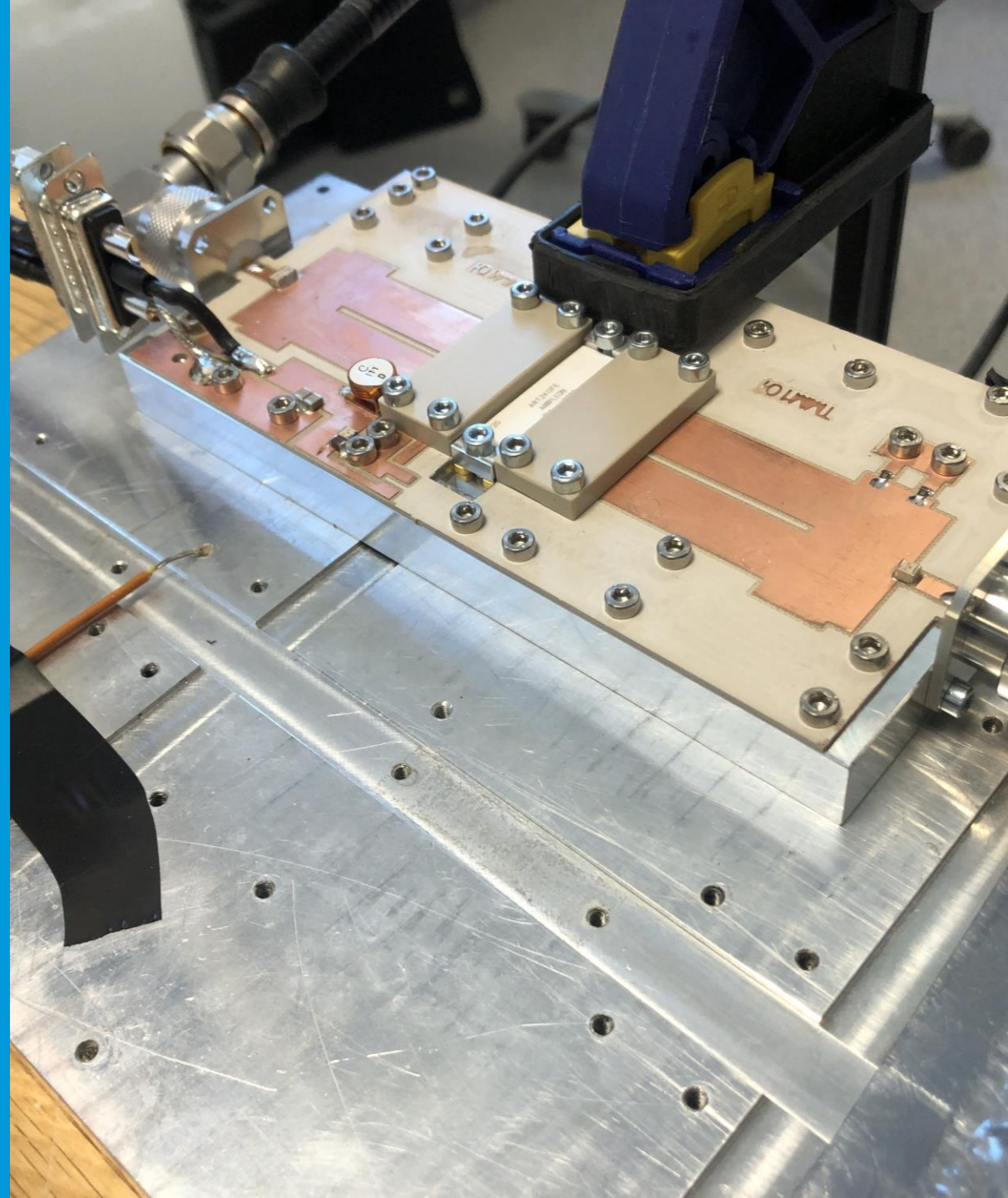
UPPSALA
UNIVERSITET



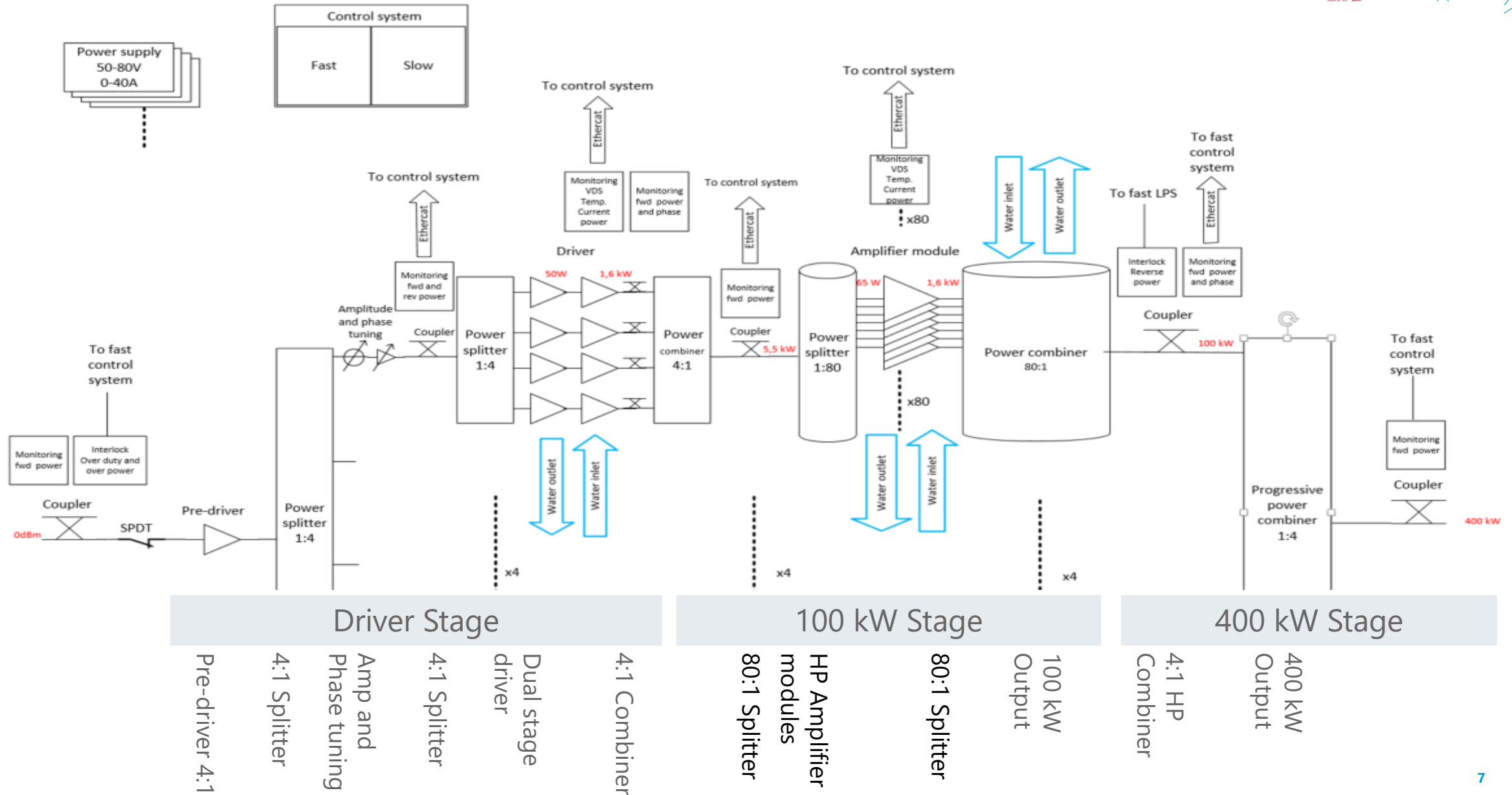
Key Specifications

Operating frequency	352.21 MHz
-1 dB bandwidth	$\geq \pm 1$ MHz
Peak output power, Max.	400 kW
RF pulse width	Up to 3.5 ms
Minimum RF Pulse Width	140 μ s
Repetition rate	Up to 14 Hz
Gain	≥ 88 dB
Nominal RF Drive	-2 dBm
Harmonic content	< -30 dBc
Spurious and sideband in ± 20 MHz	< -60 dBc
Input/output impedance	50 Ω
Input VSWR	$\leq 1.2:1$
Load max RL	-26 dB
Gain flatness	$\Delta G \leq \pm 2$ dB
Phase flatness	$\leq 15^\circ$ (over 10dB dynamic)

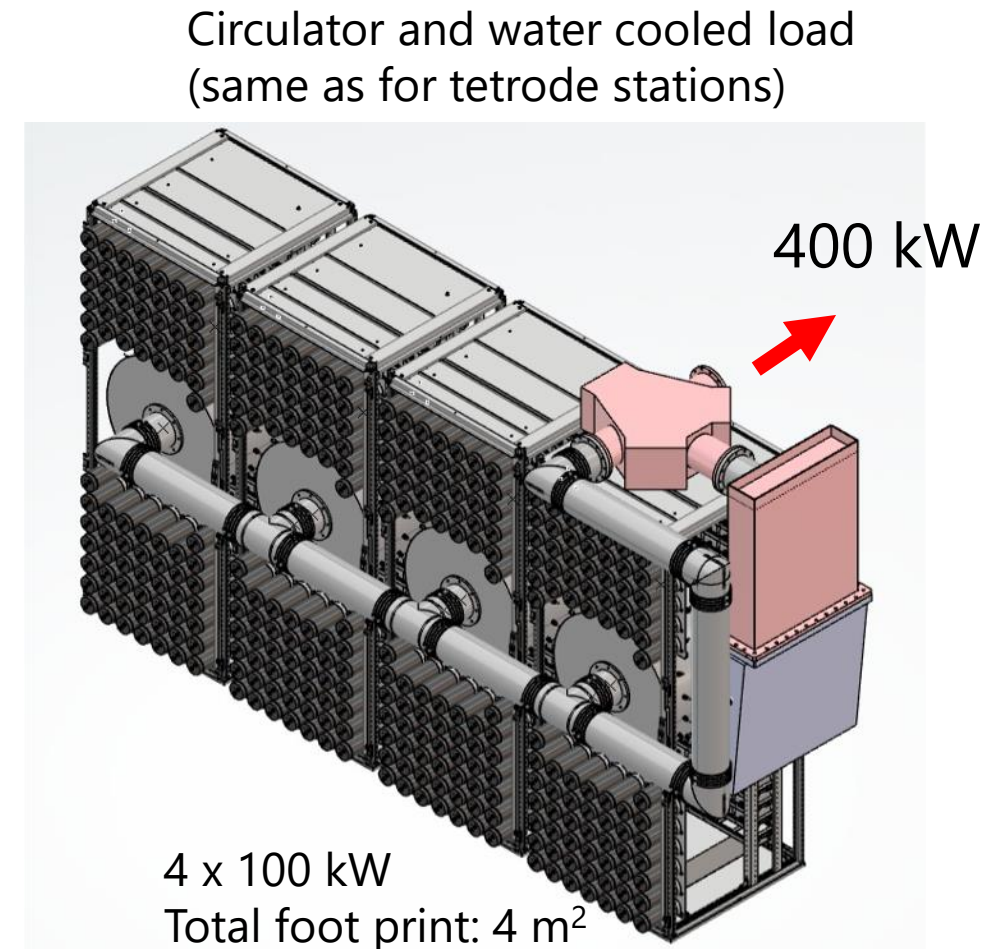
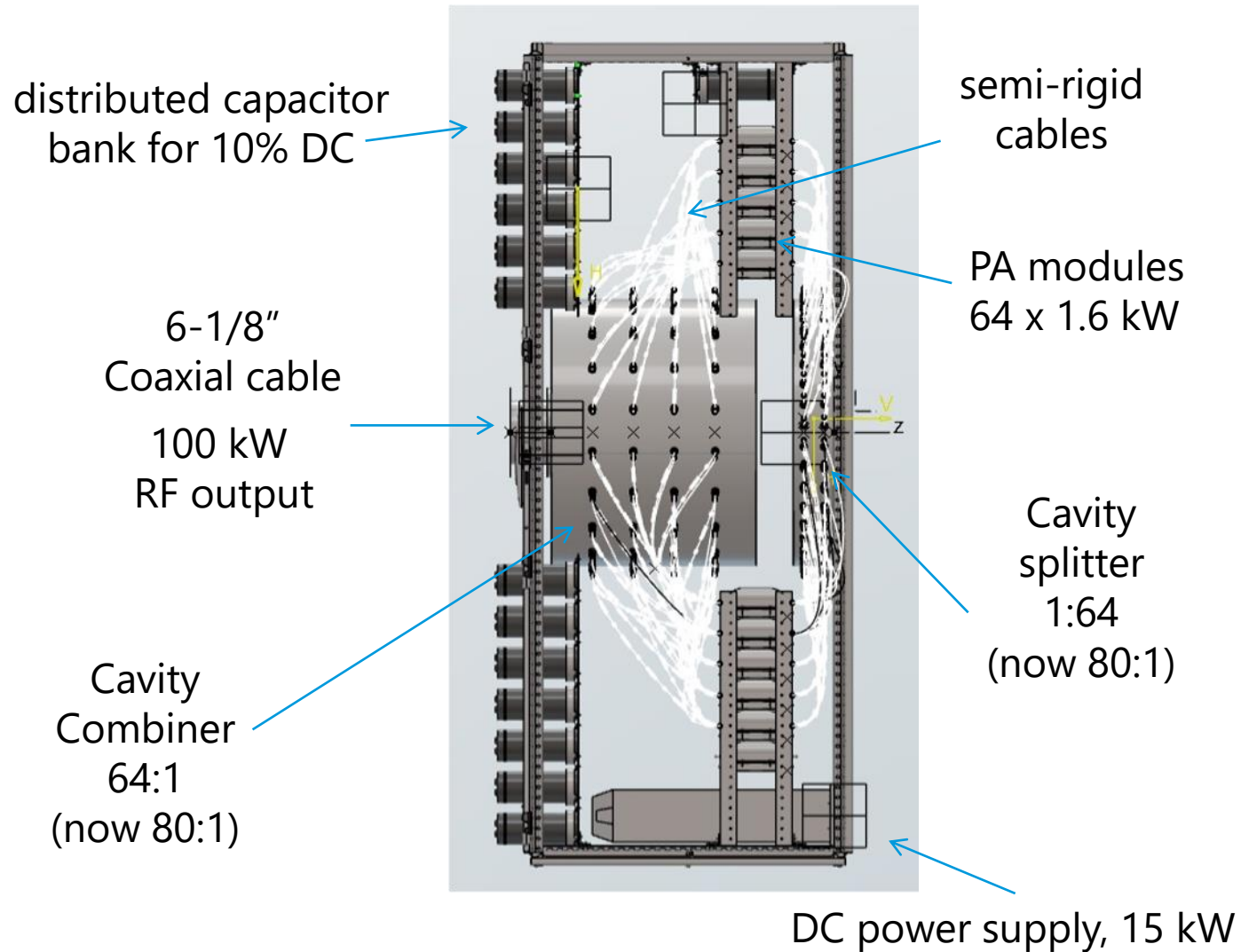
Technical Background



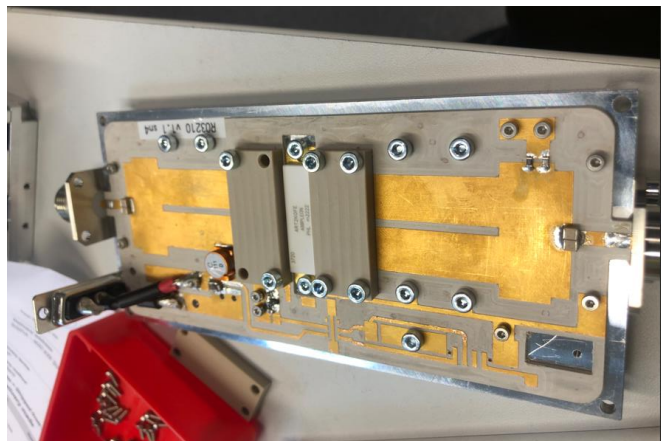
Architecture



SSPA: 400 kW Station at 352 MHz

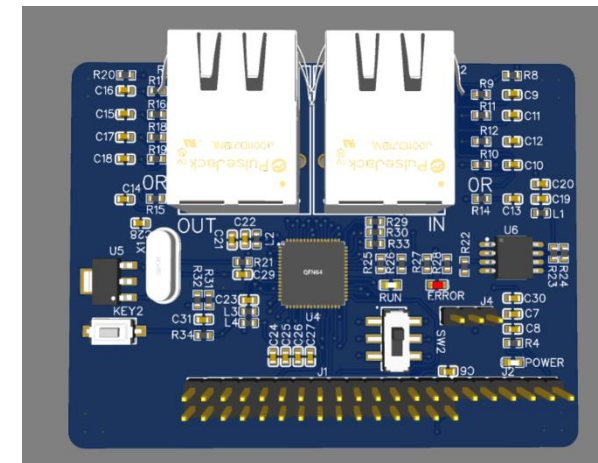


1.6 kW RF Power Amplifier Module (15 manufactured and tested)



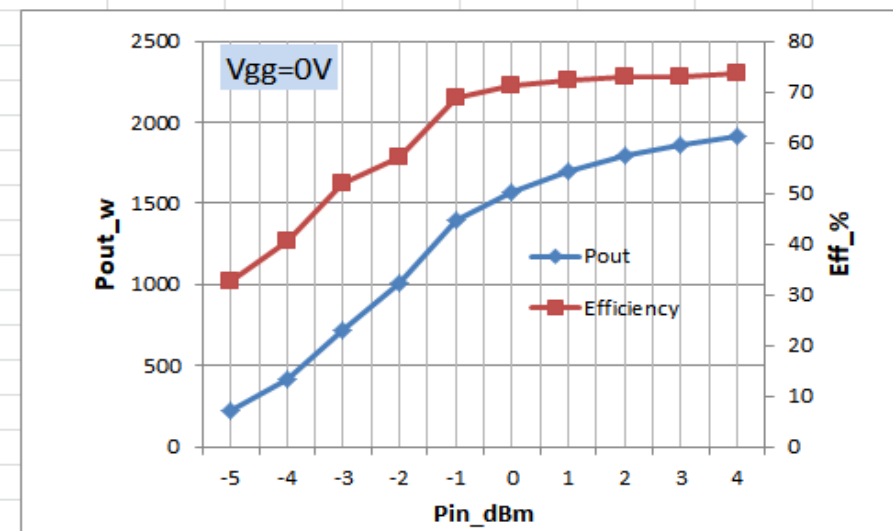
1.6 kW amplifier
←

Control board
→

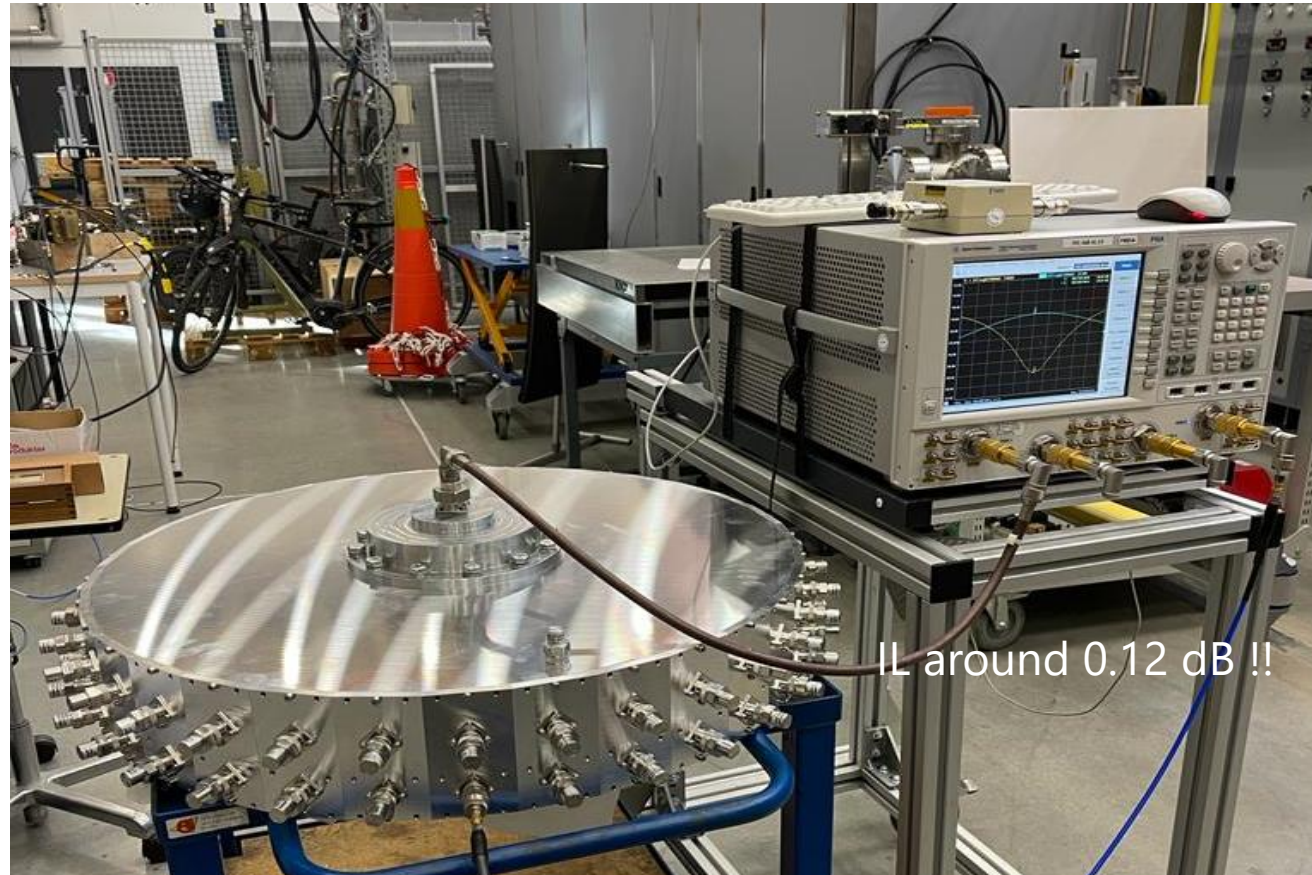


Vdd= 75 Vgg= 0		PRF= 100Hz, 1% Freq= 352MHz	
Pin	Pout_w	Idc_Peak_Amp	Eff_ %
-5	218	8.9	32.66
-4	421	13.8	40.68
-3	716	18.4	51.88
-2	1013	23.6	57.23
-1	1400	27.1	68.88
0	1571	29.4	71.25
1	1700	31.4	72.19
2	1792	32.7	73.07
3	1860	33.9	73.16
4	1917	34.7	73.66

Pout > 1.6 kW
Eff > 72 %



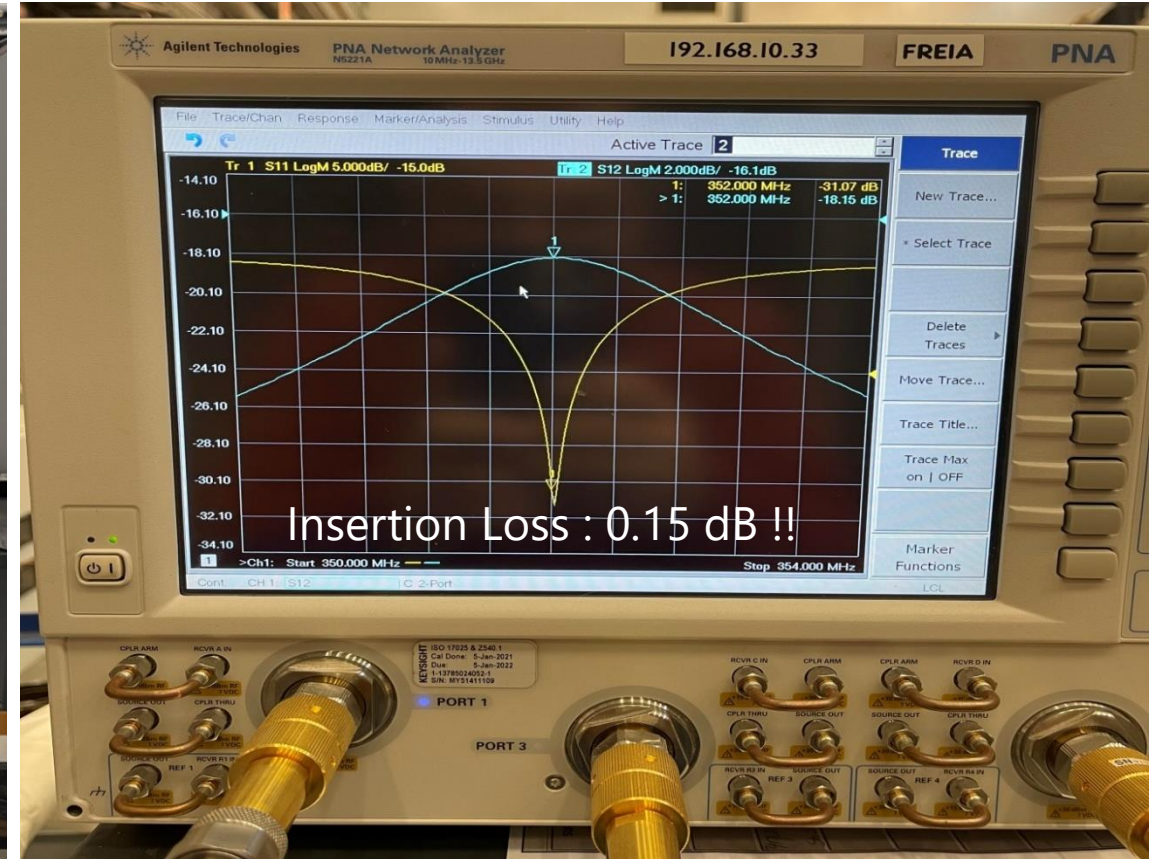
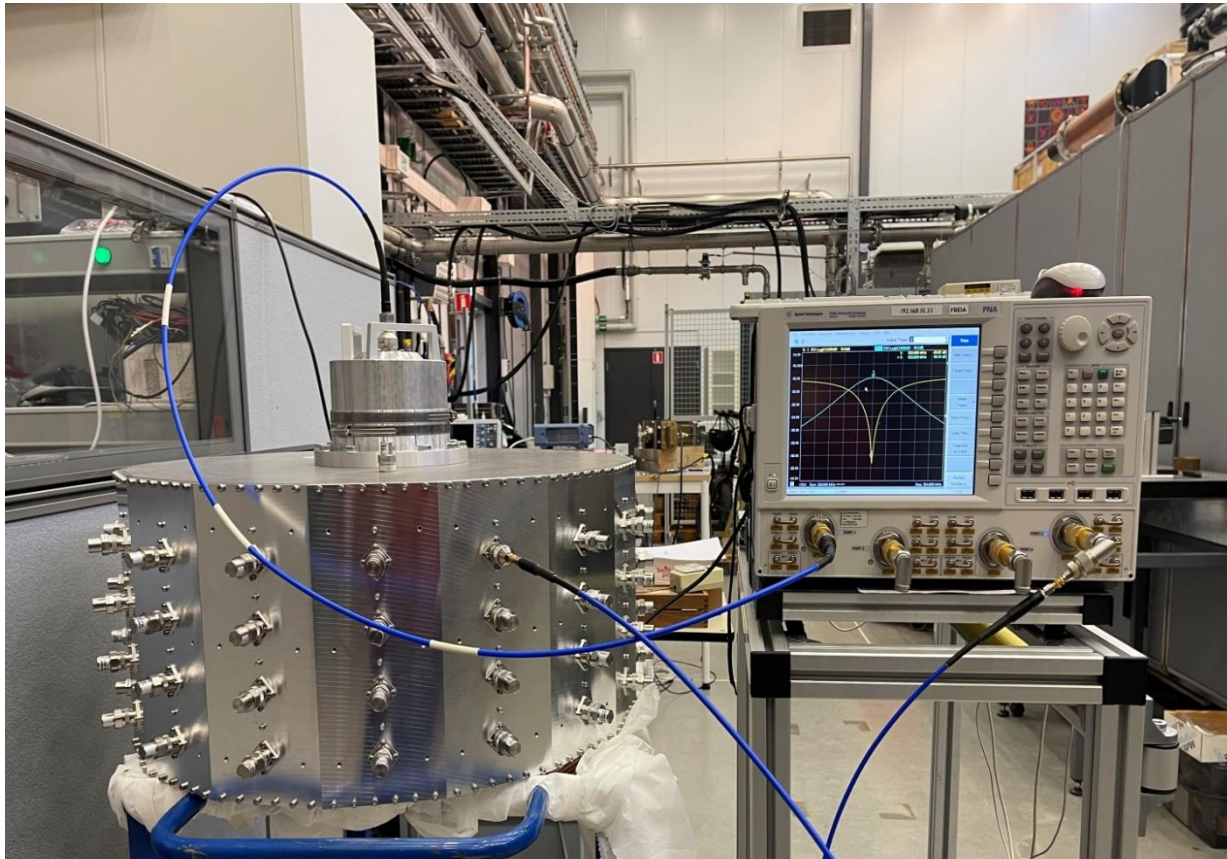
1:64 power splitter (First unit manufactured and tested)



64:1 power combiner - 100-kW (two units manufactured and tested)



UPPSALA
UNIVERSITET



Planning and Direction



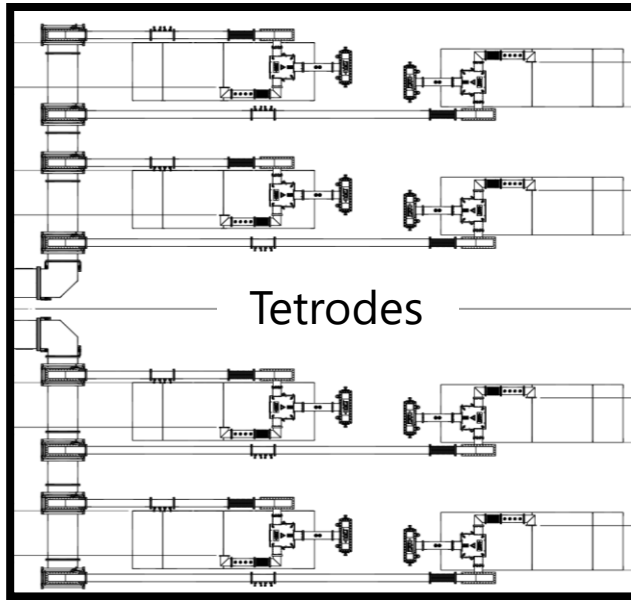
Layout in the Gallery



UPPSALA
UNIVERSITET

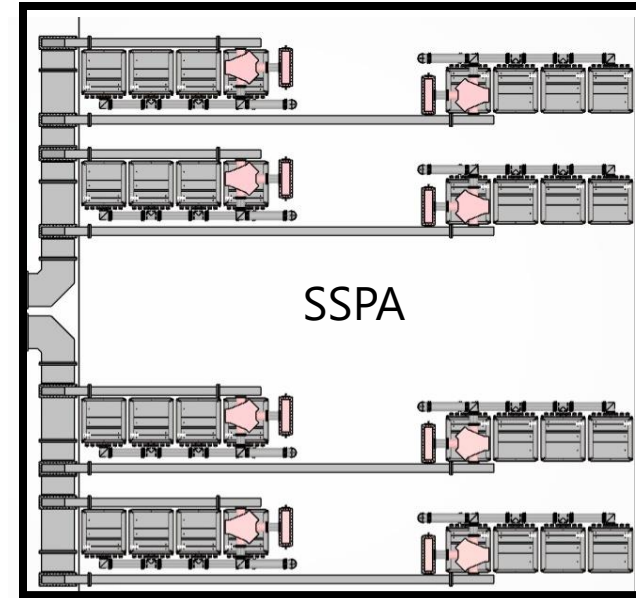
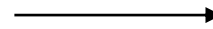


Plan view of
Current Layout
with tetrodes



10m

11m

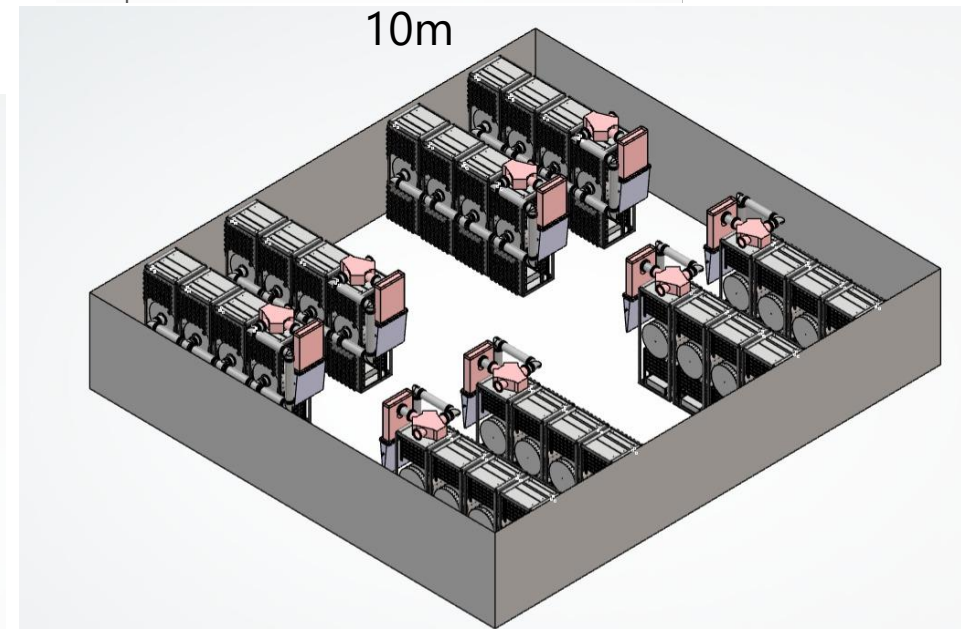
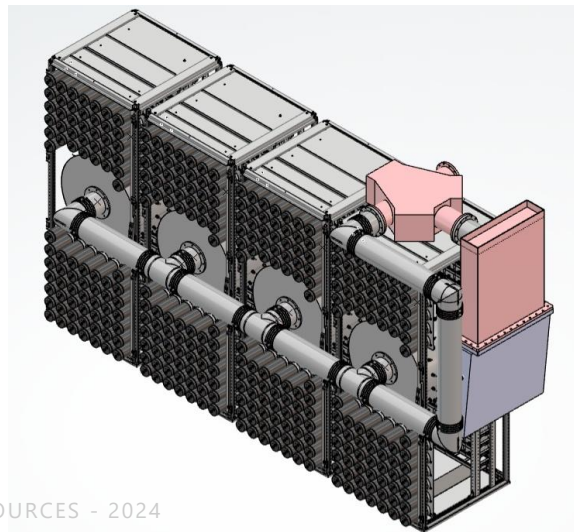


SSPA

11m

Anticipated Layout
with SSPAs

Single 400 kW
unit



10m

Planning



Project formally started February 2024

3 main milestones obtained so far

- 1.6 kW module (tested up to 2 kW)
- Combiner and splitter with 64 inputs
- Combiner qualification at 100 kW

Dec 2024/ January 2025: 100 kW 1st rack

- Order 100 PCBs in September – start by manufacturing in-house RF boards
- Design of the combiner and splitter with 80 inputs in order to start the manufacturing
- Start manufacturing of boxes, cooling plates, and 4:1 splitter in October.

End 2025/ Beg 2026: 400kW prototype

- Successful qualification of the 1st rack (100 kW): March 2025
- Control system HW design done: March 2025

Key Directions and Challenges



UPPSALA
UNIVERSITET



Use of LDMOS for cost, robustness and market availability

Full power/gain budget was reviewed: power per module evaluated at 1600 W to 1850 W.

- 64:1 splitter/combiner cavities changed to 80:1
 - 256 power modules increased to 320.
- 1850 W may be OK but puts the drain voltage out of specification (70 V).
 - Priority on lower risk with option to test at higher power ahead of future production

Current measurement changed to reduce cost

Low cost, on board RF power measurement

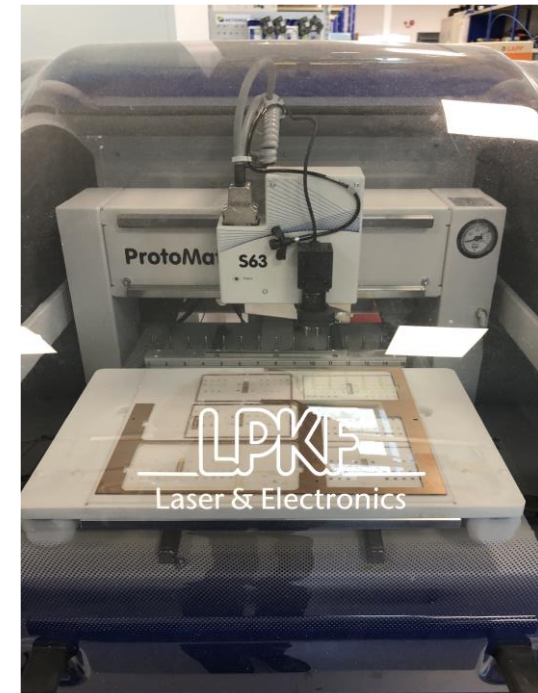
PCBs milled in-house to reduce cost and control risk

Full module, housing, monitoring and controls integrated and designed ease of maintenance

Stepwise soak testing in progress.

New technical developments are considered as opportunities for personal development where it aligns with other ESS technologies

In-house PCB production



Efficiency consideration

Class AB or class C

In operation Module efficiency to consider: 65%

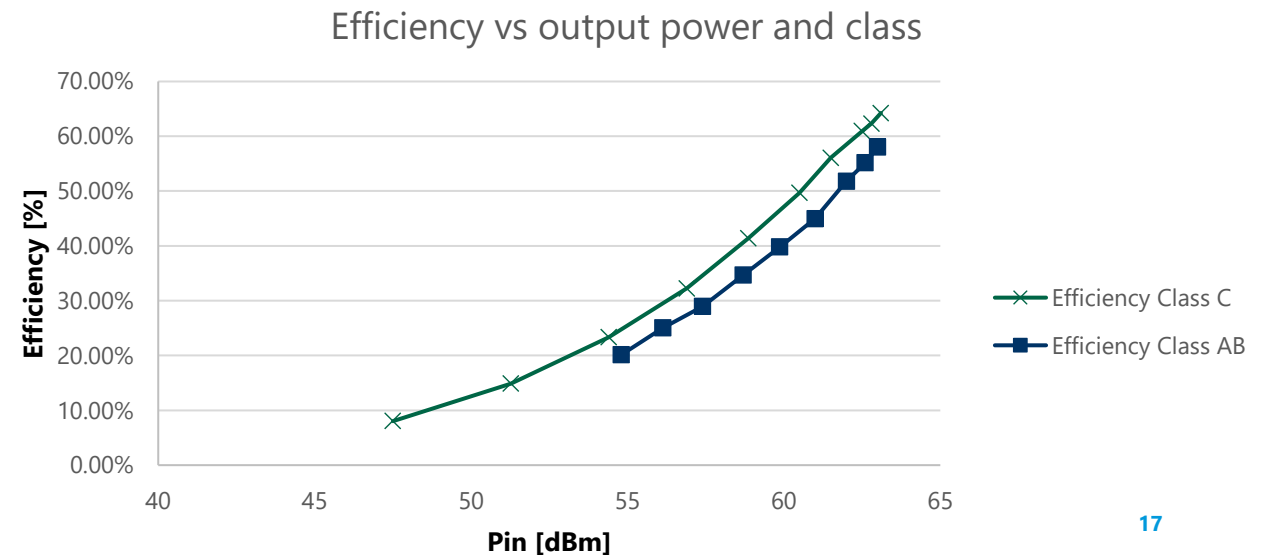
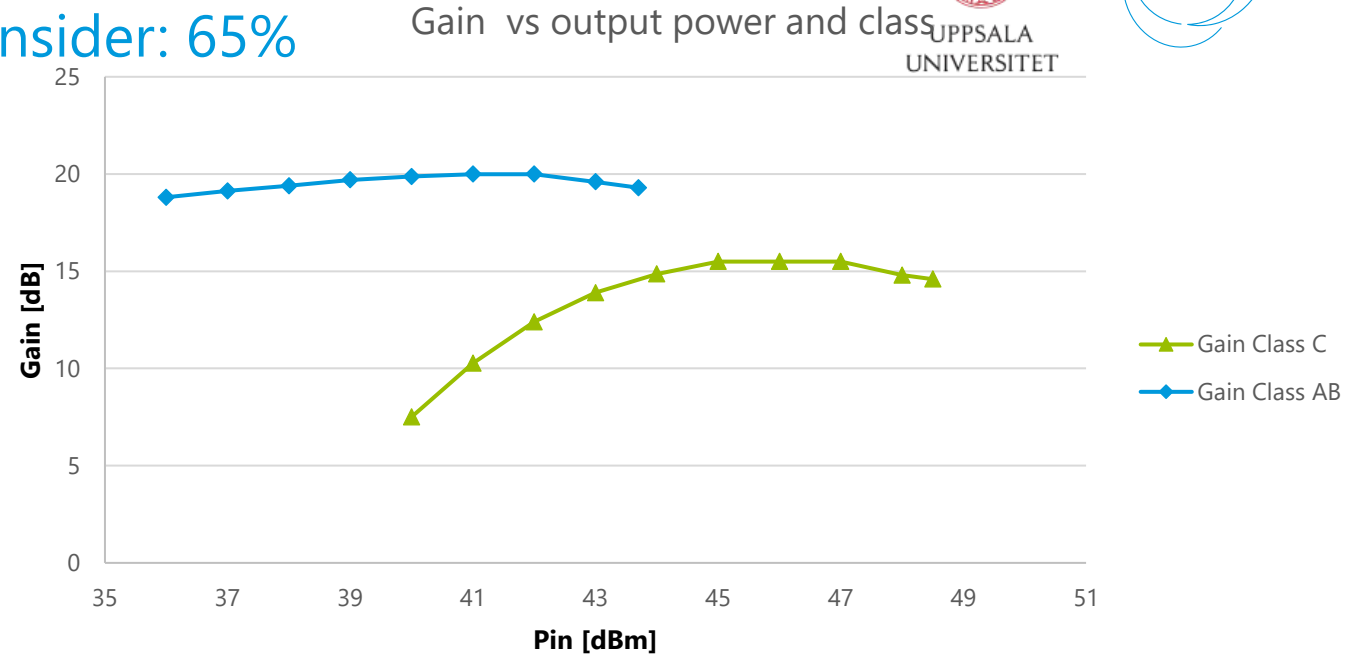


UPPSALA
UNIVERSITET



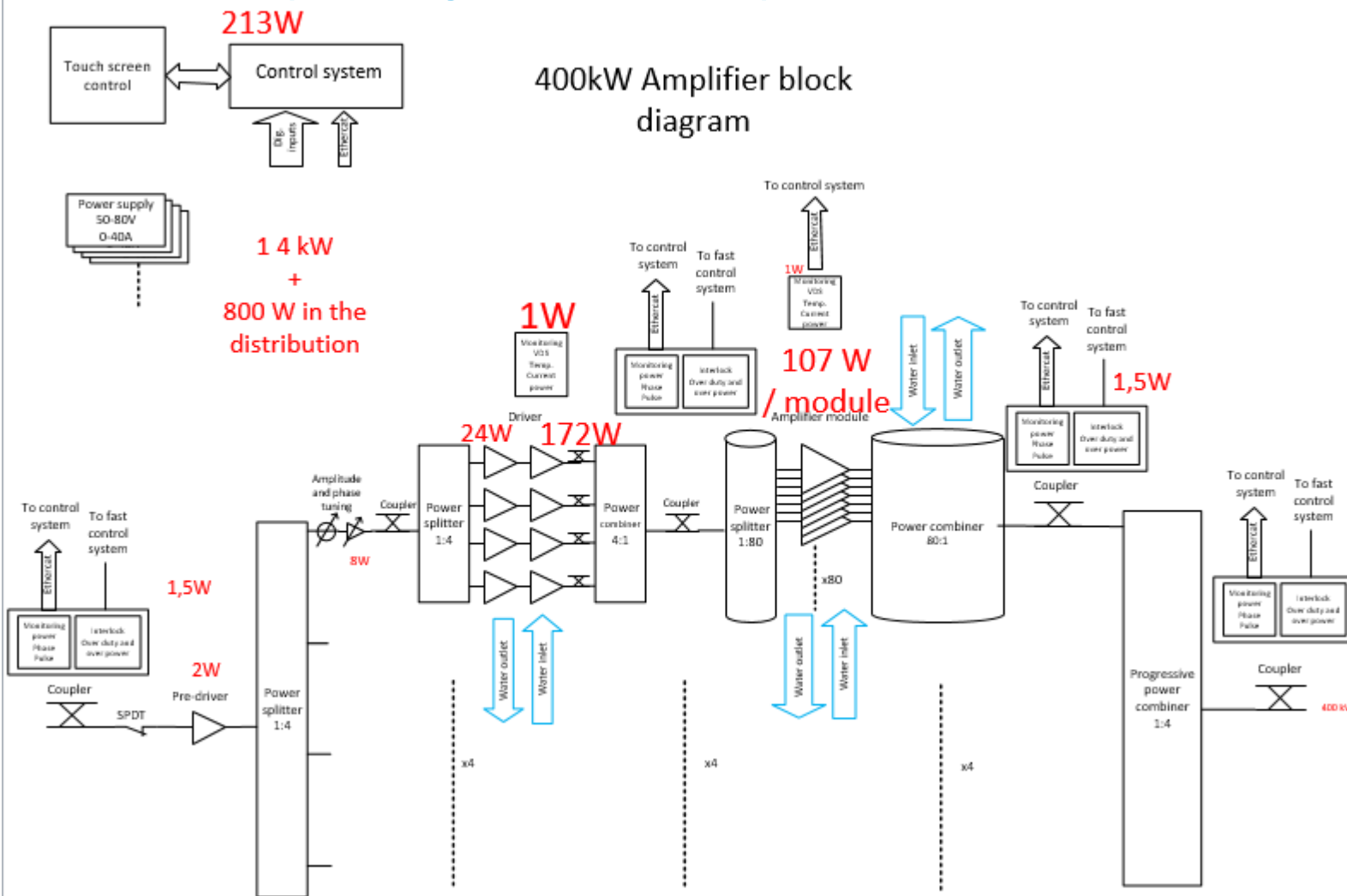
- Class C
- Efficiency ●
 - Linearity ●
 - Gain ●
 - Less components ●
 - Reliability ●

- Class AB
- Linearity ●
 - Efficiency ●
 - Gain ●



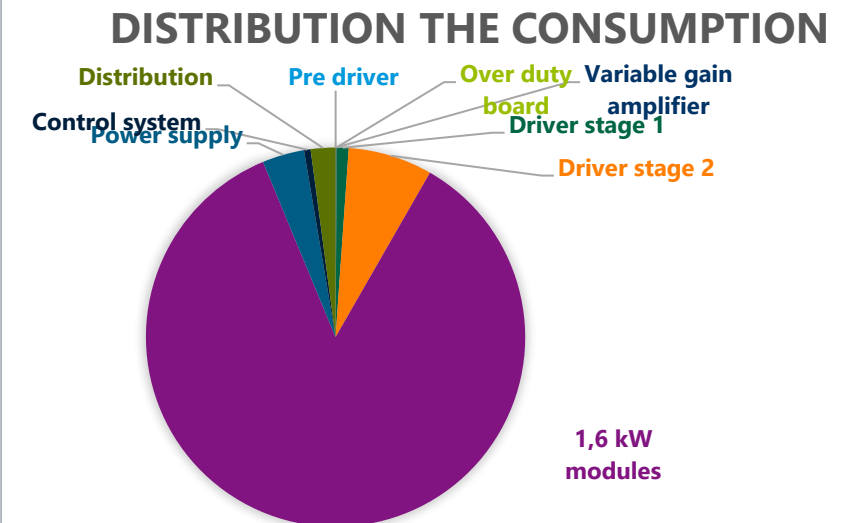
Global efficiency

From power grid to RF output



Loss between the amplifier module and the output are a key point: 0,5dB is 5% on the global eff.

Electrical consumption	Per Unit	nb of Unit	Total	
Pre driver		2	1	2W
Variable gain amplifier		8	4	32W
Over duty board		1,5	4	6W
Driver stage 1		24	16	384W
Driver stage 2		172	16	2752W
1,6 kW modules		102,2	320	32711W
Power supply		4,1	336	1374W
Control system		213	1	213W
Distribution		2,4	336	806W
Total				38280W
Eff				52,2%



Class C or Class B

We need flexibility



UPPSALA
UNIVERSITET



Class C Eff Module: 65%

Electrical consumption	Per Unit	nb of Unit	Total
Pre driver	2	1	2W
Variable gain amplifier	8	4	32W
Over duty board	1,5	4	6W
Driver stage 1	24	16	384W
Driver stage 2	172	16	2752W
1,6 kW modules	102,2	320	3271 W
Power supply	4,1	336	1374W
Control system	213	1	213W
Distribution	2,4	336	806W
Total			38280W
Eff			52,2%

Class AB Eff Module: 55%

Electrical consumption	Per Unit	nb of Unit	Total
Pre driver	2	1	2W
variable ampi	8	4	32W
over duty	1,5	4	6W
driver syage 1	24	4	96W
driver stage 2	121,4	4	486W
1,6 kW module	121,4	320	38864 W
power supply	4,9	324	1574W
control system	213	1	213W
distribution	2,4	324	778W
Total			42050W
Eff			47,6%



Work in Progress



Rack Layout



UPPSALA
UNIVERSITET



Rack layout with 80 modules

It will be challenging to get the cables in place.

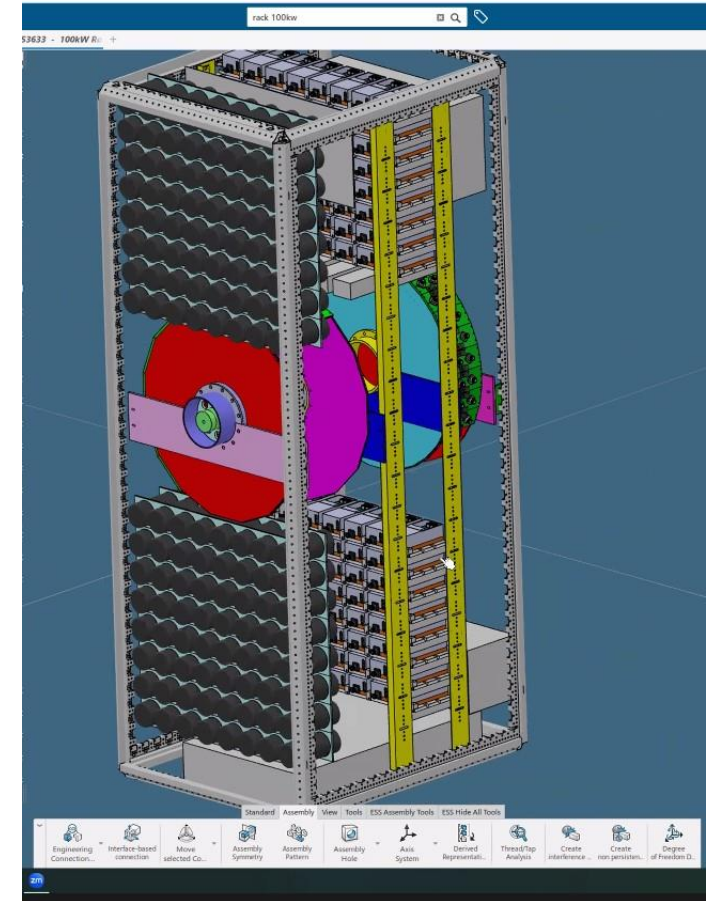
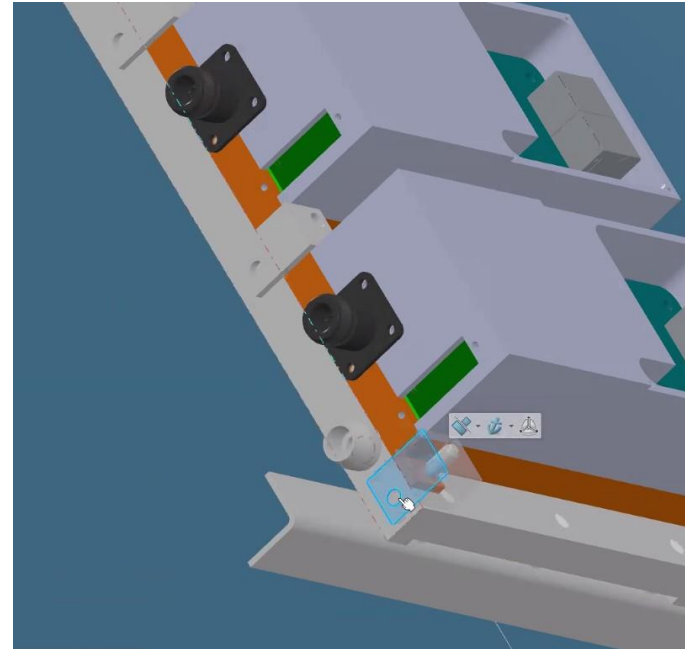
Cooling plate design in progress

Design of the heat sink and box for the module - completed

Working on an easy solution to get the module in and out for easy repair

Investigation with 128 modules (not yet possible)

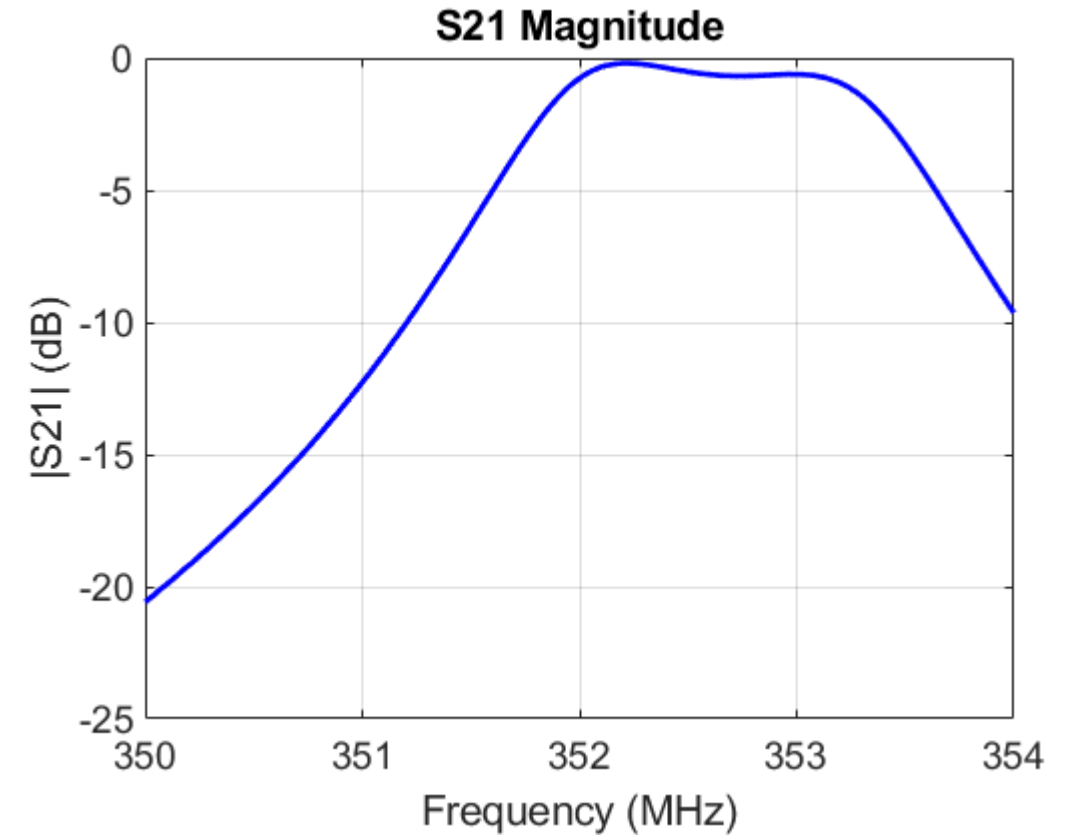
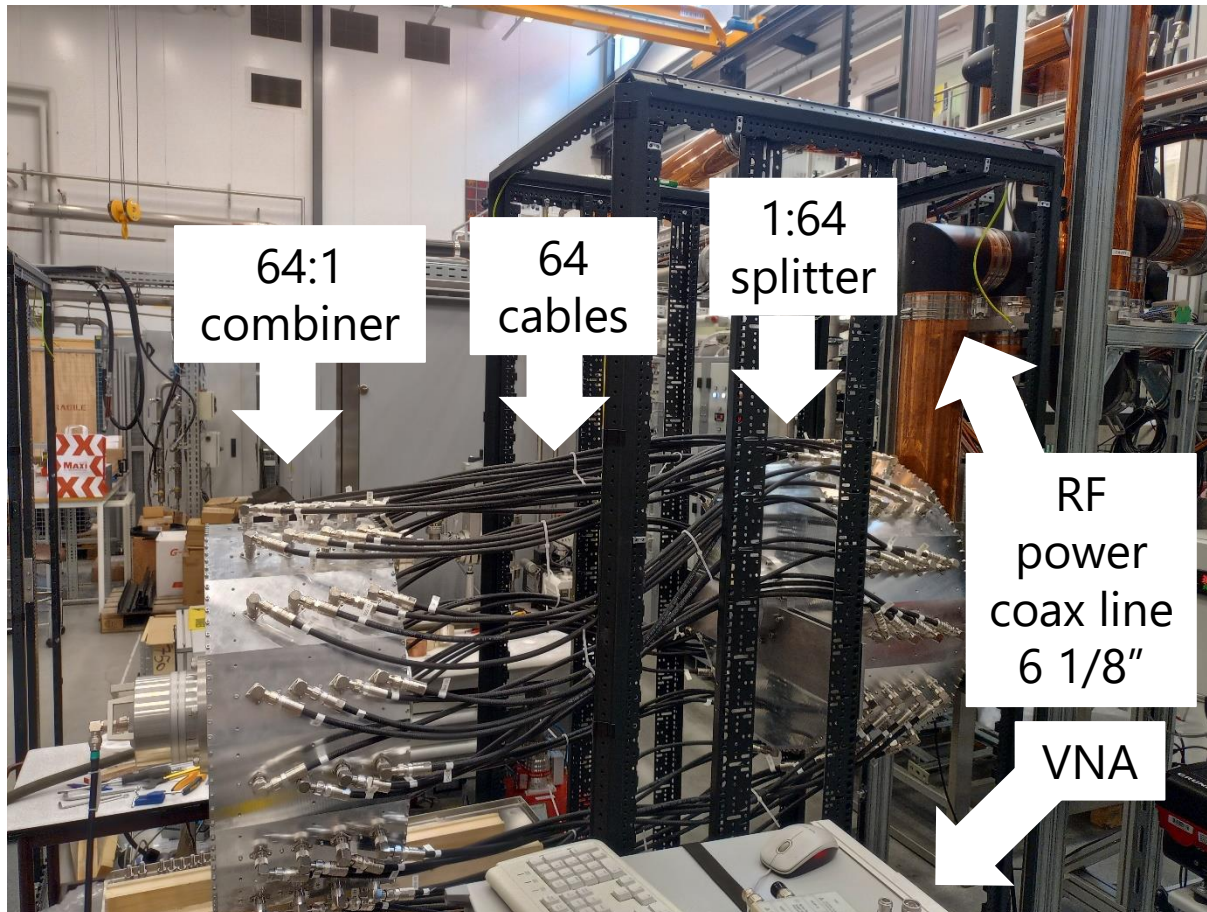
- Would allow doubling of power per rack



Back to back combiner test: low power



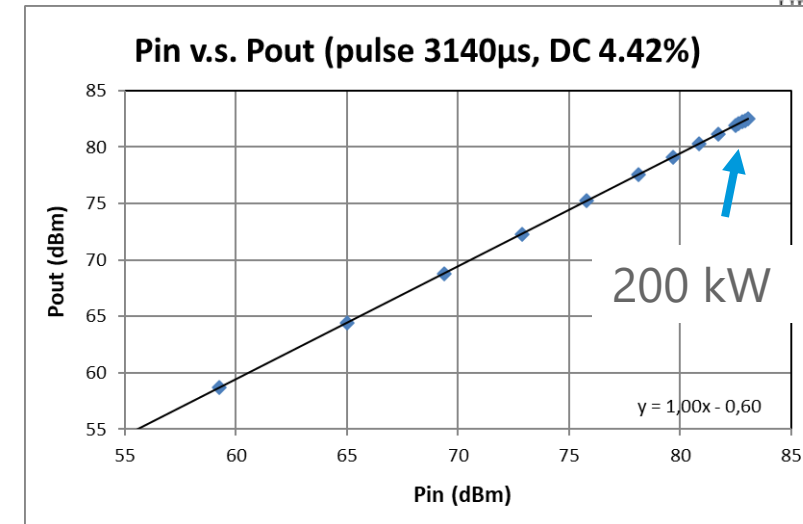
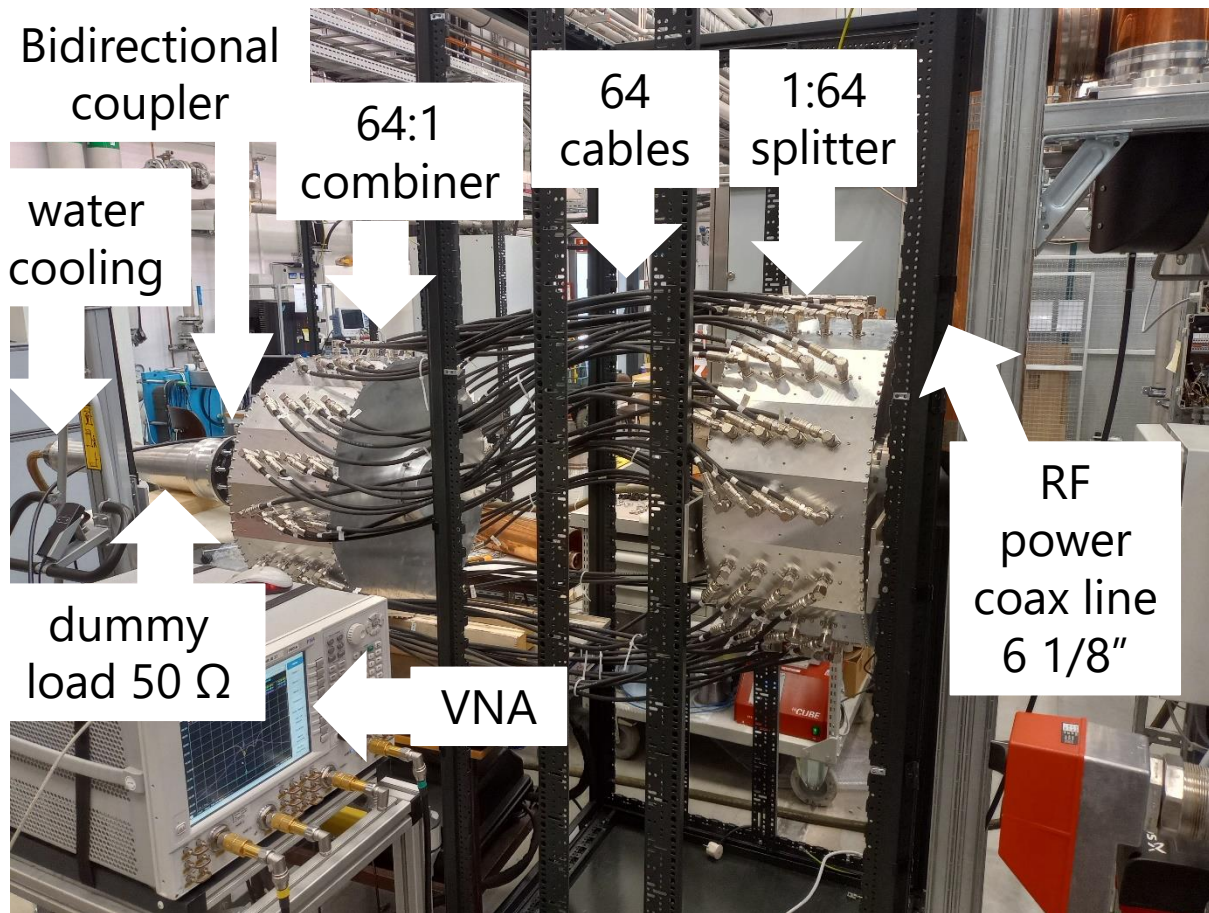
UPPSALA
UNIVERSITET



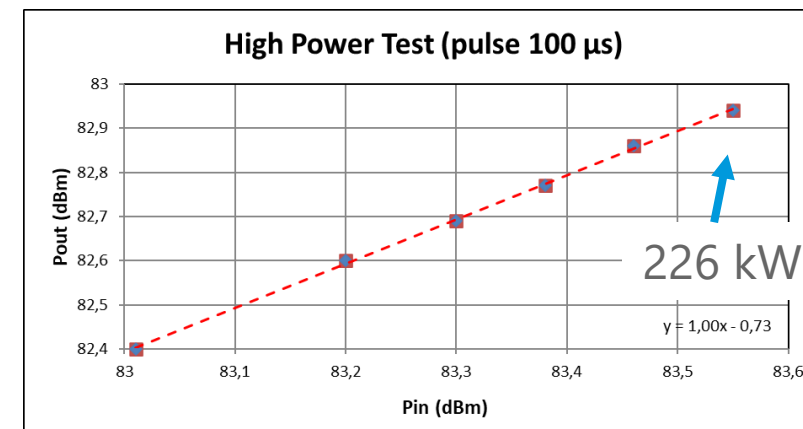
IL = 0.3 dB (calibrated: i.e. wo cables, connectors, etc.)

Back to back combiner test: high power

Verification of High Power Output Coupler



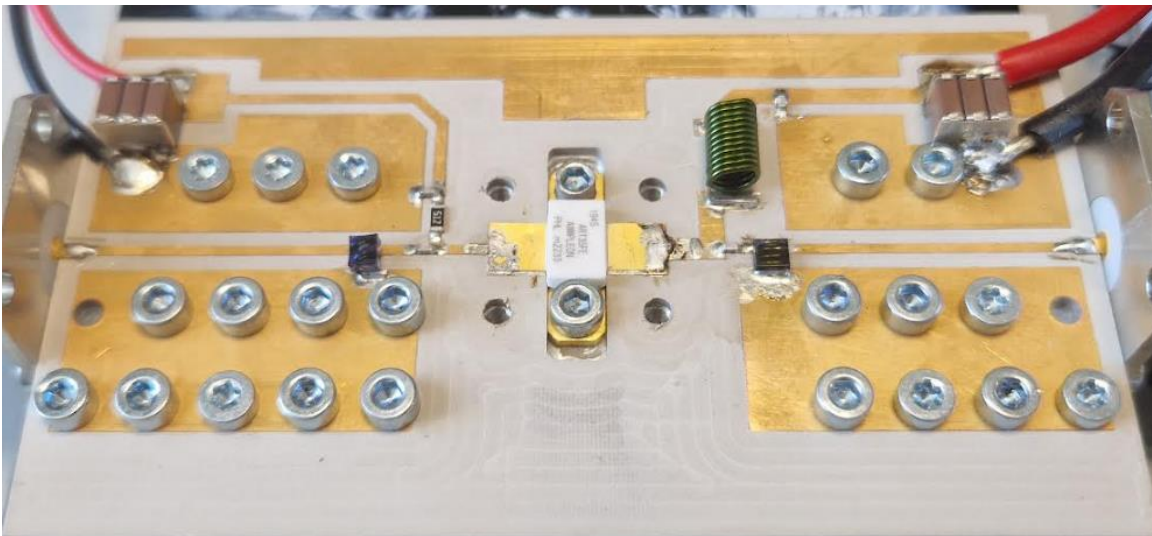
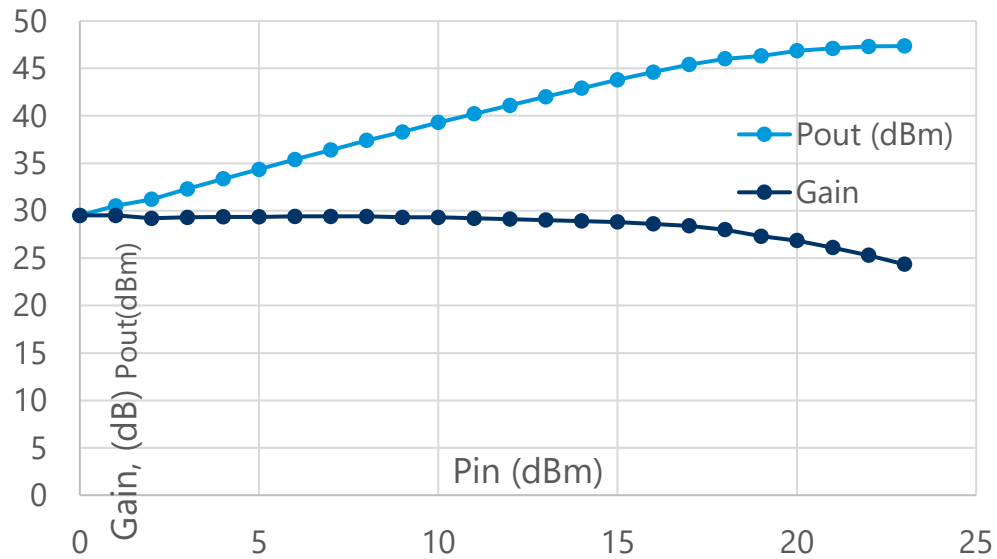
IL = 0.58 dB
(with cables, connectors, etc.)



IL = 0.61 dB
(with cables, connectors, etc.)

Test successfully carried out to 220 kW without incident. (100 kW is required)

Driver 50W based on LDMOS ART35FE

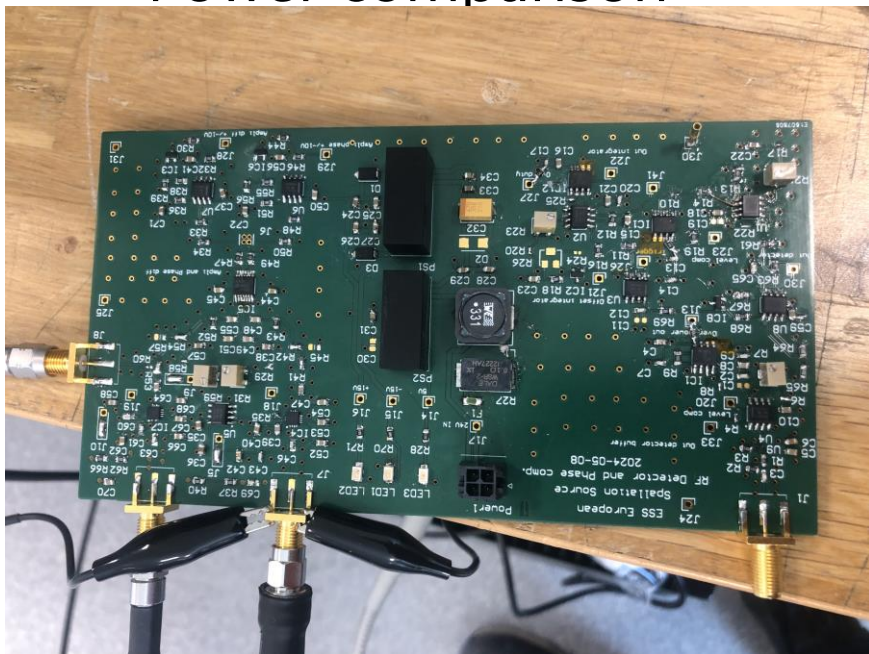


Design Parameters	Specifications	Simulation Results	Measurements
Operational frequency	352.21 MHz	352.21 MHz	352.21 MHz
Gain at nominal power 50 W output	27 dB min	27.1 dB	26.85 dB
Efficiency	>50%	65%	62%
Input/output impedance	50 Ω	50 Ω	50 Ω
Gain flatness (over 10dB dynamic)	$\Delta G \leq \pm 0.5$ dB		$\Delta G : +/- 1,6$ dB
2 nd , 3 rd Harmonic content	<-30 dBc	-20 dBc -26 dBc	-20 dBc -26 dBc
Input VSWR	$\leq 1.12:1$	1.07:1	1.12:1
Output VSWR	$\leq 1.12:1$	3:1	3.5:1

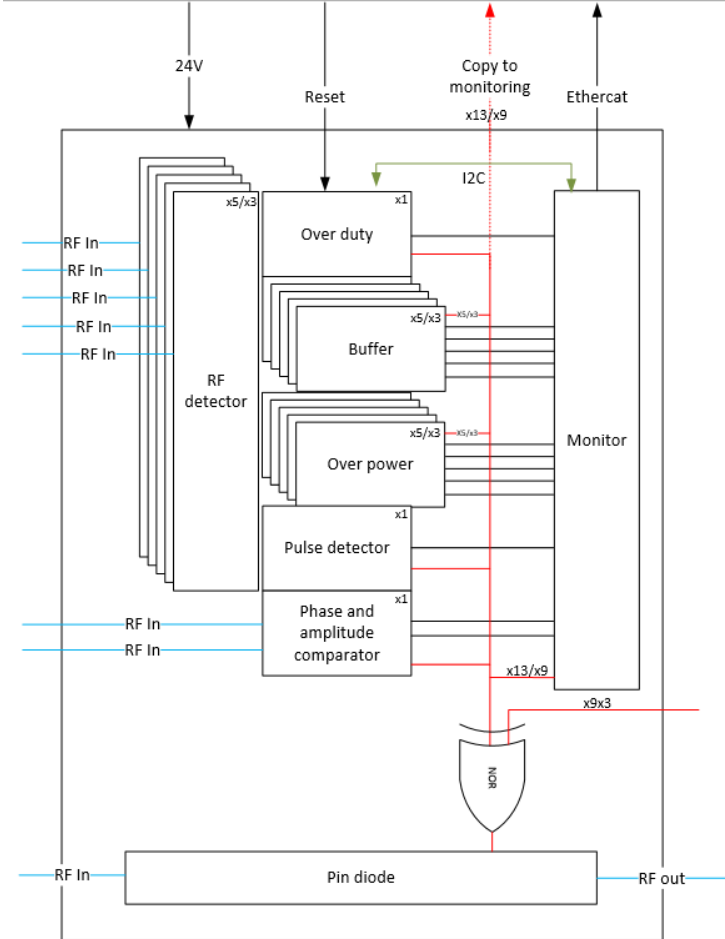
Power, Phase, Over-duty Measurement Board

A board to measure

- RF power
- Over-duty
- Phase to ref
- Power comparison



Control board



Power measurement
Pulse length
Interlock signal



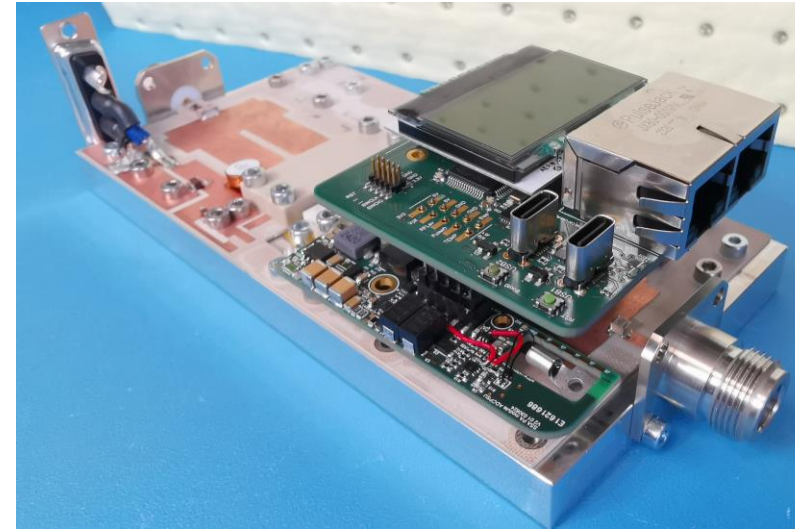
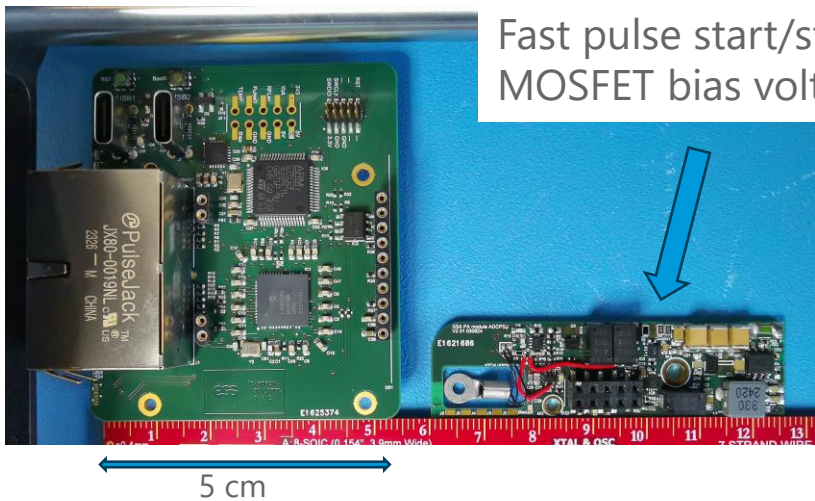
Monitoring and Control



UPPSALA
UNIVERSITET



PSU down conversion
Analogue data buffers
NCT linearisation
Fast pulse start/stop detection
MOSFET bias voltage



Amplifier Module with control boards



Full integrated assembly

STM32 MCU for A/D conversion and comms
LAN9252
USB interfaces
(Optional) LCD for debugging and display

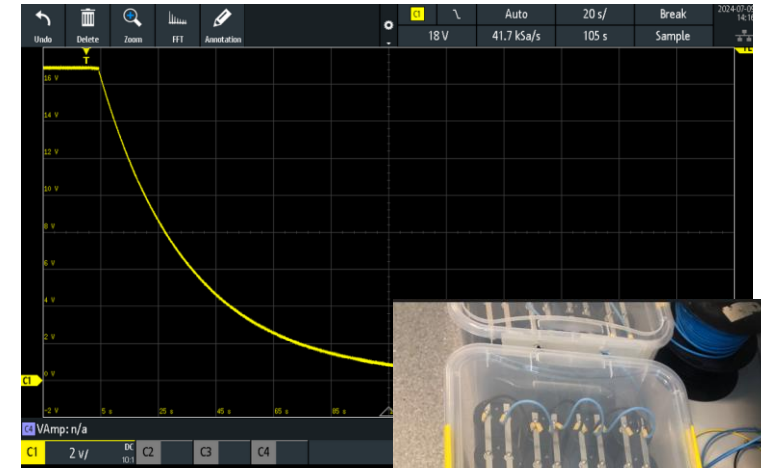
Other Developments



UPPSALA
UNIVERSITET



- Power module design optimisation including change of substrate, housing and cooling
- Control system under development. Platform will be common and supported by ESS.
- Electrical Schematics
- 1:80 cavity splitter/combiner (scale from 1:64)
- Rack layout
- Discharge protection circuit
- High Power 4:1 progressive combiner (400 kW stage)
- 4:1 driver combiner
- Soak testing.
- Setting up for in-house assembly and production
- Plus some more...



Tested with 72 capacitors
90% discharged in 85 sec

Soak test with 8 modules



UPPSALA
UNIVERSITET

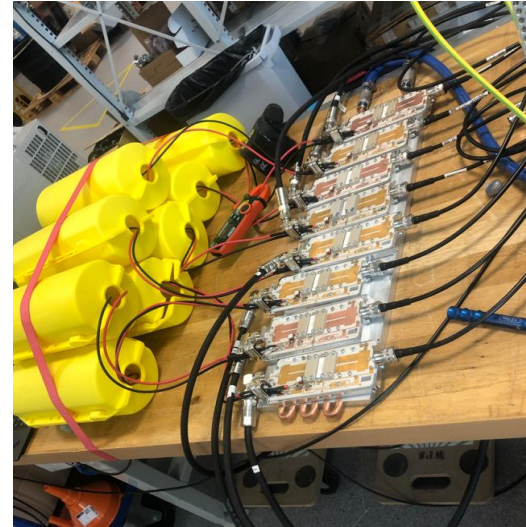


Initial difficulties encountered

Soak testing using 8:1 combiner (loan from Soleil)
Initially paused due to uneven heating.

Investigation ongoing:

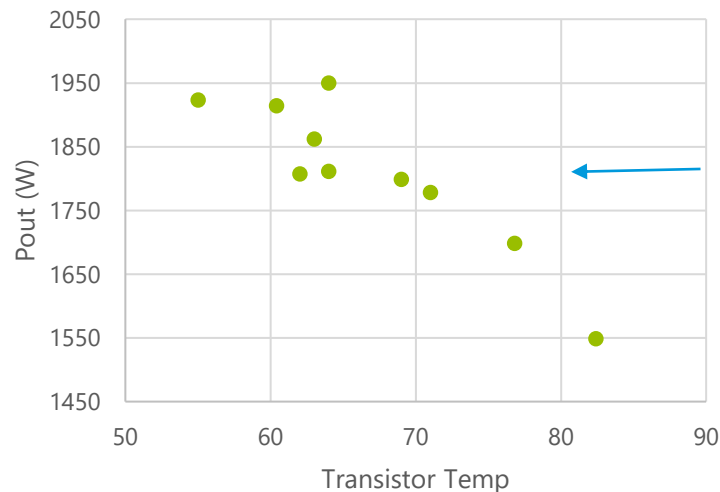
- Possibly due to output and phase mismatch
- 12 kW achieved



Temperature measurements vs duty cycle

pulse period	transistor temp	Pout (dBm)	Pout (W)	dutycycle
1000	25,5	62,6	1 819,70	0,4%
300	28,4	62,52	1 786,49	1,2%
140	35	62,48	1 770,11	2,5%
71	49	62,33	1 710,02	4,9%

Output power vs temp



Each point represents a different module



Summary



UPPSALA
UNIVERSITET



- Technology demonstrator development started in February 2024 as risk reduction to Spoke power stations.
- Development is based on a high power module delivering about 1.8 kW with auxiliaries, low power and high power stages being developed as part of this project.
- Priority on reliability and availability via risk reduction rather than prioritising absolute minimal cost.
- Control strategy is to use supported ESS technology for ease of integration.
- Timescale is challenging (2 years). Good progress made to date.
- Project is providing great staff morale boost, allows for personal development and for enhancing ESS in-house expertise.



Thanks for your attention !

Questions

Project Team:

Dragos Dancila (Uppsala)

Alireza Mohadeskasaei (Uppsala)

Bruno Lagoguez (ESS)

Gustav Mörk (ESS)

Panagiotis Vlachos (student @ ESS)

Slavisa Micic (ESS)

Morten Rostrup Forup Jensen (ESS)

and other colleagues from ESS and Uppsala

Swedish Research Council's (VR) Grant for investment in existing research infrastructure, project grant agreement No 2021-00329.

Bilateral development project ESS-UU.

2024-09-25