MT electronics: design/prototyping needs for the TDR

On behalf of the MT Readout Electronics team

Pratik Gheewalla, Ashley Greenall, Stephan Eisenhardt, Mike Perry – 10/7/24

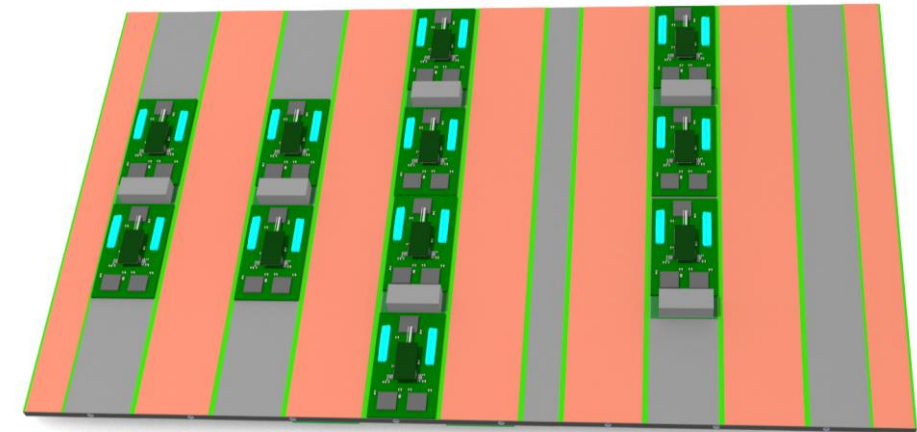# Overview of design for new baseline

- 12 row self-contained (single/pair) column units
- 1.0×10^{34} significantly reduces data links from MightyPix
  - Reduced component count (lpGBT, VTRx+, etc)
  - Reduced flavours
  - Simplified interconnect
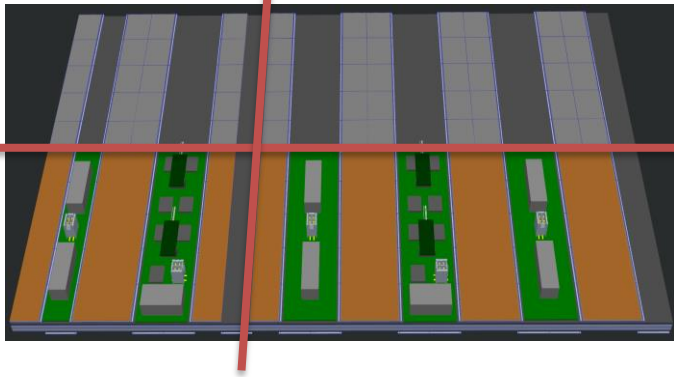
10 row, 4 sub-modules
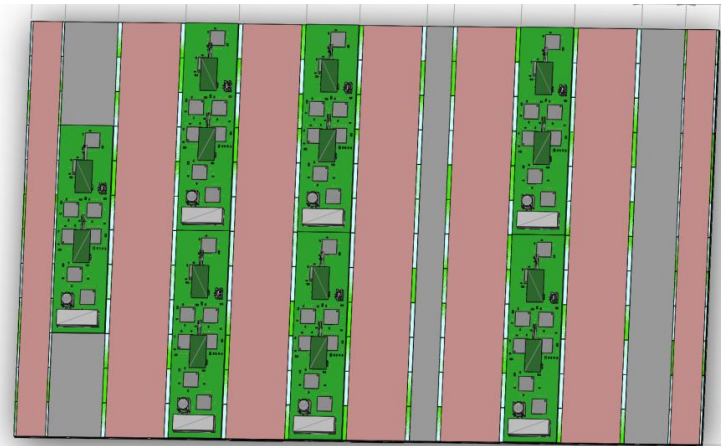
1.5×10^{34}
Old 8 lpGBT board as placeholder

1.0×10^{34}
New readout board

Serial Powering of MightyPix

- Follow same approach as Atlas ITK implementation

- 12 chips/column simplifies modularity
  - Split into smaller sub-modules made up of 4 chips/group (Quads) – shown below
    - Dual column *cw* 6 Quads, Single column *cw* 3 Quads
  - Approx 1.4A draw/quad – sets min. shunt current that a single chip should be able to sustain for redundancy

- Align SP chain to HDI board and a column pair
  - 9 to 12 quads per chain

Single column Quad

Dual column Quad

Column Pair SP chain

SP Chain

PSU channels

3
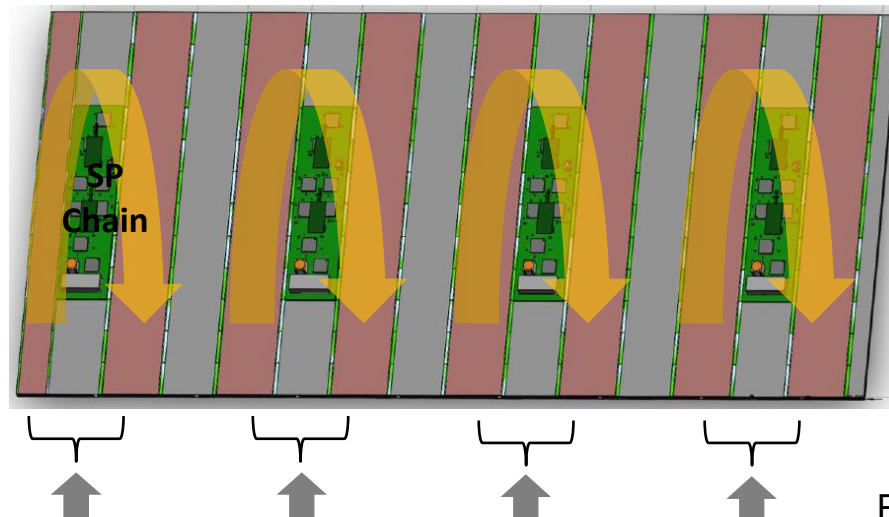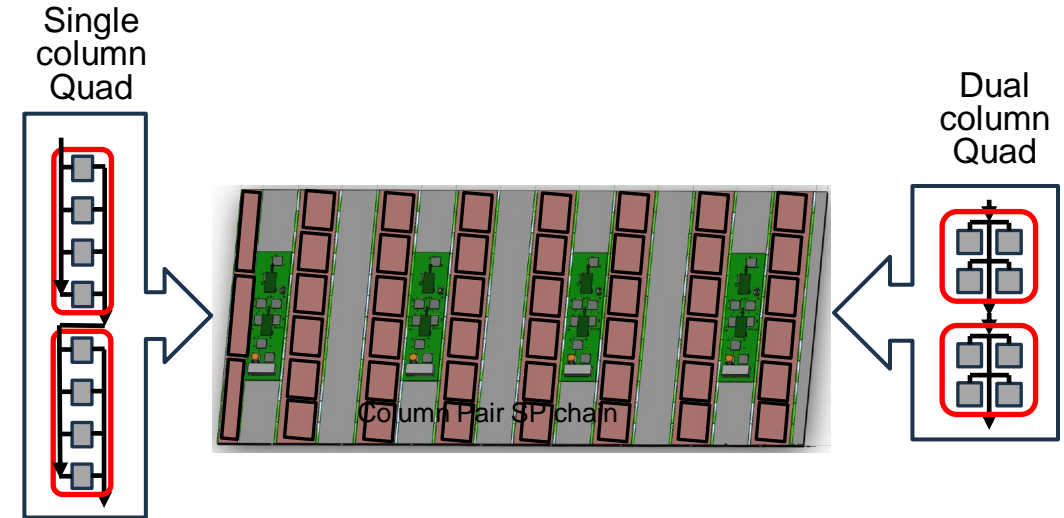
MightyPix HV bias

- ATLAS: Sensor HV should be aligned to a specific SP chain with no mixing across chains
- ITk Pixels specify 2 x HV per serial chain
  - If adopted, HV channel count can be between 8 to 16 for a Long module side

HV channels
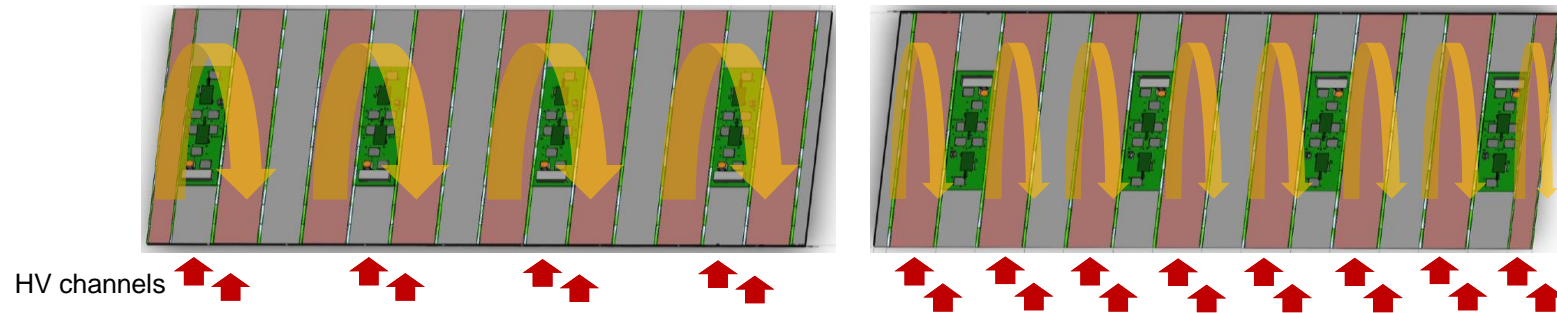
- Add HV switch to increase modularity of single HV line
  - Works well for dual column with ability to switch a column off if required
- Used in Atlas ITK but needs development for this application

HV switch

HV channels
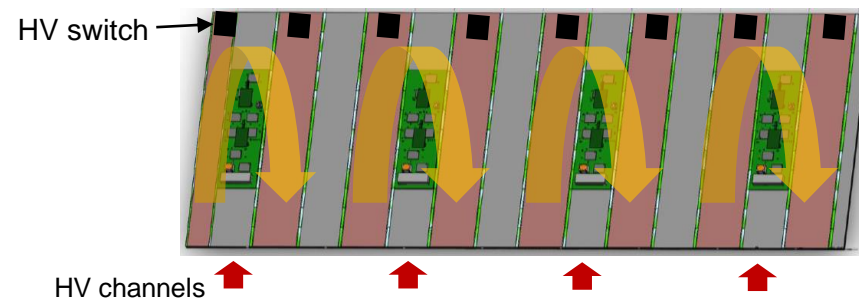
Readout (HDI) Board

- Adopted 3 data + 1 config/control lpGBT as baseline unit (Instead of 7+1)
  - Less efficient use of components but improves readout granularity
  - Small HDI PCB reduces cost and complexity
  - Can still be partially populated
  - Power is provided separately by DCDC on cheaper flex PCB technology with fewer layers

- Architecture and logical connectivity is well defined
- Physical interfaces to be defined
- Power domain complexity to be studied

32.2 x 55 mm

32.2 x 57 mm
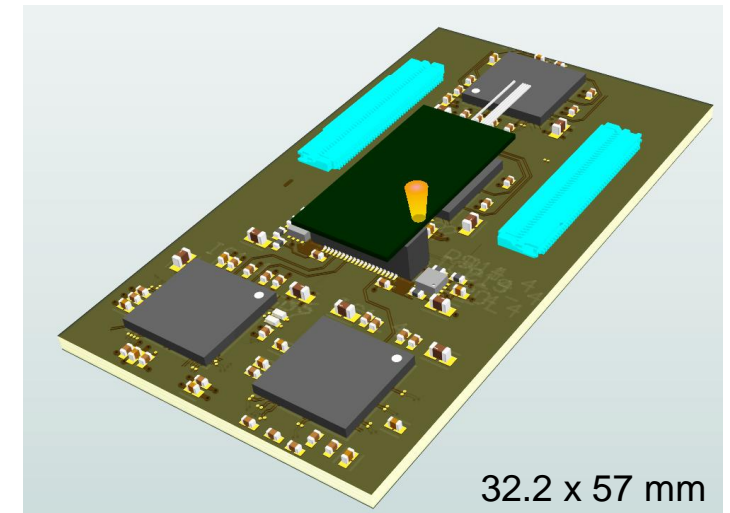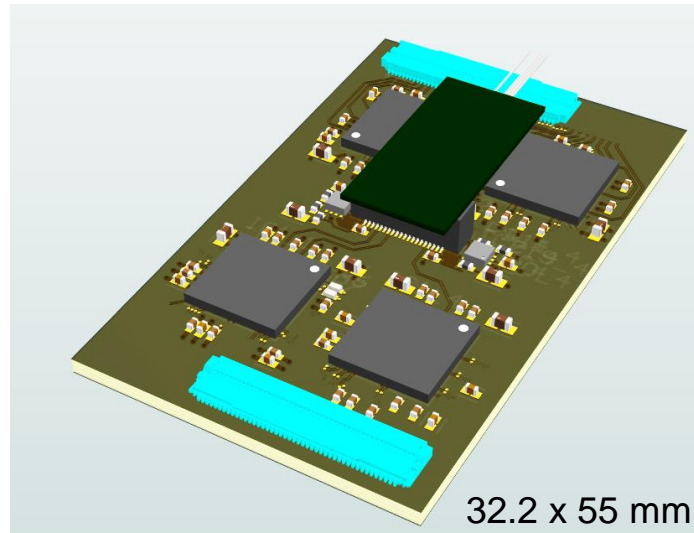
Possible component arrangements

MightyPix Flex and Interconnect

- FPC interconnect connects from Readout board to Sensor assembly Flex

- Wirebonding from Sensor assembly Flex to MightyPix

- Routing from lpGBTs to MightyPix currently undefined
- MightyPix2 Pinout undefined

- Plan to work forwards from lpGBTs to:
  - Define FPC connector
  - Define routing on Sensor assembly Flex
  - Negotiate MightyPix pad assignment with chip designers
  Will take many iterations!

- Currently undefined and being investigated:
  - Physical properties/shape of FPC
  - Choice of FPC connector
  - FP connector orientation
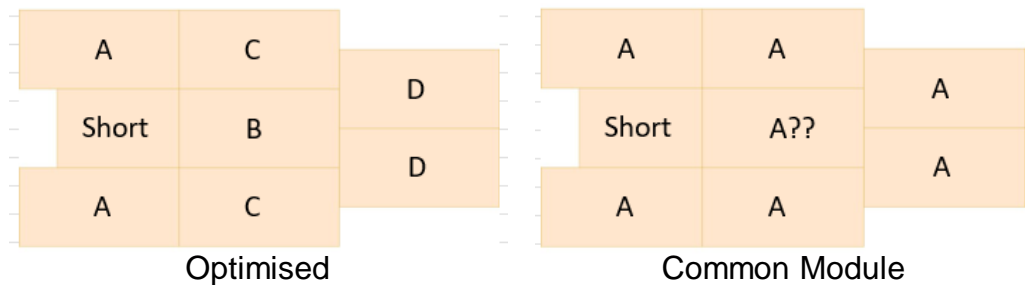 - How to protect wirebonds
  - How many flavours are required

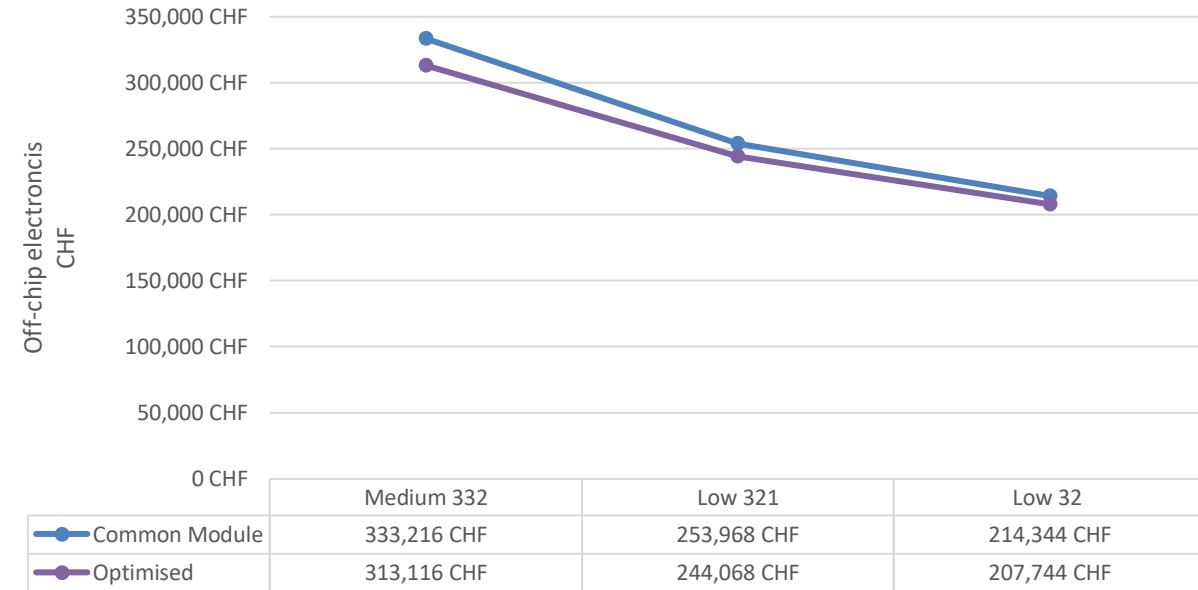
MightyPix

Sensor assembly Flex
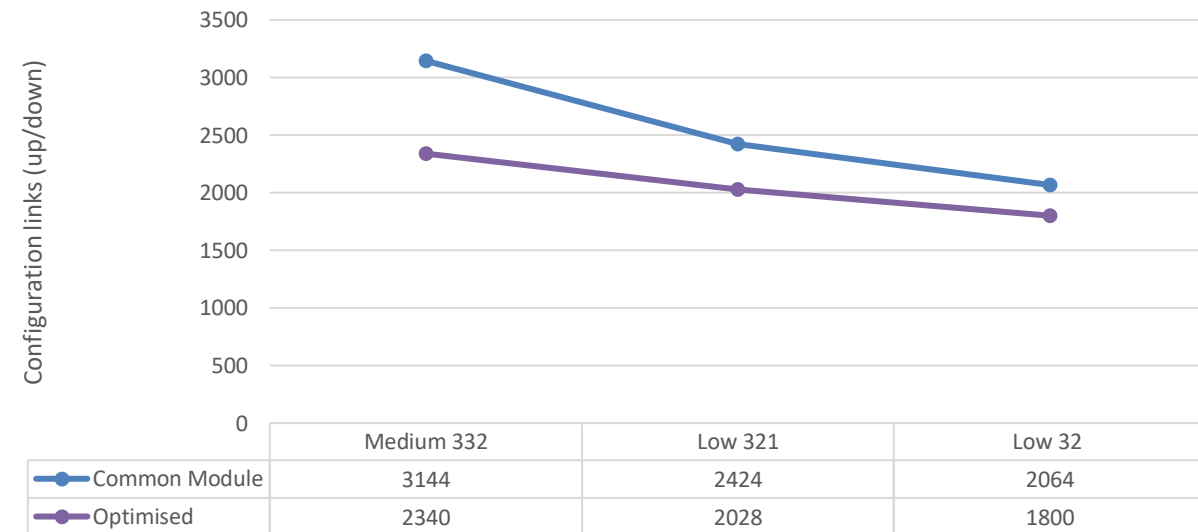
FPC
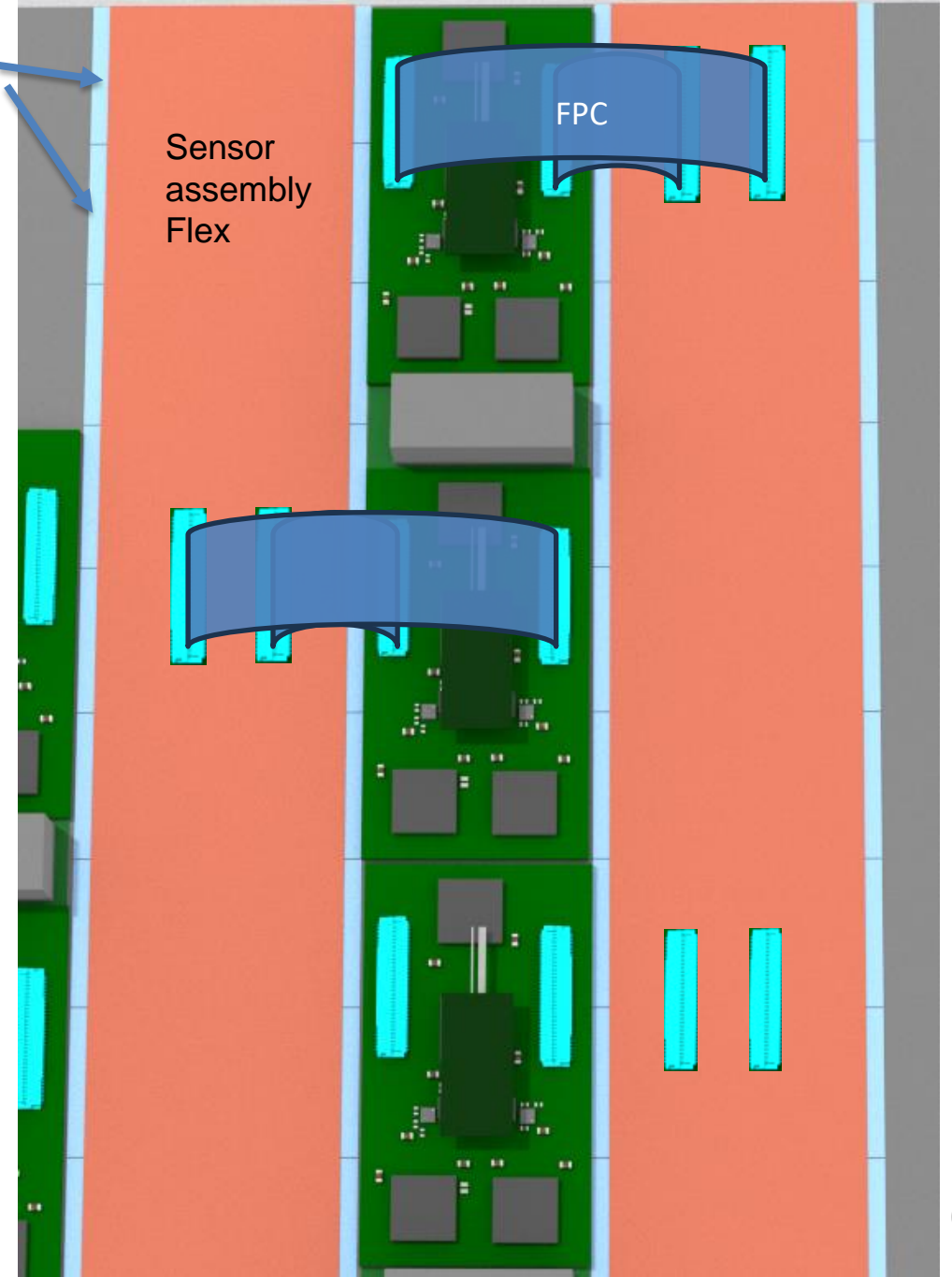
Optimisation vs Commonality

- 1.5 luminosity required significant optimisation of link distribution to fit in limited space
- 1.0 luminosity allows for a large reduction of flavouring / assembly complexity
- Where to draw the line between optimisation and number of flavours?

- Example:
  - Optimised approach has up to 4 different long modules
    - Low-rate modules have fewer readout boards and readout boards with fewer lpGBTs populated
  - Common module approach has 1 long module type but more wasted bandwidth / Backend channels

Optimised

Common Module

Cost of CERN parts

	Medium 332	Low 321	Low 32
Common Module	333,216 CHF	253,968 CHF	214,344 CHF
Optimised	313,116 CHF	244,068 CHF	207,744 CHF

Fibre data uplinks

|	Medium 332	Low 321	Low 32
Common Module	3144	2424	2064
Optimised	2340	2028	1800

Updated prototype board plan

- Board is now universal so hopefully immune to further changes
- Build board as envisaged for final modules
- Board will have additional ports for debugging purposes (I2C, etc)
- Allows for full system test including
  - Connector effect on signal integrity and reliability
  - Test routing density and establish minimum suitable layer count
  - Characterise transmission line (flex links)
  - Test power integrity
  - Serial powering tests
  - Test architecture
  - Test readout chain
- Should be versatile enough to be a generic readout
  - E.g. Test with other FE chips
- **High priority!** Production anticipated Early August

Connector Saver flex

Debugging interface

FE

FE

FE

FE
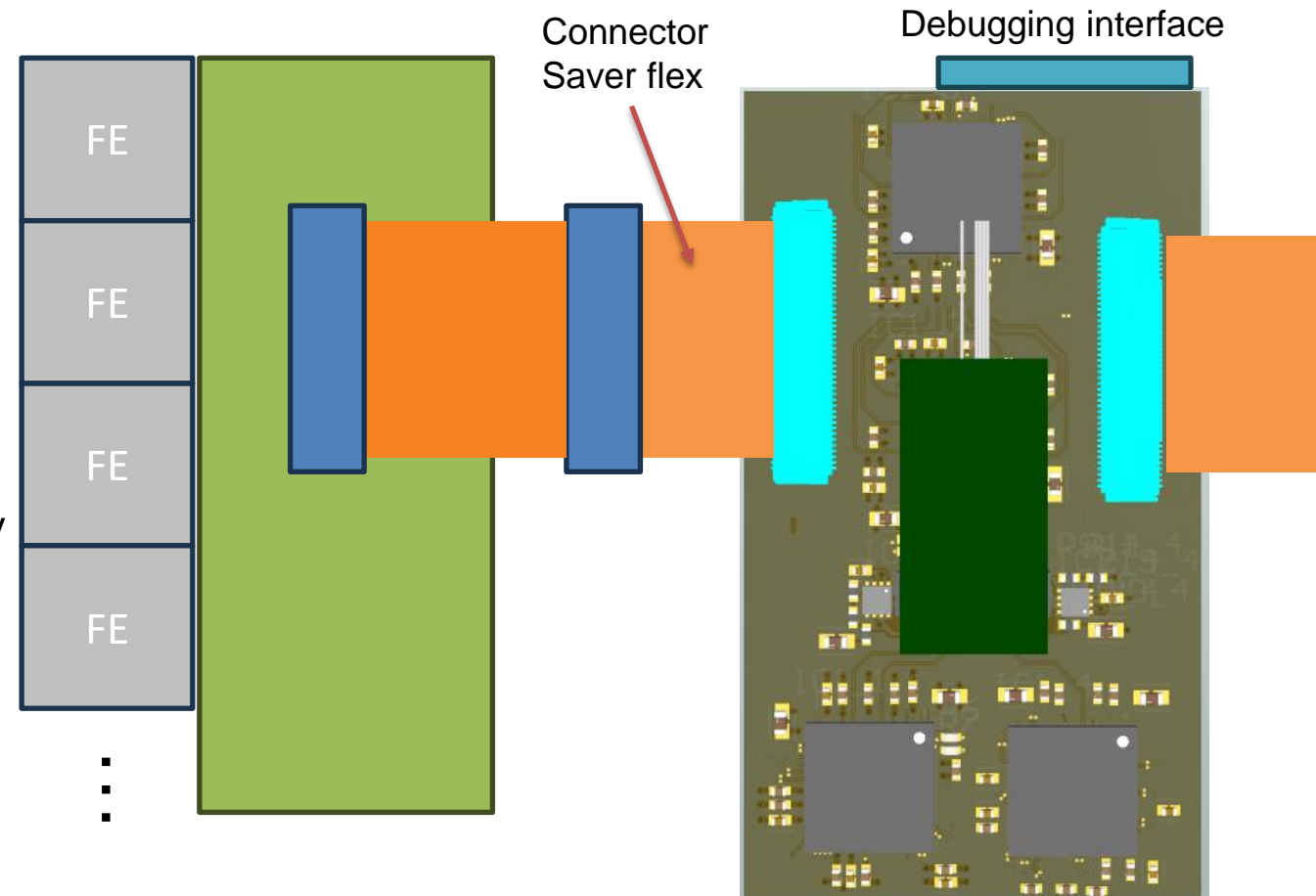
Readout Board QC System

- ~1600 (+spares) Readout HDI boards will be produced.
    - Complex object with fine pitch BGA components
    - ~55 differential pairs on FPC connectors
    - 4x10Gbps pairs to backend
    - etc

- Need a plug & play system to verify full functionality

- E.g. FPGA system to
    - Read signals & Inject signals on FPC connector
    - Interface to VTRx+ connector (Without VTRx+)
    - Check for <u>a</u> signal or verify full signal integrity?
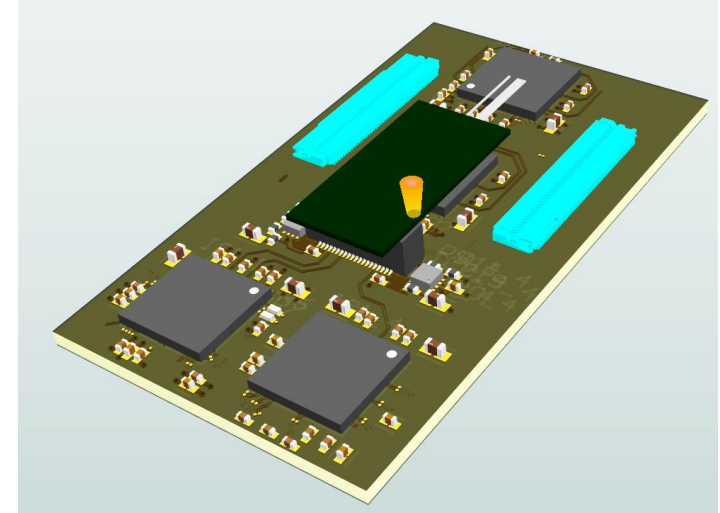
Summary of Remaining Development work

- Serial power chain
  - Element size and chain length
  - Testing and verification of implementation – Relies to some extent on MightyPix2 delivery (Submit early 2025)
- HV switch development
- DCDC module derived from Atlas Strips design
- Study of optimisation level
- Readout board development
  - Define physical interface
  - Study PDN
  - Complete layout and routing of prototype
  - Full suite of tests
- MightyPix sensor assembly
  - Routing affected by serial power unit size, MightyPix pinout, readout board pinout
  - Number of flavours to be determined by optimisation approach
- FPC interconnect
  - Routing depends on above
  - Study physical constraints
- QC
  - Readout board validation
  - Systems to test various stages of assembly

Objects to be developed

- Prototype items:
  - Readout prototype board
  - DCDC module (For readout board)
  - Flex(es) or interfaces for non-MT FE chips to test serial powering and comms with readout board
  - Flex to interface to MightyPix2
  - HV switch test board
  - Readout board QC system

- Production items:
  - Readout board
  - MightyPix assembly flex (Multiple flavours)
    - HV switch
  - Interconnect
    - Data/Control FPC (Readout to MightyPix assembly)
    - Power (Serial power between MightyPix assemblies)
  - Cabling