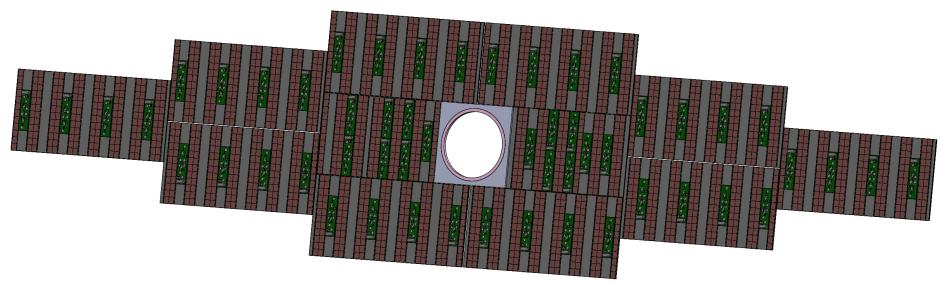
MIGHTY TRACKER - PIXEL MODULE MECHANICS AND ELECTRONICS

Overall Design, Pixel Module Design, Chip Matrix, and more...



ALEX BITADZE



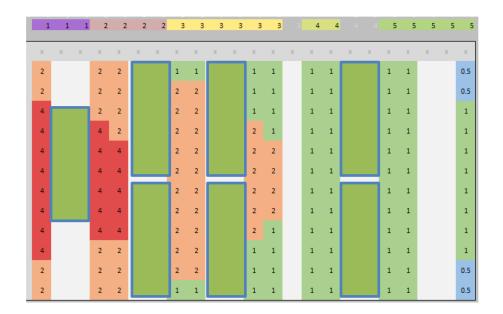
 Side A (30 x 12 Chips)
 Side B (30 x 12 Chips)

 (Reversed)
 (Reversed)

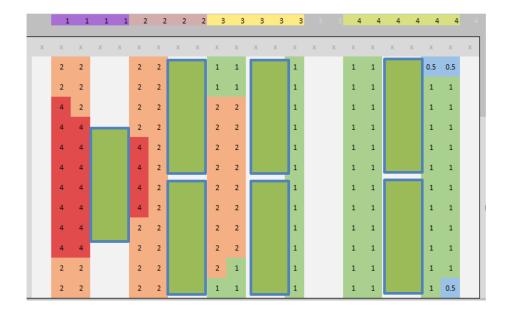
1	1 1 1 1	1 1 2 2	2 2 2 2	2 2 3 3	3 3 3 3	3 3 4 4	4 4 4 4	4	1 1	1 1 1	1 1 1	2 2	2 2 2 2	2 2 3 3	3 3 3 3	3 3 4 4	4 4 4
×	x x x x	x x x x	x x x x	x x x x	x x x x	х х х х	x x x x	х	х х	x x x x	x x	х х х	x x x x	х х х	x x x x	x x x x	х х х
0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.25 0.25	0.25 0.2	25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.25 0.25	0.25 0.2	25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.25 0.25	0.25 0.2	25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.25 0.25	0.25 0.2	25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.25 0.25	0.25 0.2	25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.25 0.2	25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.5 0.	5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.5 0.	5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.5 0.	5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.5	0.5 0.5	0.5 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.5 0.	5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.5	0.5 0.5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.5 0.	5	0.5 0.5	0.5 0.25	0.25 0.25	0.25 0.25	0.25 0.25	0.25
0.5	0.5 0.5	0.5 0.5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25 0.25		0.5 0.5	0.5 0.	5	0.5 0.5	0.5 0.5	0.25 0.25	0.25 0.25	0.25 0.25	0.25

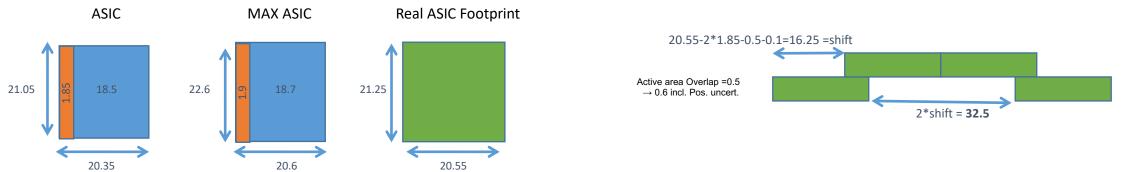


Side A (23 x 12 Chips)

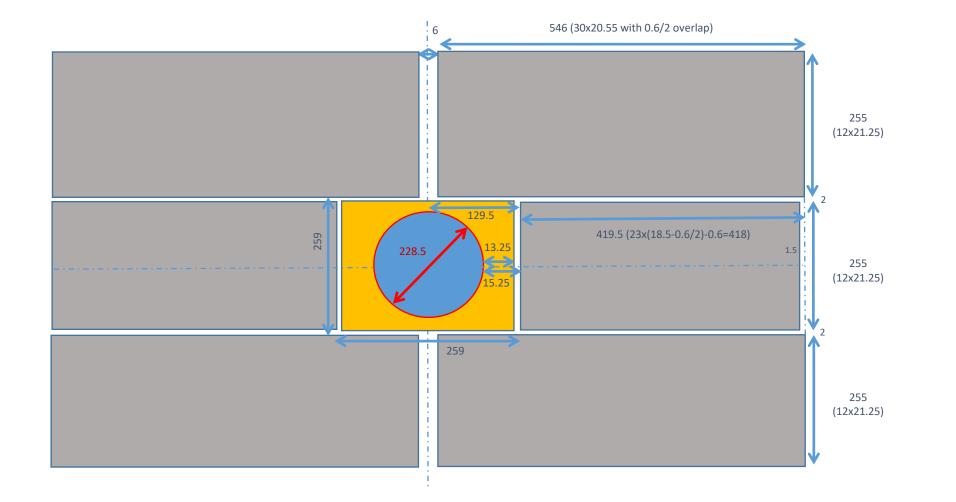


Side B (23 x 12 Chips) (Reversed)

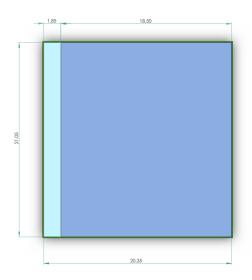




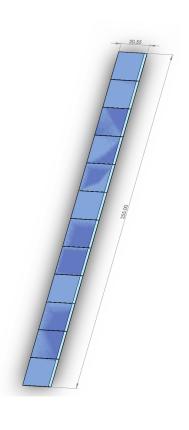
20.35



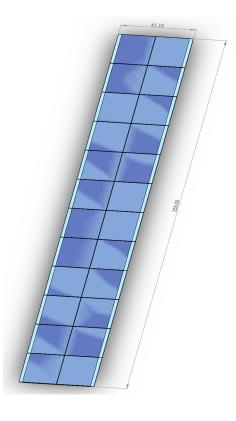




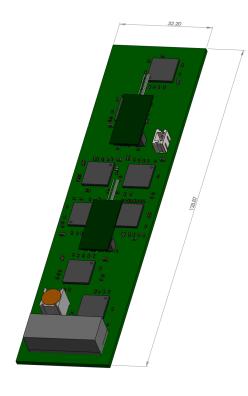
* Footprint: +200 μm



1 x 12 Flex Assembly

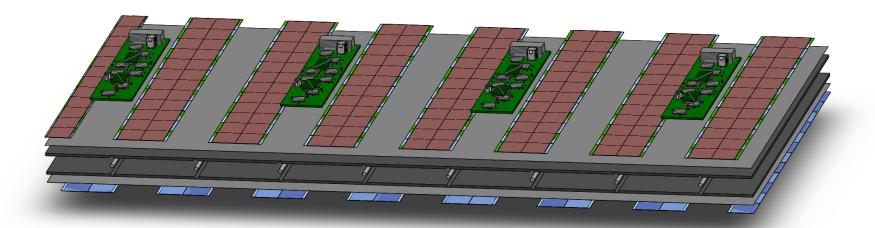


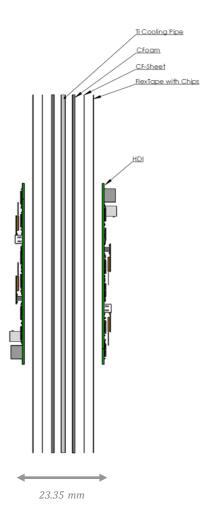
2 x 12 Flex Assembly



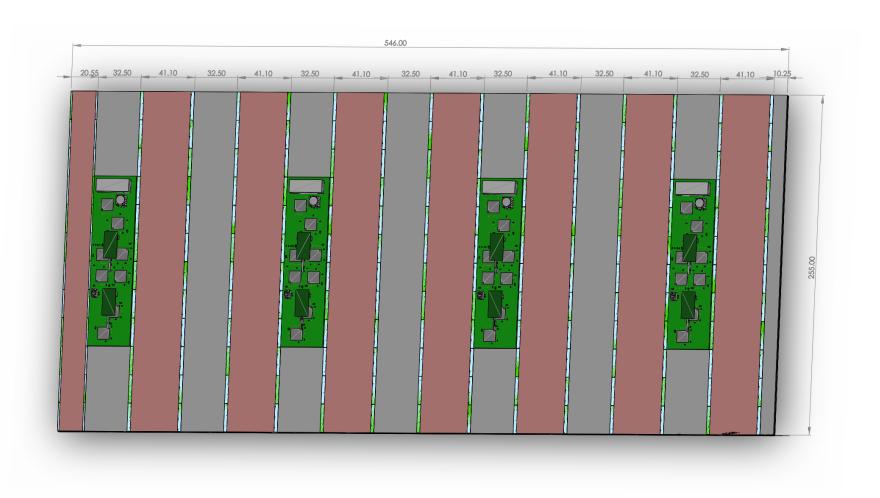
HIGH DENSITY INTERCONNECT (HDI) PCB

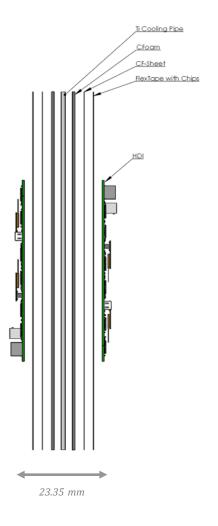




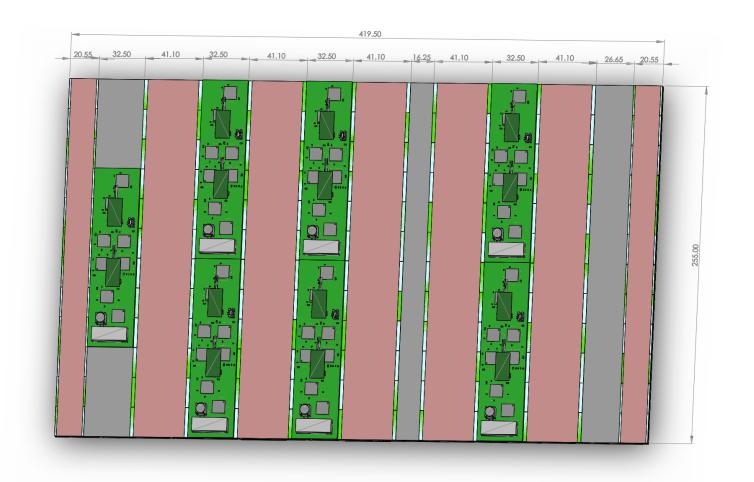


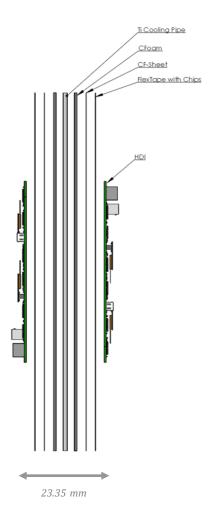




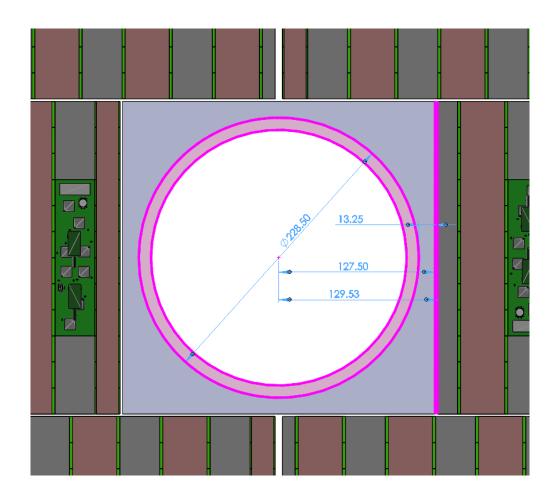






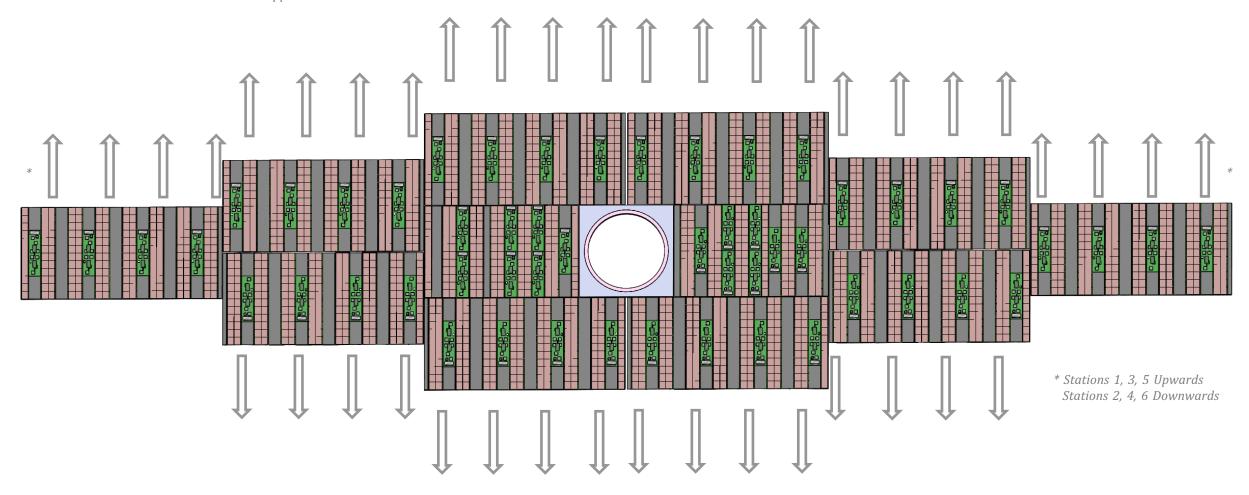








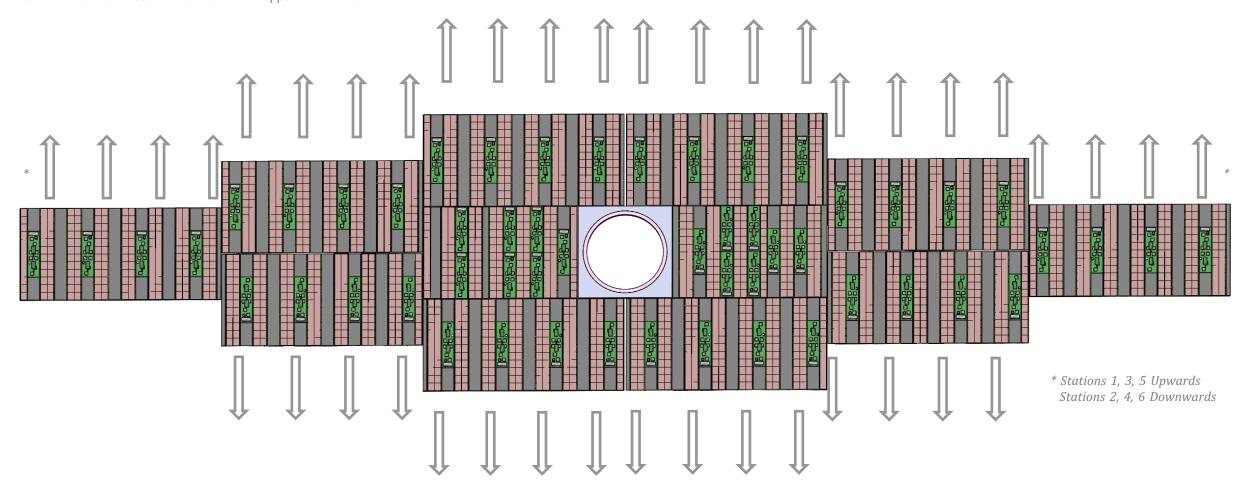
Long Module Services – Front & Back - Same Direction Short Module Services – Front & Back - Opposite Direction







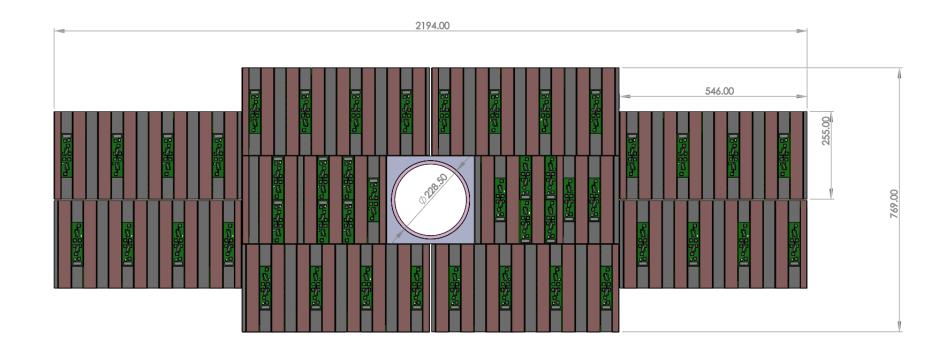
Long Module Services – Front & Back - Same Direction Short Module Services – Front & Back - Opposite Direction



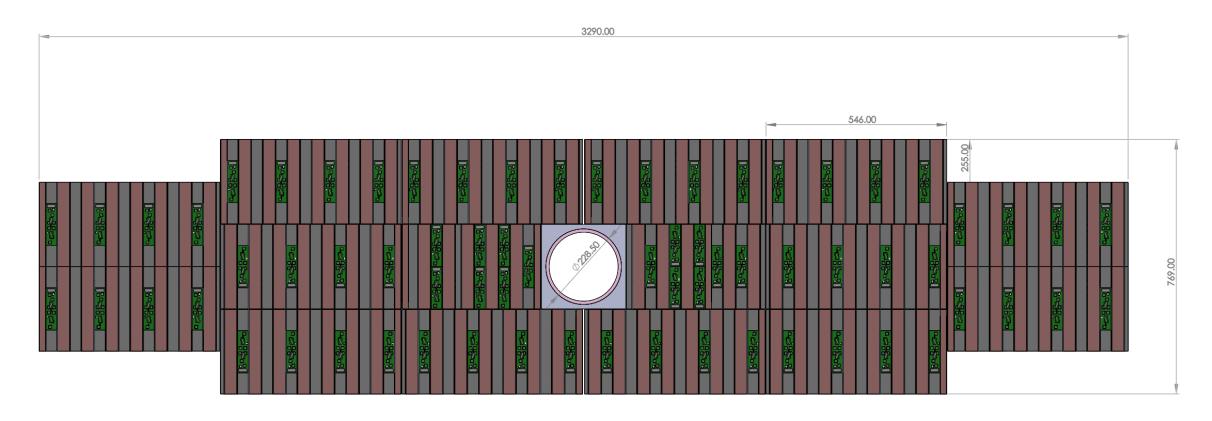






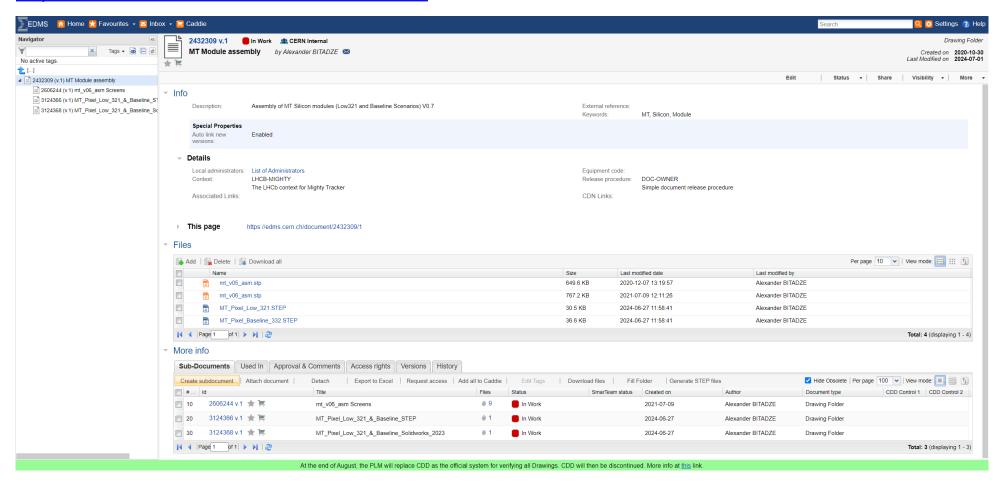






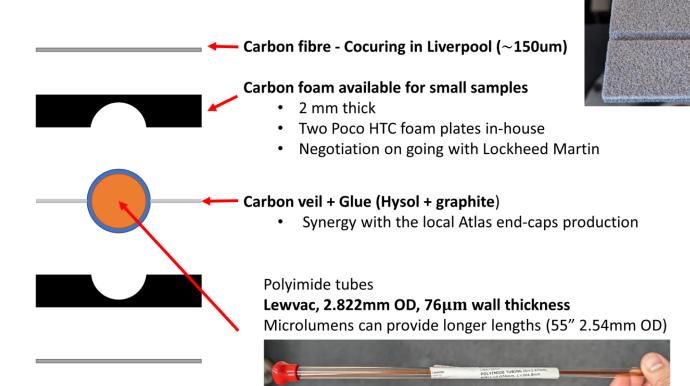


https://edms.cern.ch/document/2432309/1





Base module exploded view

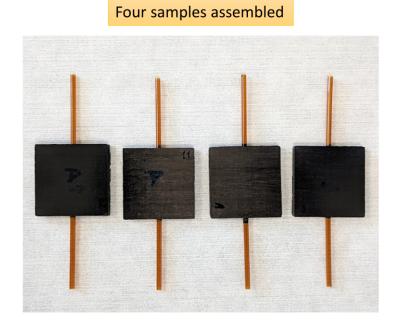




Mode details in Stefano's talk

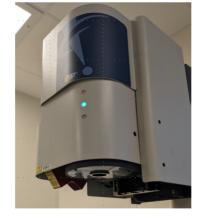


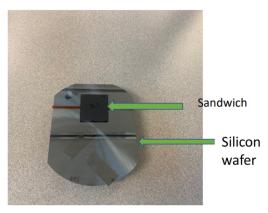
Baby modules

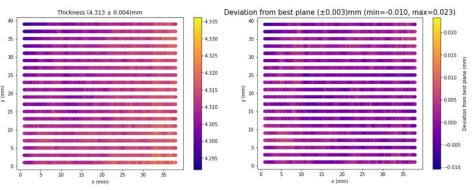


Metrology presentation

Smartscope measurements

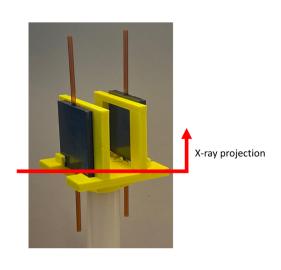


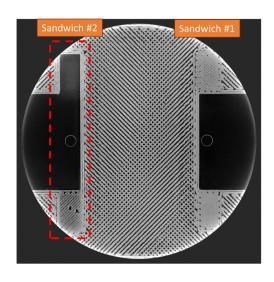


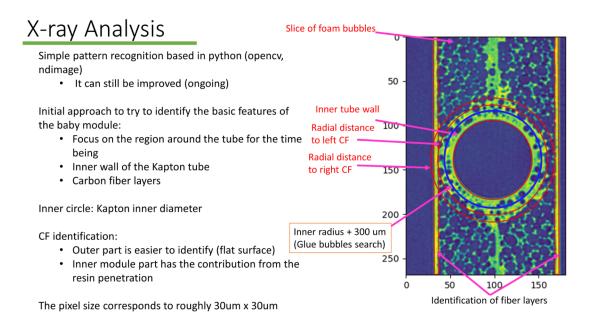




X-ray Tomography (NXCT UK)







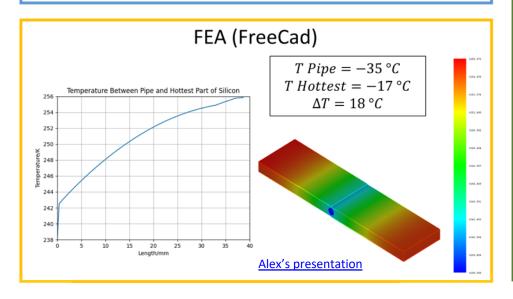


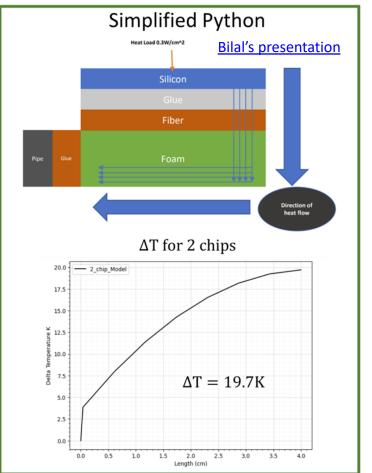
Comparison between FEA and Simplified

Model with 2 chips distance (simplified geometry)

FEA (FreeCad)	$\Delta T = 18^{\circ}C$
Simplified Python	$\Delta T = 20^{\circ}C$

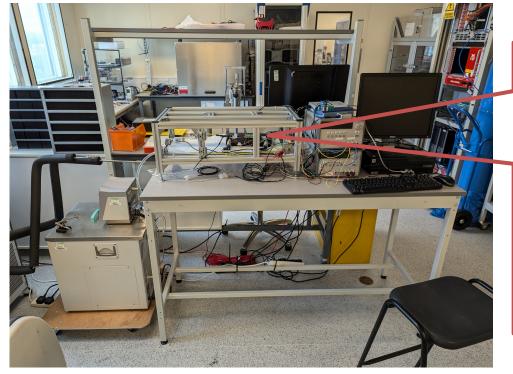
Difference of 2°C, python code is a fast tool for feasibility studies and better understanding of the complete FEA

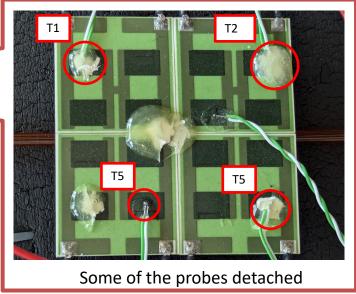




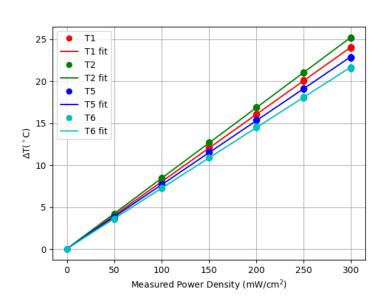


Experimental set-up

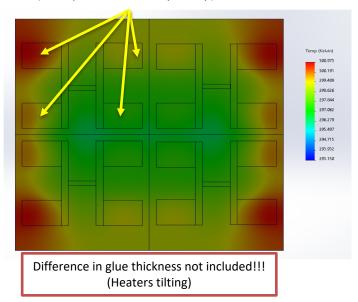








FEA (0.3W per block – 1.2W per chip)



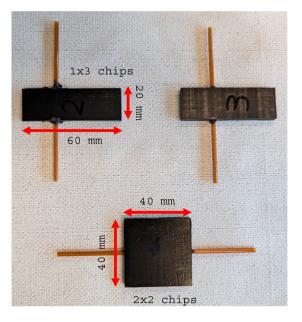
- ✓ First cooling performance results obtained and compared to FEAs
- ✓ Intermediate upgrade to HFE7100 soon
- ✓ Upgrade to CO2 evaporative cooling in the coming month or so (Ti tubes prototypes)
- ✓ New samples 1x3 chips size will allow us to estimate the cooling performance for 1 and 2 chips cooling spacing 2 Kapton tube samples assembled Titanium sample will also be assembled Comparison
- ✓ Custom-made heaters coming 20mm x 20mm (~10 working days)

1. FEA

- Convection is not included
- 2. Heater tilting not included
- 3. Assuming temperature inside the cooling line at 0°C
- 4. 1.2W per heater (192mW/cm²)
- 5. $\Delta T_{initial} \sim 28^{\circ} C$

2. Measurement

- Largest convection estimated as 1.6W (25W/m 2 K at $\Delta T \sim 25$ °C) -> loss of additional 62mW/cm 2 (link)
- 2. Effective power -> 254mW/cm^2
- 3. $\Delta T_{initial} \sim 21^{\circ} C (254 \text{mW/cm}^2)$
- 4. $\Delta T_{initial} \sim 25^{\circ} \text{C} (300 \text{mW/cm}^2)$



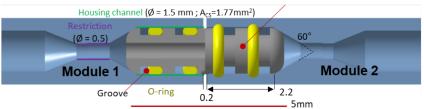


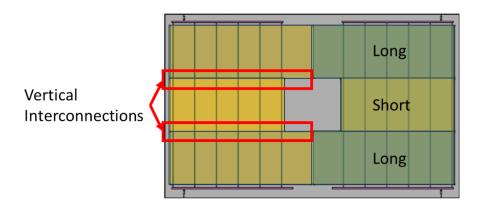
Vertical interconnection

- Reliable hydraulic and mechanical interconnection (CERN EP-DT)
- Very compact
 - Seal fitting is 5 mm long and has 1.5 mm OD
- Proposal to solve the vertical integration of the modules
 - Module can still be replaced
 - Near seamless
- Radiation hardness of O-rings being investigated

EP-DT day meeting

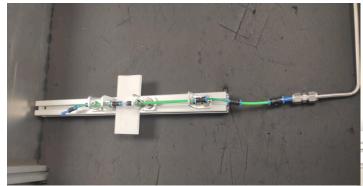


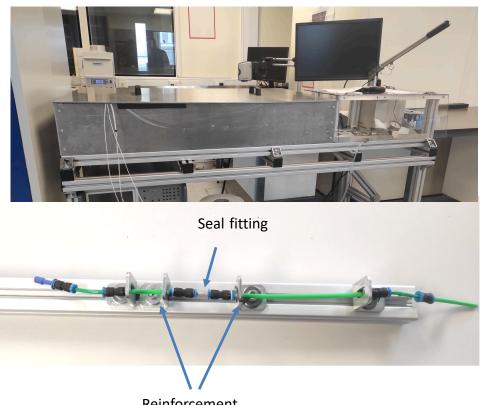






We used a compact reinforcement test stand to assess the seal fitting. During the procedure, we incrementally raised the pressure to detect any potential leaks or tube ruptures.

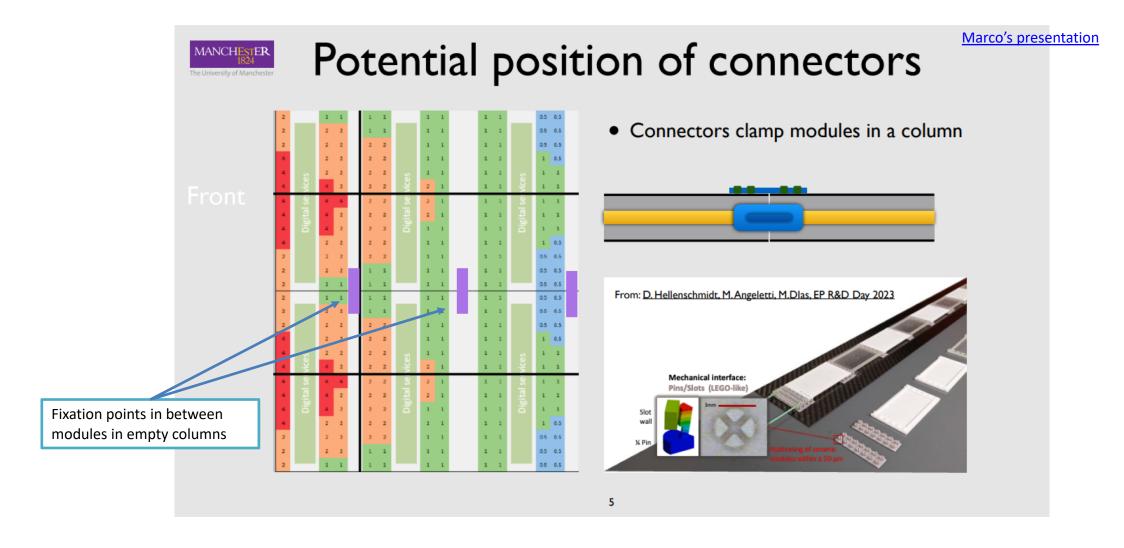




Reinforcement

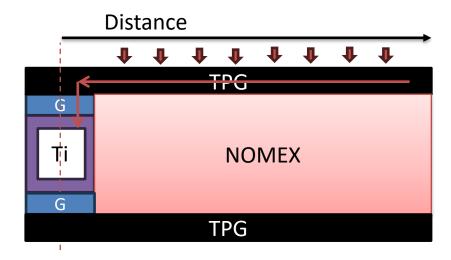
At approximately **40 bar** of pressure, there were no observable leaks detected. Upon surpassing the 40 bar threshold and reaching around 50 bar, leaks remained undetected. However, there was noticeable deformation in the plastic tubes, eventually leading to tube rupture







No Foam alternatives (TPG calculation)

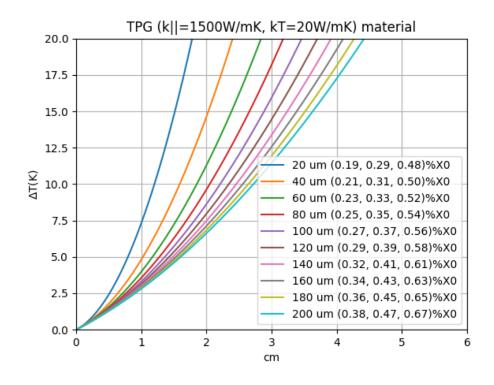


3mm titanium squared tube (250um wall)

TPG: k||=1500W/mK, kT=20W/mK, X0=19.23cm

G: kT=1W/mK, X0=35.5cm Ti: k=16W/mK, X0=3.56cm

X0 calculated averaging the Ti tube over 8 cm, 4cm and 2cm respectively (one cooling line every 4, 2 and 1 chip columns)





Ongoing activities and plans

- \checkmark Implement cooling connection fittings into the CAD
- ✓ Implement module interconnection clamps into the CAD
- ✓ Finalise the 3D CAD Design for the Pixel Module Assembly
- ✓ Cooling connection fittings pressure tests / Reliable interconnection design
- ✓ Thermal test setup (FEA validation) New sample tests Novec HFE7100 and CO₂
- √ Validate the on-detector cooling system (DT)
- ✓ FEA Analyses for No Foam solutions (New Materials)
- ✓ FEA Analyses for Full assembly (thermal box / support structures) for Gravitational sag and vibrations
- ✓ Define QA/QC procedure for chips/flexes assemblies, along with the implementation of proper reworkability procedures
- ✓ Define Pixel module assembly serviceability and maintenance procedures after installation