Towards 4D Vertexing

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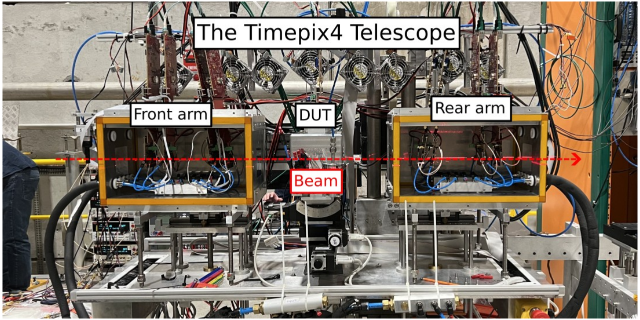
10th July, 2024

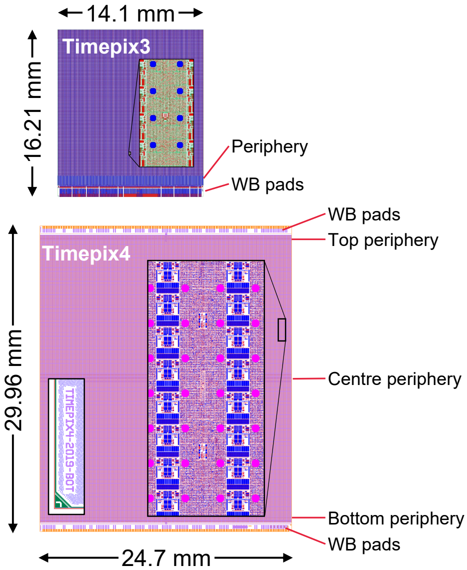
The Timepix4 telescope

Timepix4 telescope

- **Test sensor + ASIC assemblies**
- **Proof of concept of a 4D tracker**
- **Design specifications**
  - $2\,\mu m$ pointing resolution
  - $< 50\,ps$ track-time resolution
  - operation at $1\,Mtracks/s$ to $10\,Mtracks/s$



The Timepix4 readout ASIC

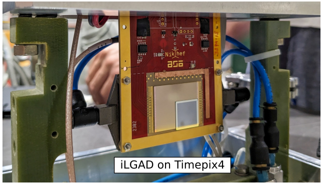


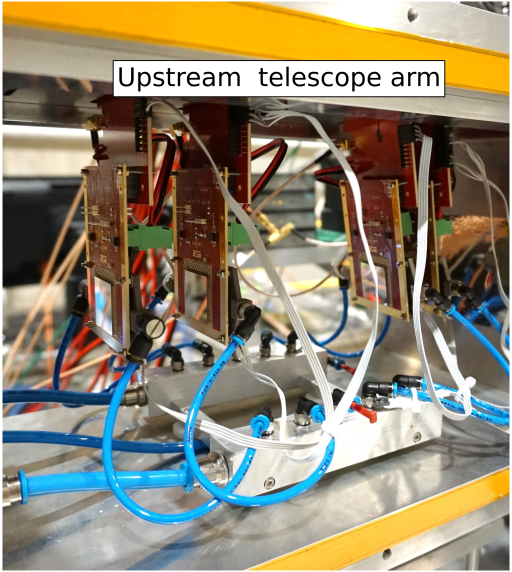
			Timepix3 (2013)	Timepix4 (2019)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	**6.94 cm^2** 3.5x
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	0.43x10^6 hits/mm²/s	**3.58x10^6 hits/mm²/s**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel** 8x
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
		Max count rate	~0.82 x 10^9 hits/mm²/s	~5 x 10^9 hits/mm²/s
TOT energy resolution			< 2KeV	< **1Kev**
TOA binning resolution			1.56ns	**195ps** 8x
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)** 32x
Target minimum threshold			<500 e^-	<500 e^-

Llopart 2022

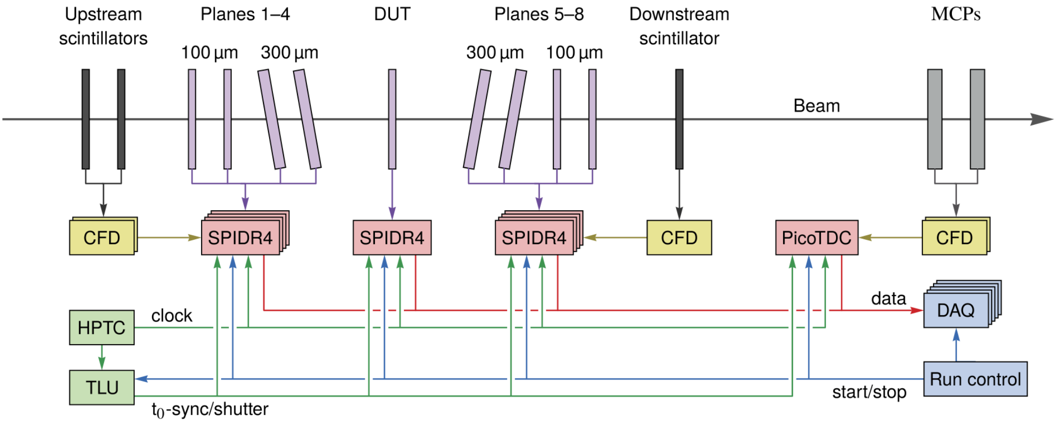
Plane assemblies

- Eight telescope planes with n^+-on-p planar silicon sensors:
  - 4 x 300 µm sensors for spatial resolution (angled)
  - 4 x 100 µm sensors for temporal resolution (perpendicular)
  - Sensor upgrades are anticipated (LGAD, 3D, ...)
- Several DUT assemblies
  - 50 µm, 100 µm, 200 µm and 300 µm n^+-on-p planar silicon
  - 300 µm p^+-on-n planar silicon
  - 2 x 250 µm iLGAD sensors with 55 µm and 110 µm pitch (Timepix3 sized)
  - 2 x TI-LGAD sensors (single trench and double trench)
  - 3D sensor
- All bump-bonded to Timepix4.2 ASICs



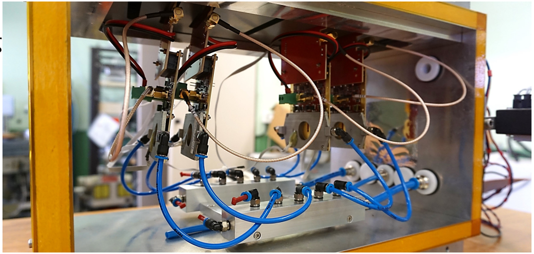


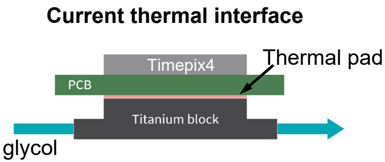
Telescope configuration

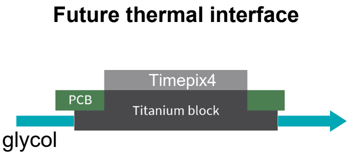


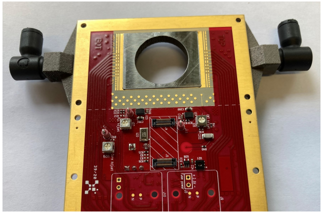
Assembly cooling

- All assemblies have a 3D-printed titanium cooling block
- Cooled using glycol at $20\,^{\circ}$C
- Could go to $-20\,^{\circ}$C in the future
- Plan to mill PCB to have direct thermal contact with Timepix4







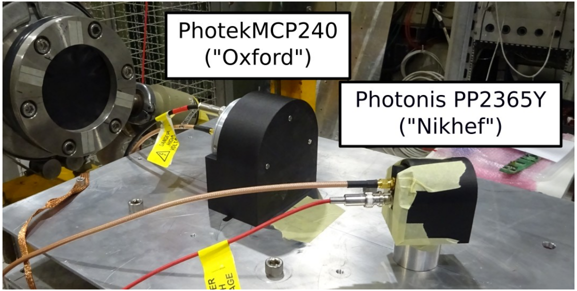


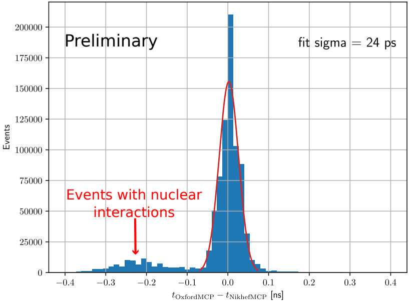
Telescope configuration

- Telescope installed at H8 beamline at SPS
- $180\,\text{GeV}$ mixed hadron beam
- Finished commissioning of telescope in 2023
- First testbeam in May 2024 focussing on DUT studies (iLGAD, TI-LGAD, 3D)

Time reference system
Micro channel plate detectors

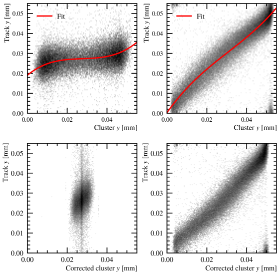
- Separate time reference system to study telescope timing
- Two MCP-PMTs in coincidence
- Current resolution per MCP-PMT: 17 ps
- Combined resolution: 12 ps

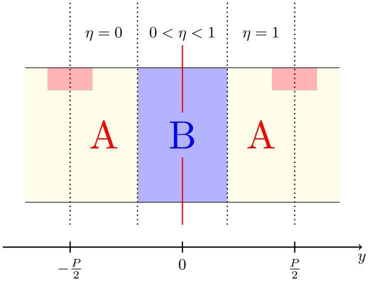




η-corrections

- Charge sharing is non-linear for planes at normal incidence
- Reconstructed cluster positions systematically wrong for multi-pixel clusters
- Variable $\eta = \frac{Q_L - Q_R}{Q_L}$ quantifies charge asymmetry for multi-pixel clusters
- Can use η-distribution to correct the reconstructed cluster position

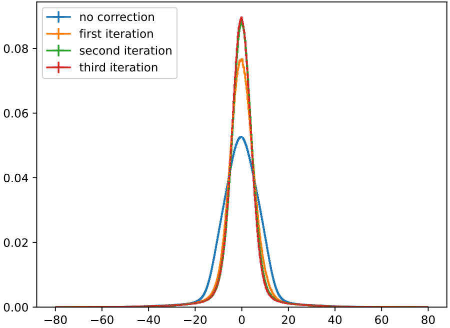




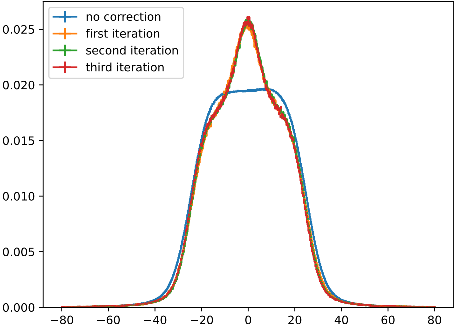
η-corrections

- η-correction done with two iterations (depends on alignment)
- Unbiased residuals improve from $7\,\mu m$ to $5.6\,\mu m$ on thick planes
- Unbiased residuals improve from $15\,\mu m$ to $14.3\,\mu m$ on thin planes

Thick plane



Thin plane



Tracking requirements

TABLE: List of the standard selection requirements for the track reconstruction.

Requirement	Default value	Description
Cluster time window	< 100 ns	Maximum time difference of hits within the same cluster
Cluster width in x and y	≤ 2	Rejects large clusters from δ-rays, nuclear interactions, etc.
Track time window	< 5 ns	Clusters within 5 ns are considered for the pattern recognition
Number of clusters in time window	$= 1$ per plane	Rejects multiprong interaction vertices
Number of clusters per track	$= 8$	Maximizes track precision
Opening angle	< 0.01 mrad	Angle that defines the reconstruction window from plane to plane, assuming straight tracks
Fit χ^2/ndof	< 10	Cut on χ^2 divided by the number of degrees of freedom for track quality

Tracking efficiency

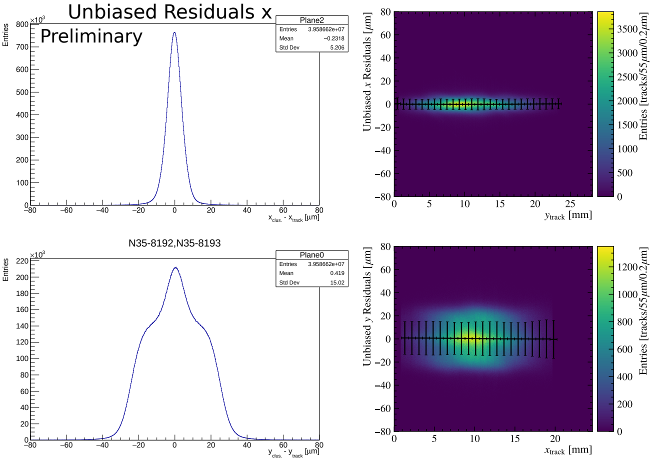
- Measure cluster efficiency per plane using selection requirements
- Total tracking efficiency as product of all individual plane efficiencies
- Uncertainties from variation across different runs
- Thick planes have lower efficiency due to cluster width cut (needed for better spatial resolution)

TABLE: Single plane cluster efficiencies and the total tracking efficiency of the telescope.

Assembly (thickness)	Cluster efficiency
N10 (100 µm)	$98.72 \pm 0.02\,\%$
N18 (300 µm)	$93.2 \pm 0.2\,\%$
N22 (300 µm)	$93.37 \pm 0.12\,\%$
N33 (300 µm)	$93.80 \pm 0.19\,\%$
N34 (300 µm)	$91.66 \pm 0.17\,\%$
N35 (100 µm)	$98.52 \pm 0.19\,\%$
N36 (100 µm)	$98.9 \pm 0.3\,\%$
N38 (100 µm)	$98.00 \pm 0.03\,\%$
Telescope	$70.6 \pm 0.4\,\%$

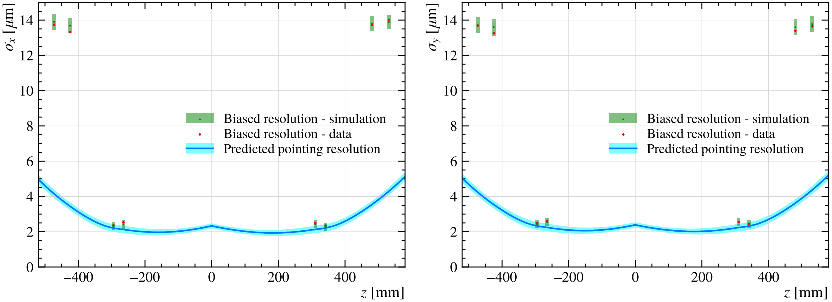
Alignment

- Check unbiased residuals as a function of position on the sensor to spot alignment issues



Spatial resolution

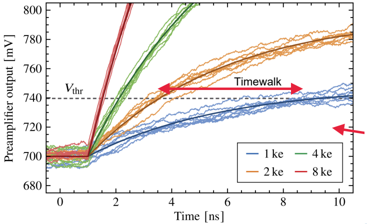
- Compare biased residuals in simulation and data to per-plane resolutions of all planes
- Use simulation to predict pointing resolution at DUT position

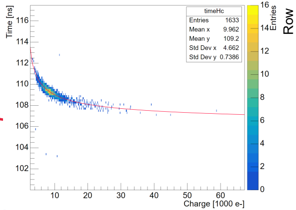


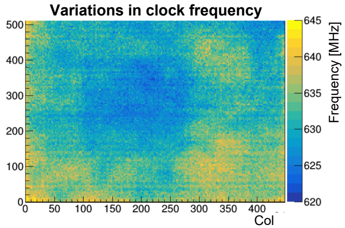
- Per plane resolutions
  - x: (3.3 ± 0.3) µm (thick planes), (14.4 ± 0.5) µm (thin planes)
  - y: (3.5 ± 0.3) µm (thick planes), (14.3 ± 0.5) µm (thin planes)
- Pointing resolution at DUT
  - x: (2.32 ± 0.12) µm
  - y: (2.38 ± 0.12) µm

Time resolution

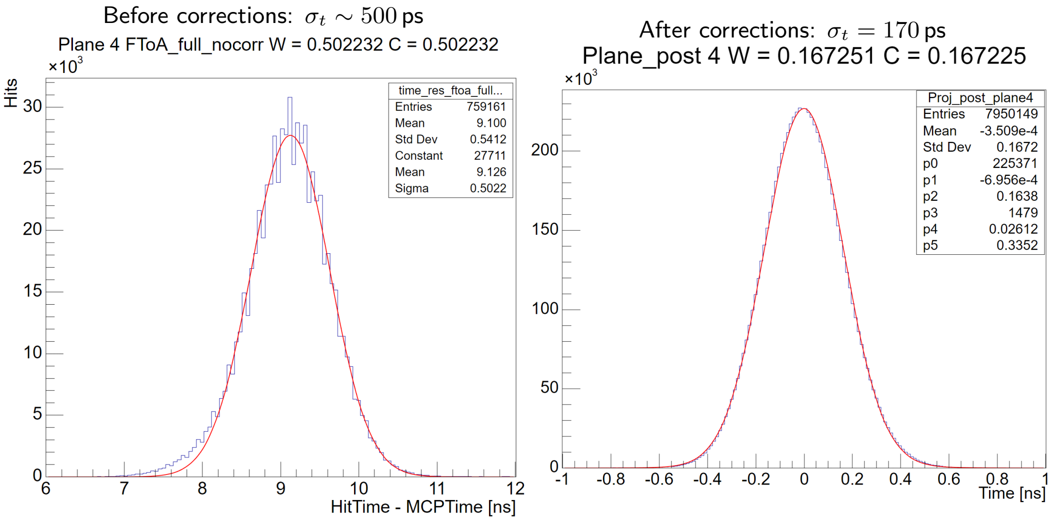
- Apply per-pixel corrections due to timewalk and VCO frequency variations
- Timewalk
  - Preamplifier has fixed rise-time → Time-to-threshold (TtT) amplitude dependent
  - Correct by fitting TtT distribution as function of charge per pixel with $TtT = \frac{a}{(Charge+b)^c} + d$
- VCO frequency corrections
  - Timepix4 timestamps given by 640 MHz voltage controlled oscillator (VCO) shared by 8 pixels
  - Variations of VCO frequencies lead to incorrect timestamps
  - Apply correction per VCO





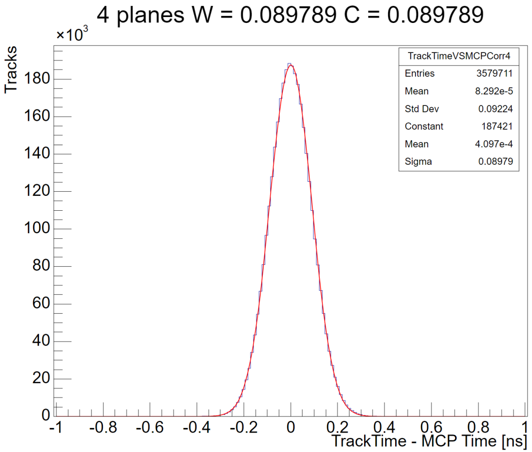


Time resolution



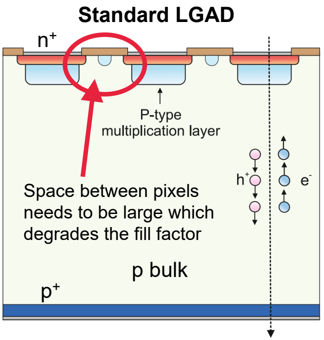
Track Time resolution

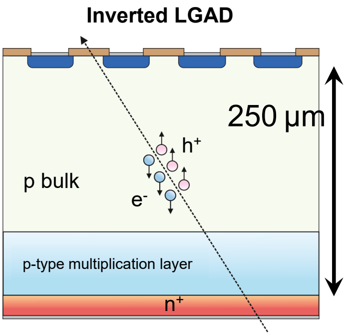
Track time resolution: $\sigma_t = 90$ ps

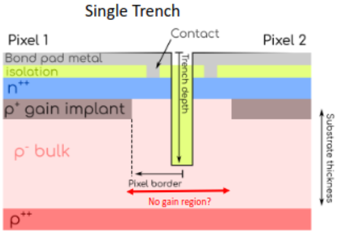


LGADs on Timepix4 as DUT (very preliminary)

- Low-gain avalanche diodes (LGADs) use charge multiplication to deliver larger input signals
- Small pixel size cannot be achieved in standard LGAD technology ($\sim 100\,\mu m$ dead area between pixels)
- Inverted LGADs (iLGADs) solve this by placing the gain layer on the backside
  - Sensors produced by Micron and provided by Glasgow ($250\,\mu m$ thickness)
- Trench-Isolated LGADs (TI-LGADs) reduce the dead area to $\sim 10\,\mu m$
  - Sensors produced by FBK for RD50 ($50\,\mu m$ depletion depth)

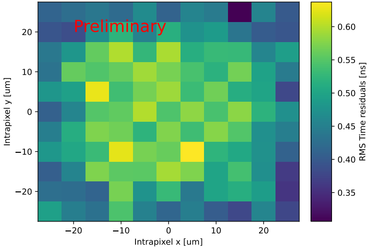


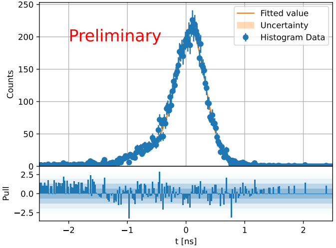




iLGAD time resolution (very preliminary)

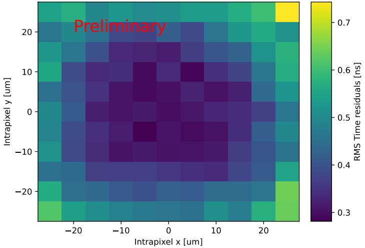
- iLGAD needs to be operated in h^+-collecting mode
- Long drift time due to large thickness ($250\,\mu m$)
- Need to operate at large threshold to not cross threshold from non-amplified signal already
- Cannot operate at threshold large enough (19 ke)
- Best time-resolution at edge of pixel: $240\,ps$
- Working to understand behaviour better and extract better time resolution

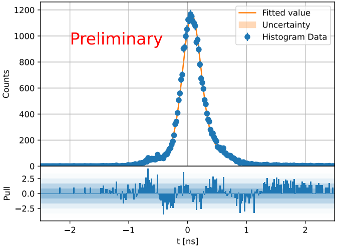




TI-LGAD time resolution (very preliminary)

- TI-LGAD operated in e^{-}-collecting mode
- Small drift time due to small thickness ($50\,\mu m$)
- Time resolution worse at edge or pixel due to trenches
- Best time-resolution at of pixel: $150\,ps$
- Working to understand behaviour better and extract better time resolution

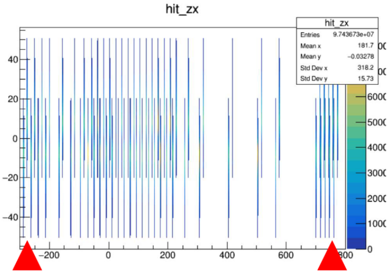




VELO simulation status

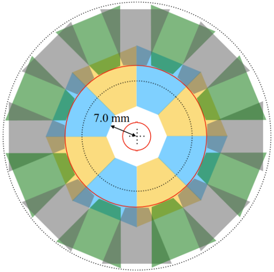
Current status (scoping document)

- Baseline model layout with 32 stations (Scenario X)
- Scoped Scenario H with 28 stations, reduced η-coverage and thicker RF-foil
- Problems present: Modules are currently spaced too closely for realistic installation
- Reconstruction for qualifying the detector fully present and working (full 4D tracking and 4D vertexing)



Path towards TDR

- Conceptual stage
  - Alternative designs to be proposed and tested against baseline
  - Adopt if alternative gives better results
- Start simulating more realistic detector scenarios (pixel dead areas, inefficiencies, actual spatial and time resolutions, etc.)



Space for ideas ("blue sky")

- Many things (e.g. clustering) will move from the FPGAs to the ASIC
- Free computing space for ideas on FPGAs (spatial ordering, support pattern recognition, etc.)