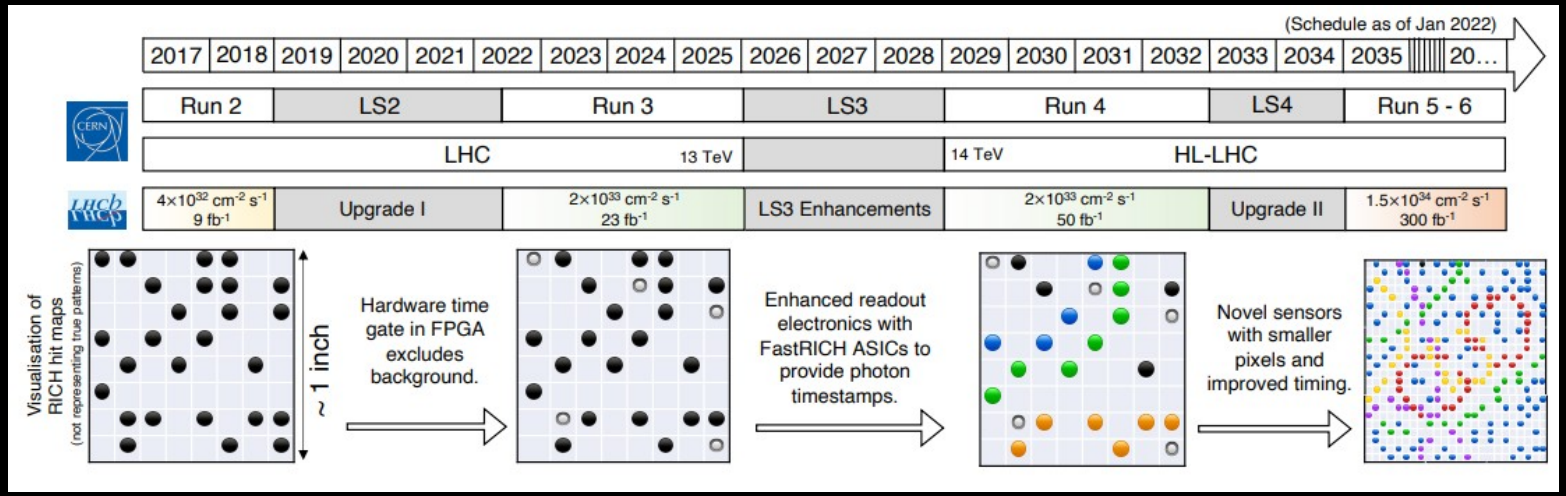
# LS3E and U2 electronics

- Overview
- Prototypes
- FastRICH
- Back-end

# Overview

## LS3E electronics

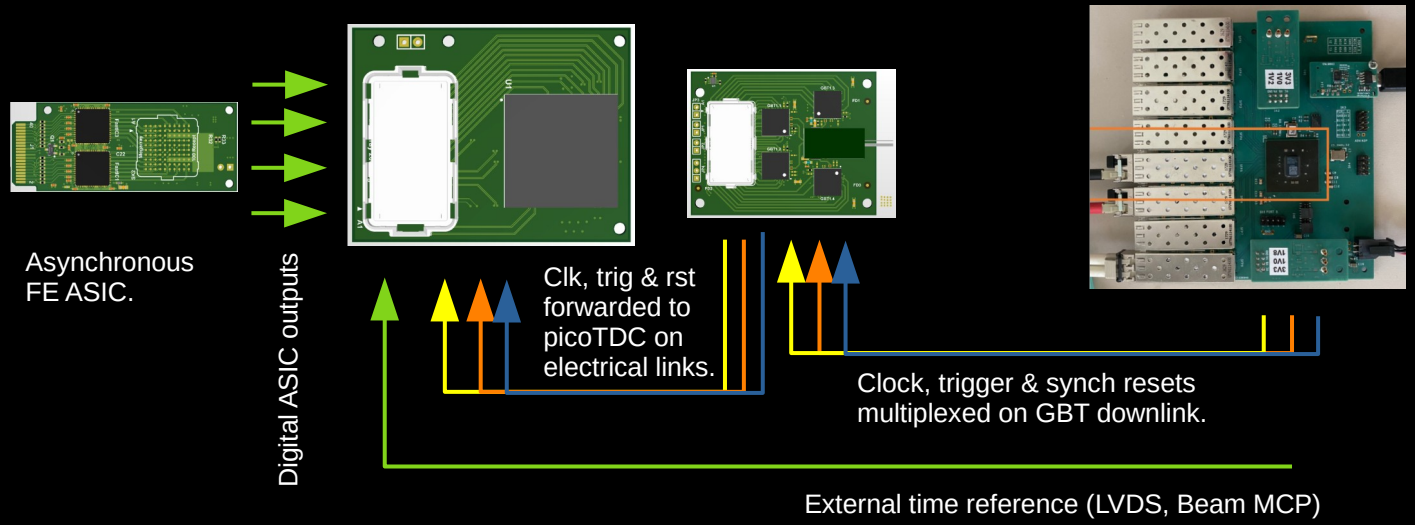
- Replace FE electronics but keep photon sensors same for Run4, new sensors for Run 5
- Benefit from longer LS3 to front-load some developments required for Upg2 (25ps time-resolved photon readout)
- Minimise other changes (power distribution, cooling infrastructure, mechanical envelope)
- Also
  - Back-end (pcie40) development
  - Reconstruction updates to exploit timing information



# Prototype development

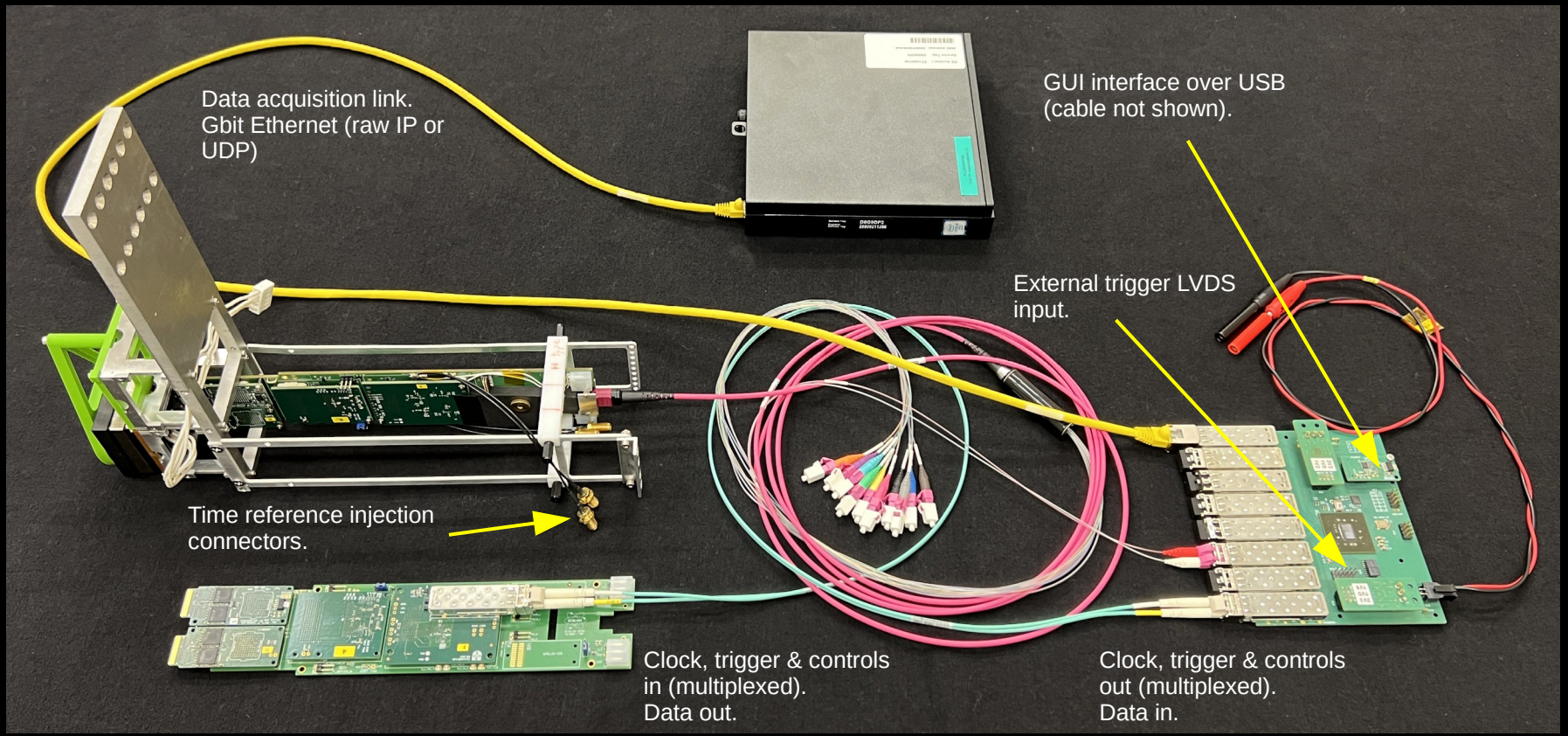
## Testbeam/lab electronics

- Light-weight, modular system developed for lab, beam tests
- Successful read out of ca. 500 photon sensor channels
- Good timing performance achieved in distributed system
- Excellent reliability at high data rate – many millions of events in a few days
- Next step – design a FastRICH plug-in



# RICH 2024 testbeam

## Hardware connections



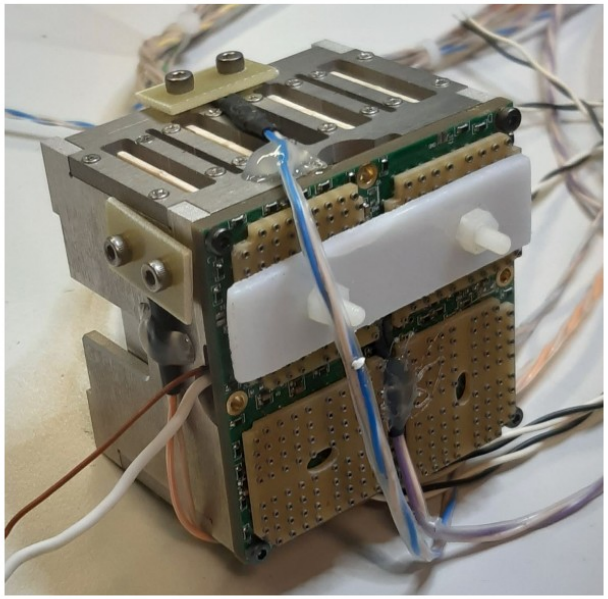
## EC thermal studies

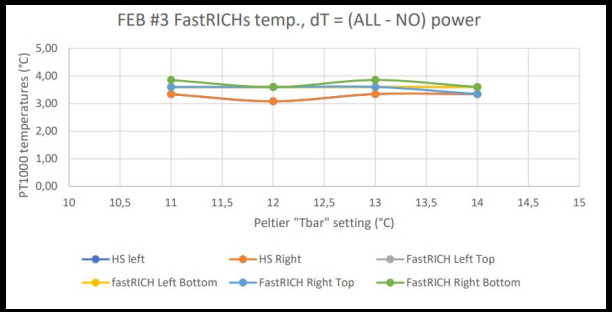
- https://indico.cern.ch/event/1427786/contributions/6005378/attachments/2886133/5058317/EC+_FASTRICH_cooling-27062024_SM.pdf

## EC thermo-mechanical design

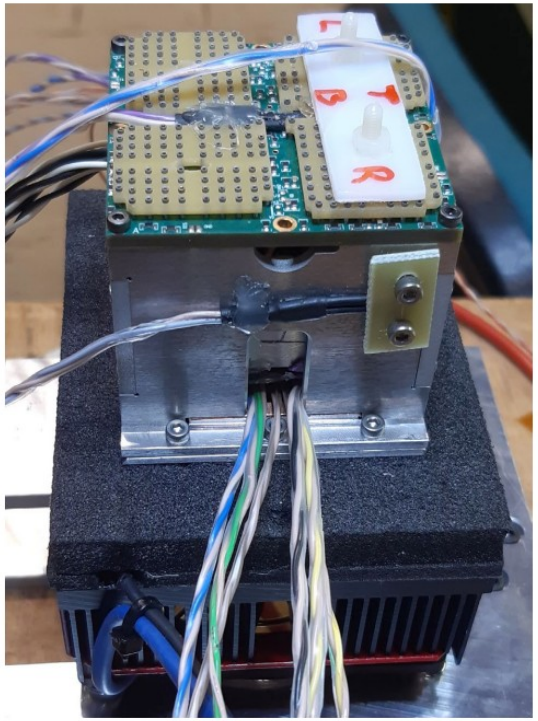
- Note: Modifications (even additional screw holes) of existing infrastructure difficult/impossible due to RP requirements
- Power load distribution shifts towards EC
- Thermal coupling of EC to cold spine is not ideal
- Mock-ups of new FastRICH EC under study (Genova)
- FastRICH power still uncertain (simulation/ estimation evolving)
- Must keep within constraints of existing power budget (Maratons)

EC+ Instrumented



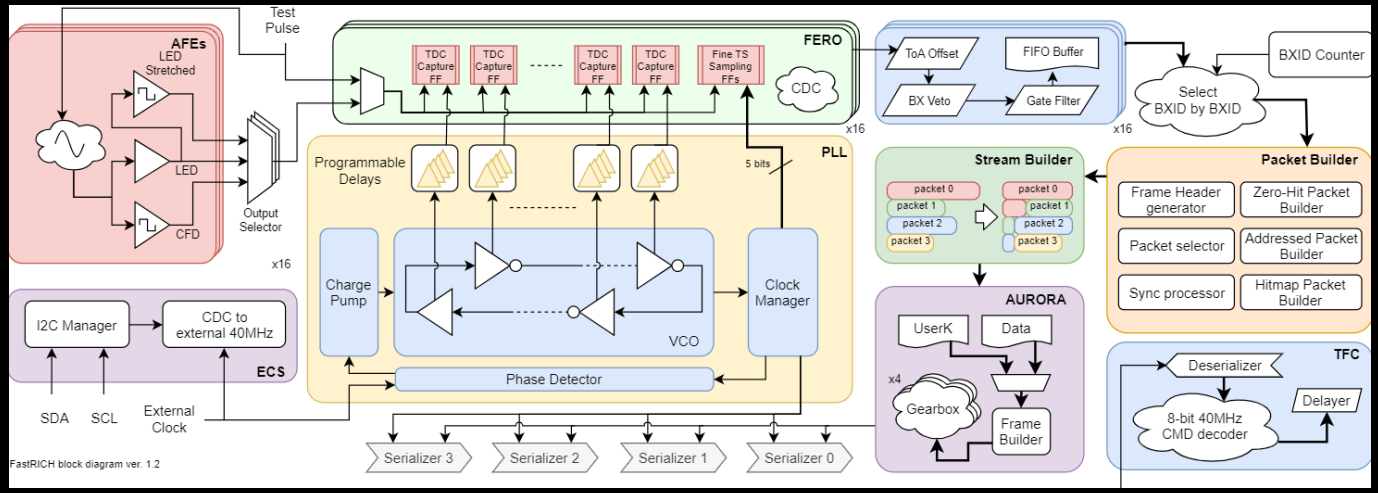



EC+ mounted on Peltier cell.



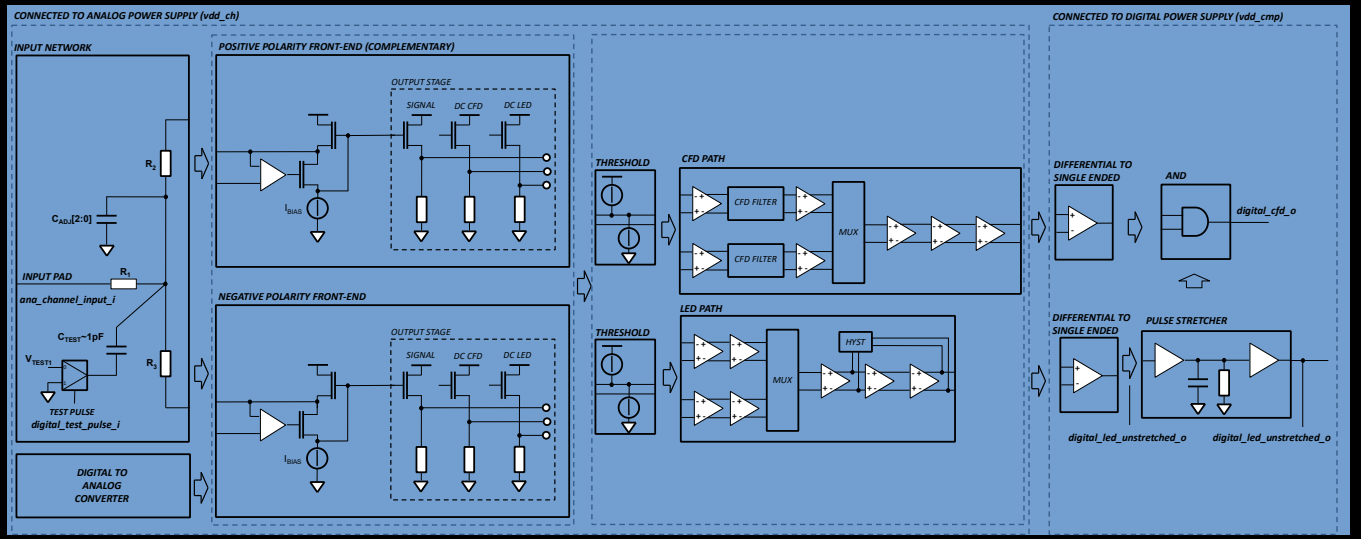
| FastRICH |
| --- |
| https://indico.cern.ch/event/1398911/ |

| Review 16th May 2024 |
| --- |
| Analogue |
| TDC |
| Readout |
| ECS |
| Verification |
| September submission |



# FastRICH

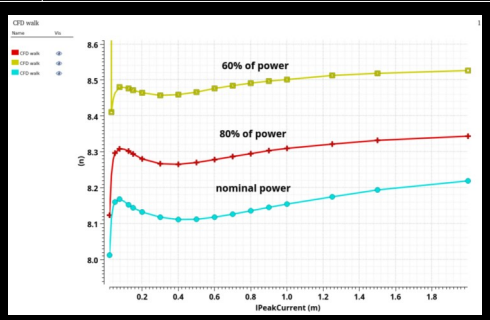
## Analogue

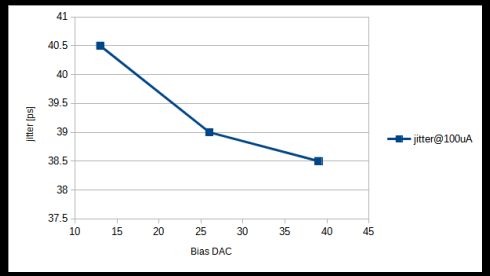


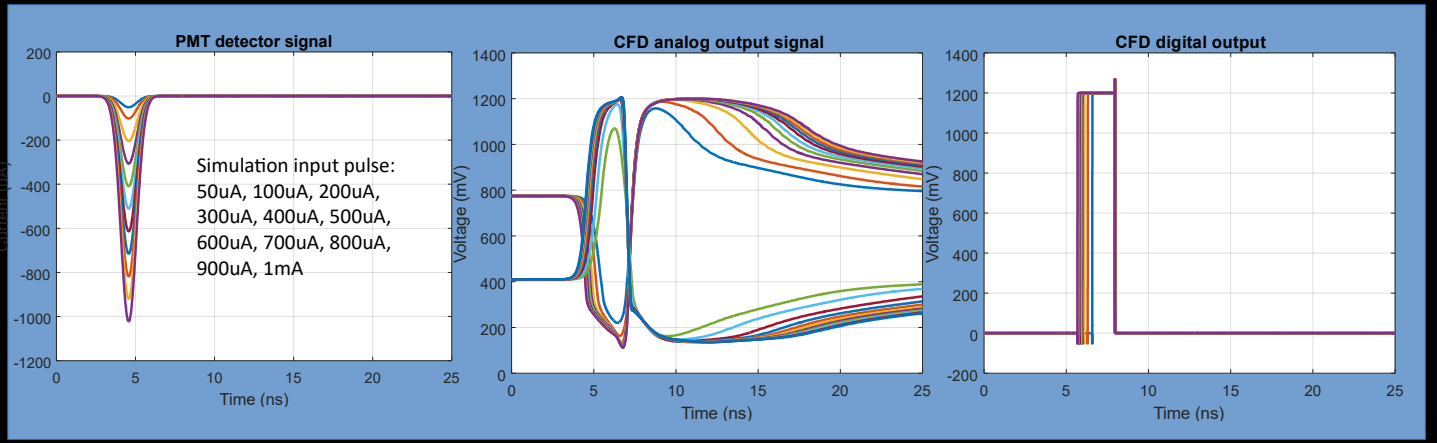

| Features |
|---|
| Positive or negative polarity |
| Test pulse injection |
| Constant fraction discriminator (CFD) or leading edge discriminator (LED) |
| Programmable gain and threshold |
| Differential signalling (internally) |

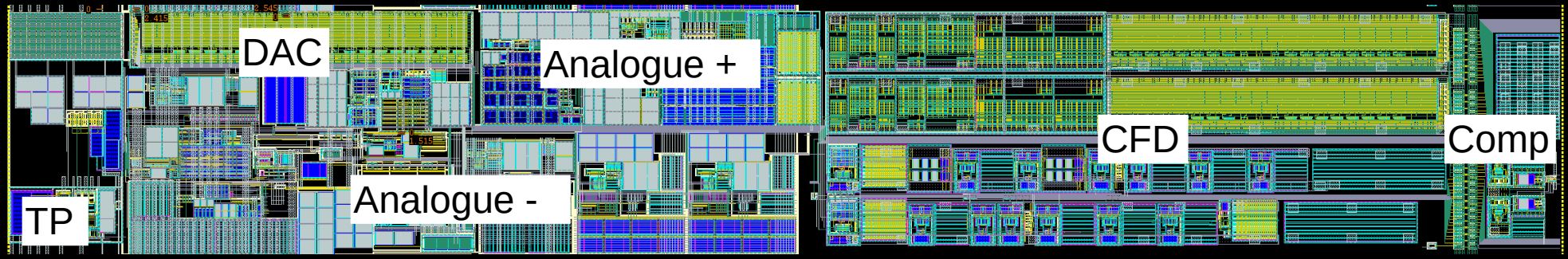
# FastRICH

## CFD simulations

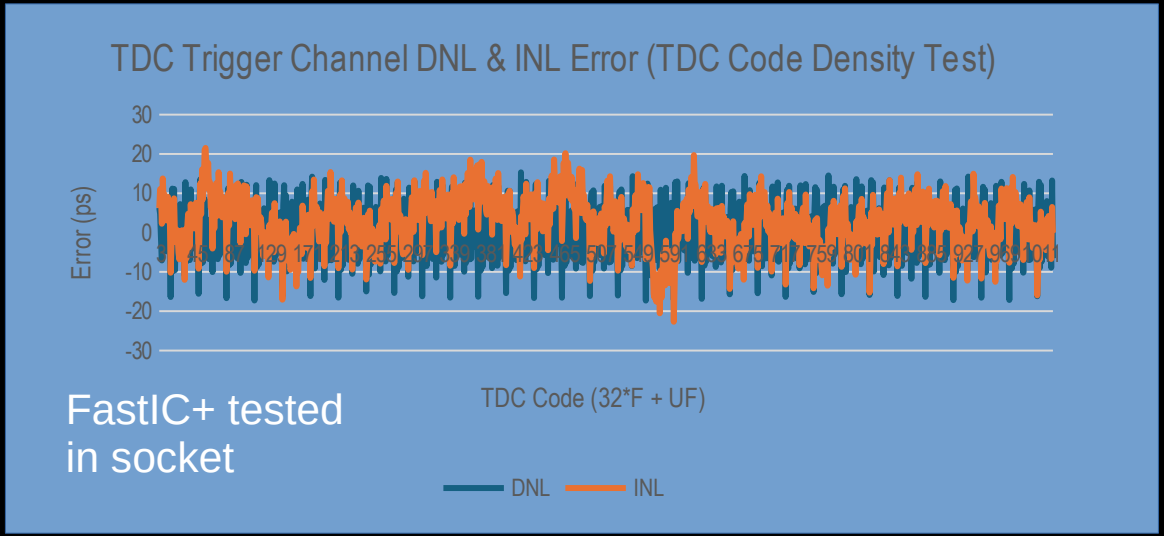


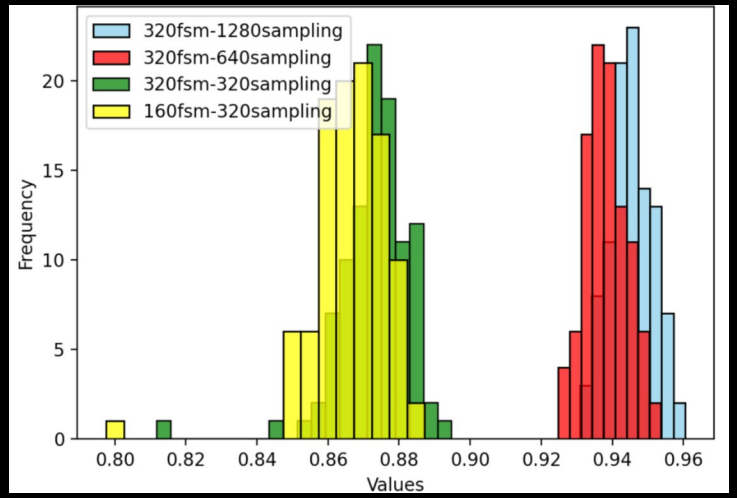



- FastRICH
  - FERO (TDC)




FastIC+ tested in socket

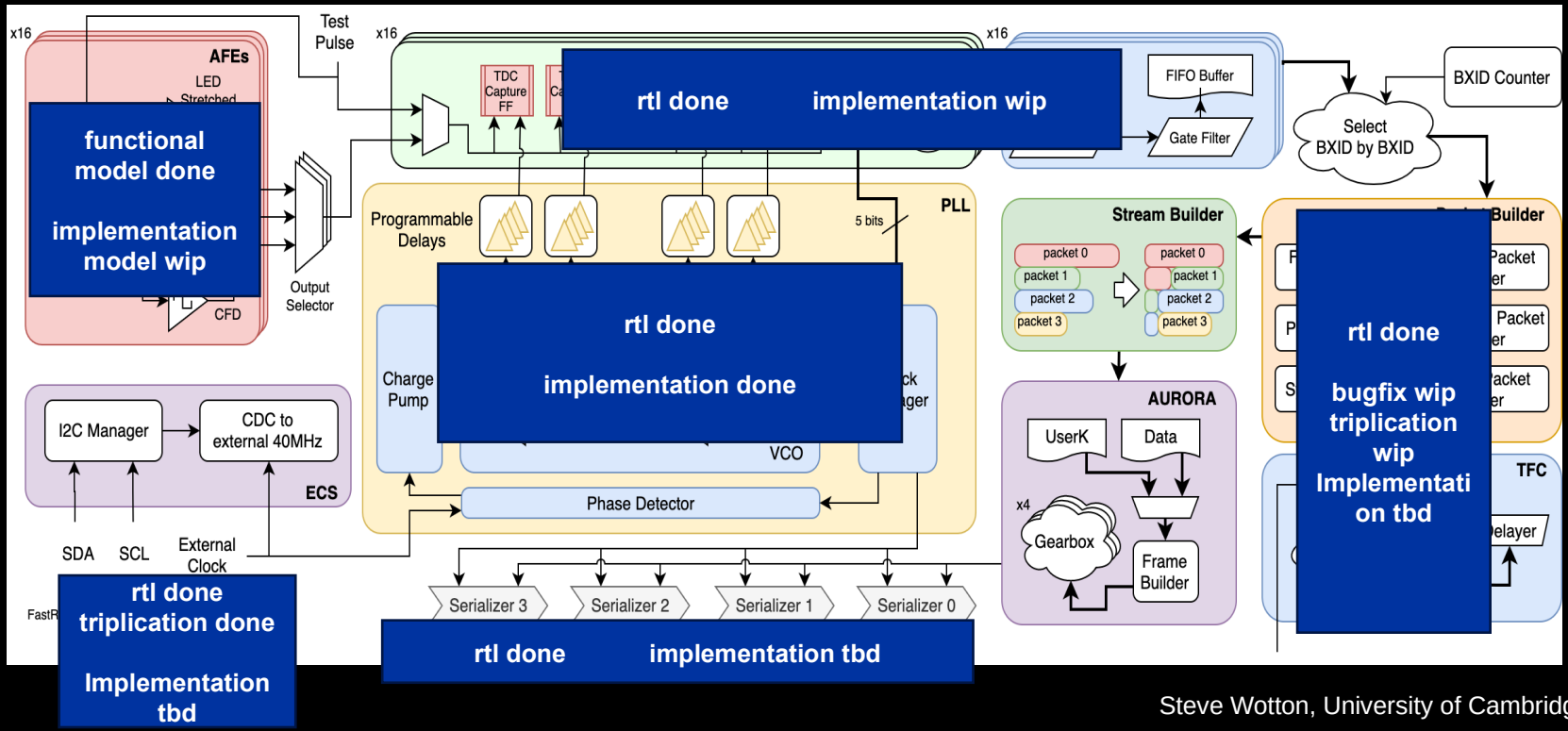



- Performance
  - TDC architecture largely verified in recent tests of FastIC+
  - Excellent DNL (6ps) & INL (+/-22ps), FastIC+
  - Jitter 14ps, FastIC+
  - Studies of FERO efficiency vs. clock ratios. 95% of hits from analogue registered.

# FastRICH

## Dataflow

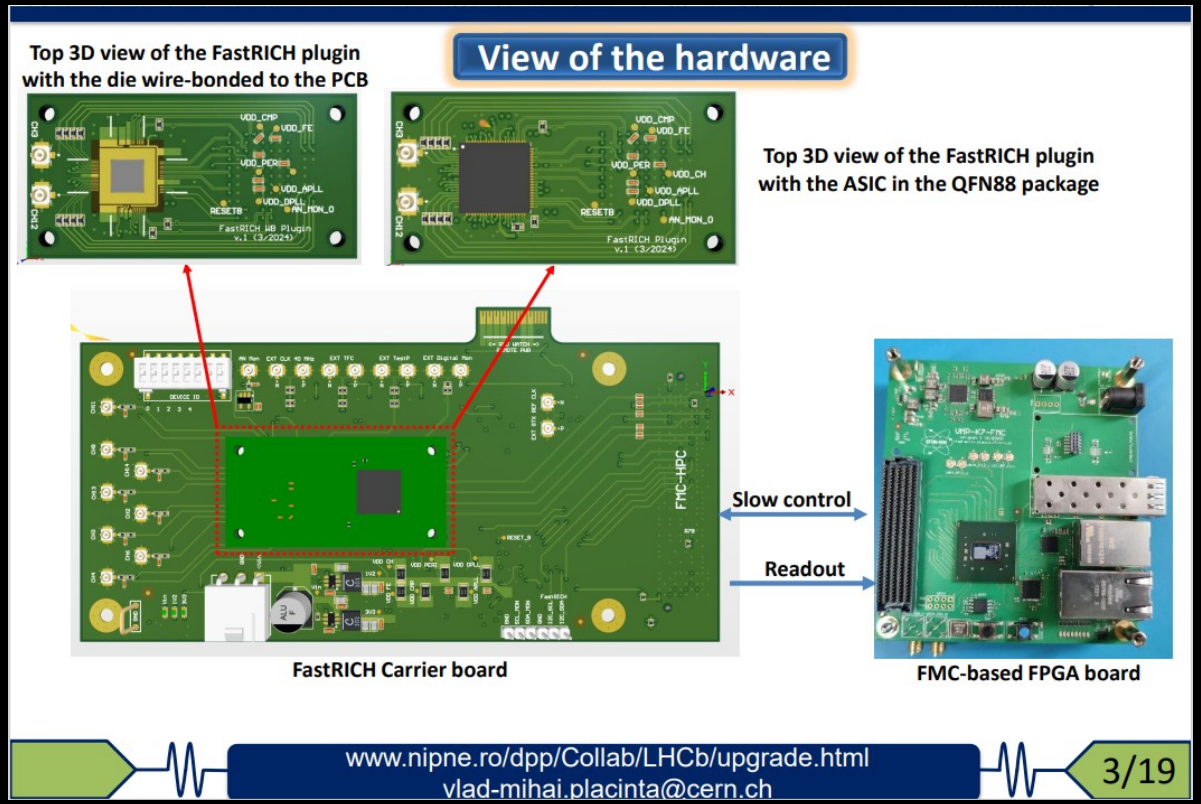
| Status (at review, A. Paternò) |
|---|
| PLL: post-layout characterization done |
| TDC Block: RTL Done, implementation ongoing |
| Packet and Frame Builder: RTL almost complete |
| AURORA: RTL done |
| Top Digital block: RTL almost complete, triplication and synthesis starting soon |



# Test environment

## Single ASIC functional testing (hardware verification)

- Bespoke test station under development (Bucharest)
- Semi-automatic testing of MPW devices (100's), wire bonded or QFN88
- Add automated ASIC handling for production volumes
- Full functional testing to confirm:
  - Configuration functionality and reliability
  - Analoque performance and CFD operation
  - TDC operation
  - Timing resolution
  - Readout functionality for all data lane configurations
  - Response of FastRICH to TFC
  - Yield



# LS3E BE development

| Planning |
| --- |
| Work needs to start on BE firmware |
| A few areas identified for priority development (e.g Aurora handling in BE FPGA) |
| Invite contributors from RICH, ASIC and on-line teams |
| Contributions also needed to help develop controls software, specify testing protocols and help design testing environments |
| Define tasks, assign responsibilities and agree timescales |
| A preliminary meeting of interested parties has taken place – “hands on” session planned in August |

| Summary of required BE development |
| --- |
| LpGBT core implementation for pcie40 (similar to current GBTX core) |
| Aurora receiver FPGA firmware (FPGA resource-sensitive design) |
| LHCb data synchronisation logic (response to TFC commands) |
| RICH data packet building (merging Aurora lanes into events) |
| Porting of firmware to pcie400 when available |

# LS3E schedule