Controls and software status for the HL-LHC IT String

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On behalf of the IT String team

The HL-LHC IT String facility includes accelerator systems such as power converters, quench protection, cryogenics, insulation vacuum and alignment. The applications for the system controls and for the operation of the HL-LHC IT String facility compose a three-layer architecture. The front-end layer is composed of Programmable Logic Controllers (PLC) or Front-End Computers (FEC). The systems' layer is composed of monitoring, control, and supervisory applications. The operation layer is composed of supervisory, sequencer, and magnet circuit test analysis applications. As a preparation of the HL-LHC commissioning phase, the definition of all the required software interfaces, in line with the HL-LHC era, is essential to guarantee the suitable operation of the String facility control system. The readiness status of the controls and software is reported. The Dry Run tests are essential to validate the operation applications and the complete control system before the cooling and the powering test phase of the HL-LHC IT String commissioning program.
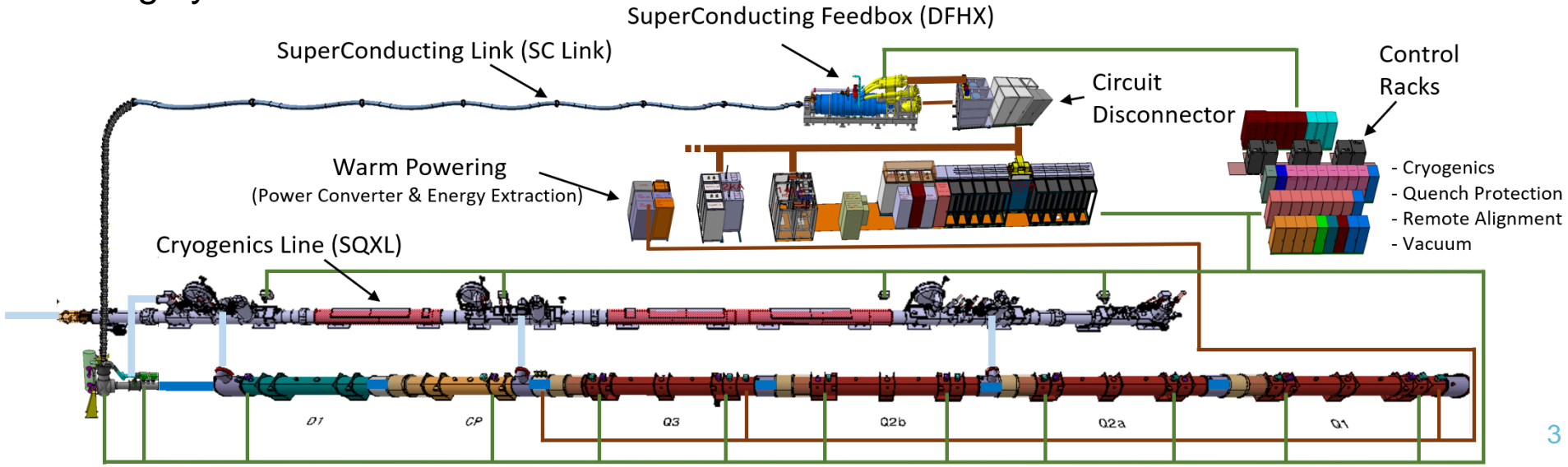
HL-LHC Inner Triplet String Day IV - https://indico.cern.ch/event/1408524/timetable/

Outline:

- Introduction
- Architecture&Readiness
- Frameworks&Development
- Configuration&Logging
- Access Controls
- Interfaces
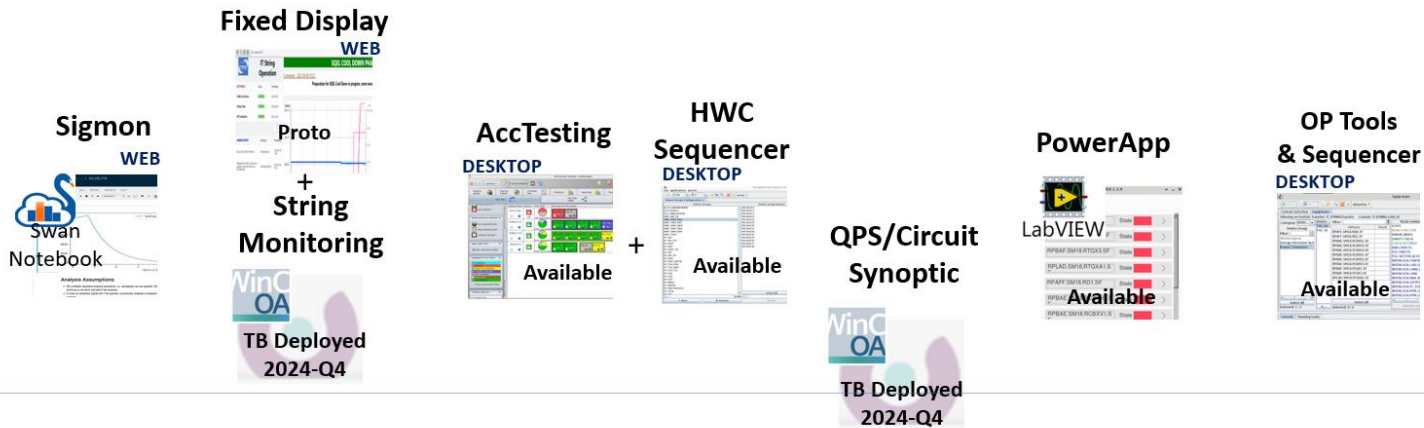- Schedule
- Organization
- Conclusion

Introduction

- The String Facility needs an effective operation software layer to achieve the controls, diagnostics, logging and analysis of the HWC and String specific tests program.
- Includes the controls of vacuum (VAC), cryogenics (CRYO), power converters (PC), quench protection (QPS), alignment (FRAS), and all the software required for the OPERATION & ANALYSIS
- Highly interconnected with both hardware and software interfaces.
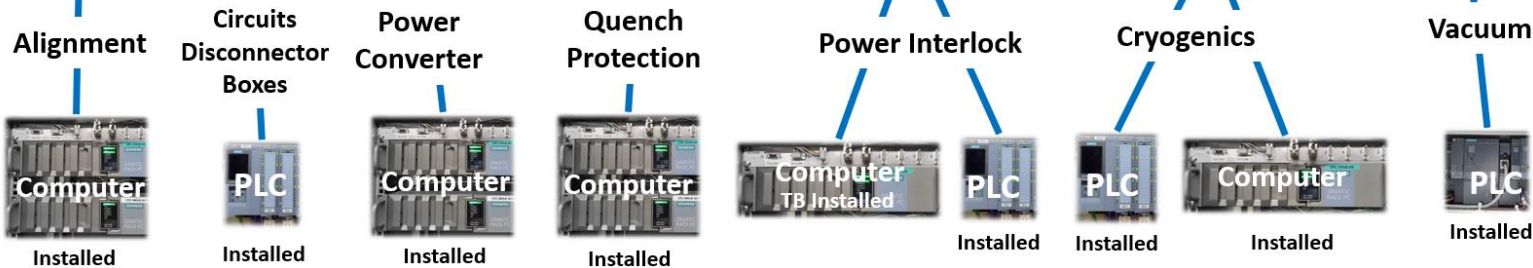
Architecture & Readiness

Operation & Analysis Application Layer

- Sigmon — WEB — Swan and Notebook
- Fixed Display — WEB — Proto + String Monitoring — WinCC OA — TB Deployed 2024-Q4
- AccTesting — DESKTOP — Available
- HWC Sequencer — DESKTOP — Available
- QPS/Circuit Synoptic — WinCC OA — TB Deployed 2024-Q4
- PowerApp — LabVIEW — Available
- OP Tools & Sequencer — DESKTOP — Available

Systems Application Layer

- FRAS — At String 2025-Q1 — WinCC OA
- CDB — WinCC OA — Final Version
- FGC — WEB — Available
- QPS — DESKTOP — Energy Extraction
- PIC — WinCC OA — Operational Version
- CRYO & CIET — WinCC OA — SQXL Version
- VAC — WinCC OA — SQXL Version

Front-End Layer

- Alignment — Computer — Installed
- Circuits Disconnector Boxes — PLC — Installed
- Power Converter — Computer — Installed
- Quench Protection — Computer — Installed
- Power Interlock — Computer — TB Installed / PLC — Installed
- Cryogenics — PLC — Installed / Computer — Installed
- Vacuum — PLC — Installed
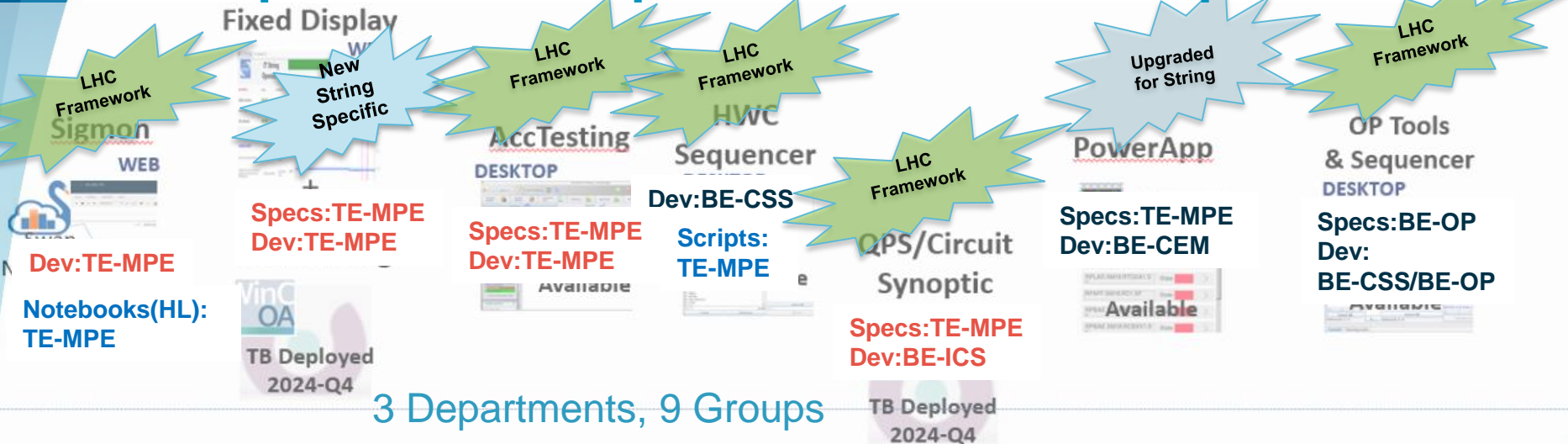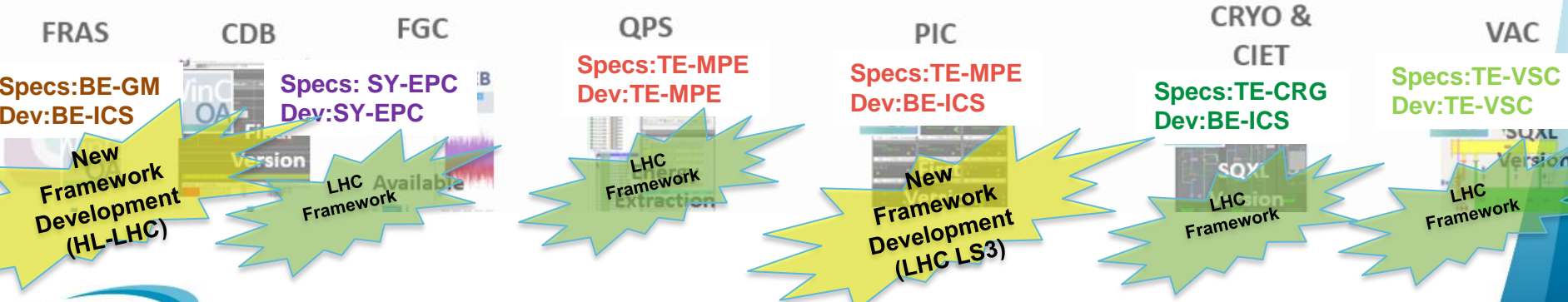
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Frameworks & Development

- Based on:
  - **Industrial control** systems (Vacuum, Cryogenics, CDB, PIC)
  - **FESA** accelerator control systems (Power Converter, QPS, FRAS)
  - Accelerator **standard commissioning, operation and diagnostic software** (AccTesting, HWC Sequencer, e-logbook, OP tools, SWAN notebooks)

- **Use frameworks**: FESA, UNICOS/JCOB, LSA/InCA, SWAN notebooks, WebApp framework (Spring, React…)

- Use commercial software applications (for Industrial controls): WinCC OA ™

- **No specific framework development:** LHC or HL-LHC developments

- Operation software configured with Accelerator Databases (CCDB, LSA DB, Layout DB)

Responsabilities specifications & development

Fixed Display

LHC Framework

New String Specific

LHC Framework

LHC Framework

Upgraded for String

LHC Framework

Sigmon WEB

AccTesting DESKTOP

HWC Sequencer

PowerApp

OP Tools & Sequencer DESKTOP

Dev:TE-MPE

Notebooks(HL): TE-MPE

**Specs:TE-MPE
Dev:TE-MPE**

**Specs:TE-MPE
Dev:TE-MPE**

Dev:BE-CSS

Scripts: TE-MPE

LHC Framework

QPS/Circuit Synoptic

**Specs:TE-MPE
Dev:BE-ICS**

TB Deployed 2024-Q4

**Specs:TE-MPE
Dev:BE-CEM**

**Specs:BE-OP
Dev: BE-CSS/BE-OP**

TB Deployed 2024-Q4

3 Departments, 9 Groups

FRAS

CDB

FGC

QPS

PIC

CRYO & CIET

VAC

**Specs:BE-GM
Dev:BE-ICS**

**Specs: SY-EPC
Dev:SY-EPC**

**Specs:TE-MPE
Dev:TE-MPE**

**Specs:TE-MPE
Dev:BE-ICS**

**Specs:TE-CRG
Dev:BE-ICS**

**Specs:TE-VSC
Dev:TE-VSC**

New Framework Development (HL-LHC)

LHC Framework

LHC Framework

New Framework Development (LHC LS3)

LHC Framework

LHC Framework

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String Controls Configuration & Logging

Configuration:

- AccTesting and HWC Sequencer have a **unique source for parameters**: **LSA DB**.
- All the layout information is populated from Layout DB to LSA DB.
- **Other parameters, test definitions, sequence attributes** are populated from test procedures to LSA DB (See presentation "IST, SCT and Powering Test for the HWC").
- Sequences are coded in HWC sequencer according to **test procedures**, **sequence transition** conditions coming from equipment owner.

Logging:

- Logging to NxCALS - CERN Accelerator Logging Database
- Logging to Post Mortem DB - high-rate logging for post-mortem event analysis.
- Supervisory Application logging (SCALAR DB) – better granularity than NxCALS

Access Control and Test Signatory

- FESA device: Group of devices with access rules based on **RBAC roles and locations**

- Signatory of tests: **Expert RBAC roles**

- Vacuum/Cryogenics/PIC/FRAS devices: Supervisory Application **Specific permissions** policy based on **Access Domains** and LDAP authentication
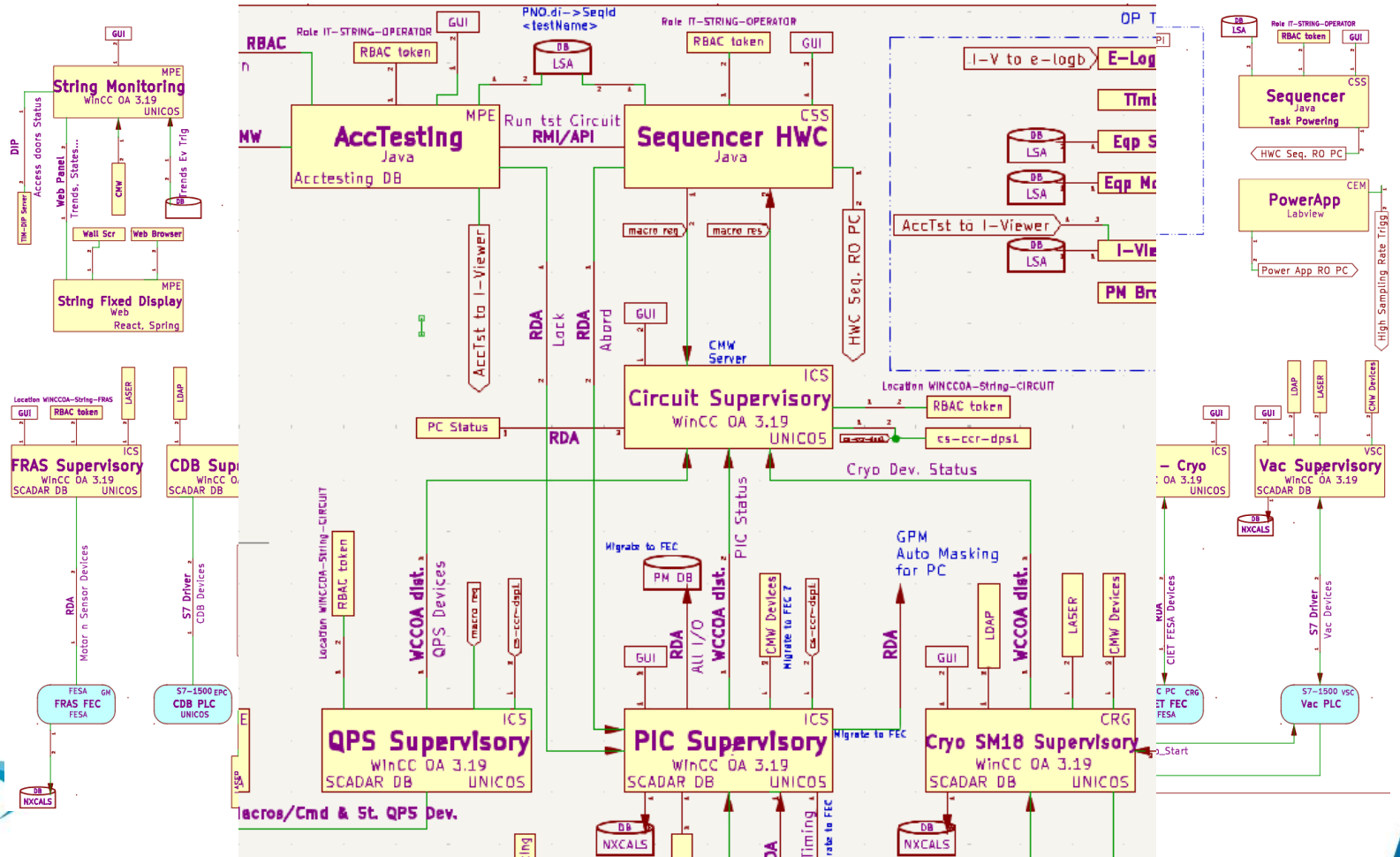
Interfaces

Goal: **Not specifications** but intends to **check** that all the required interfaces has been implemented.

Only interfaces between different systems or services are considered:

- HW alarm signals between systems
- HW Central Timing ↔ FEC
- PLC ↔ PLC
- Supervisory application ↔ FESA devices
- **AccTesting/HWC Sequencer ↔ Devices/Applications**
- **Configuration DB (CCDB, LSA DB) ↔ Applications**
- Applications ↔ Logging NxCALS/Post Mortem
- Applications ↔ Applications

- ~60% of the interfaces are available and ~40% tested during commissioning, SCT, Dry Run 1 (estimation not taking into account the weight of interfaces)
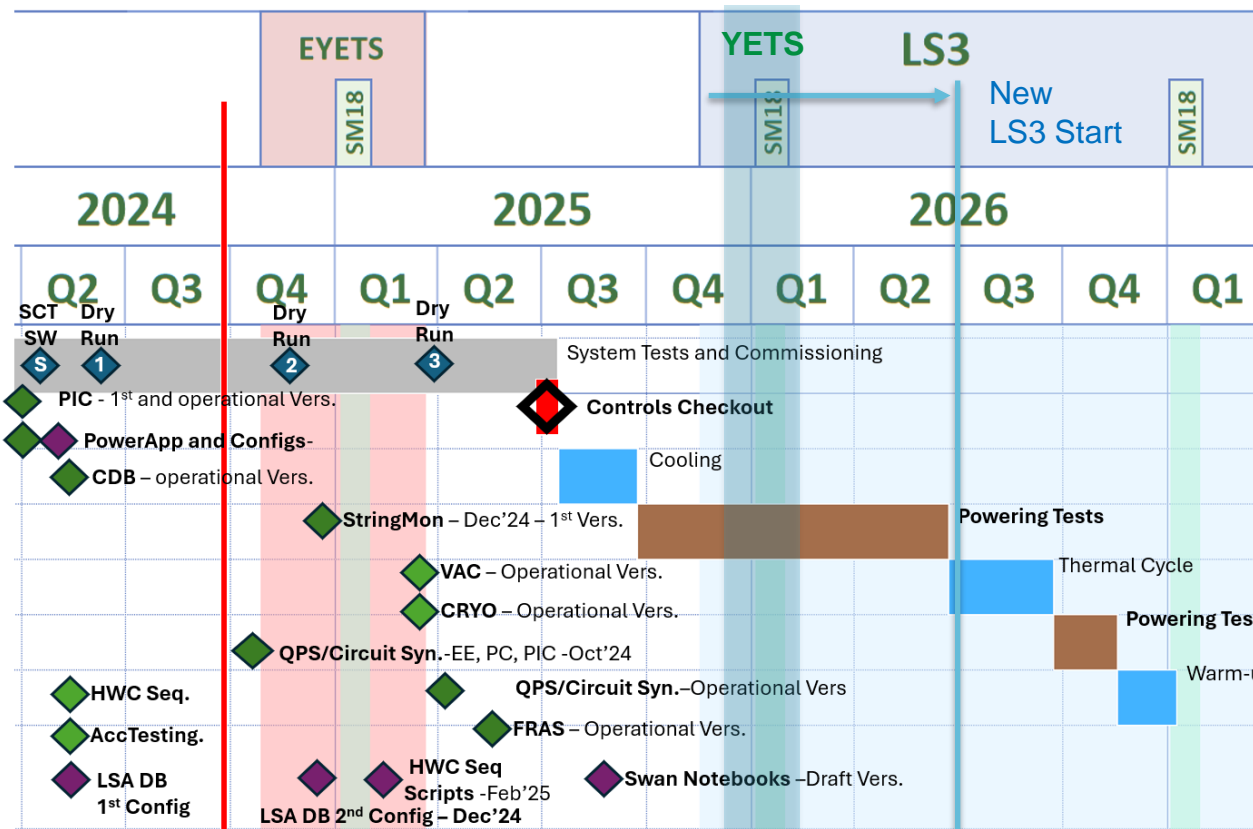
Milestones

Commissioning and Dry Run1 Checks and Validation

Dry Run 1 2024-Q2

Dry Run 1 2024-Q3

Sigmon
WEB

Swan Notebook

Fixed Display
WEB

Proto
+
String
Monitoring

WinCC OA
TB Deployed

AccTesting
DESKTOP
Available

HWC Sequencer
DESKTOP
Available

QPS/Circuit Synoptic
WinCC OA
TB Deployed

PowerApp
LabVIEW
Available

OP Tools & Sequencer
DESKTOP
Available

SCT 2024-Q1

**SCT 2024-Q1
Dry Run 1 2024-Q2**

SCT 2024-Q1

SQXL Cool Down 2023-Q3

FRAS
At String
2025-Q1
WinCC OA

CDB
WinCC OA
Final Version

FGC Portal Apps
WEB
Available

DB Configured

QPS
Energy Extraction

PIC
WinCC OA
First Operational Vers.

CRYO & CIET
WinCC OA
SQXL Version
SQXL Vers.

VAC
WinCC OA
SQXL Vers.

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Dry Run 1

Environment:
- Power Converters are operated in **Simulation Mode**.
- Access RBAC limits the access to **IT String devices only**.
- Configuration Database: LSA DB "NEXT" schema of **DEV environment.**
- LSA DB configured with circuits, power converters, parameters (but not all), and tests definition (TE-MPE, BE-OP, BE-CSS).

Objectives and results:
- Validation of PowerApp LabVIEW software
- Configuration of LSA DB with the additional information required for the Dry Run tests.
- Check String instance AccTesting and HWC Sequencer application.
- Interface checks:
  - AccTesting ↔ LSA DB
  - AccTesting ↔ HWC Sequencer
  - HWC Sequencer ↔ LSA DB
  - HWC Sequencer ↔ FGC Devices

Next Dry Runs

Dry Run 2 objectives:
- Test Interfaces AccTesting/HWC Sequencer with remaining devices: PIC, Energy Extraction,...
- Test Post Mortem Triggering.
- Check/update HWC sequencer sub-routine

Dry Run 3 objectives and outcome :
The conditions to be able to **proceed with the Dry Run depends on the availability of devices.**
- Test complete sequences involving all connected components.
- Test the global behaviour of available circuit devices.
- Optimize the HWC sequencer routine/sub-routine for HL-LHC.
- Test interfaces with analysis software (SWAN notebooks)
Trigger the coding of the remaining HL-LHC HWC test sequences.

Organization

- Coordination and follow-up meetings to address the **readiness and availability** of **applications/functionalities**

- Topical meetings to address the **implementation**/availability of **interfaces, configuration of DB**, and **coding of HWC sequences**.

- **Dry Runs** and control **Checkout** to check the **operational devices** instantiation and functionality of **interfaces.**

- **Hardware interfaces tests** integrated in Q&A plan (See presentation "Quality Assurance & Control").

Conclusion

- Front End **Hardware** (FEC, PLC, DIOT), Servers (Supervisory Applications) are **installed and available**.
- An estimated of ~70% of the **applications** are available and operational (but not necessary with all the functionalities and devices)
- ~60% of the **interfaces** are available and 40% tested (during commissioning, SCT, Dry Run 1)
- Intensive validation and **tests** of the software and it interfaces (during **Dry Runs**)
- **Positive feedback** on the functionalities & performance of the already tested and operational applications (from Commissioning, SCT & Dry Run tests)
- Still a lot of work for the **configuration**, **sequences** implementation, **tests**, and **learning** of operation applications and tools.
- Risk not completing the Dry Runs before Magnets ready.
- With the **Dry Run** tests the goal is to **test, check, validate, optimize, give feedback,** and **train** team.
- The conditions to be able to **proceed with the Dry Runs depends on the availability of devices.**
- LS3 start delay is beneficial (accelerator **control services availability**) but the impacts during YETS and LS3 (mid-2026-2027) remain a concern and will be addressed.

Spare Slides

Stakeholders…

PIC: Alain Antoine (TE-MPE), Michal Kalinowski (TE-MPE), Jesus Cortes (BE-ICS)

Cryo: Antonio Tovar-Gonzalez (TE-CRG), Thomas Barbe (TE-CRG), Nikolaos Trikoupis (TE-CRG), Alexandros Foivos Kostopoulos (BE-ICS)

Vacuum: Andre Rocha (TE-VSC)

Supervisory QDS, PIC, Circuit: Alexandros Foivos Kostopoulos, Enrique Blanco Vinuela (BE-ICS), Brad Schofield (BE-ICS), Lukasz Goralczyk (BE-ICS)

QPS Expert/AccTesting/Sigmon/Post-Mortem: Daniel Wollmann (TE-MPE), Aleksandra Mnich (TE-MPE), Jean-Christophe Garnier (TE-MPE), Marc-Antoine Galilee (TE-MPE), Gustavo Enrique Sanchez (TE-MPE)

QDS: Reiner Denz (TE-MPE), Tomasz Podzorny (TE-MPE), Jens Steckert (TE-MPE)

FRAS: Mateusz Sosin (BE-GM), Borja Fernandez Adiego (BE-ICS)

HWC Sequencer/LSA/InCA: Michi Hostettler (BE-CO), Lukasz Burdzanowski (BE-CSS), Maciej Peryt (BE-CSS), Roman Gorbonosov (BE-CSS)

PowerApp: Hubert Reymond (BE-CEM), Patryk Dawid Jankowski (BE-CEM), Alvaro Martinez Landete (BE-CEM)

… Apologies for those I have certainly forgotten in this non-exhaustive list

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