WP11 Reporting period 2

CERN 20 jun 2024

WP 11

Microelectronics

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WP11 Objectives

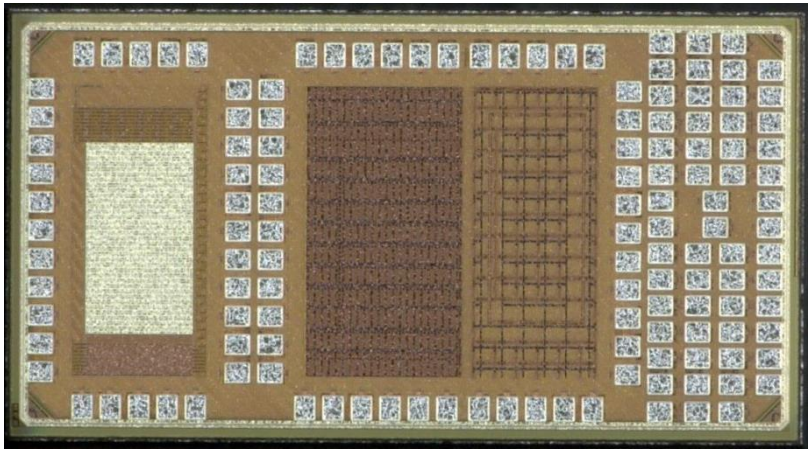
- **Task 11.1. Coordination and Communication [CNRS+INFN]**

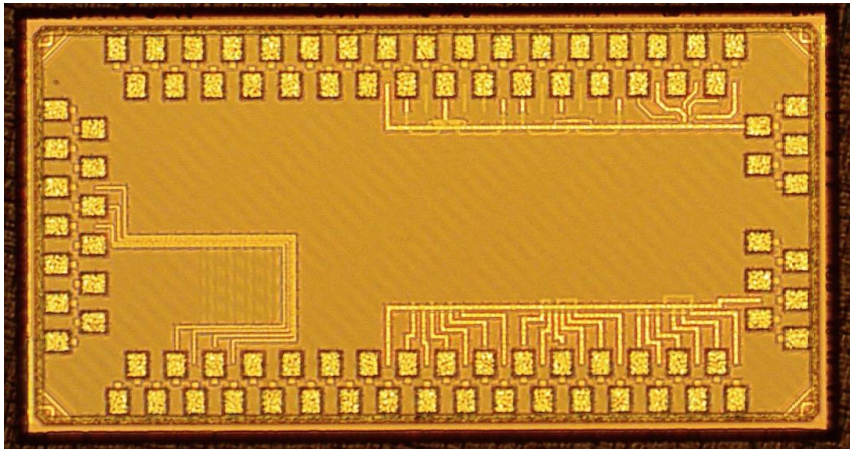
- **Task 11.2. Exploratory study of advanced CMOS (28 nm)**
  - INFN PV, AGH, CNRS CPPM, UBONN
  - Explore advanced 28 nm CMOS for future trackers AGH, CNRS CPPM
  - Design and test front-end prototypes INFN PV, UBONN
  - Milestone MS45 and deliverable D11.1

- **Task 11.3. Networking and ASICs for other WPs (65/130 nm)**
  - AGH, CNRS OMEGA, IP2I, DESY, INFN (BA, BO, PV, TO) Uni Heidelberg, WEEROC (industry)
  - Cold and timing ASICs in 65/130nm CMOS : CNRS OMEGA, IP2I
  - MPGD readout ASICs : INFN (BO, TO)
  - Silicon and SiPM readout ASICs for future colliders and timing applications : AGH, CNRS OMEGA, DESY, UniH, WEEROC
  - Milestone MS46 and delivierable D11.2

WP11.2 deliverable

- D11.1 : MPW in 28 nm
  - 2 chips submitted by CNRS/CPPM and INFN PV/BG fabricated mid 2023
  - Deliverable exists but report delayed





28 nm @CPPM

28 nm chip design

R&D on hybrid pixels

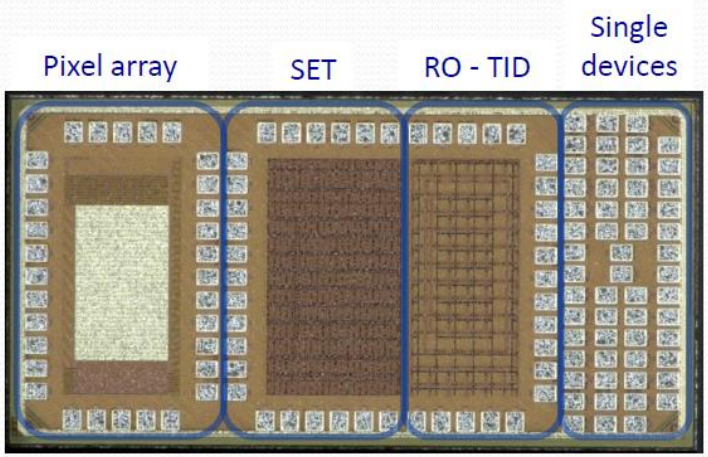
- Process qualification in terms of performance for analog, low-power and low-noise circuits
- Architecture studies
- Fast charge amplifier array

Study of Single Event Effects (SEE)

- Measure the SET cross-section
- Measure the SET pulse width with a good resolution < 20 ps
- Measure the effect of the std cell size

TID tests and qualification

- Compatibility with typical dose levels for future projects
- 28 nm process device qualification
- Gate delay evolution with TID and the effect of the std cell size
- TID Effects modeling → Analog and digital simulations with TID effects

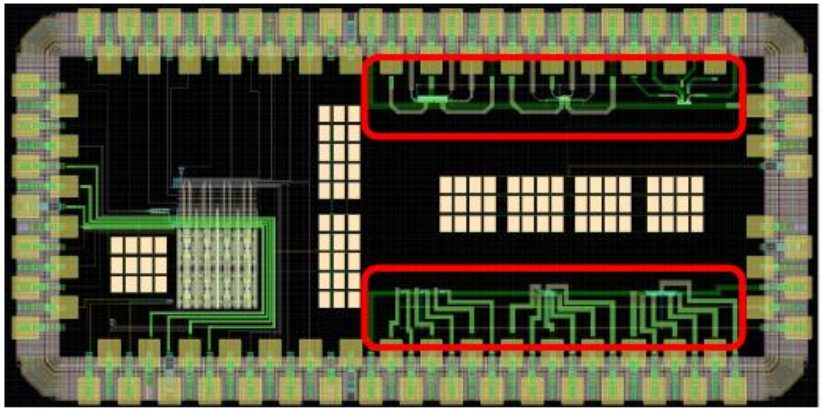


Mini@sics of 2×1 mm2 received June 2024, consisting of 4 main blocks

- Analog pixel array (25×25 µm2) with Fast charge amplifiers for high time resolution
- SET test structures
- Ring Oscillators for TID tests on digital standard cells
- Test structures for TID tolerance studies

Technology characterization

- 18 differently sized core, standard-threshold devices, both P-channel and N-channel in triple well
  - channel length: 30 nm, 60 nm and 180 nm
  - channel width: 100 um, 200 um and 600 um (finger width Wf = 2.5 um -> 40 , 80 and 240 fingers)



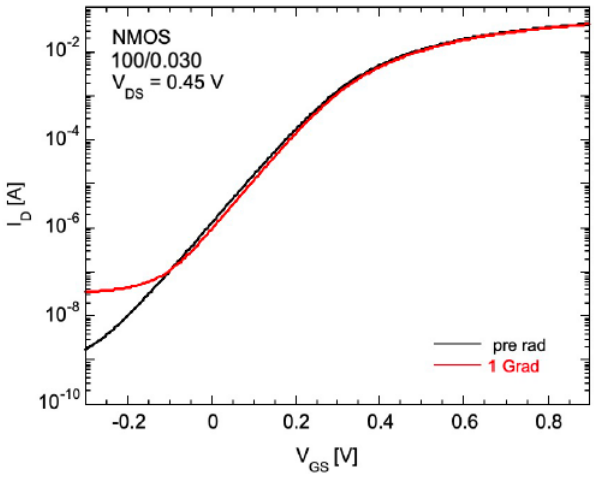
- **Static and signal parameters** measured with an Agilent B1500A Semiconductor Parameter Analyzer
- **Noise power spectral density** measurements carried out with an HP4395A Network/Spectrum Analyzer and a noise amplification system
  - Drain current in DUTs: from 50 µA to 500 µA → low power operation as in high density front-end circuits

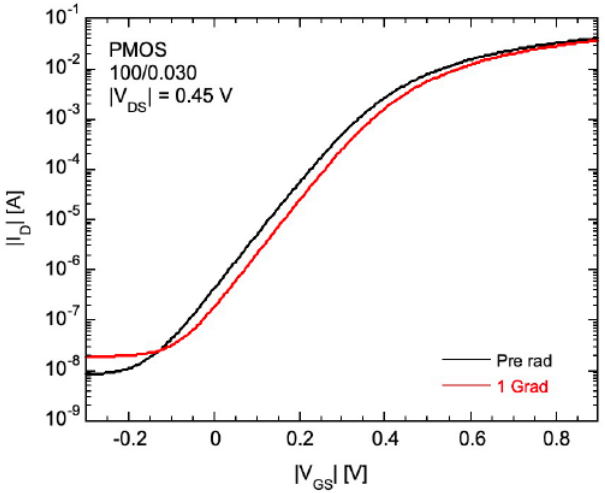
Ionizing radiation effects

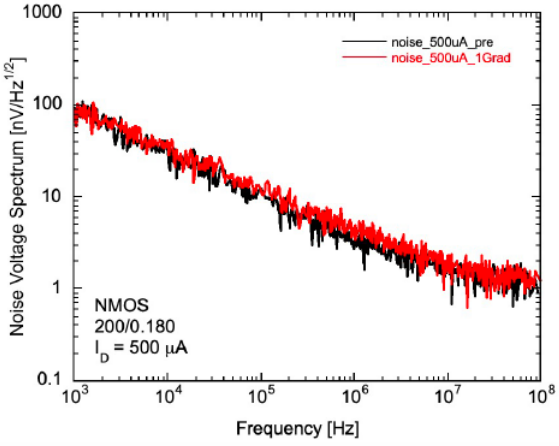
- Investigated devices **irradiated up to 1 Grad(SiO_2)** total dose with X-rays (5.5 Mrad/h dose rate)
- MOSFETs biased during irradiation in the **worst-case condition**
- Slight increase in drain leakage current after irradiation
- **Limited threshold voltage changes** (depending on MOS polarity and geometry)

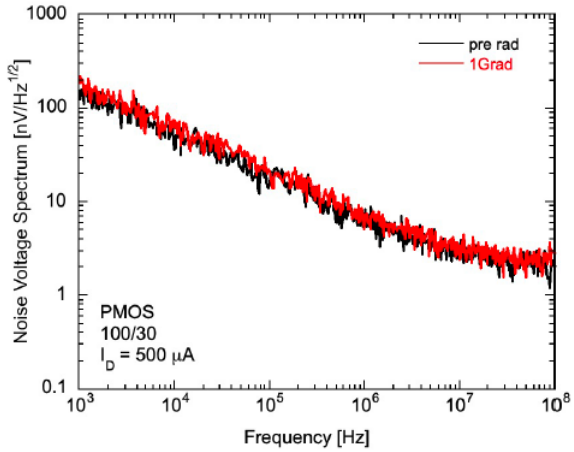
- Up to 1 Grad, NMOS and PMOS do not feature significant change in their **noise properties** after irradiation

Thanks to Serena Mattiazzo and Devis Pantano (INFN PD) for their valuable support during the irradiation campaign!



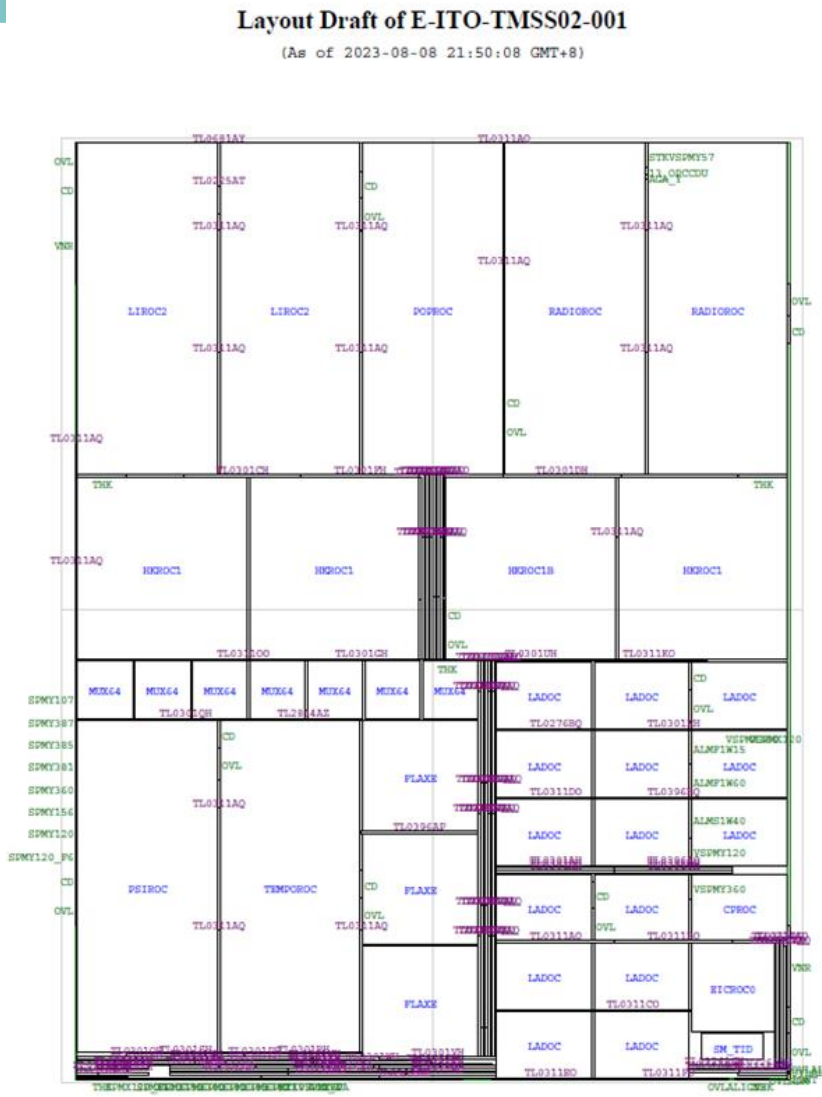






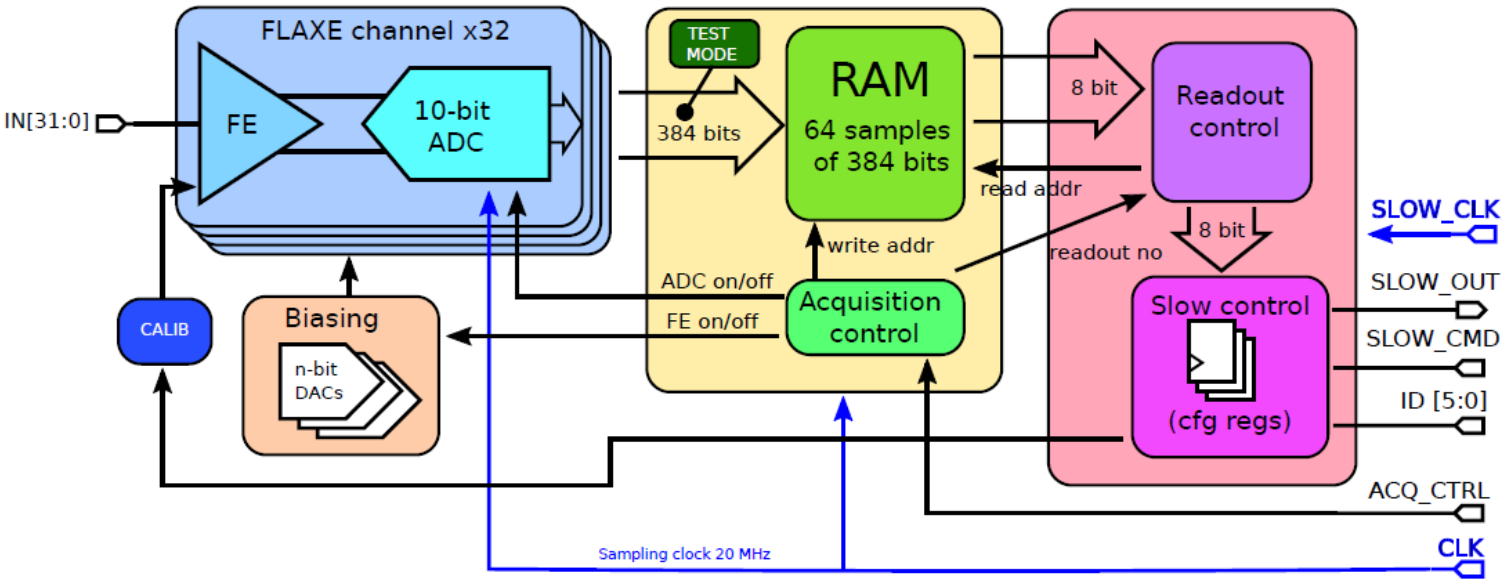
WP11.3 Deliverable

- D11.2 : MPW in 130 nm
  - AIDA participation in a 130nm engineering run
  - ~25% of the reticle area (total cost 300k€)
  - Fabricated in may 23 received jan 24
- 5 chips from AIDA :
  - FLAXE (AGH) : Si/GaAs readout
  - EICROC (OMEGA/AGH/CEA) : LGAD readout
  - CPROC (OMEGA) : RISC5
  - LIROC (WEEROC) : SiPM timing
  - PSIROC (WEEROC) : Si readout



130 nm at AGH

Activities in CMOS 130nm
FLAXE ASIC for ECAL-p in LUXE experiment



- FLAXE is a modified 32-channel FLAME in CMOS 130nm without high speed serialisers&transmitters – readout rate in LUXE ~10 Hz
- More than 1000 FLAXE chips were produced. Sent for dicing and packaging recently…

130 nm at WEEROC

Applications for LIROC

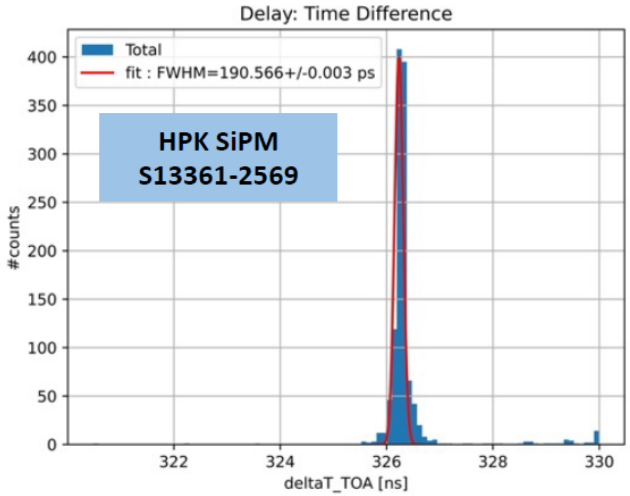
- QUANTUM : True Random Number Generation : Random Power spa
- LIDAR : atmospheric LIDAR : ADS / CNES
- LIDAR : Onera
- LIDAR : ISRO
- LIDAR : Leica Geosystem

130 nm at WEEROC

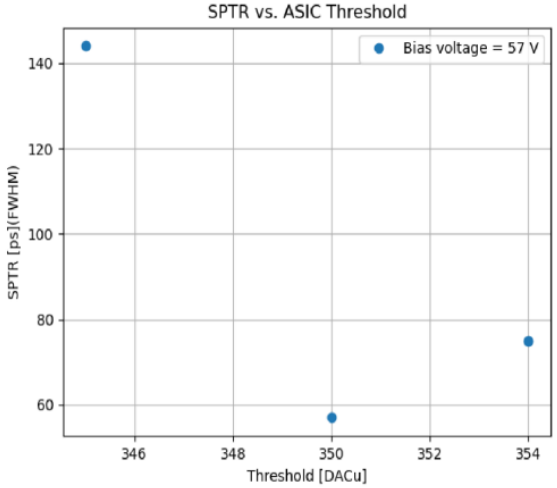
Liroc-picoTDC system: Improved time resolution (SPTR)

HPK SiPM S13361-2050NE-08

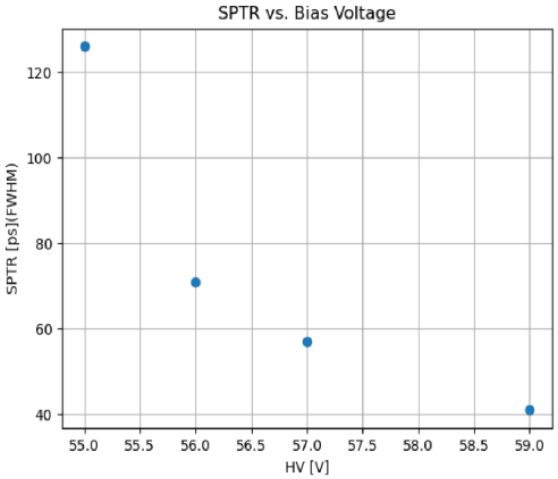
TOA Distribution



SPTR vs. Threshold



SPTR vs. Bias Voltage



→ TOA measurement: best SPTR HPK S13361-2569 is **191 ps** (FWHM) at 57 V .

→ Improved SPTR for a standard HPK S13361-2050NE-08: **58 ps** (picoTDC) compared to 167

Jinst

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Study experimental time resolution limits of recent ASICs at Weeroc with different SiPMs and scintillators

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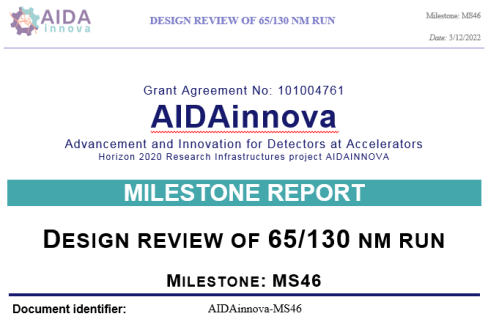
Summary

- 2 main pillars in AIDA INOVA
  - Explore 28 nm technology performance for HEP
  - Provide readout ASICs in 130nm for other WPs
- 2 fabrications done in 2023 to match these objectives
  - Milestones MS45/46 and deliverables 11.2/11.3
- First results shown at the annual meeting, more to come…
  - Complex chips => long testing time
- More designs also continuing in 28, 65 and 130 nm…
- At least 3 publications (AGH), probably more to be counted

backup

Deliverables/Milestones

- 2 Milestones and 2 deliverables
  - MS 11.1 and 11.2 (MS45 MS46) passed end 2022
  - D11.1 and 11.2 are the corresponding chips


AIDA innova DESIGN REVIEW OF 65/130 NM RUN Milestone: MS46 Date: 3/12/2022

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

DESIGN REVIEW OF 65/130 NM RUN

MILESTONE: MS46

Document identifier: AIDAinnova-MS46

MS11.1	**Design review of 28 nm MPW**	**11.2**	**18**	**report**
MS11.2	design review of 65/130 nm run	11.3	18	report

Deliverables related to WP11	
D11.1: MPW 28 nm *The deliverable is a multi-project wafer fabrication with the different test ASICs in CMOS 28 nm*	24
D11.2: MPW 65/130 nm *The deliverable is a multi-project wafer fabrication with ASICs in CMOS 65 and/or 130 nm that can be used to readout detectors from the other WPs and in particular WP8*	24
D11.3: Measurement reports *Each of the ASIC fabricated in the 2 previous deliverables will have its design and performance documented in a report*	42