

Second Project Review meeting

June 20th, 2024

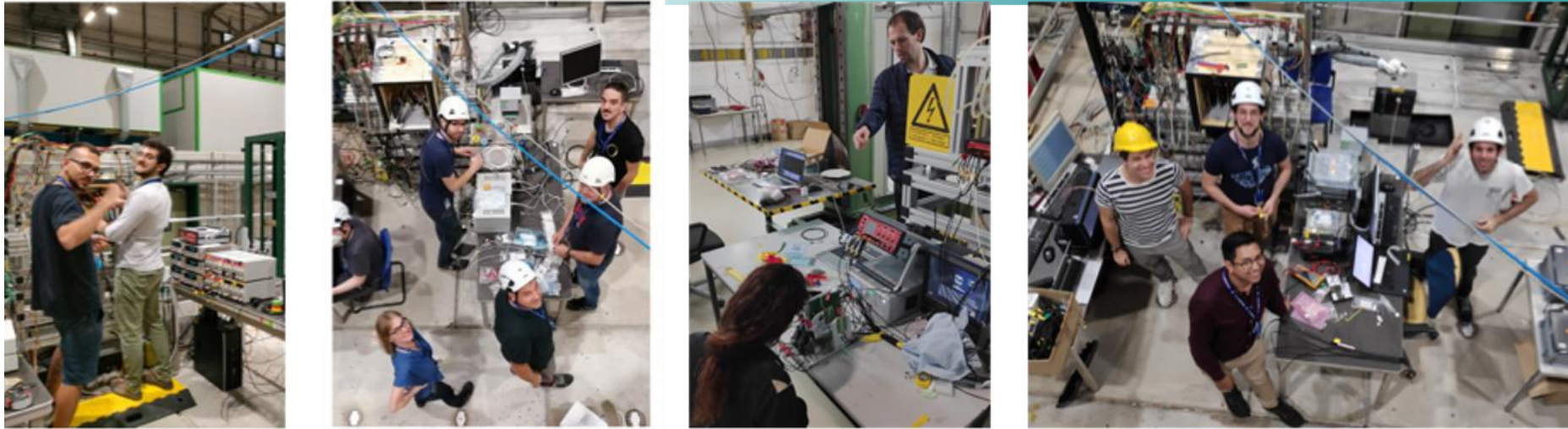
WP 6

Hybrid Pixel Sensors for 4D Tracking and Interconnection Technologies

Claudia Gemme (INFN Genova), Anna Macchiolo (UZH Zurich)

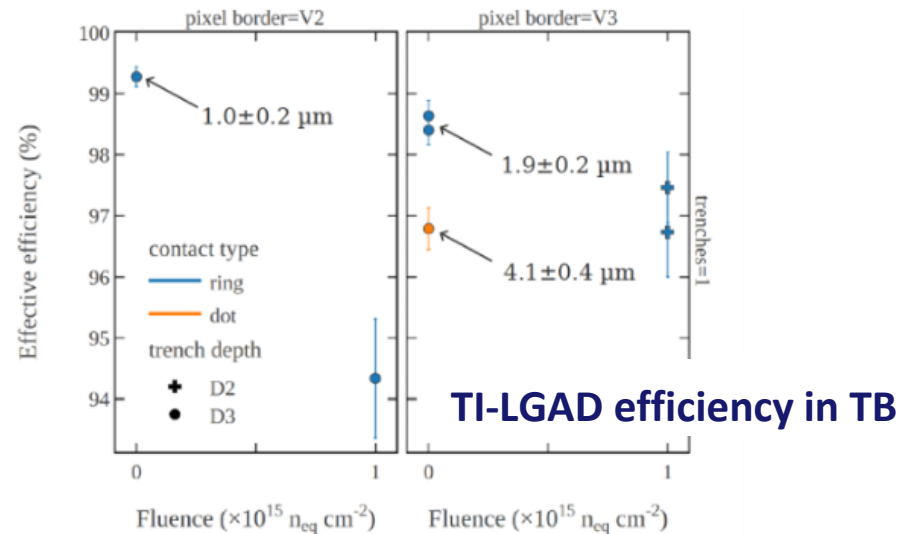


- The primary goal of this WP is to add precise timing measurements to the spatial information in silicon pixel sensors to provide **4-dimensional tracking** for the future detectors for High Energy Physics.
- This feature will help to disentangle tracks and vertices of spatially overlapping particles and improve event reconstruction in the high occupancy environment of experiments at HL-LHC and beyond.
- Only hybrid sensors in connection with high-performance ASICs can at the moment fulfil the extreme timing requirements of 4D tracking and therefore **advanced interconnect technologies** are required for the hybridisation in large areas and at small pixel sizes.
- For this reason, Anisotropic Conductive Films (ACF) and Wafer-to-Wafer (W2W) interconnection, such as Metal-Oxide Hybrid Bonding or Metal-Metal-Fusion Bonding are being developed in this WP.



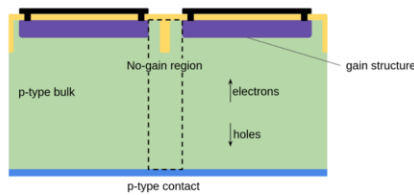
- Establishment of an innovative Test-beam set-up for sensors for 4D Tracking
- Comparison of the performance of different timing sensors
- Participation of several groups from different experiments, very useful to spread experiences, technological solutions and for community build-up

coordinators: Gregor Kramberger and Ivan Vila



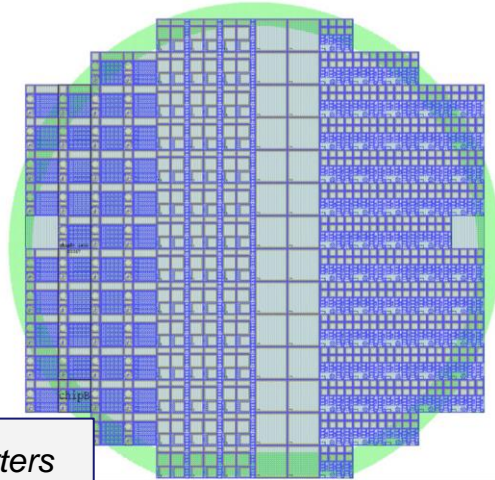
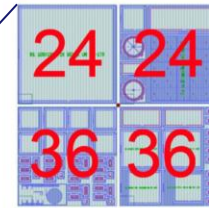
Status: Fabrication completed, devices distributed, irradiated and tested in lab and TB

- ❑ The goal is to realize an LGAD compatible with small pitch (55micron or less) and with high fluences
 - ❑ Isolation made by trenches
 - ❑ Carbon co-implantation to increase radiation hardness
- ❑ Previous experience
 - ❑ Internal FBK batches
 - ❑ Batches in RD50



Wafer Layout

- the wafers are divided into a regular grid (1cm²)
- in each column are printed the same quarter of the reticle



Process split in the 12 wafers

	Wafer	Thickness	Carbon	Trench depth	Trench process
<i>baseline</i>	1	45	Y	D2	P2
	2	45	Y	D2	P2
	3	45	Y	D1	P2
	4	45	Y	D1	P1
	5	45	Y	D2	P1
	6	45		D2	P2
	7	45		D2	P2
	8	45		D1	P1
	9	55	Y	D3	P2
	10	55	Y	D2	P2
	11	55	Y	D2	P2
	12	55		D2	P2

One full reticle (about 2x2 cm²) in 4 quarters

- Pixel & Strip
 - PCM FBK
 - 2x1 Test devices
- In order to explore*
- Pitch
 - Border: 4 versions
 - Number of trenches : 1 or 2

Status: Fabrication completed, devices distributed, irradiated and tested in lab and TB

Production completed in October. Several tests run at wafer level in FBK to qualify the wafers, see example in next slides:

- Extremely high yield for small sensors, >60% for large sensors; well above 95% on small structures.

Wafers 1, 6 and 10 diced

- parts being distributed to Institutes and JSI for irradiation.
- Large sensors sent to be interconnected via ACF to Timepix3 chips
- Parts (not irradiated and irradiated up to $2.5e15$) tested at DESY and SPS on beam in Feb.

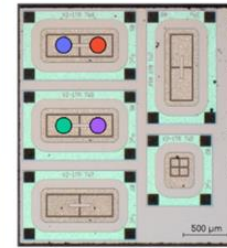
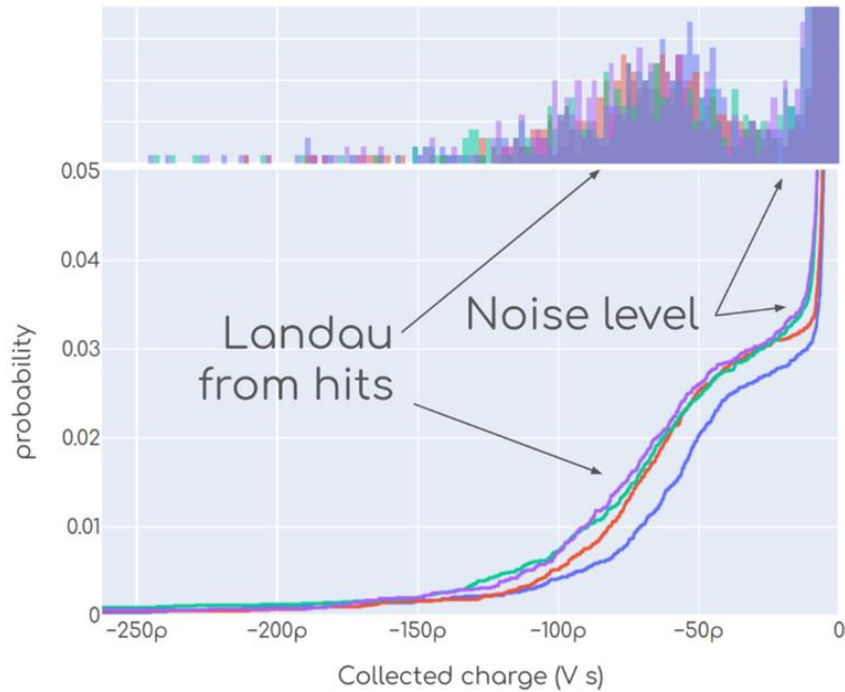
All the other wafers have temporary metal layer removed. Next:

- Send these wafers to IZM for UBM and hybridization

First glance at February TB results:

TI-LGAD w/carbon, irradiated to $25e14 \text{ n}_{eq} \text{ cm}^{-2}$

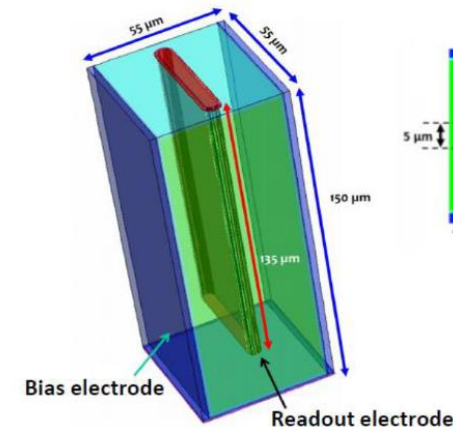
Bias voltage = 650 V, T = -25 °C



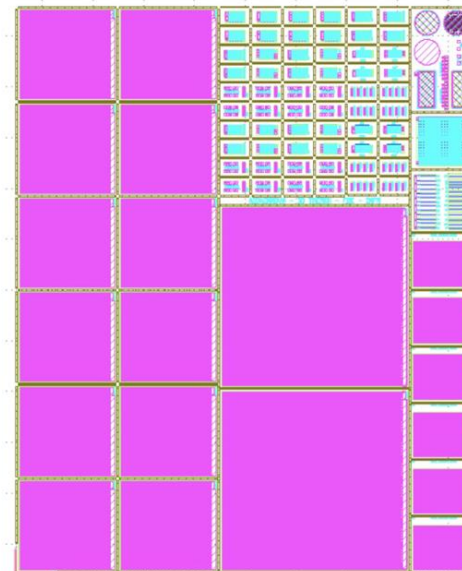
Clear separation between Landau and noise ✓

Sensor still works at the highest fluence 🙌

Status: Fabrication just completed, running tests on wafers at FBK with temporary metal

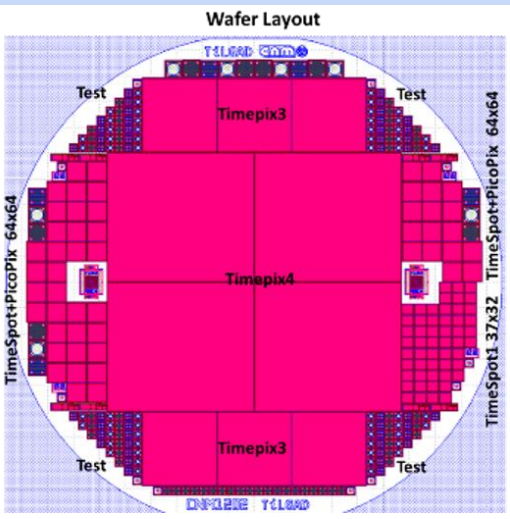


- **Pixel sensors (55 μm pitch)**
 - 32x32 pixels, multiplicity = 6 (3 std, 3 dashed)
 - 64x64 pixels, multiplicity = 12 (6 std, 6 dashed)
 - 128x128 pixels, multiplicity = 2 (1 std, 1 dashed)
- **Device test structures (55 μm pitch and 42 μm pitch, std and dashed)**
 - Groups of individual pixels
 - Strips
 - Diodes
- **Technological test structures**



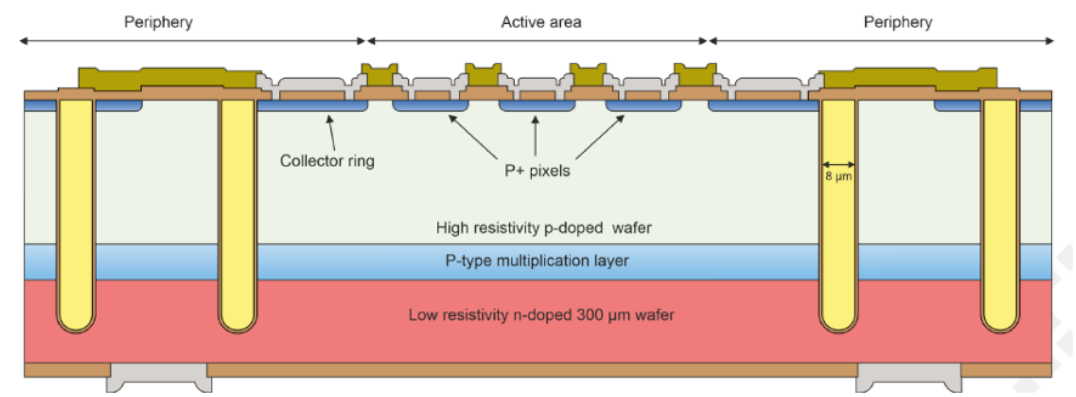
- Mainly 55x55 μm² pixel cell devices compatible with existing or in design readout chips (Timespot, IGNITE, Timepix ASICs)
- 6" Wafers with photolithography on a reticle

Status: Prototyping production at CNM suffered from a too high doping of the multiplication layer in Epi wafers → APD behaviour
 AidaInnova layout ready to be produced on Si-Si 4" wafers with Timepix4 and Timepix3 structures, plus smaller matrices → **end of the production foreseen in October-November**

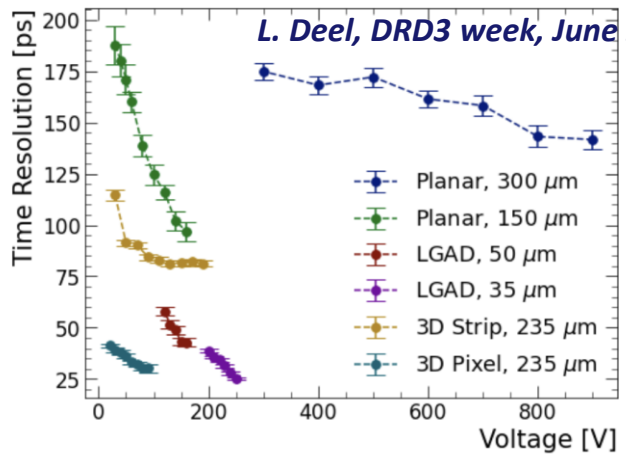


- Trenches to isolate the active area
 - ✓ Multiplication region is fully isolated.
 - ✓ Simpler single-side process and 50% less fabrication steps.
 - ✓ Devices are able to sustain higher voltages.
 - ✓ Slim-edge technology.
 - ✓ Optimization of the multiplication layer is independent of charge collection and cross-talk at the electrodes.

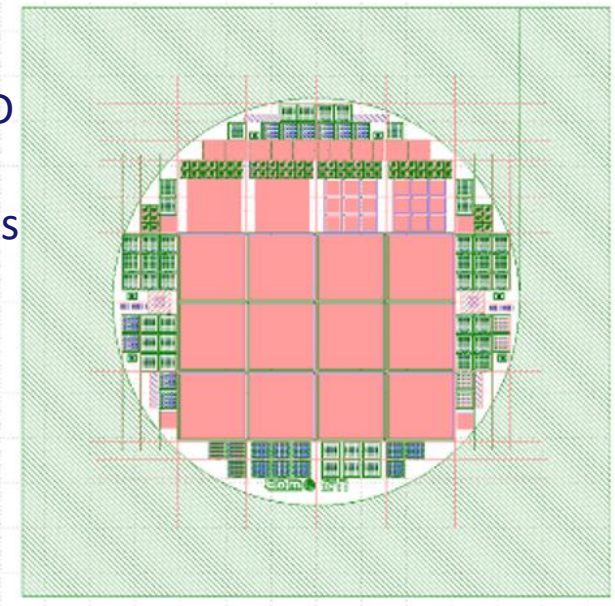
Deliverable D6.1 was due in October 2023 → even considering only ¾ of the productions, it has to be moved to October 2024



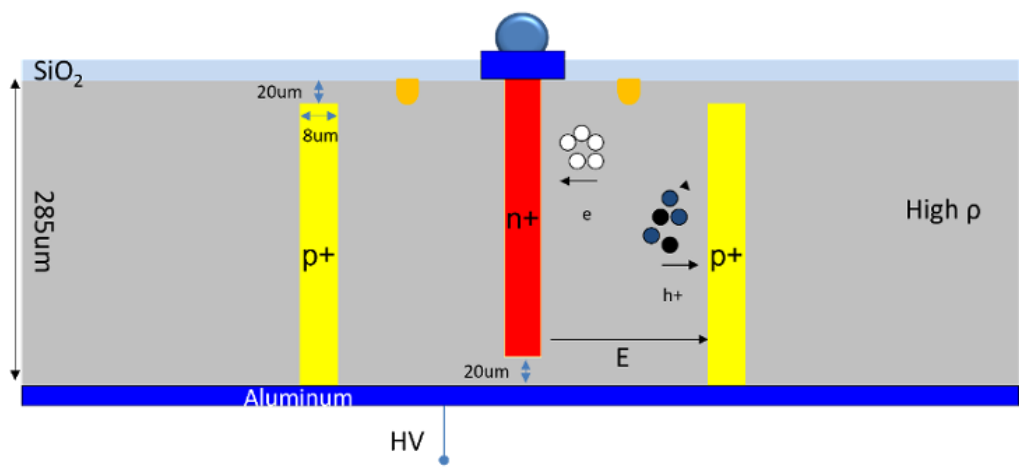
Status: Prototyping production (RD50) completed with promising results.



Mask design of AIDAInnova 3D production to be completed within July with test-structures requested by LHCb and production should be starting on 4" wafers in September → **one year to be completed**

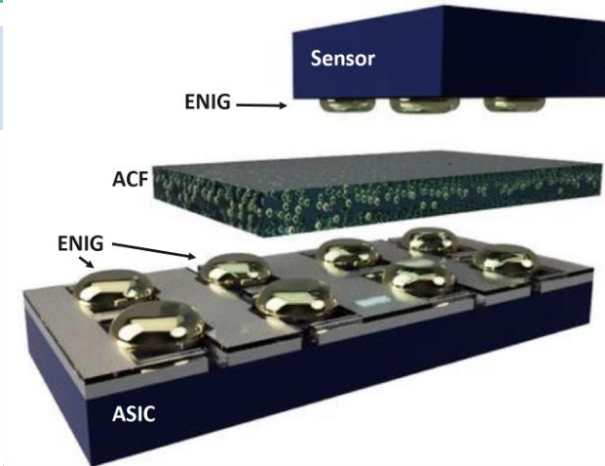


Sensor structures compatible with Timepix3, PicoPix and Ignite chips

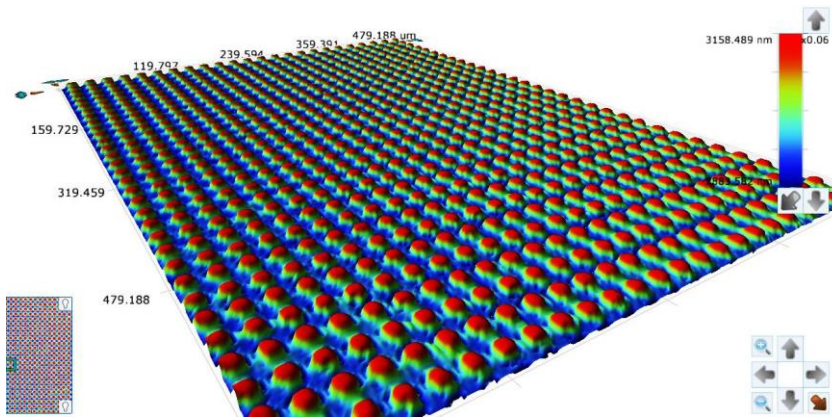


Status: ENIG deposition has been optimized

- New equipment available at Campus Biotech for characterizing all nickel bumps on a chip, allows for quick identification of problematic areas, if any.
- High bump height 10.5µm for large pitches and 4.5 µm for small pitches
- Good ENIG homogeneity with a variation of only 0.5µm
- **Very few defects, with good results for pitches down to 20-25 microns**



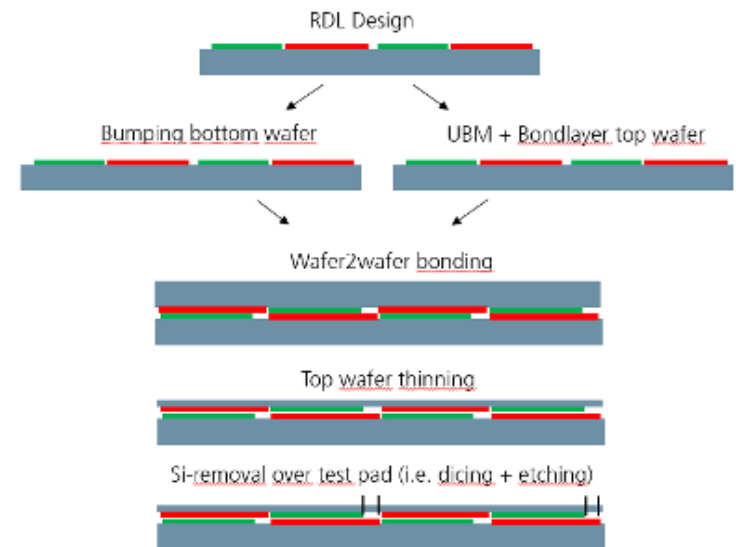
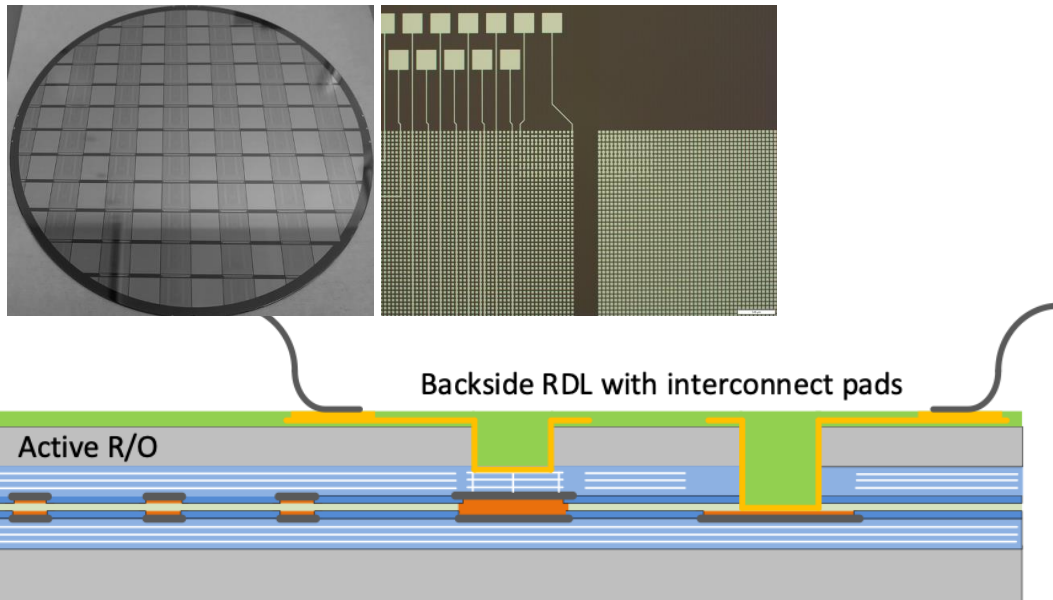
Optical profilometry after ENIG plating of CLICpix2 like daisy-chains with 20 µm pitch



- Systematically improving the ACA bonding process for a variety of hybrid pixel detector assemblies (Timepix3, ESRF-SPHIRD, ALTIROC, Timespot), as well as for dedicated daisy-chain test structures produced within the AIDAInnova collaboration
- More stability testing of assemblies (temperature, radiation hardness)
- Expanding the number of projects profiting by the technology

Status: Timepix3 wafers in hands; passive CMOS sensors wafers in fabrication at Lfoundry on 8" wafers (ready by end of summer); optimizing W2W process with daisy chains wafers.

- Combined polymer-metal-bond process flow selected for the project
- Timepix3 wafers are at IZM. Final sensors being produced with passive CMOS technology at LF.
- W2W bonding process setup with daisy chain at IZM well advanced but still some optimizations



MS22+D6.1:

- So far finalized three sensors wafer layouts out of four planned.
 - Production completed in two cases at FBK
 - One production starting now at CNM and should be completed in October - November
 - Last production (3D sensors) to be started in September at CNM

MS24 (ACF interconnection):

- Dummy chains produced, used for the optimization of the ACF interconnection technique.

MS25 (W2W interconnection):

- Dummy chains produced, passive CMOS sensors being produced at LFoundry, procedure for wafer-to-wafer bonding agreed and technological tests achieved with daisy chains

Others:

- Improved simulation to estimate LGAD sensors performance and gain layer degradation. 3D simulations progressing
- Test-beam activities allowed to gain important information on LGAD performance

Backup

Objectives

Task 6.1. Coordination and Communication

See introductory section on page 29.

Task 6.2. Simulation and processing of common 3D and LGAD sensor productions

- Optimisation of processes for 3D and LGAD sensors for timing applications
- Simulations of various designs for 3D and LGAD sensors to compare and optimise the layout in terms of timing performance
- Simulations of surface and bulk radiation damage for 4D (tracking+timing) detectors toward more radiation tolerant solutions
- Processing of two common 3D sensor productions and two common LGAD productions by FBK/CNM
- Design and implementation of simulation software which is applicable to a large range of technologies and includes models for the description of effects from sensor level to readout electronics in semiconductor detectors

Task 6.3. Validation of common 3D and LGAD sensor productions

- Characterisation of the 3D sensors in terms of timing, radiation hardness, efficiency and uniformity via measurements in the laboratory and beam tests
- Characterisation of small pitch LGAD and inverse LGAD sensors (iLGADs) from the common production in terms of timing and efficiency via measurements in the laboratory and beam tests
- Feedback to the foundries for further process optimisation of 3D and LGAD sensors

Task 6.4. Development of interconnection technologies for future pixel detectors

- Development of suitable Anisotropic Conductive Films (ACF) material and die-to-die bonding process flows for small pixel pitches
- Production and post-processing of dedicated planar sensor wafers for ACF trials
- Test of the performance of sensor modules interconnected with ACF
- Production and test of ultra-thin assemblies interconnected with a wafer to wafer bonding technology
- Post-processing of sensor prototypes developed in Task 6.3

Task Leaders

T6.2

Gian Franco Dalla Betta
Giulio Pellegrini

T6.3

Gregor Kramberger
Ivan Vila

T6.4

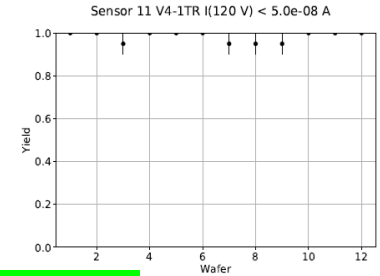
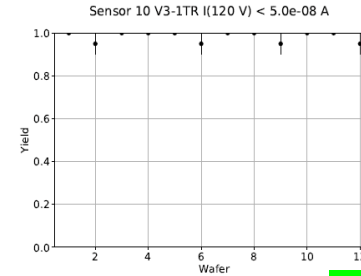
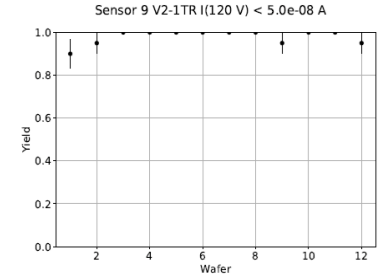
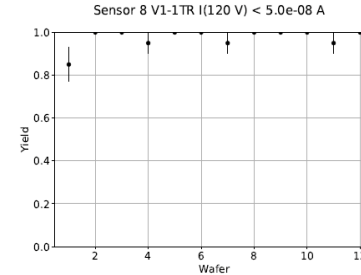
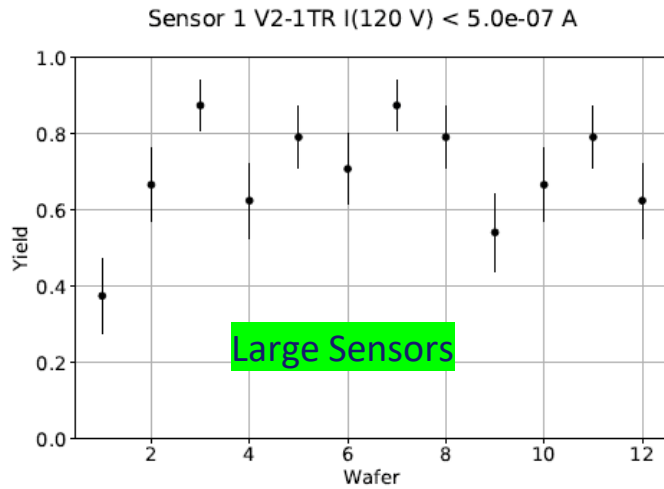
Dominik Dannheim
Fabian Hügging

Deliverable Number	Deliverable Title	Lead Beneficiary	Type	Dissemination level	Due Date (in months)	comments
D6.1	Completion of common productions	CSIC	Report	Public	30	Including preliminary char. at foundries
D6.2	Final validation of timing performance of common productions	INFN	Report	Public	46	Before and after irradiations
D6.3	Test of the final ultra-thin hybrid assemblies from wafer to wafer bonding	Bonn	Report	Public	44	Module functionality, interconnection yield and strength
D6.4	Validation of the ACF for large and small pitch assemblies	CERN	Report	Public	45	Small pixel sizes from 25 to 55 μm

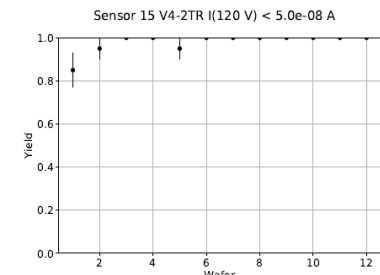
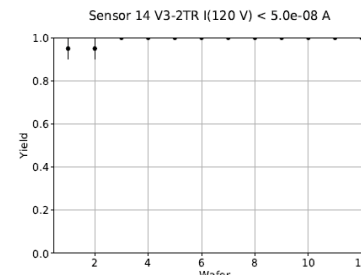
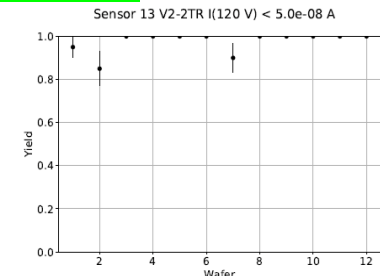
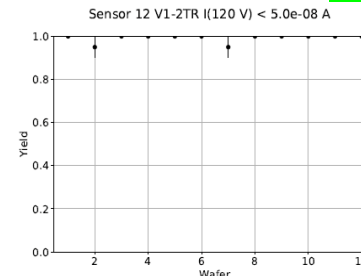
Some examples of Wafer level measurements:

The yield calculation includes only sensors with gain:

Extremely high for small sensors, >60% for large sensors

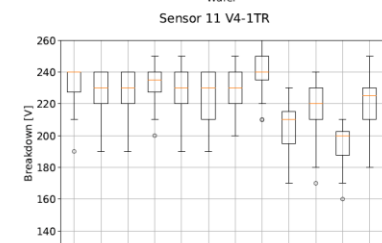
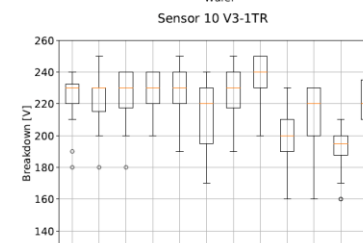
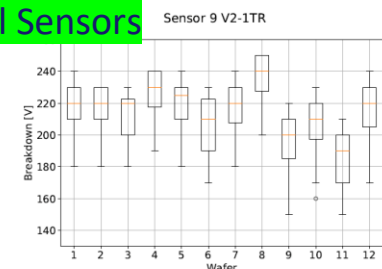
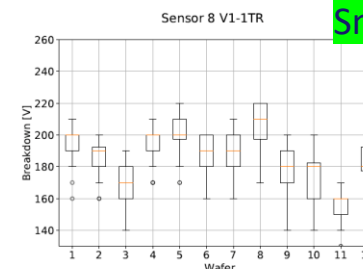
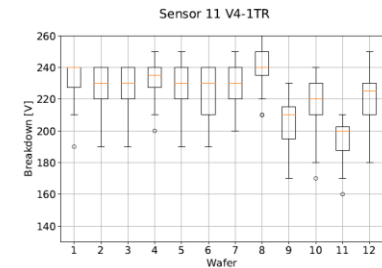
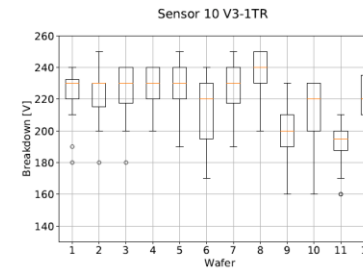
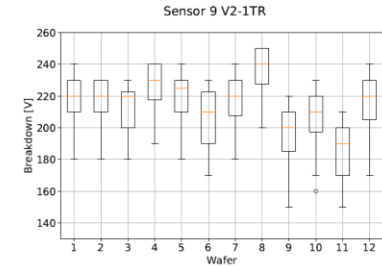
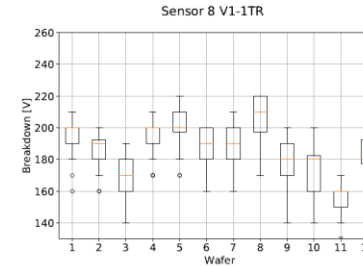
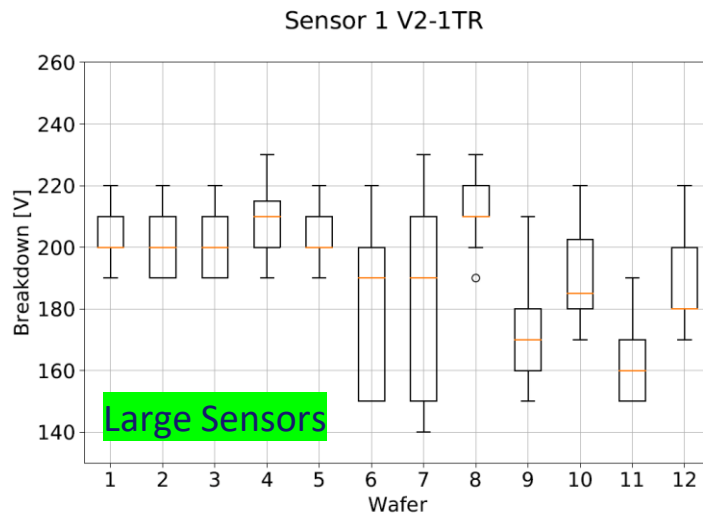


Small Sensors



Some examples of Wafer level measurements:

Breakdown voltage as expected



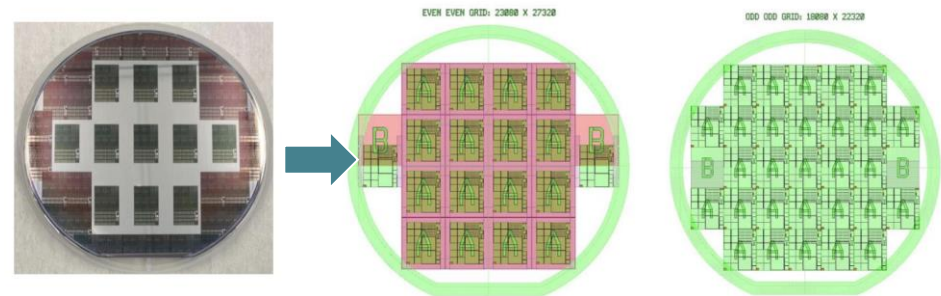
Status: 18 wafers fabrication jus completed, running tests on wafers at FBK.

Wafer Layout:

- 14 wafers with 18 DIE on wafer
- 4 wafers with 29 DIE to test high density yield.

Process Split:

- 12 poly filling
- 6 BPSG filling



Old wafer layout
11 shot exposure

18 shot exposure

29 shot exposure

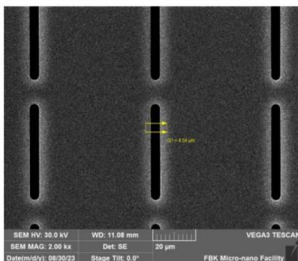
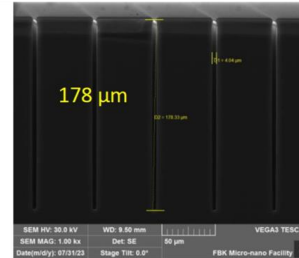
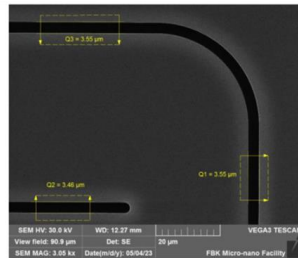
Short and narrow trenches
to improve subsequent
photolithographic process

3D AIDA

Long trenches:
3µm x ∞

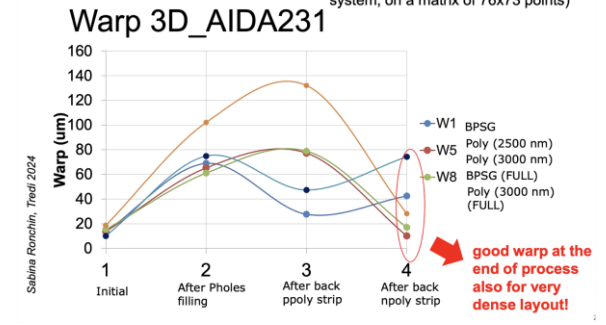
Previous
process:
trenches
4µm x ∞

Short trenches:
4 µm x 40 µm



Wafers warp under control!

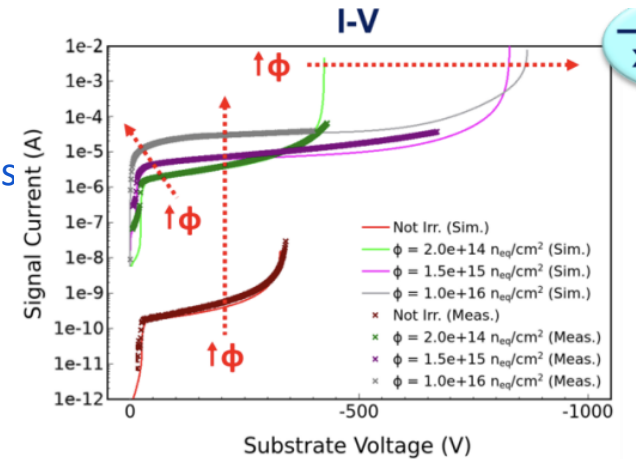
(measured with MicroProf® FRT GmbH system, on a matrix of 76x73 points)



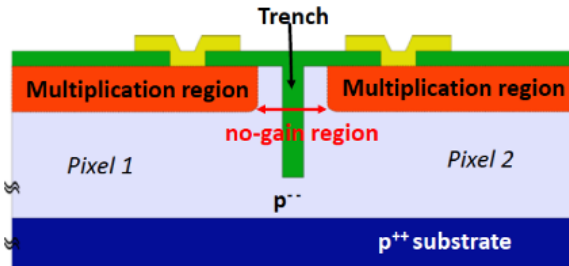
good warp at the end of process also for very dense layout!

- Simulations have been developed to predict the LGAD behaviour up large fluences.
 - The radiation damage model used in the simulation framework is the “**New University of Perugia TCAD model**” scheme, which allows to model the comprehensive surface and bulk radiation damage effects in Si by means of a limited set of physically meaningful deep-level radiation-induced traps.
 - I-V and C-V simulated curves have been compared with experimental data, allowing to fine tune parameters for predictive results that have guided the design.
 - 3D sensors applications started.

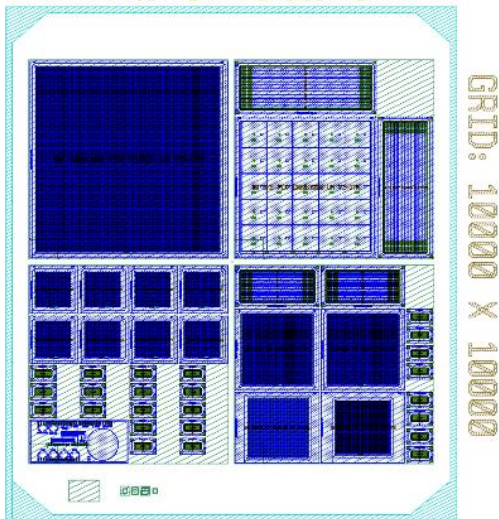
- The **Allpix Squared** Monte-Carlo simulation framework has been extended by modules to simulate the sensor response of LGAD sensors as well as by the possibility to define a flexible geometry for 3D sensor implants in different shapes from frontside and backside. A first implementation of radiation-induced trapping has been implemented.



Fabrication details



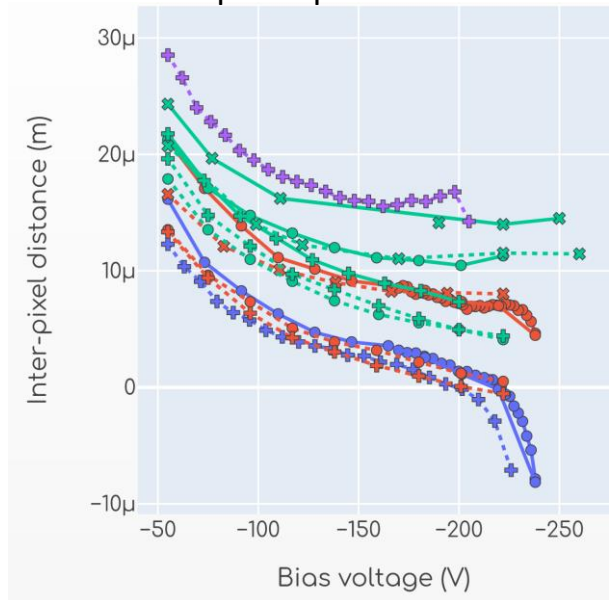
reticule structure
wafer scale



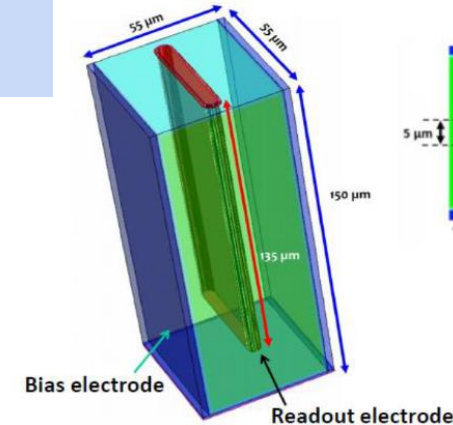
Process split

Wafer	Thickness	Carbon	Trench depth	Trench process
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2	45	Y	D2	P2
3	45	Y	D1	P2
4	45	Y	D1	P1
5	45	Y	D2	P1
6	45		D2	P2
7	45		D2	P2
8	45		D1	P1
9	55	Y	D3	P2
10	55	Y	D2	P2
11	55	Y	D2	P2
12	55		D2	P2

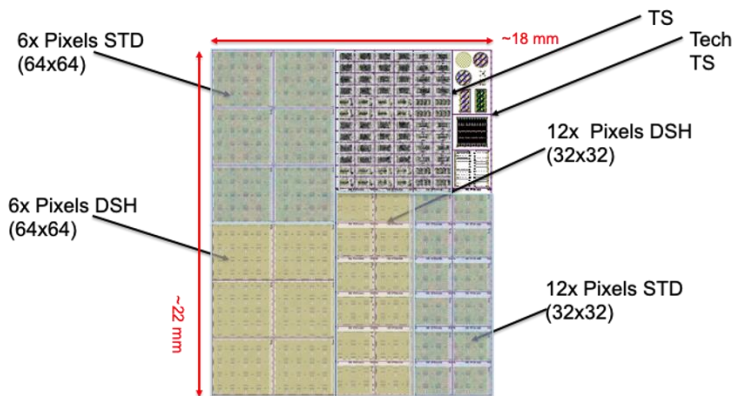
Inter-pixel distance measured on proto-production



Fabrication details



- Mainly 55x55 μm^2 pixel cell devices compatible with existing or in design readout chips (Timespot, Picopix, Timepix ASICs)
- 6" Wafers with photolithography on a reticle



Example of a 64x64 matrix with dashed trenches

