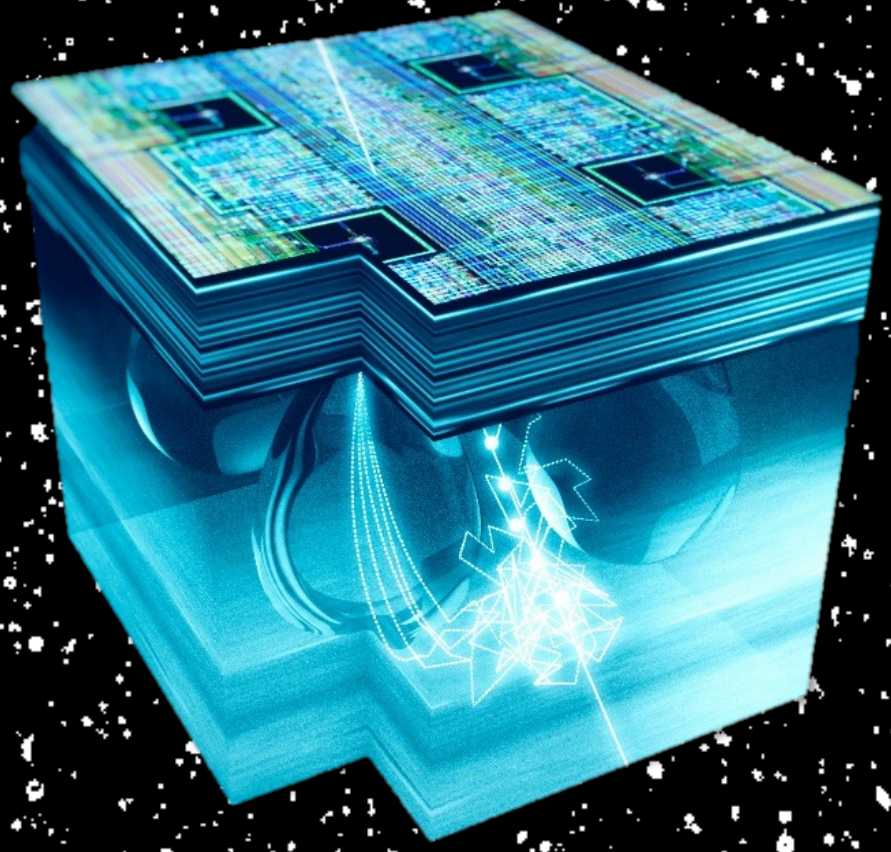
The Future of MAPS



ALPIDE prototype: 200 MeV protons at PSI

Walter Snoeys

Next generation particle detectors, Bergen, Norway, June 13th, 2024

walter.snoeys@cern.ch

Acknowledgements

- The course organizers, D. Rohrich
- Many colleagues from CERN, the ALICE ITS2 and ITS3 upgrade, ATLAS Itk, WP1.2, Stanford/Hawaii …

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

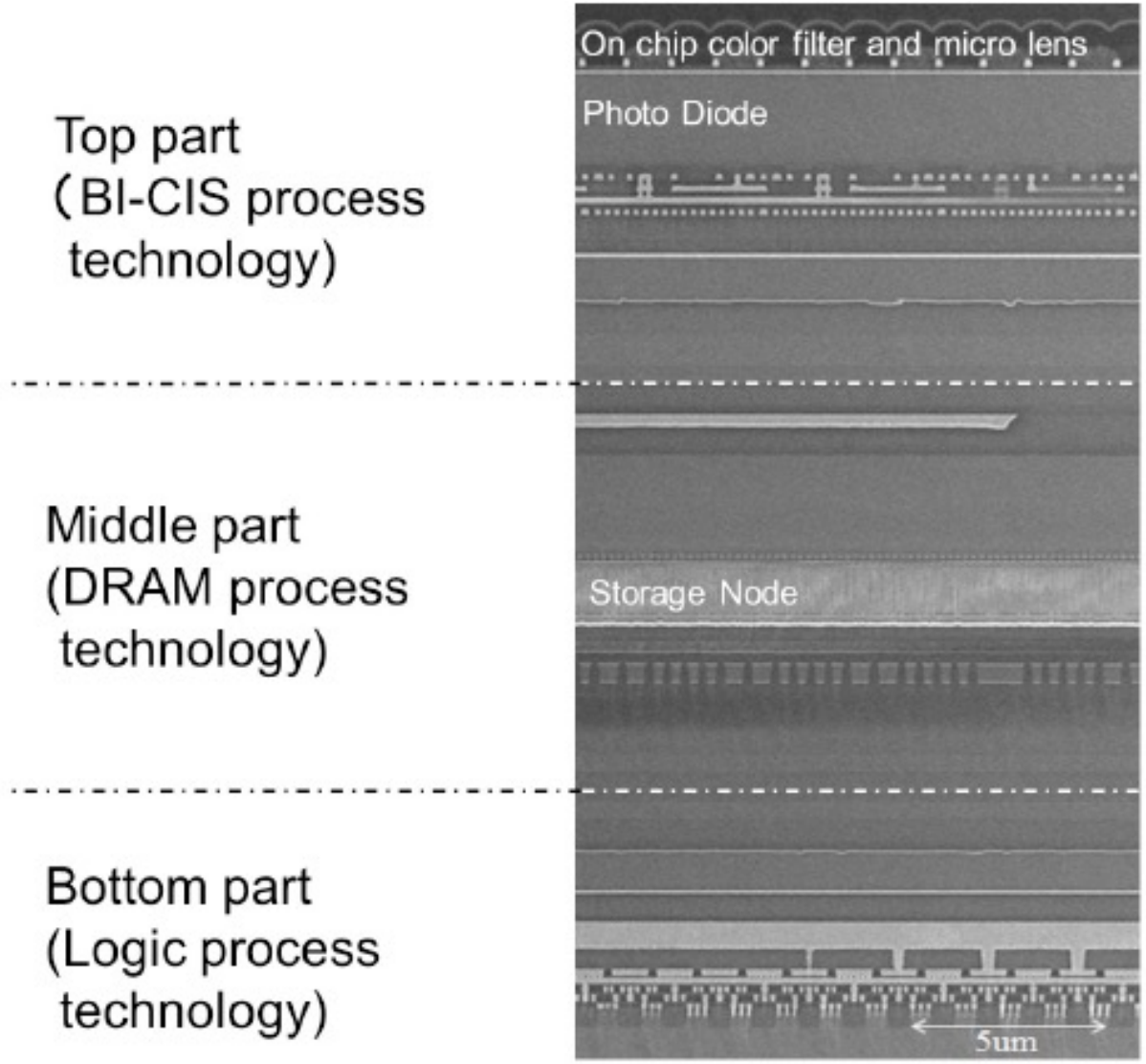
reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …

Silicon has become the standard in tracking applications both for sensor and readout

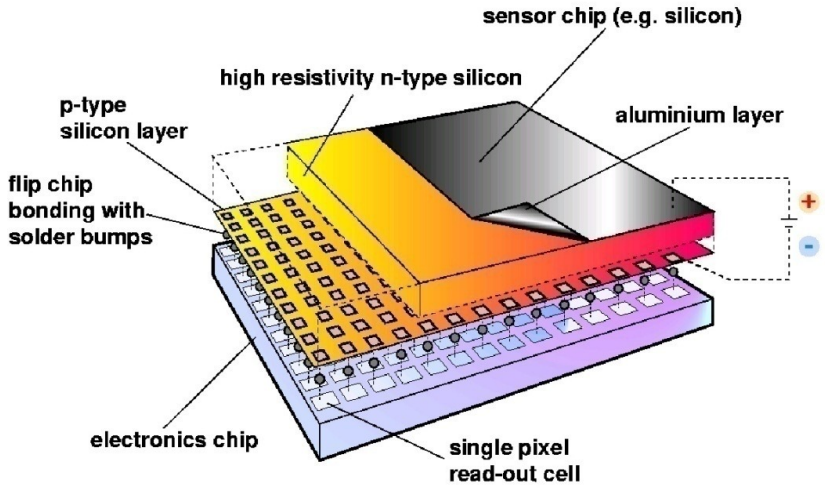
… and now CMOS MAPS make their way in High Energy Physics !

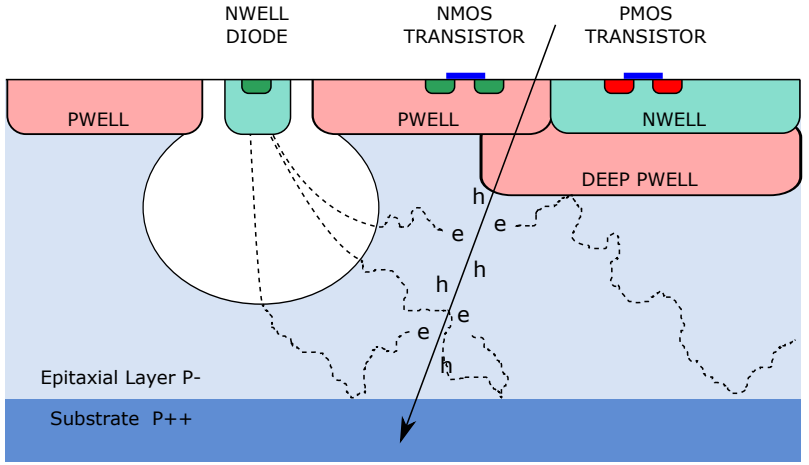
Hybrid still in majority in presently installed systems



Sony, ISSCC 2017

Hybrid vs Monolithic





Hybrid

- Large majority of presently installed systems
- 100 % fill factor easily obtained
- Sensor and ASIC can be optimized separately
- Spin-off from HEP developments:

  for example spectral photon counting chips in this workshop

Monolithic

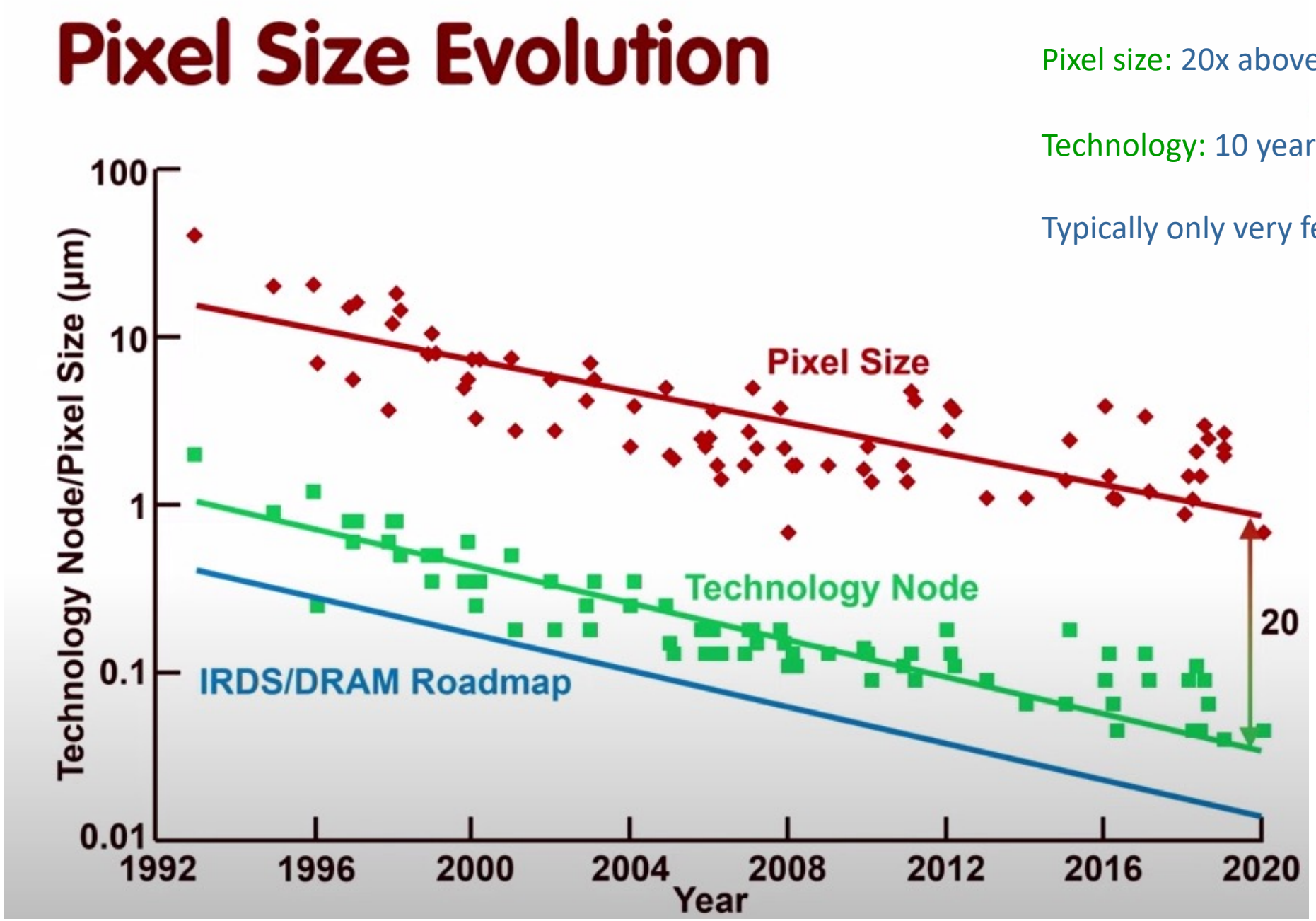
- Easier integration, lower cost
- Potentially better power-performance ratio and strong impact on material budget

Motivation for intense R&D since more than 30 years

- Trend towards more standard technologies

New technologies (TSV's, microbumps, wafer stacking…) make the distinction more vague.

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel

Albert Theuwissen, ISSCC 2021

Requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	**0.01**	**10^{-3}**
LHC	**1**	**0.1…0.3**
HL-LHC 3ab^{-1}	**5**	**1.5**
FCC	**10-350**	**3-100**

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

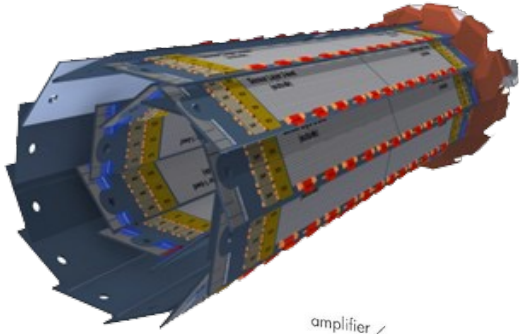
Time resolution

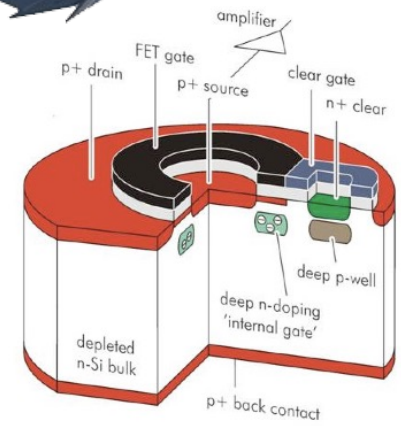
- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

Larger and larger areas

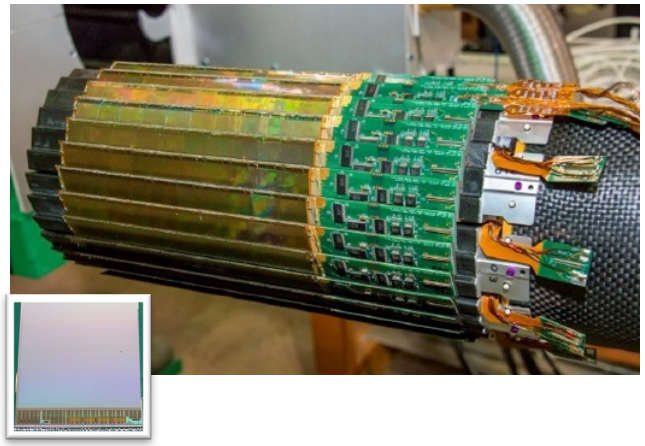
- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

Monolithic sensors in HEP move into mainstream technology





DEPFET in Belle



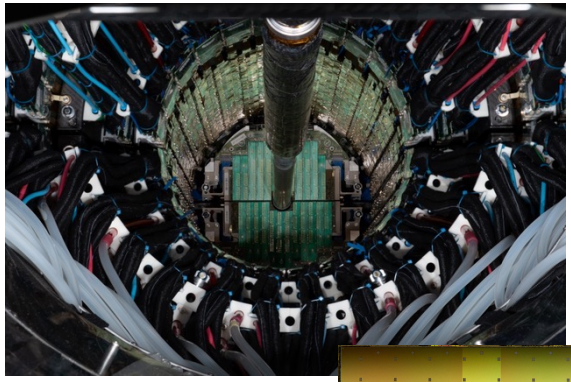
MIMOSA28 (ULTIMATE) in STAR

IPHC Strasbourg

First MAPS system in HEP

Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout



ALPIDE in ALICE

First MAPS in HEP with sparse readout similar to hybrid sensors

Quadruple well 0.18 µm CMOS

- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance

Large collection electrode

LF Monopix, MuPix,…

Extreme radiation tolerance and timing uniformity, but large capacitance

Small collection electrode

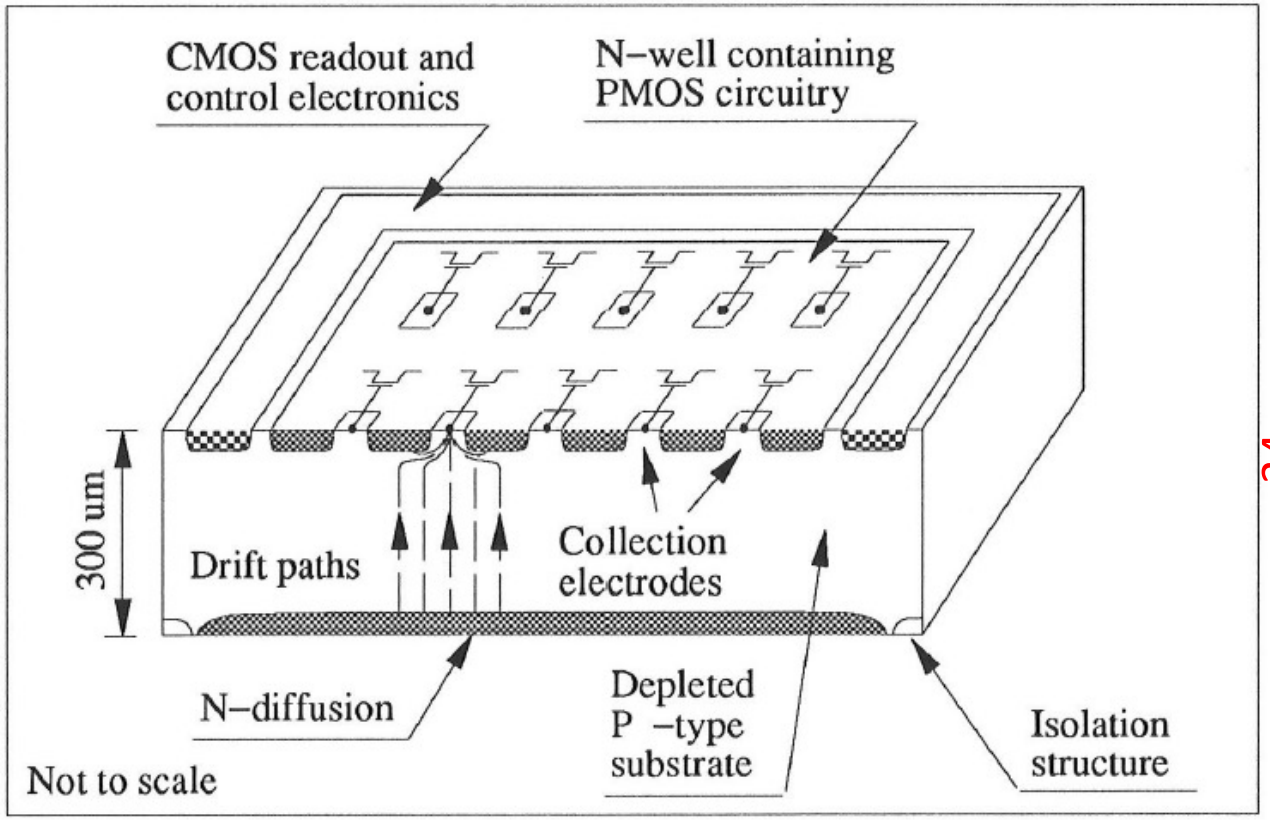
ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, …

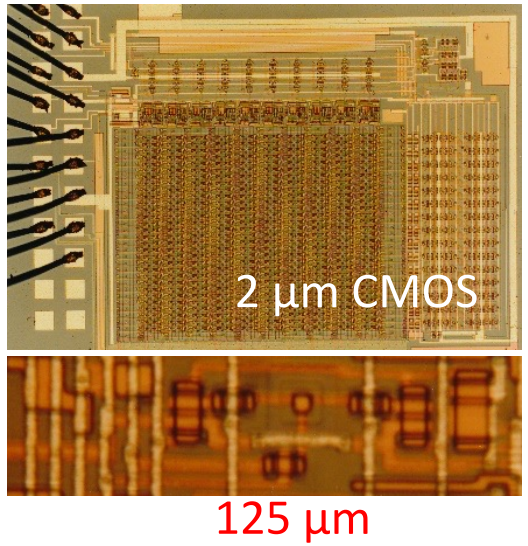
- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

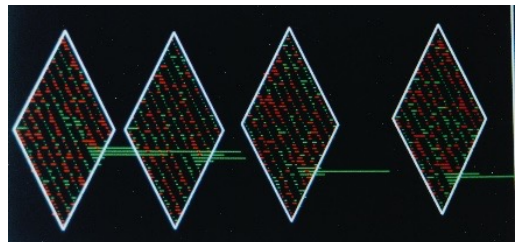
Commercial deep submicron CMOS technology evolved “naturally” towards

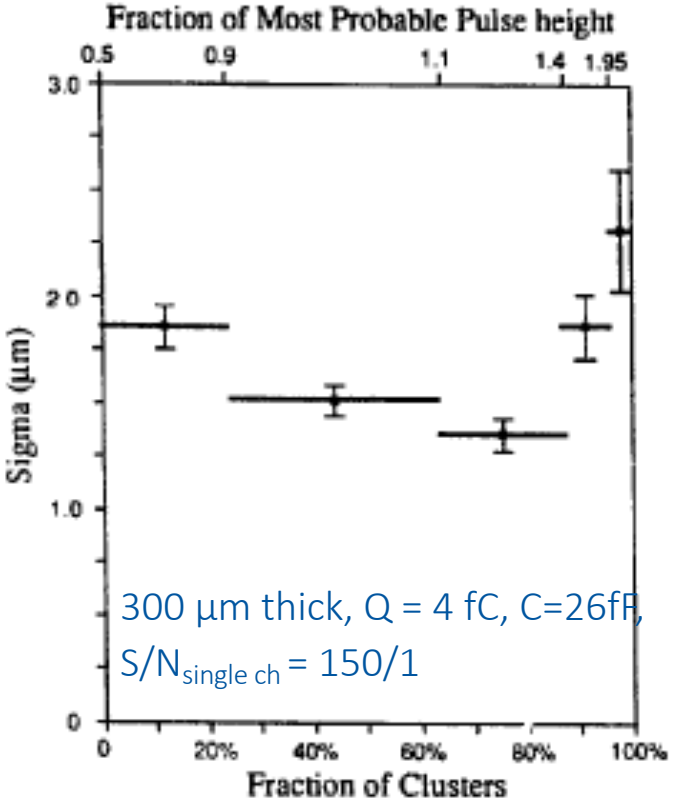
- Very high tolerance to ionizing radiation (some caveats, cfr G. Borghello, F. Faccio et al.)
- Availability of substrates compatible with particle detection
- Imaging technology not absolutely required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

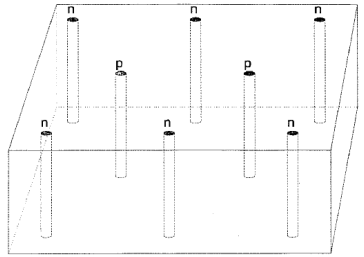
A monolithic detector for high energy physics (PhD thesis 1992), CMOS with double sided processing
Stanford University 1987-1992, and the University of Hawaii











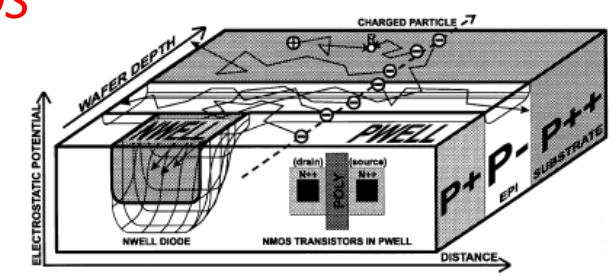
- Separation of junction from small collection electrode
- Better than 2 µm position resolution even at 34 µm pitch due to good S/N
- Improved back side trench isolation led to sensors with 3D electrodes (S.Parker, J. Segal)

C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

KEY ENABLERS: Mimosa series – IPHC Strasbourg - Move to standard CMOS

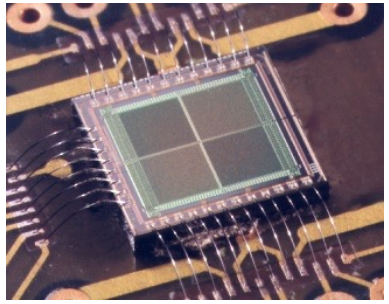
A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



NIM A 458 (2001) 677-689

Mimosa1 – 1999
AMS 0.6 µm

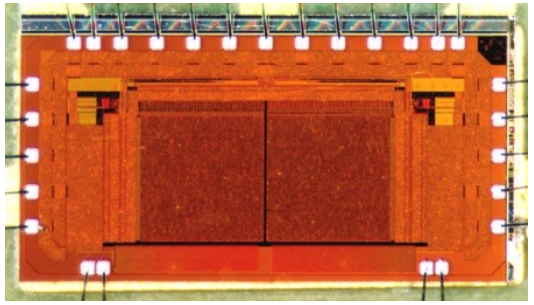


20µm pixel

Mimosa2 – 2000
MIETEC 0.35 µm

20µm pixel

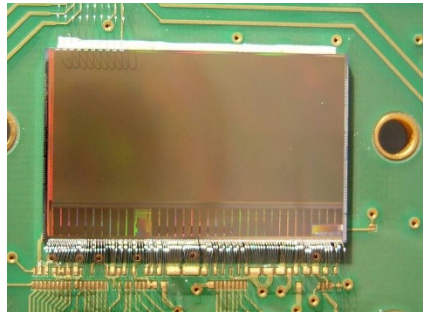
Mimosa3 – 2001
IBM 0.25 µm



8µm pixel

....

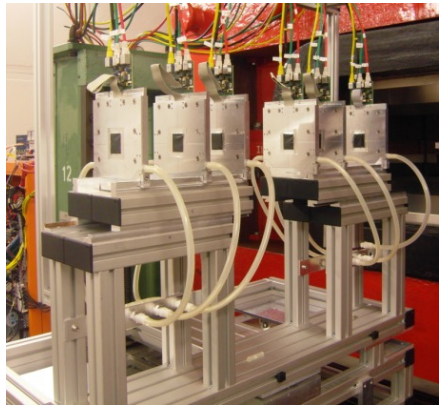
Mimosa26 – 2008
AMS 0.35 µm



18.4 µm pixel

....

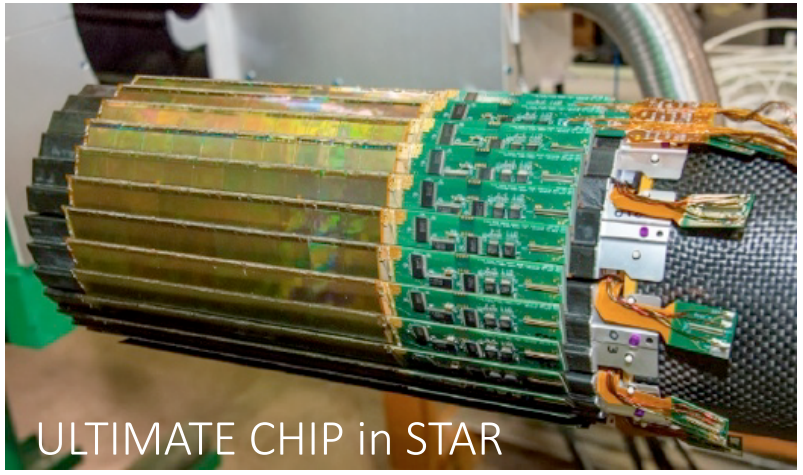
Mimosa26 – 2008 in the EUDET Telescope,



Rolling shutter readout

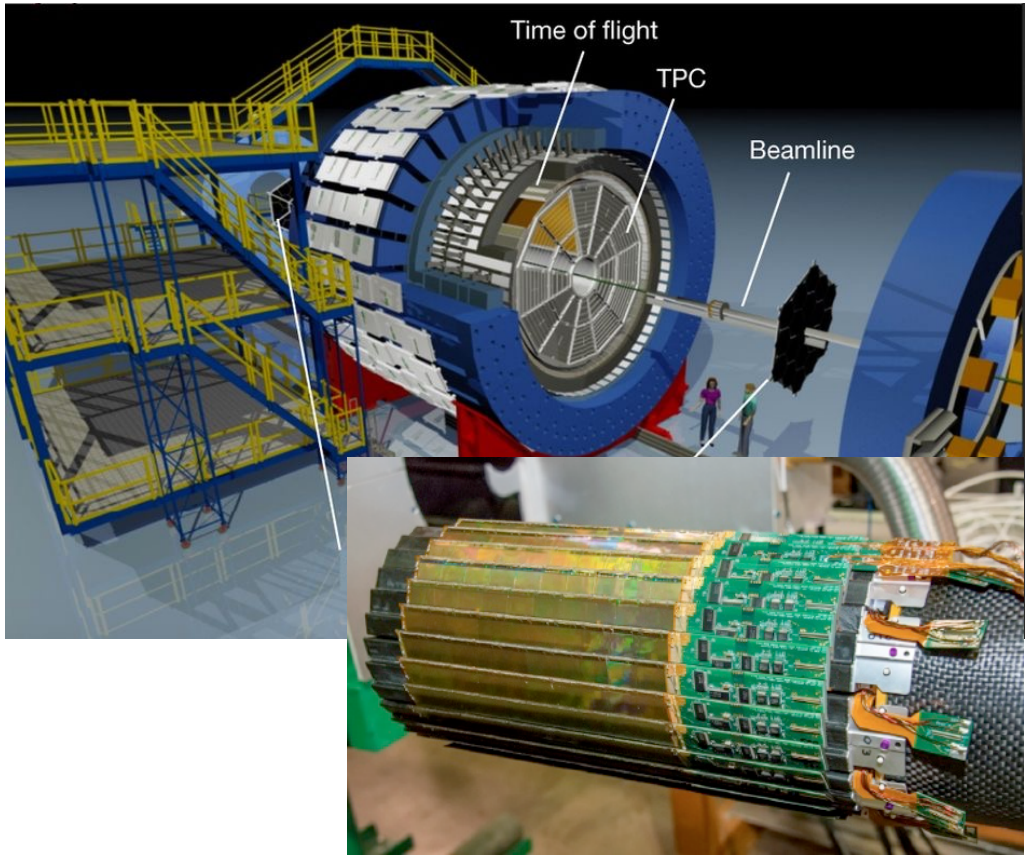
First MAPS with integrated zero-suppressed readout, used for several applications, also EUDET telescope

First use of MAPS in HEP



ULTIMATE CHIP in STAR

MIMOSA28 (ULTIMATE) in STAR PXL



courtesy of STAR Collaboration

356 M pixels on ~0.16 m² of silicon

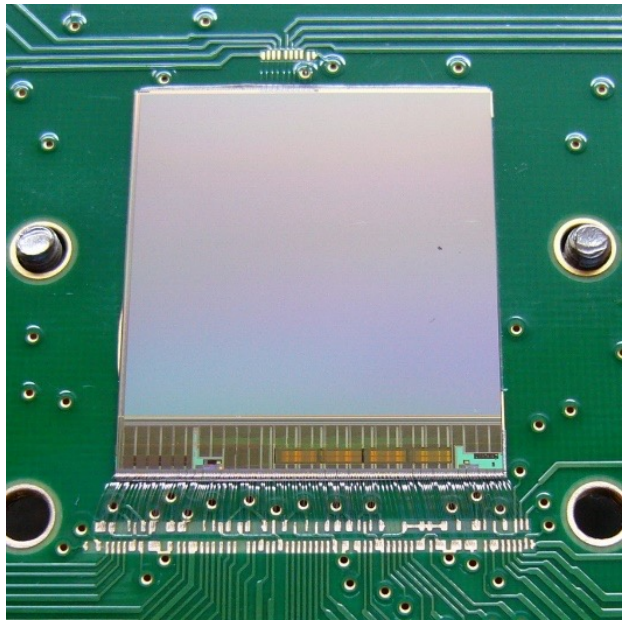
Full detector Jan 2014

Physics Runs in 2015-2016

- 2 layers (2.8 and 8 cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector
- Radiation length (1st layer)
- x/X0 = 0.39% (Al conductor flex)

Ladder with 10 MAPS sensors

2-layer kapton flex cable with Al traces



MIMOSA28 (ULTIMATE) – 2011

First MAPS system in HEP

Twin well 0.35 µm CMOS (AMS)

- 18.4 µm pitch
- 576x1152 pixels, 20.2 x 22.7 mm²
- Integration time 190 µs
- No reverse bias -> NIEL ~ 10^{12} n_{eq}/cm^2
- Rolling shutter readout

KEY ENABLERS: The INMAPS process: STFC development, in collaboration with TowerJazz: a game changer

Additional deep p-well implant allows full CMOS in the pixel and 100 % fill factor

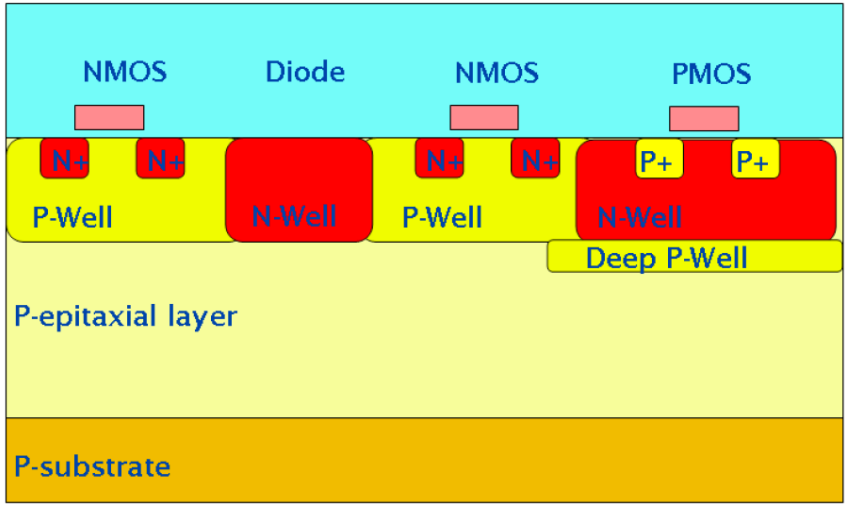
Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels

Jamie Alexander Ballin [2], Jamie Phillip Crooks [1], Paul Dominic Dauncey [2], Anne-Marie Magnan [2], Yoshinari Mikami [3,**], Owen Daniel Miller [1,3], Matthew Noy [2], Vladimir Rajovic [3,***], Marcel Stanitzki [1], Konstantin Stefanov [1], Renato Turchetta [1,*], Mike Tyndel [1], Enrico Giulio Villani [1], Nigel Keith Watson [3], John Allan Wilson [3]

[1] Rutherford Appleton Laboratory, Science and Technology Facilities Council (STFC), Harwell Science and Innovation Campus, Didcot, OX11 0QX, U.K

[2] Department of Physics, Blackett Laboratory, Imperial College London, London, SW7 2AZ, U.K

[3] School of Physics and Astronomy, University of Birmingham, Birmingham, B15 2TT, U.K

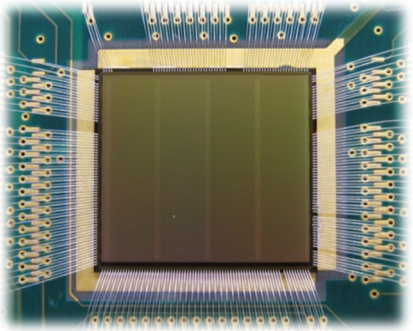


Sensors 2008 (8) 5336, DOI:10.3390/s8095336

New generation of CMOS sensors for scientific applications in TowerJazz CIS 180nm

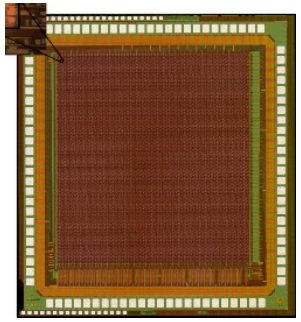
courtesy of STFC

TPAC
ILC ECAL (CALICE)



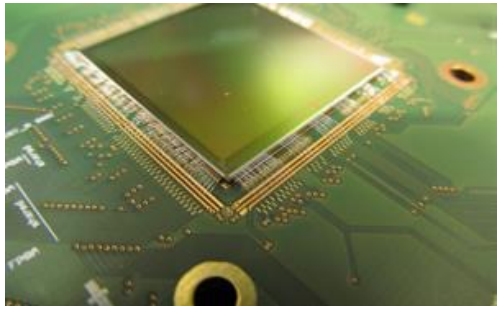
50μm pixel

DECAL
Calorimetry



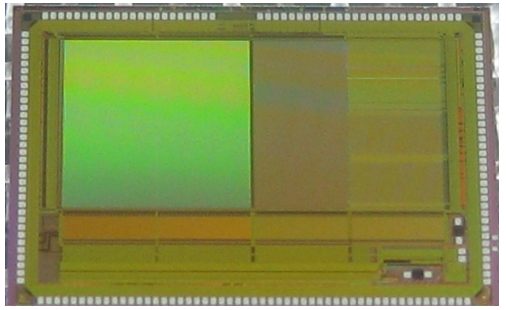
50μm pixel

PIMMS
TOF mass spectroscopy

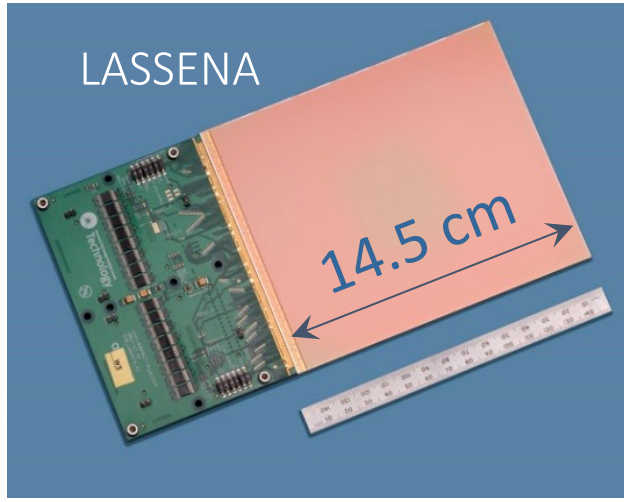


70μm pixel

CHERWELL
Calorimetry/Tracking



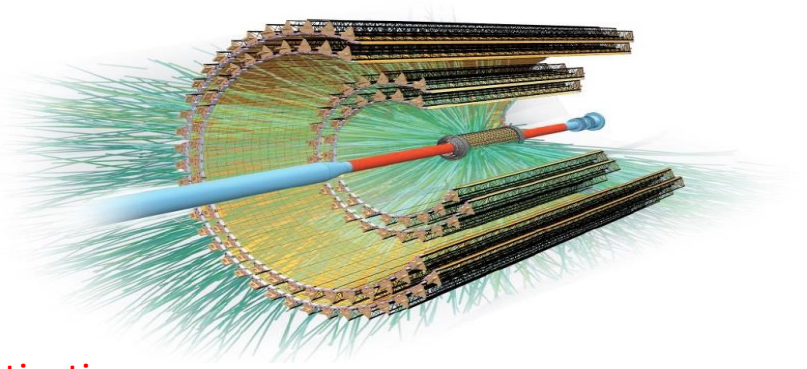
48 μm x 96 μm pixel



50μm pixel, waferscale

Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

ALICE ITS2 upgrade



Motivation

- 3x better impact parameter resolution
- Better tracking efficiency and momentum resolution at low pT
- Faster readout
- Fast removal and insertion

Technical Design Report for the Upgrade of the ALICE Inner Tracking System
J. Phys. G 41 (2014) 087002
CERN-LHCC-2013-024 ; ALICE-TDR-017

Sensor chip requirements

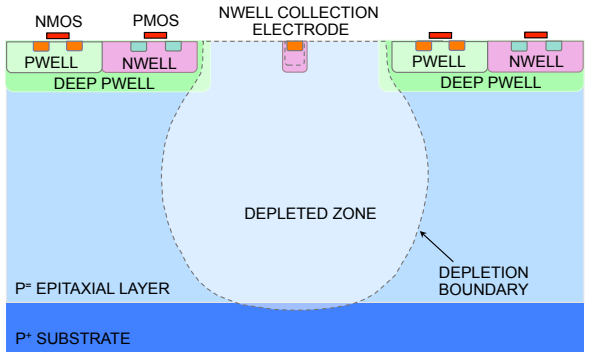
Parameter	**Inner Barrel**	**Outer Barrel**
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-5}$ evt^{-1} pixel^{-1} (ALPIDE $<< 10^{-5}$)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7 x 10^{13}	1.7 x 10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

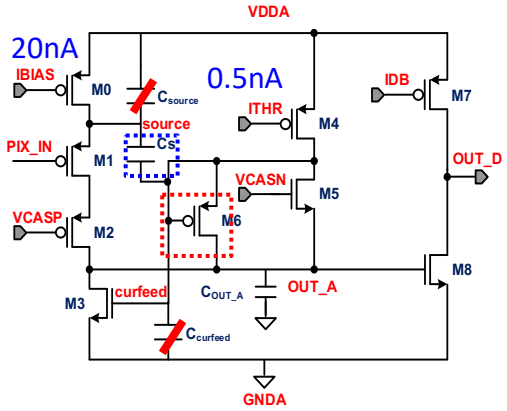
(*) In color: ALPIDE performance figure where above requirements
(**) 10x radiation load integrated over approved program (~ 6 years)

Thin sensors (50 μm), high granularity (~30 x 30 μm^2), large area (10 m^2)
moderate radiation (TID 2.7 Mrad & NIEL 1.7 10^{13} 1 MeV n_{eq}/cm^2)

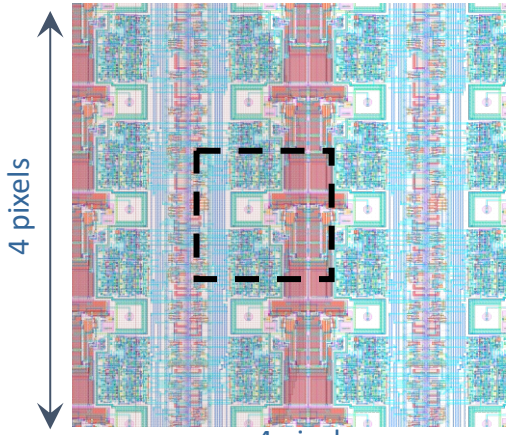
→ Monolithic Active Pixel Sensors

ALPIDE chip in ALICE ITS2

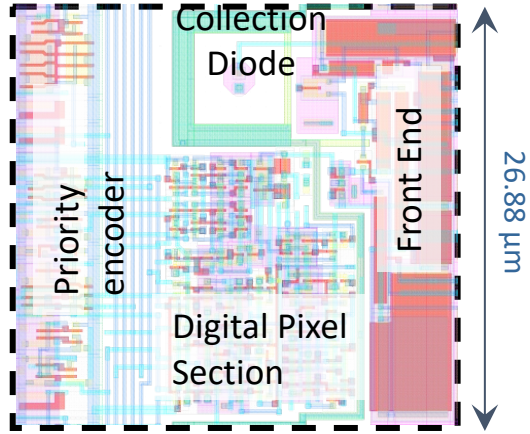




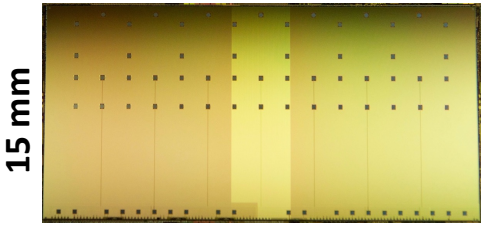
Matrix layout

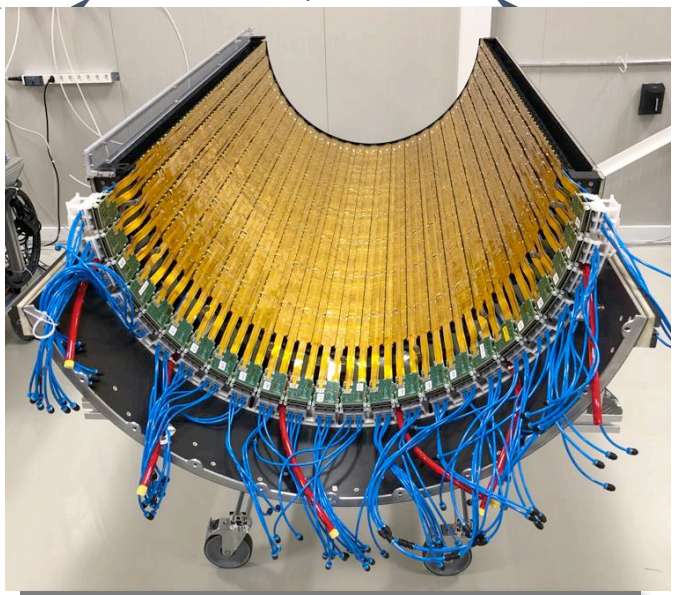


Pixel layout

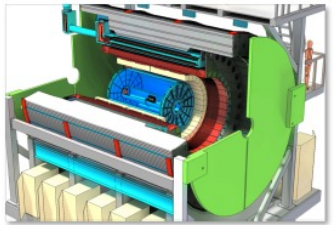


- TJ CMOS 180 nm INMAPS imaging process (TJ) > 1kΩ cm p-type epitaxial layer
- Small 2 µm n-well diode and reverse bias for low capacitance C(sensor+circuit) < 5 fF
- 40 nW continuously active front end D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- Q_{in}/C ~ 50 mV, analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- Zero-suppressed readout, no hits no digital power G. Aglieri et al. NIM A 845 (2017) 583-587
- Ratio between 15 x 30 mm² and 10 m² in the experiment not ideal -> stitching would have been of interest
- ALPIDE (ALICE Pixel Detector) to be used for several other physics experiments, in space and for medical applications

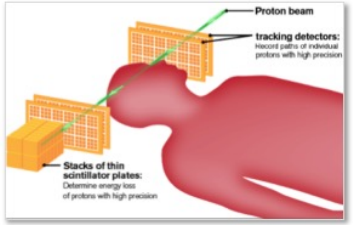




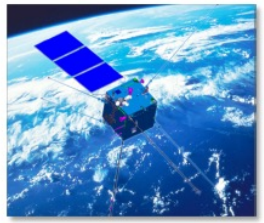
Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m² sensitive area



sPHENIX



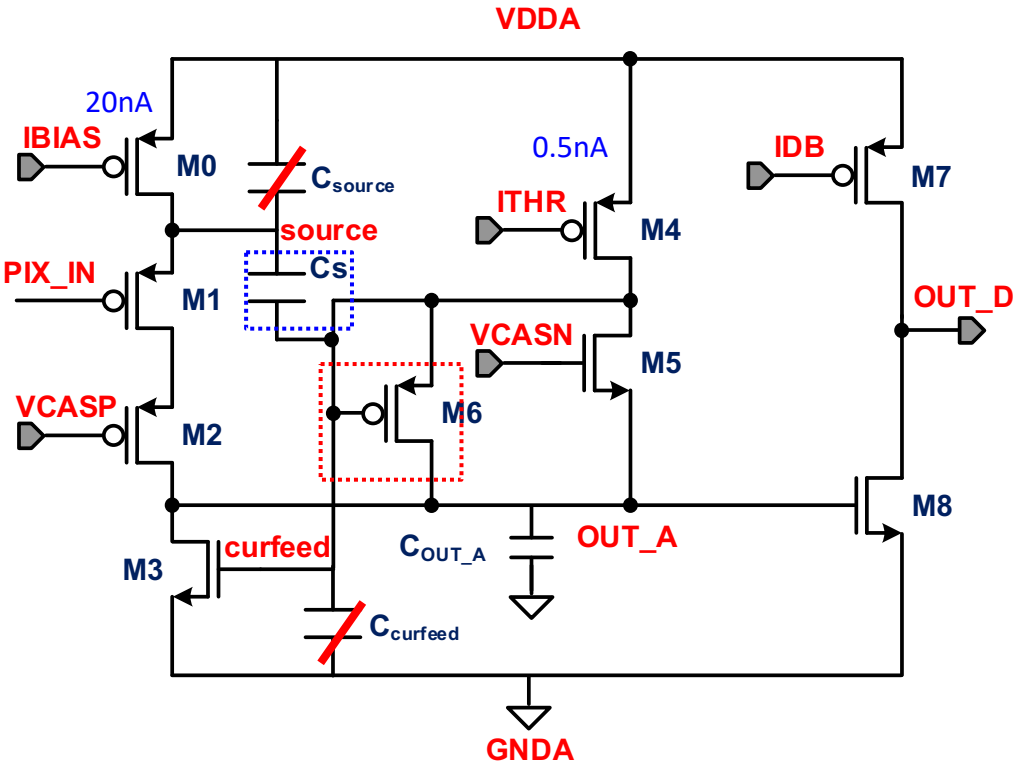
Proton CT (tracking)

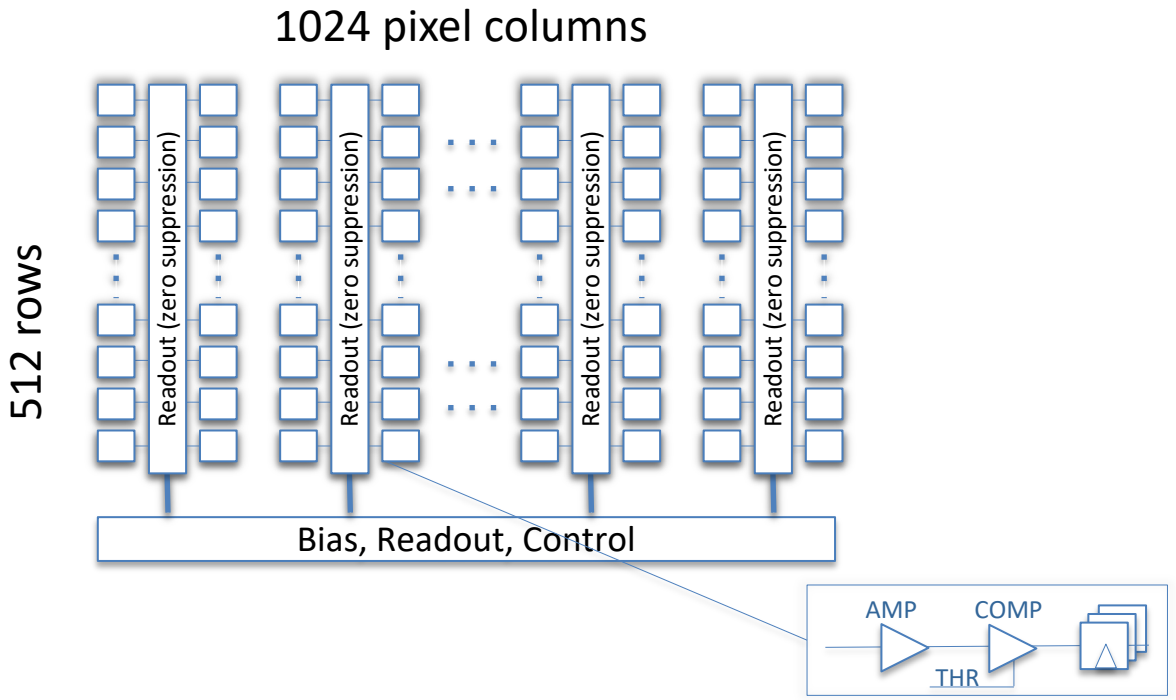


CSES – HEPD2

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test
1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

FRONT END and READOUT





Front end (40 nW, continuously active)

D. Kim et al. TWEPP 2015,

DOI 10.1088/1748-0221/11/02/C02042

- Analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- C(sensor+circuit) < 5 fF, Q/C ~ 50 mV in ALPIDE
- Used as a starting point for ATLAS development

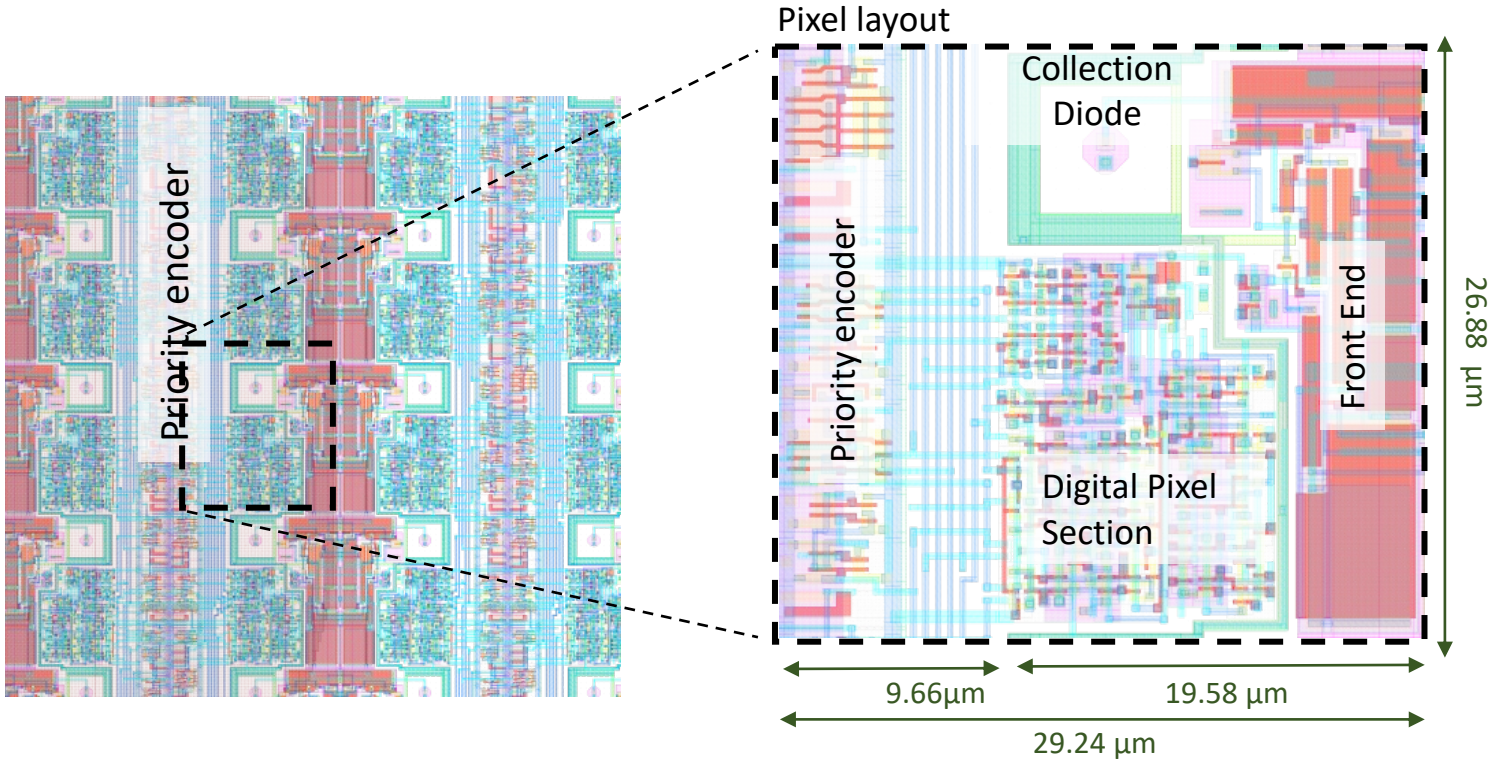
Matrix

G. Aglieri et al. NIM A 845 (2017) 583-587

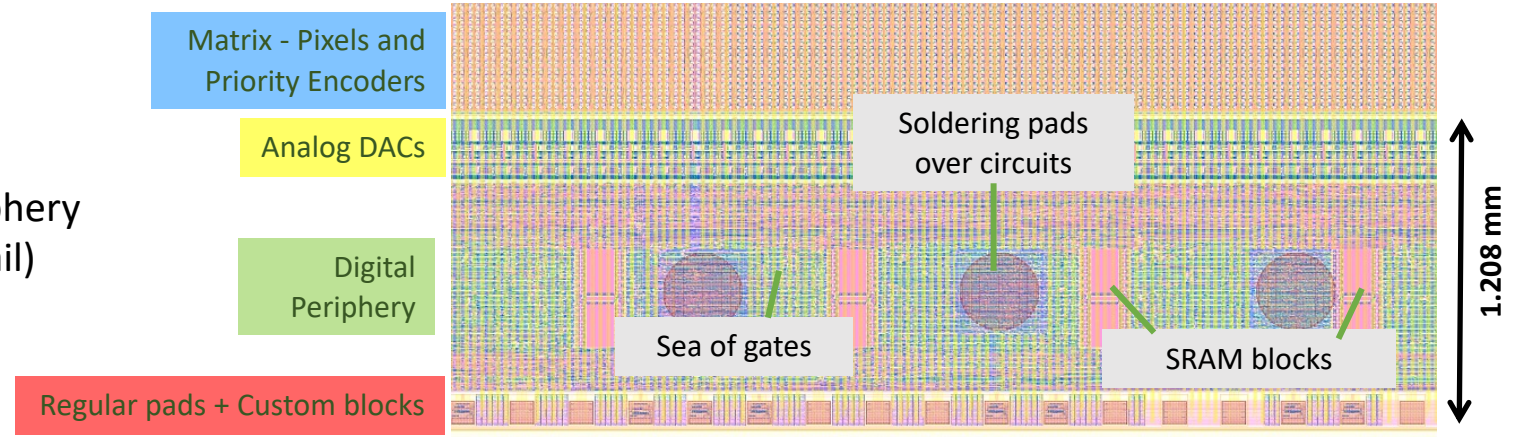
- 29 μm x 27 μm pixel pitch
- In pixel amplification and discrimination and 3 data registers
- Global shutter, triggered or continuous readout
- Zero suppressed readout, no hits no power

ALPIDE Layout features

Matrix (detail)

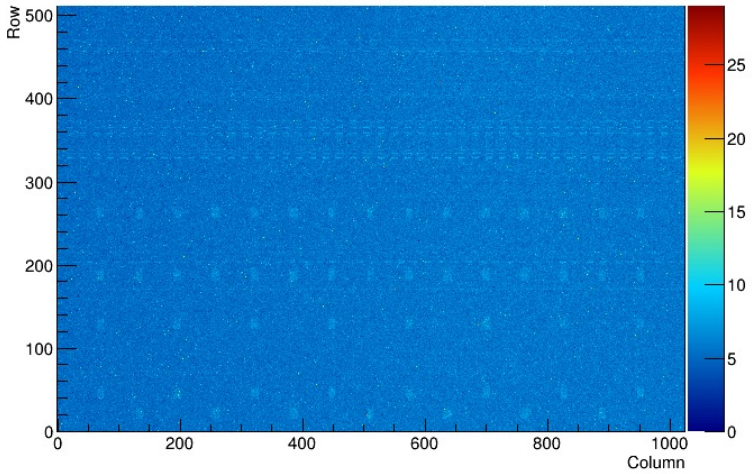


Periphery (detail)

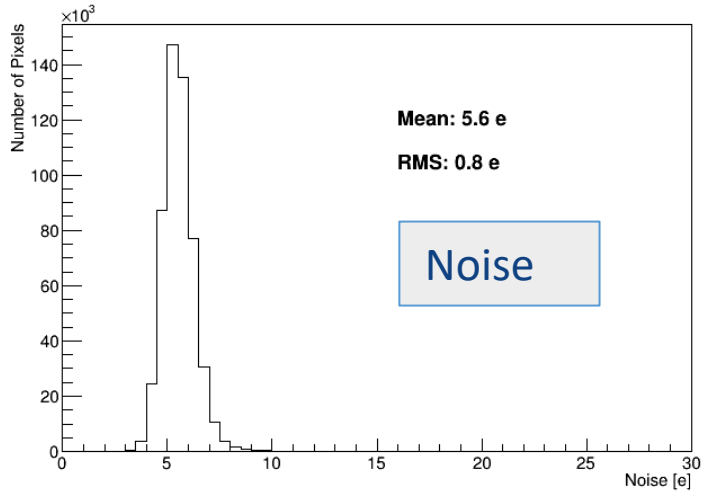


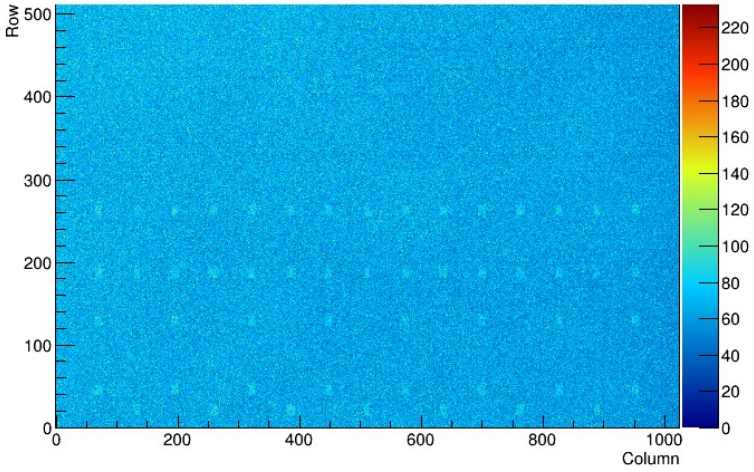
Some results: charge threshold and noise

V_{BB}=-3V

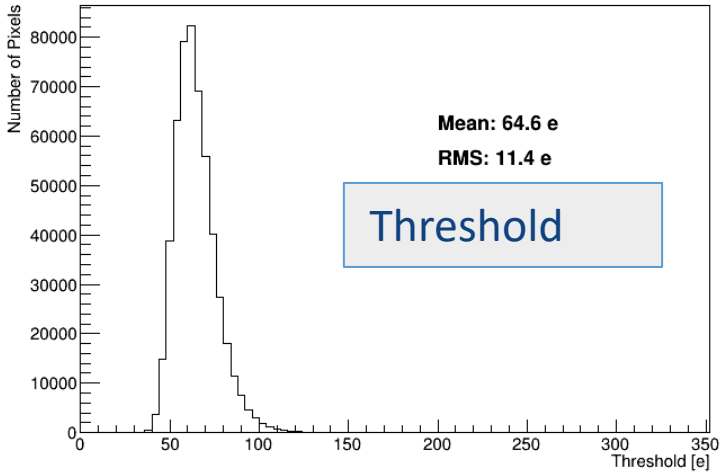


noise in electrons



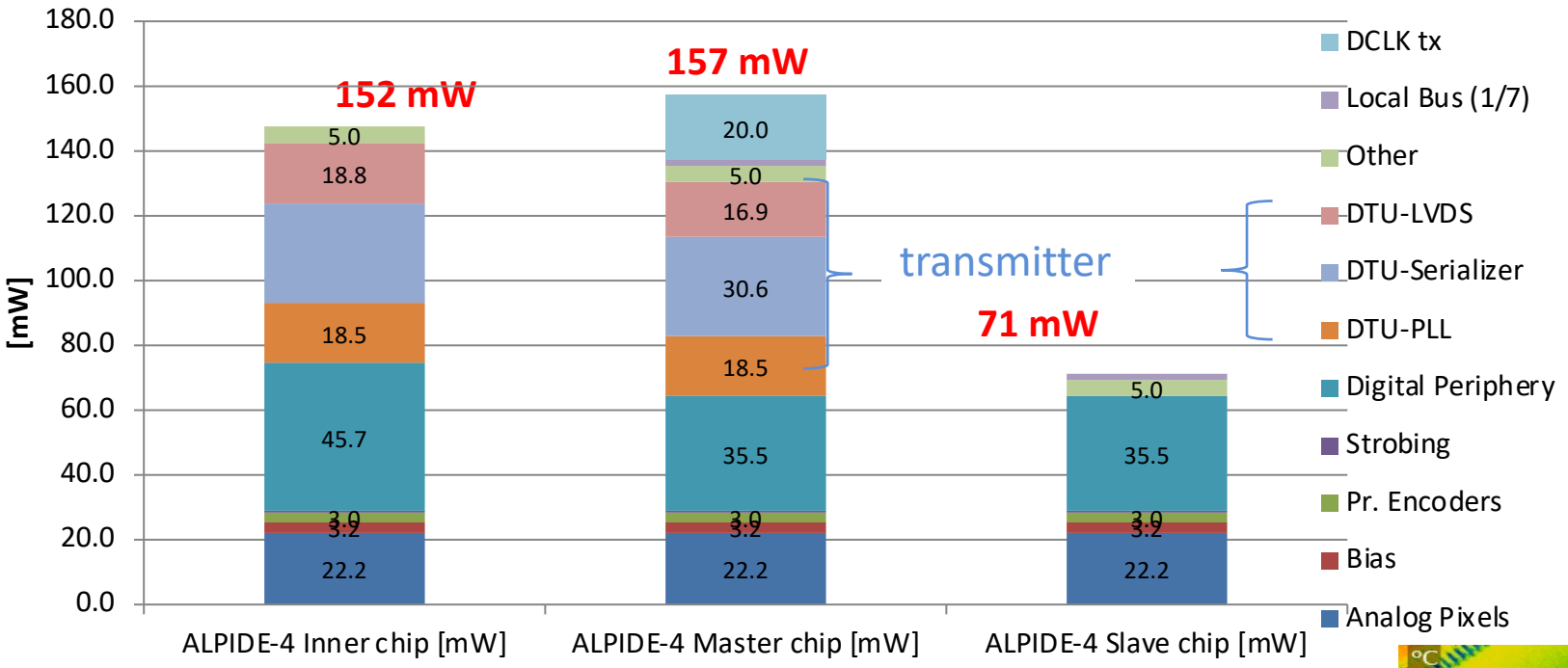


thresholds in electrons



M. Keil

ALPIDE Power consumption



Sensitive area: 4.12 cm^2

Inner Barrel: 36.9 mW/cm^2

Outer Barrel: 20.2 mW/cm^2

In the matrix:

(analog + digital)/area

(22.2 + 3.2)/4.12

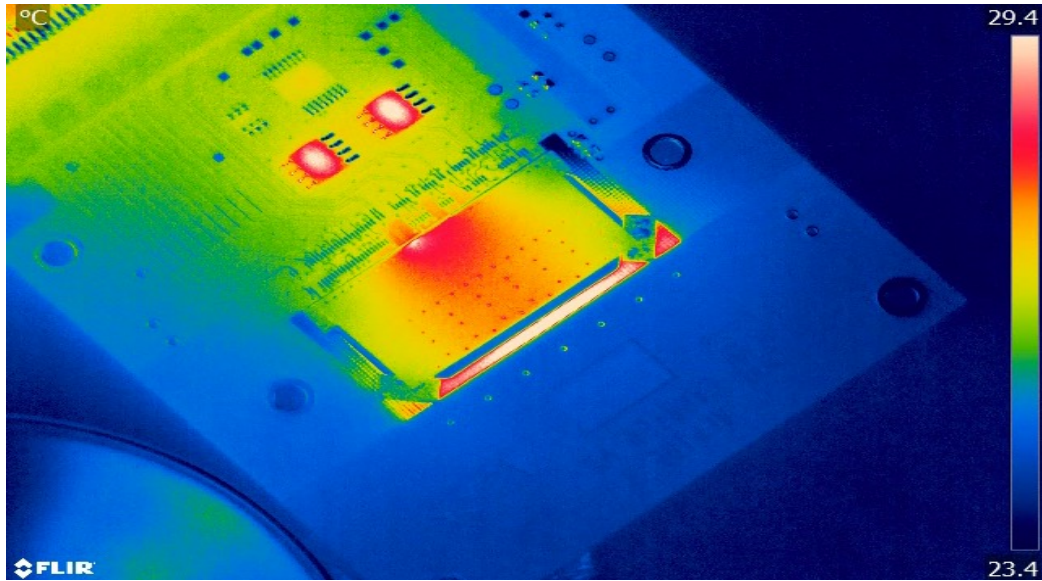
= 6.2 mW/cm^2

With 40 nW front-end and Q/C ≈ 80 mV analog power consumption still dominant within the matrix

Matrix readout only active if hit present

Clock gating in the digital periphery

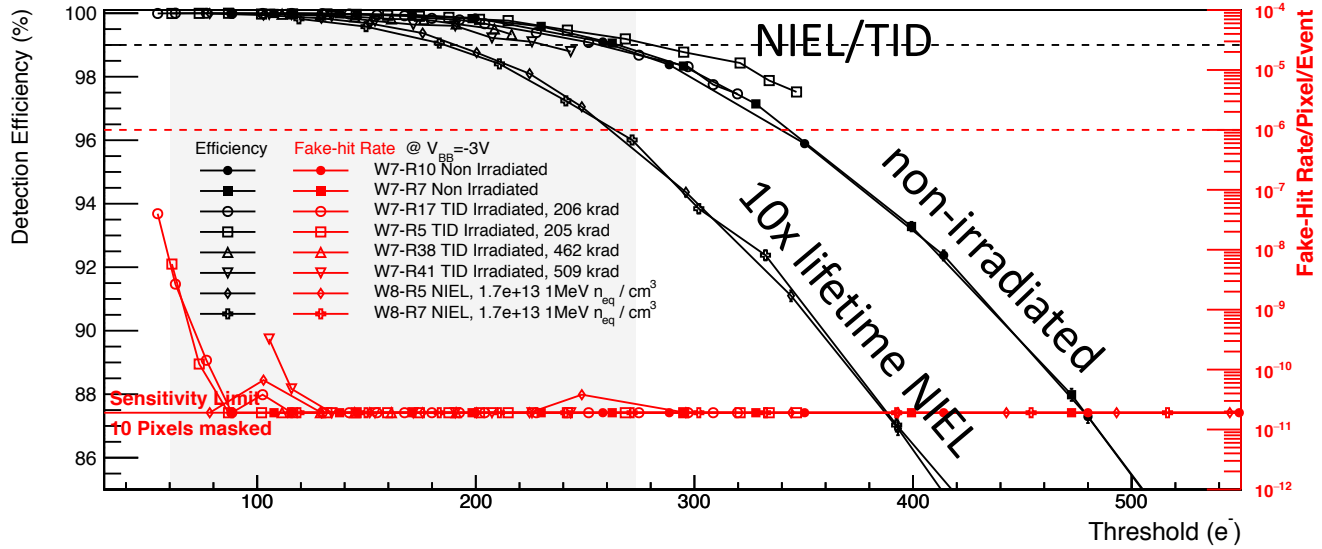
For the future more work needed on Q/C, architecture periphery and transmitter for overall power consumption



walter.snoeys@cern.ch

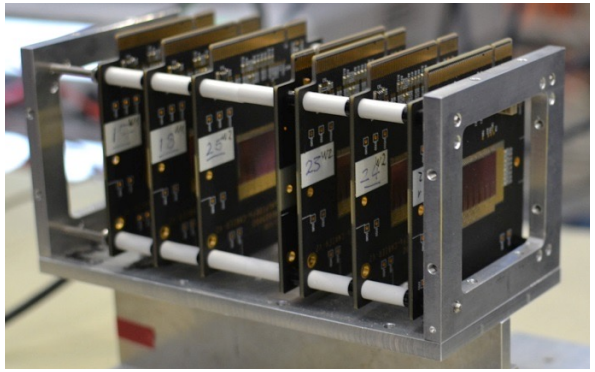
ALICE Pixel Detector (ALPIDE) sensor performance

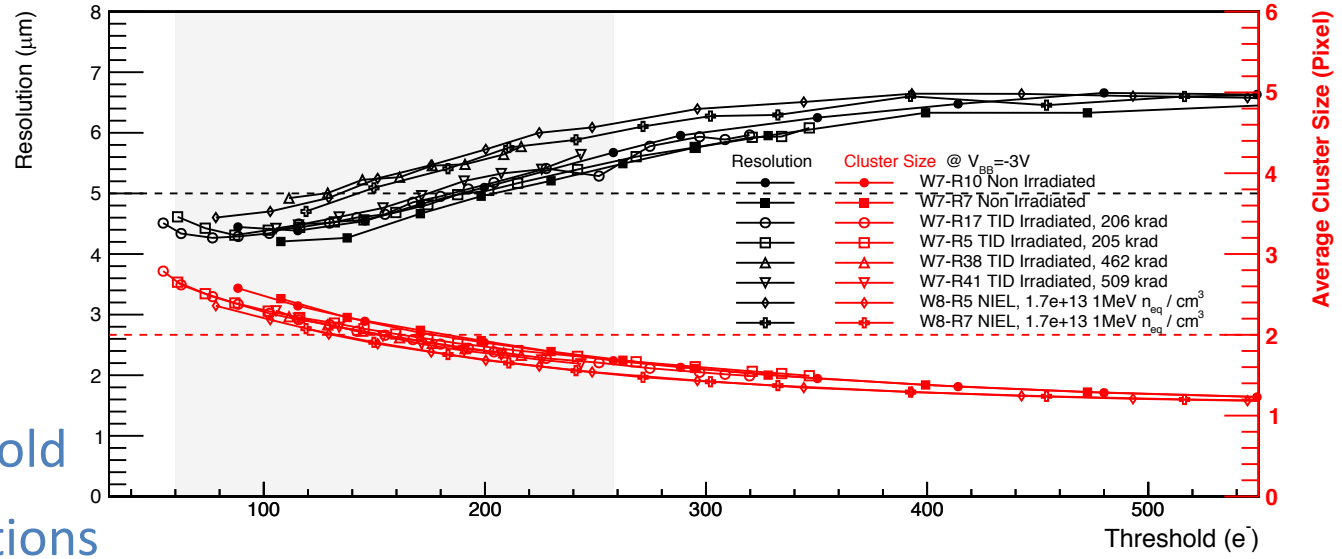
V_{BB}=-3V



Large operational margin with only 10 masked pixels (0.002 %), and 10^{-11} fake hit rate

Similar performance for non-irradiated and NIEL/TID chips





5 µm position resolution

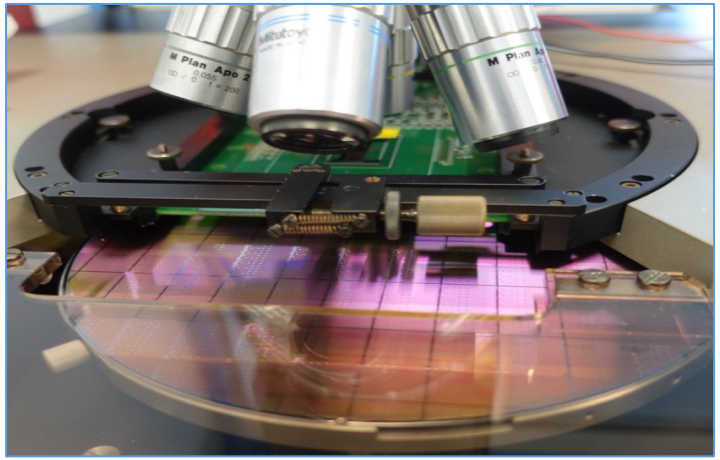
at 200 electrons charge threshold

Negligible chip-to-chip fluctuations

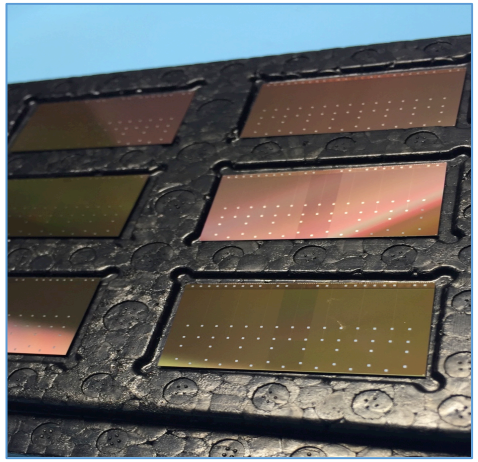
Nucl. Phys. A 967 (2017) 900-903

ALPIDE & ITS Upgrade status

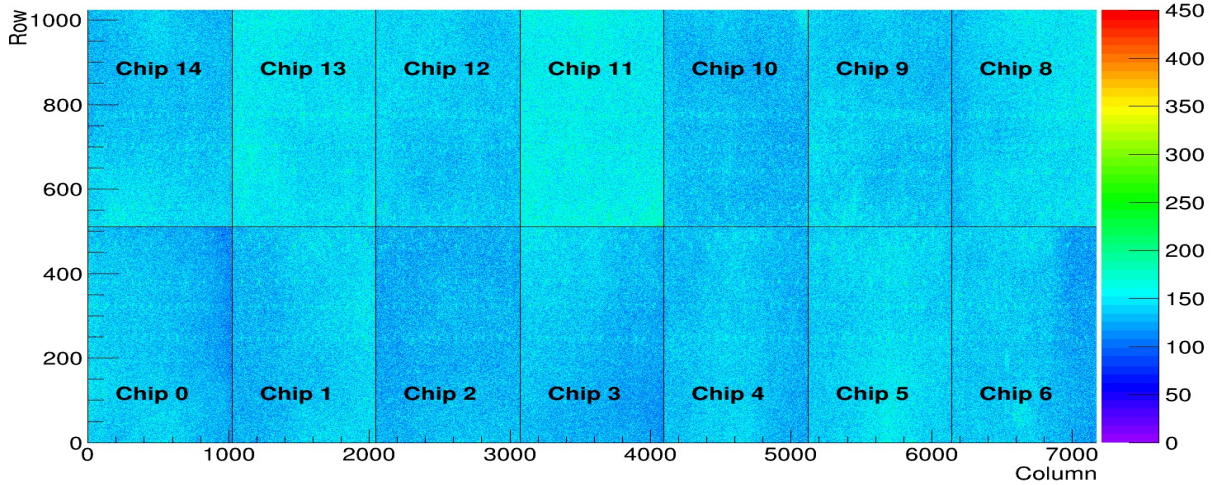
Wafer probe testing

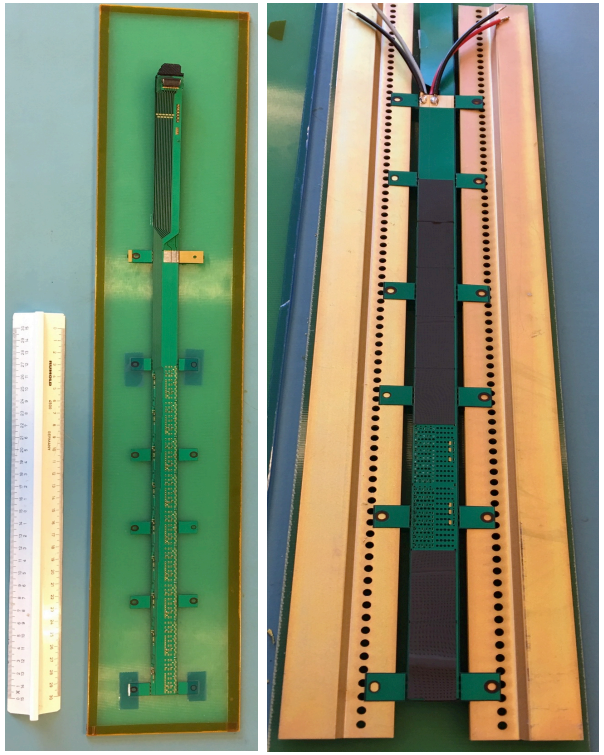


Single chips after thinning & dicing



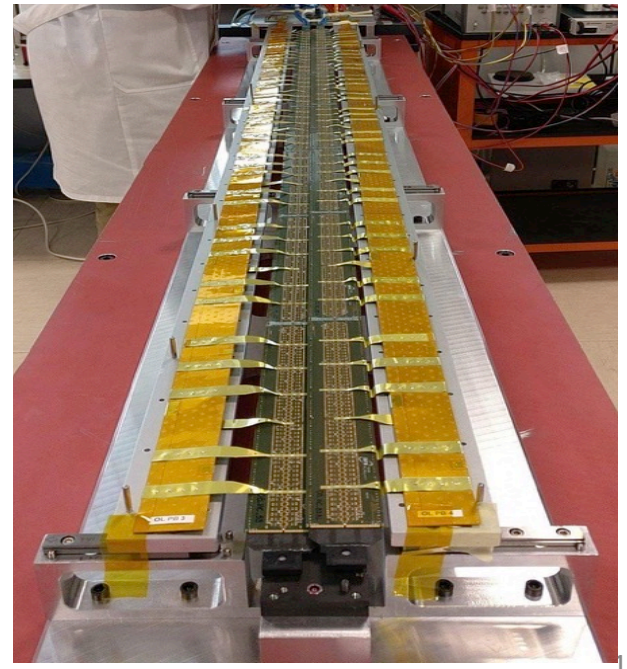
Threshold scan outer Barrel Module (14 chips)





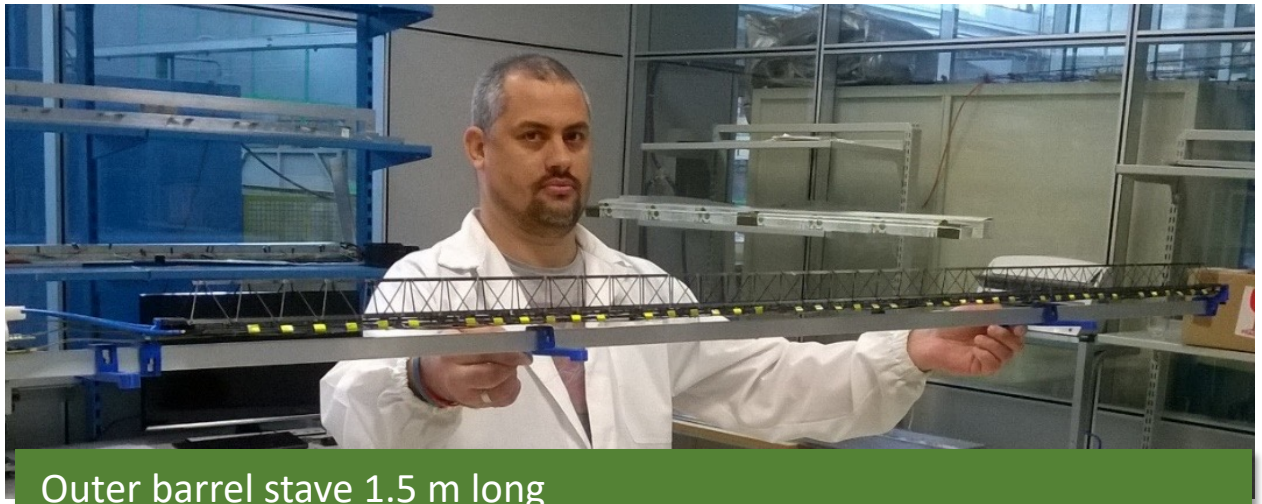
Inner Barrel Module (9 chips)

~1400 wafers produced for ITS2
3-4x more in total



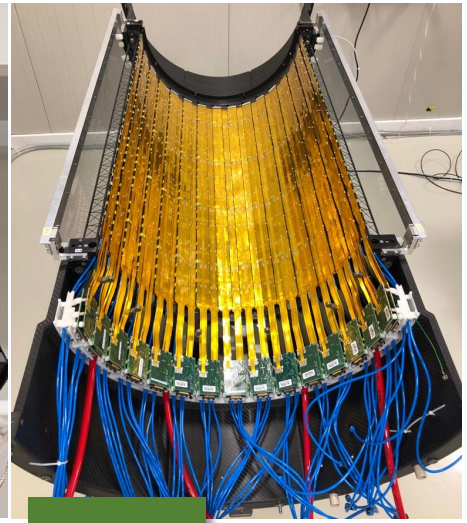
Outer Barrel Stave (~100 M pixels)

ALICE ITS construction

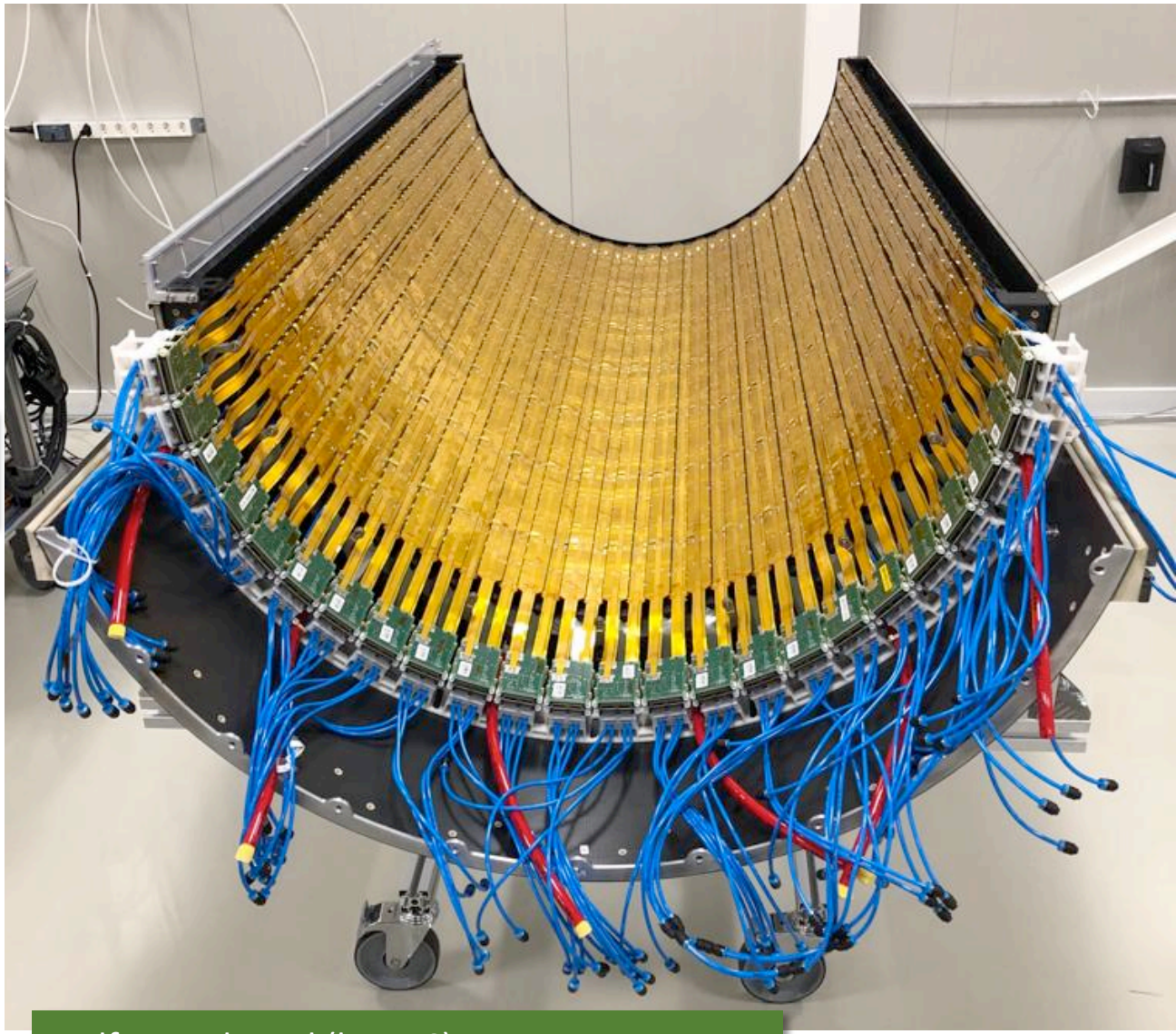


Outer barrel stave 1.5 m long
196 sensor chips, ~100 Mpixels, uniform noise 5 e^-, threshold 100 e^-

Inner layers 0 – 1 – 2



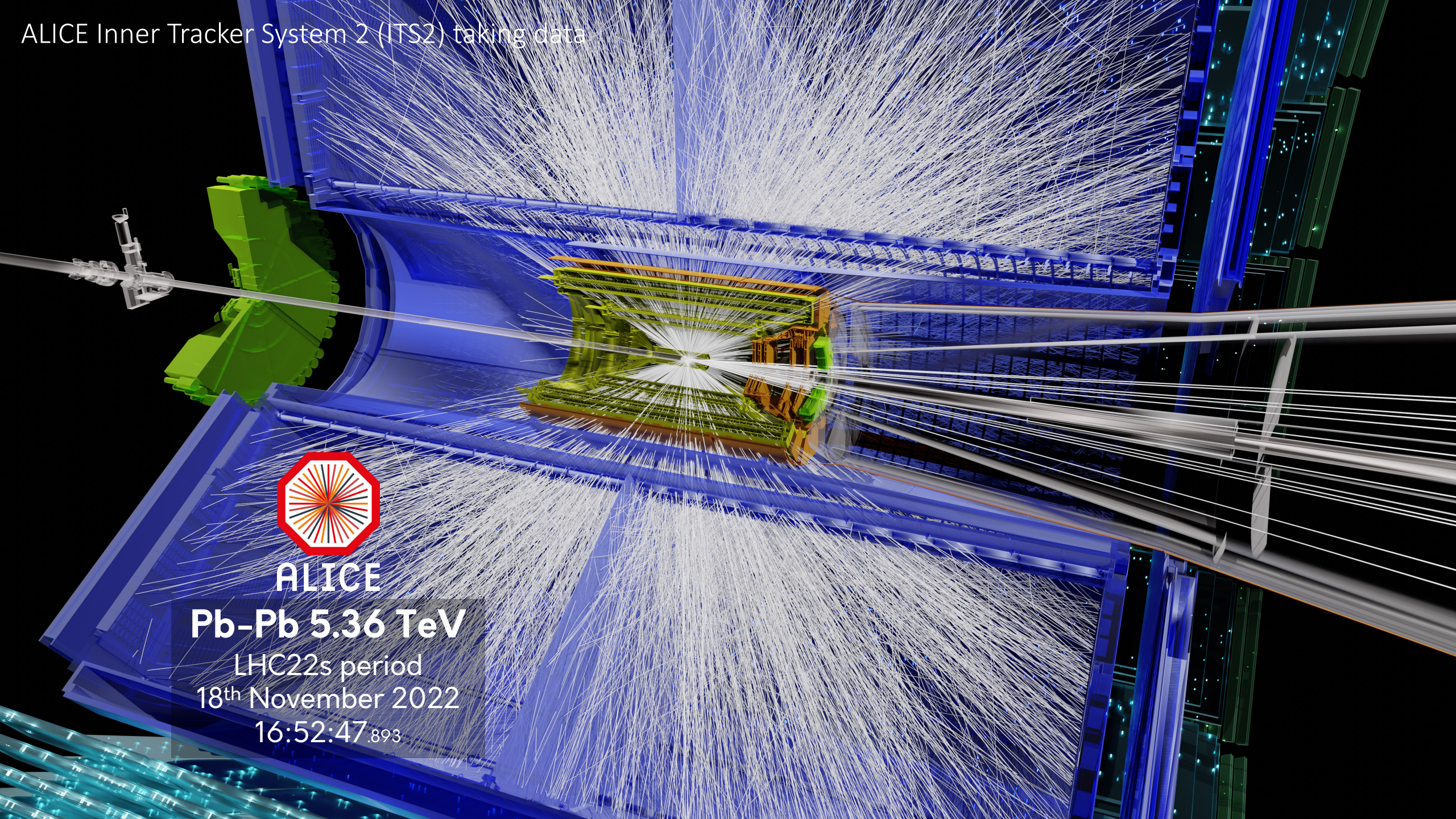
Layer 4



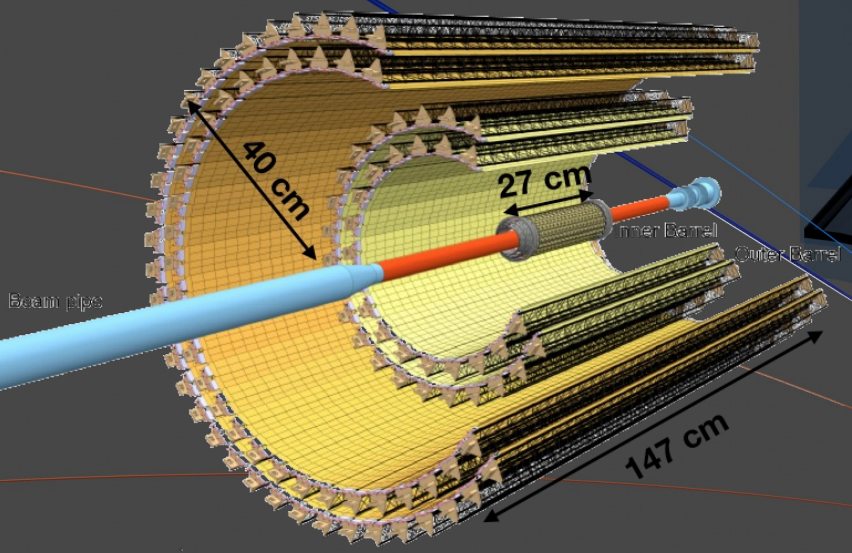
Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m^2 sensitive area

ALICE ITS installation (courtesy S. Beole)

ALICE Inner Tracker System 2 (ITS2) taking data



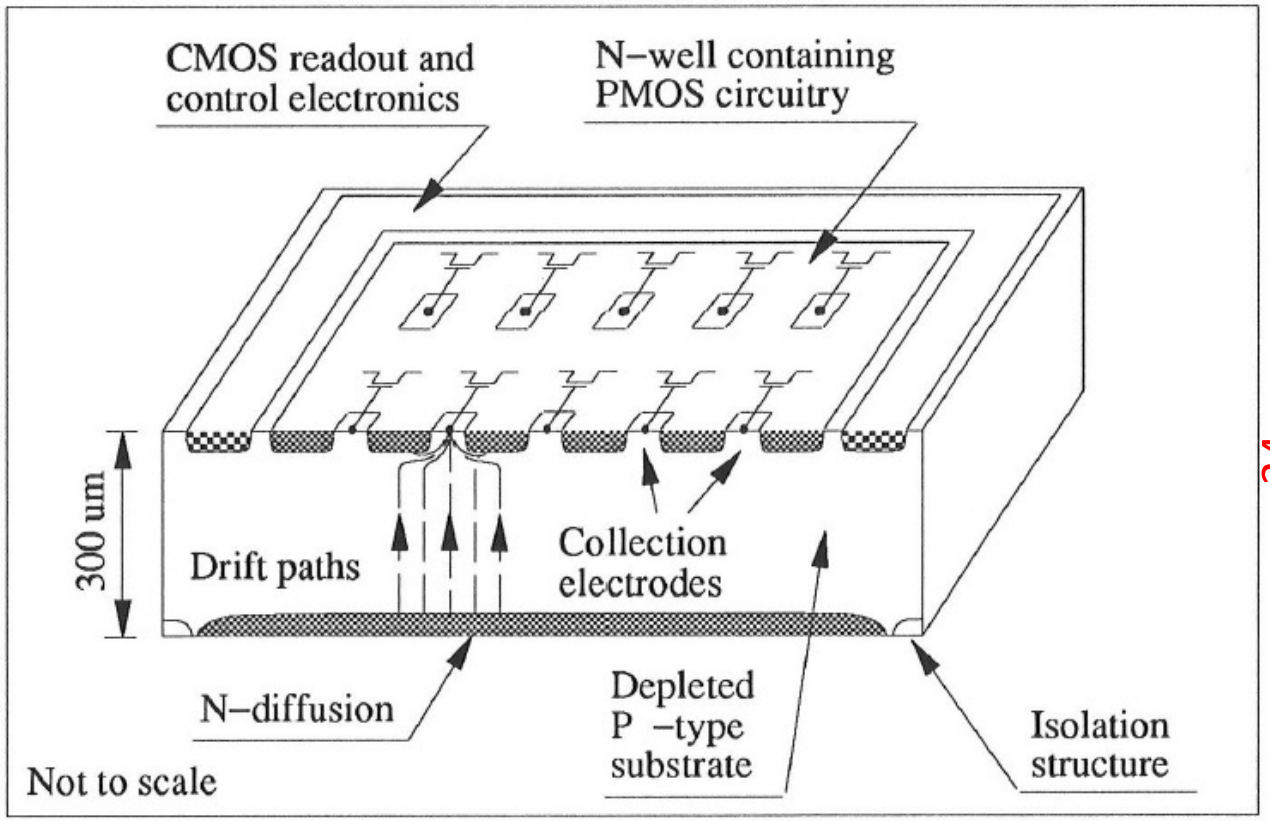
ALICE Inner Tracker System 2 (ITS2) taking data

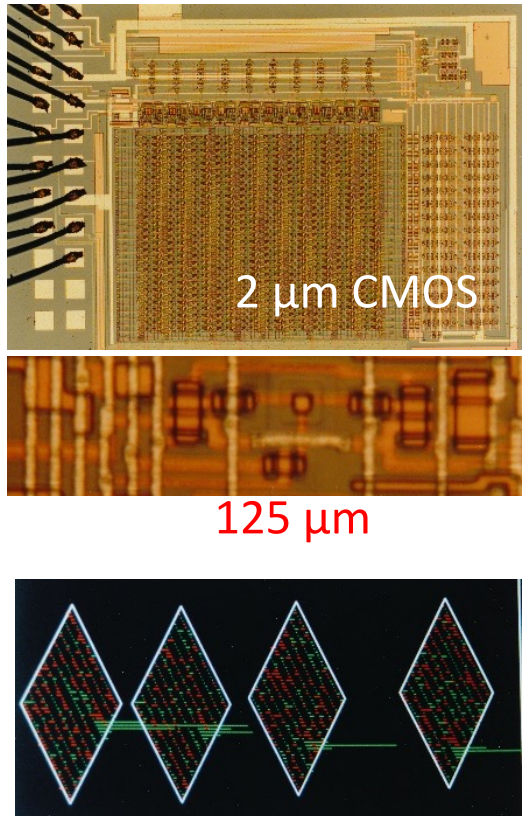


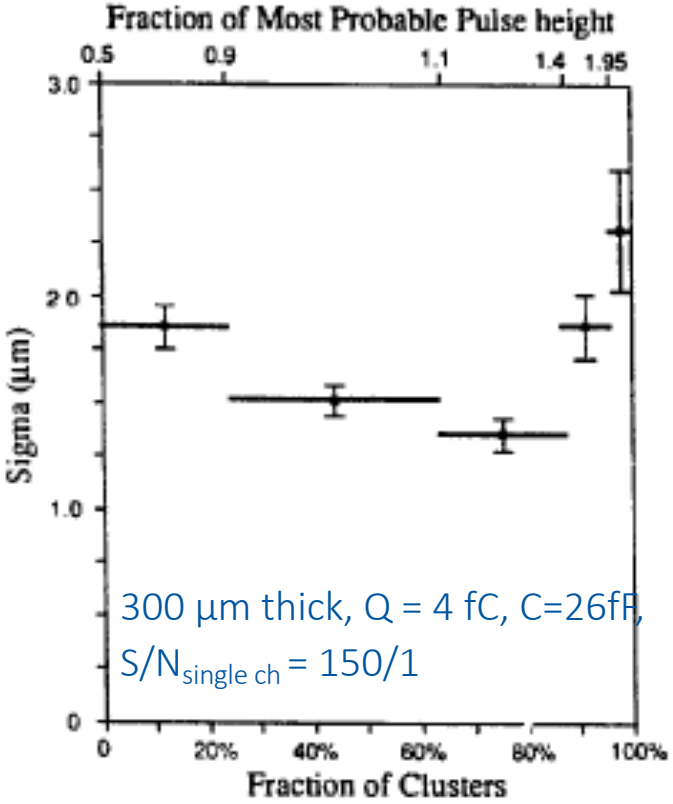
ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

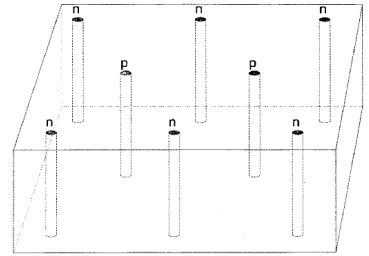
(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*
(1) ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

A monolithic detector for high energy physics (PhD thesis 1992), CMOS with double sided processing









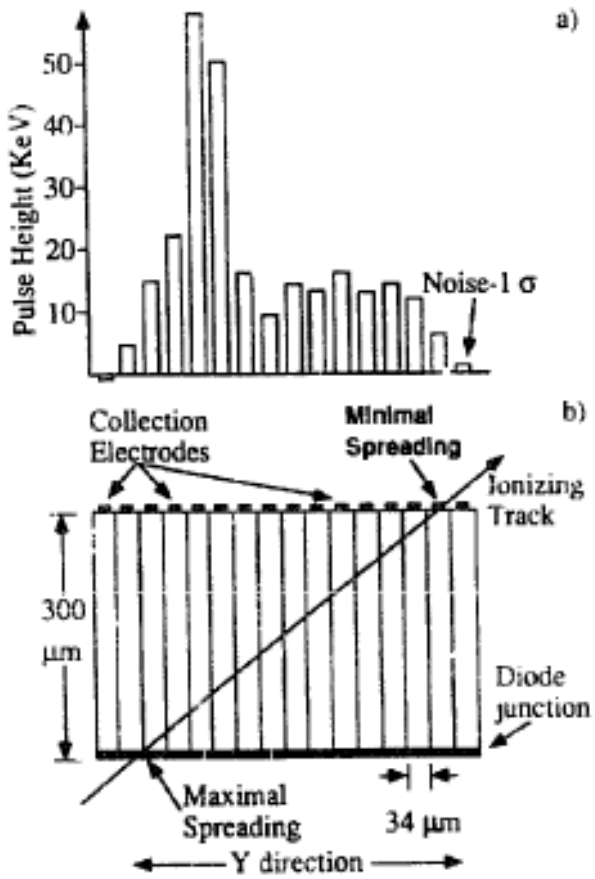
- Separation of junction from collection electrode
- Better than 2 µm position resolution even at large pitch due to good S/N
- Improved back side isolation with trenches lead to sensors with 3D electrodes (S.Parker) →

C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

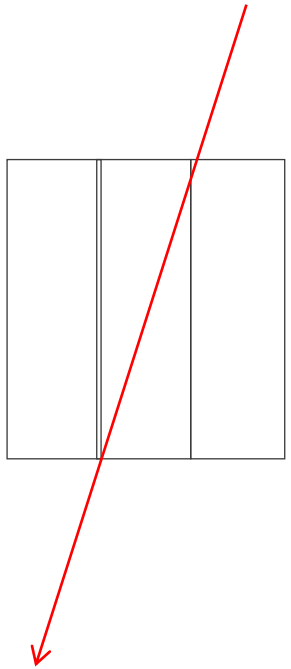
Other examples: ~ 1 µm resolution: SOI sensor, pitch 13.75 µm *M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53*

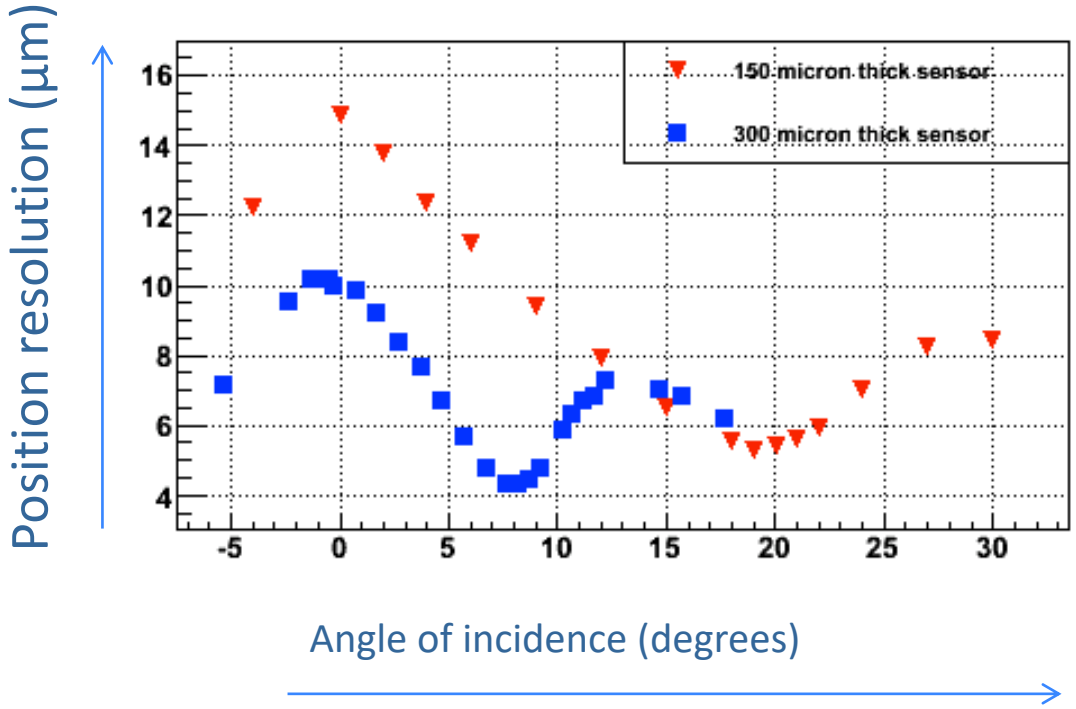
Position resolution: good S/N for interpolation Junction separation and back side processing: see below

Position resolution: inclined tracks



C. Kenney et al. NIM A 654 (2011) 258-265





Timepix3: X. Llopart, J. Buytaert, M. Campbell, P. Collins et al.

Average of extreme pixels in the cluster gives better results
In this case the signal (and the S/N) for a single channel reduces with track inclination

Can optimize resolution using track inclination to enhance charge sharing, can also be done using a magnetic field

Single point resolution

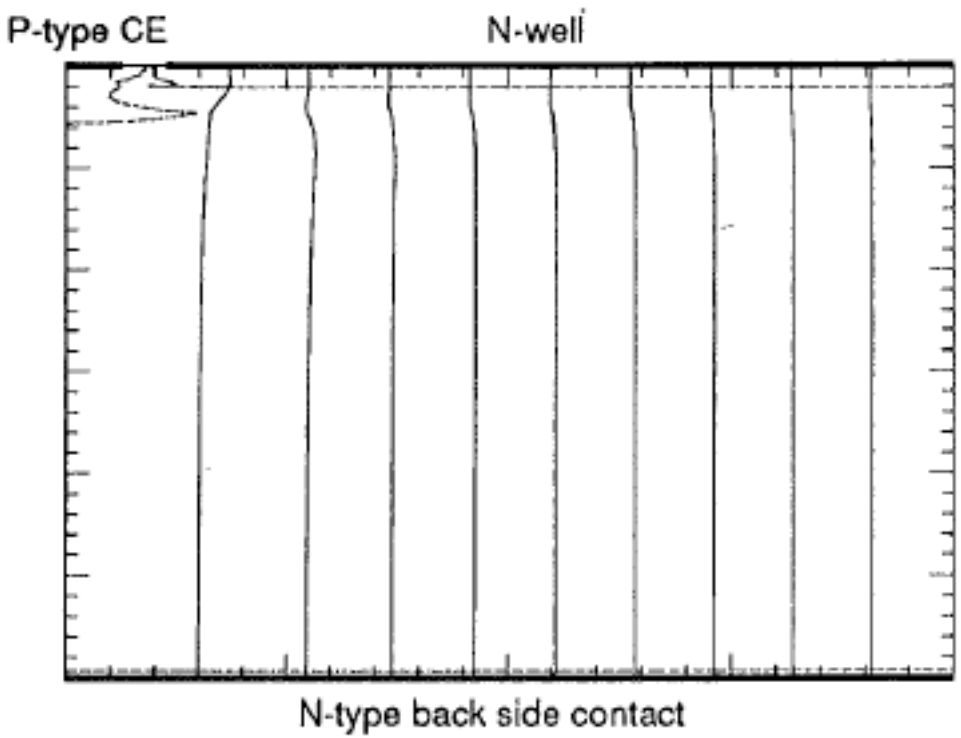
- Sensor can deliver ~ 1µm point resolution if granularity and S/N sufficient

- Examples used analog interpolation. With binary readout, single point resolution can be achieved as well. Need sufficient granularity, but also sufficient S/N.

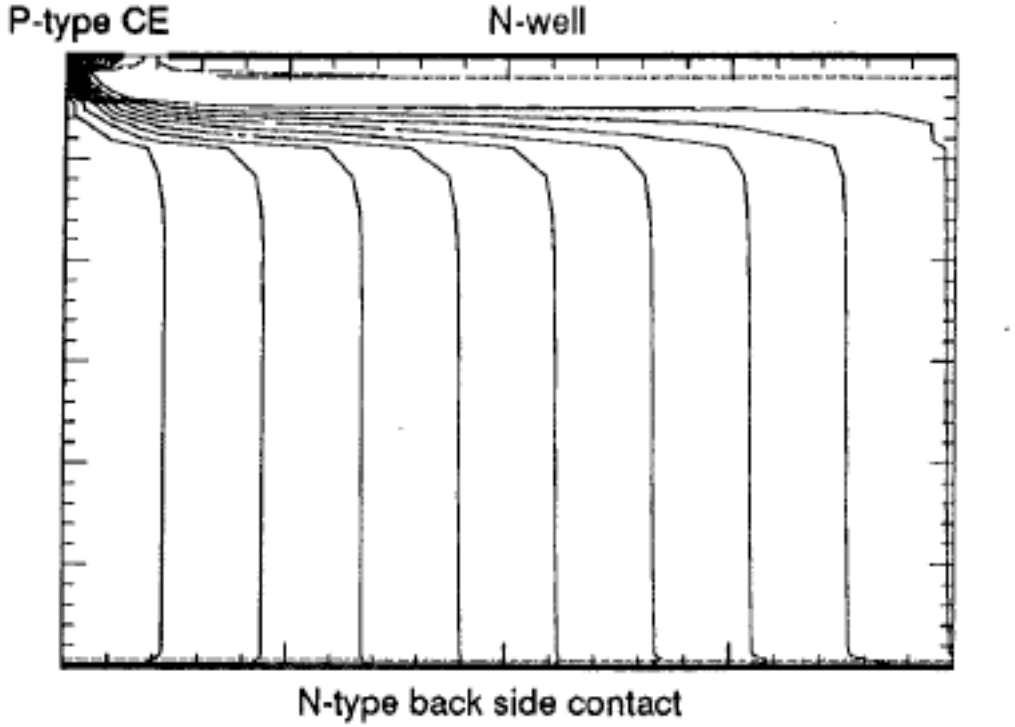
- Unless S/N is very large, detector depth and pixel pitch should be comparable to avoid degradation in S/N and hence resolution for inclined tracks.

Device simulation: Collection electrode always at gnd

Back side at 65 V to deplete from bottom to top

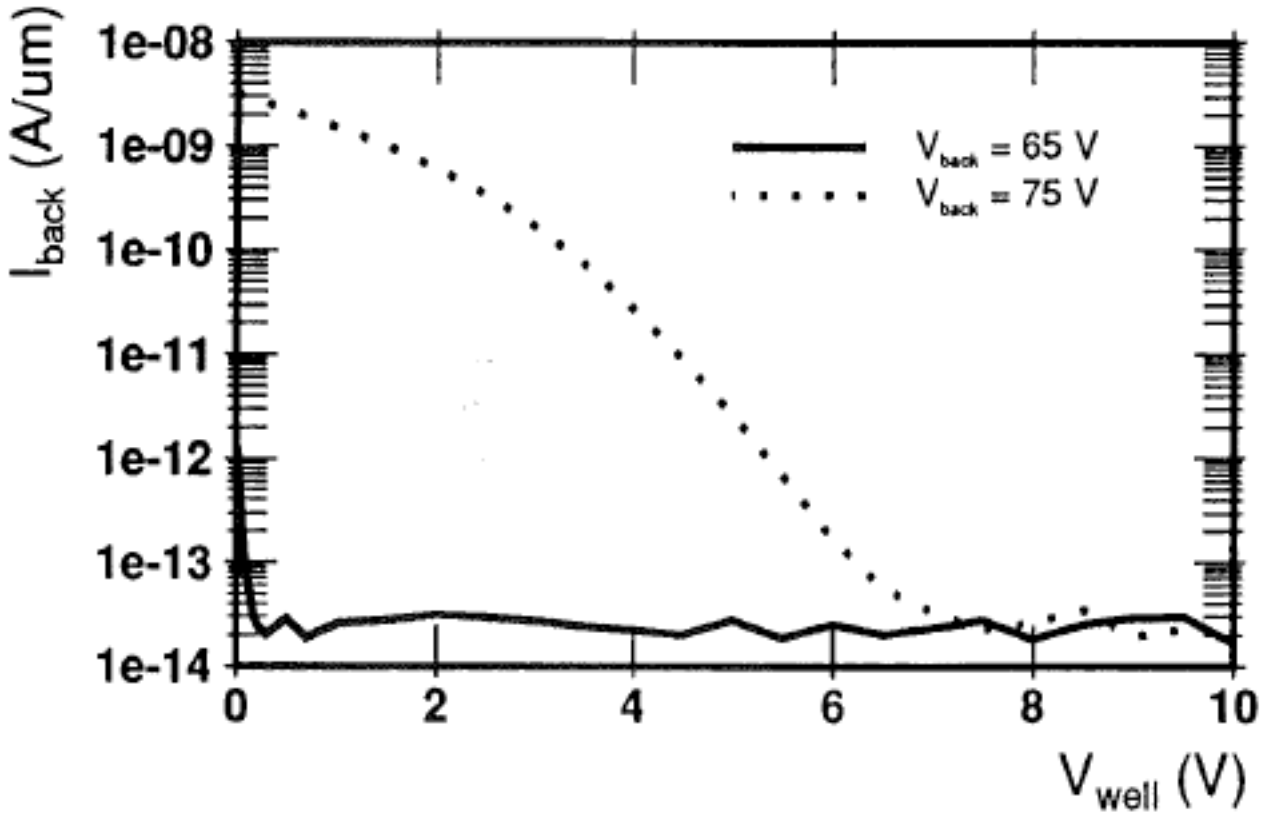


Vnwell at 0 V
punchthrough

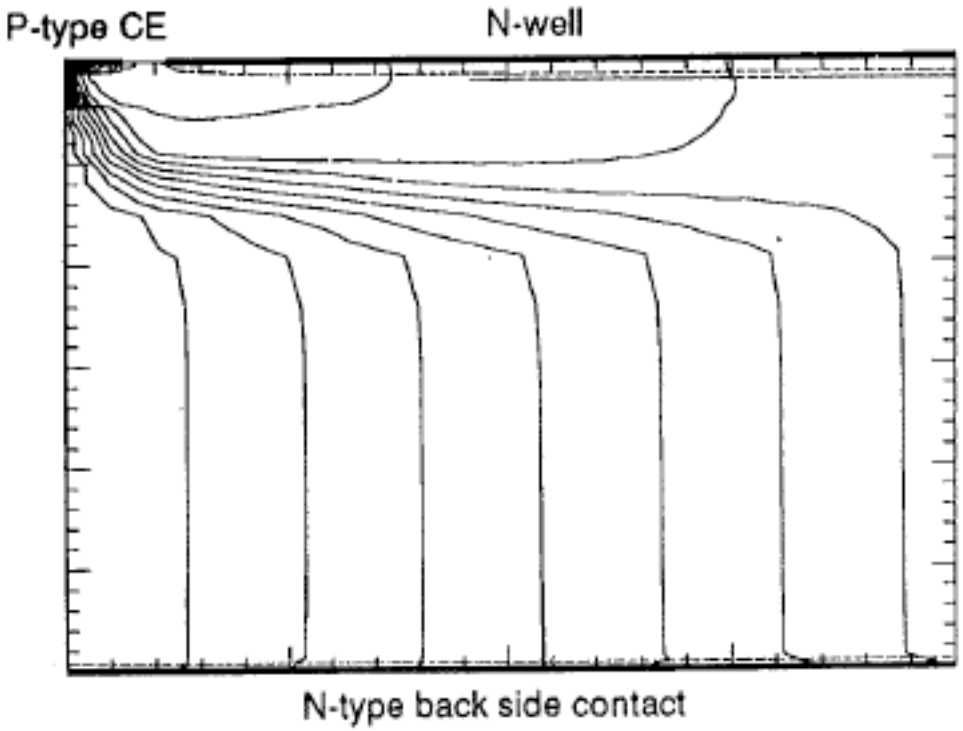


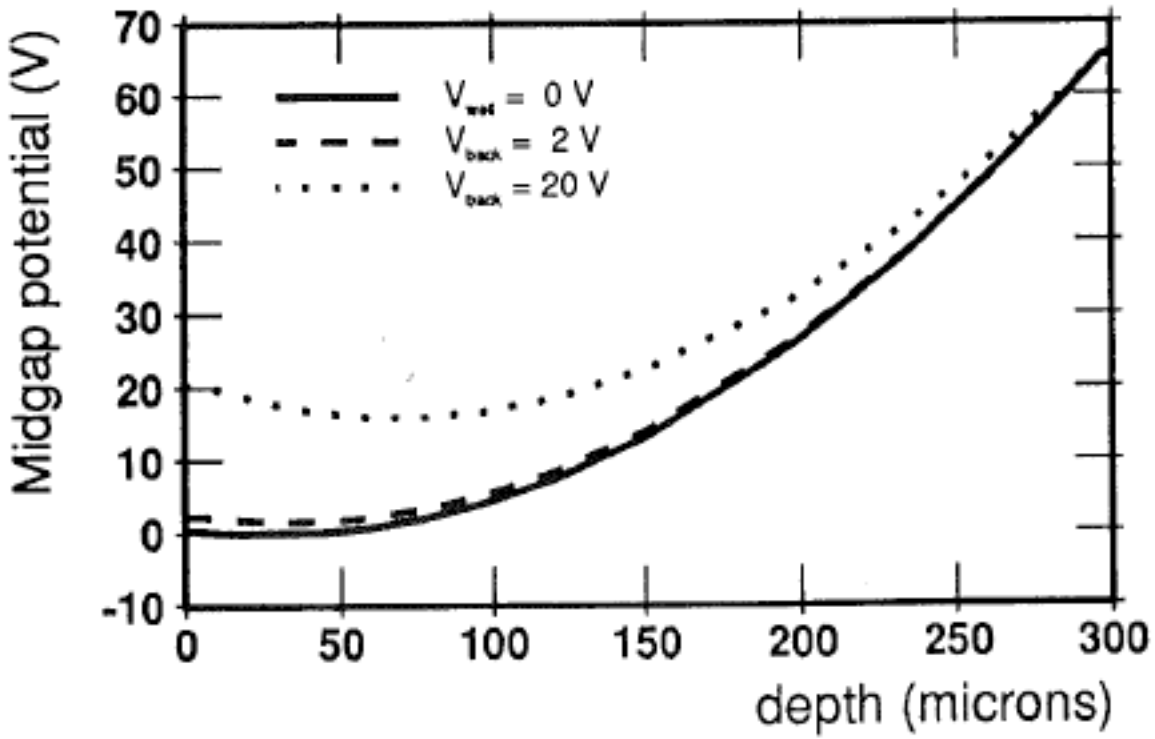
Vnwell at 2 V
No punchthrough

Device simulation: Switch off punch-through



Potential valley



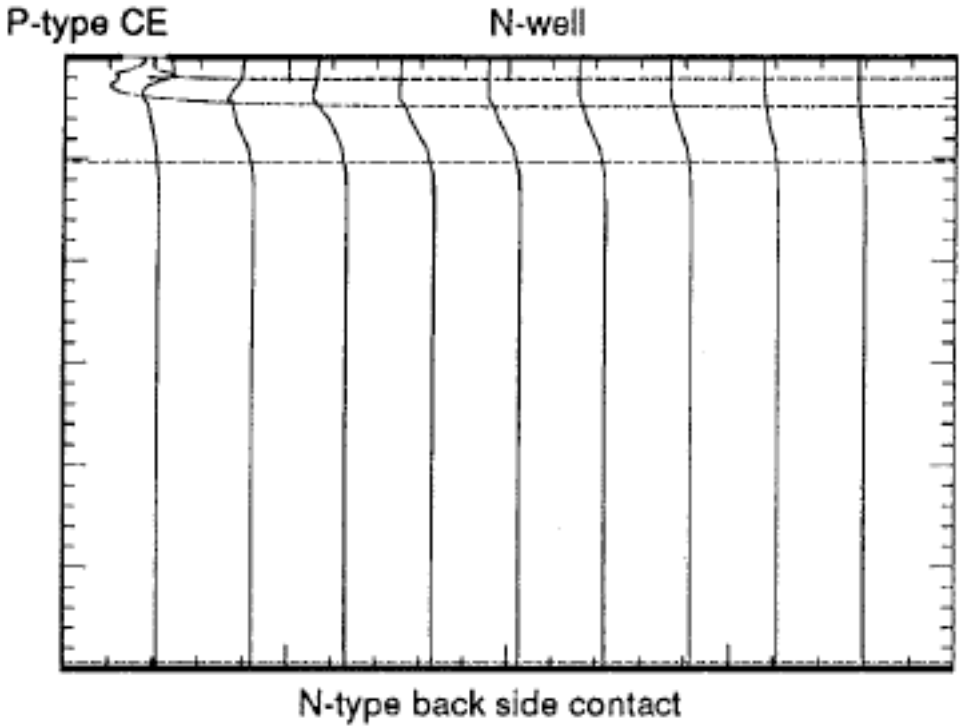


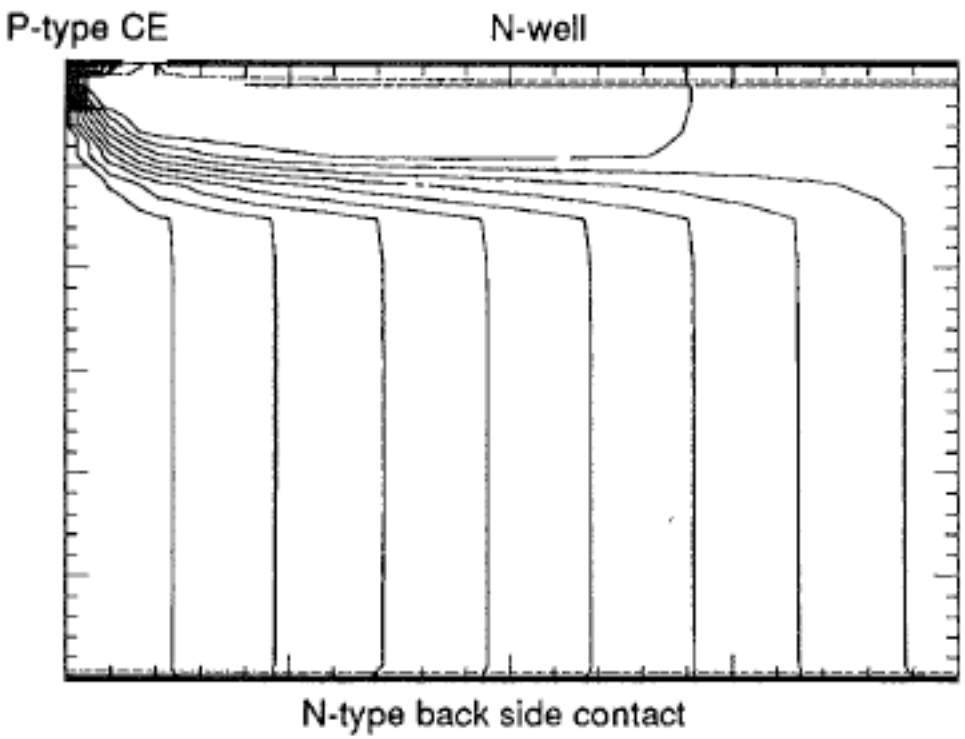
Vnwell at 20 V

Potential valley deeper into the substrate

Lower reverse bias, need extra well bias for depletion

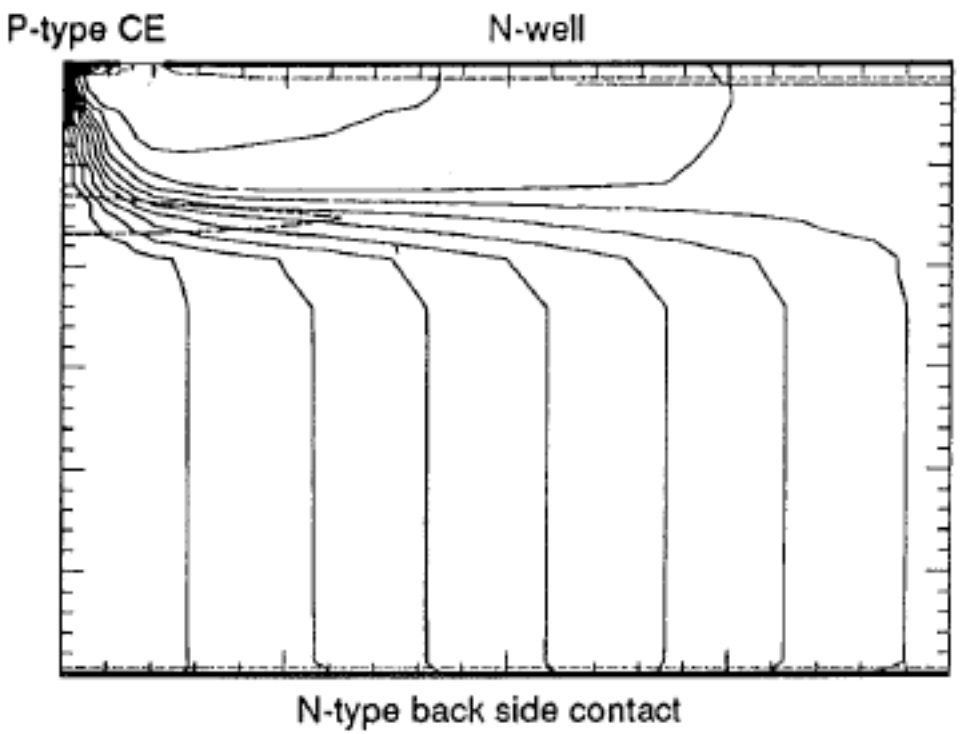
Back side at 55 V



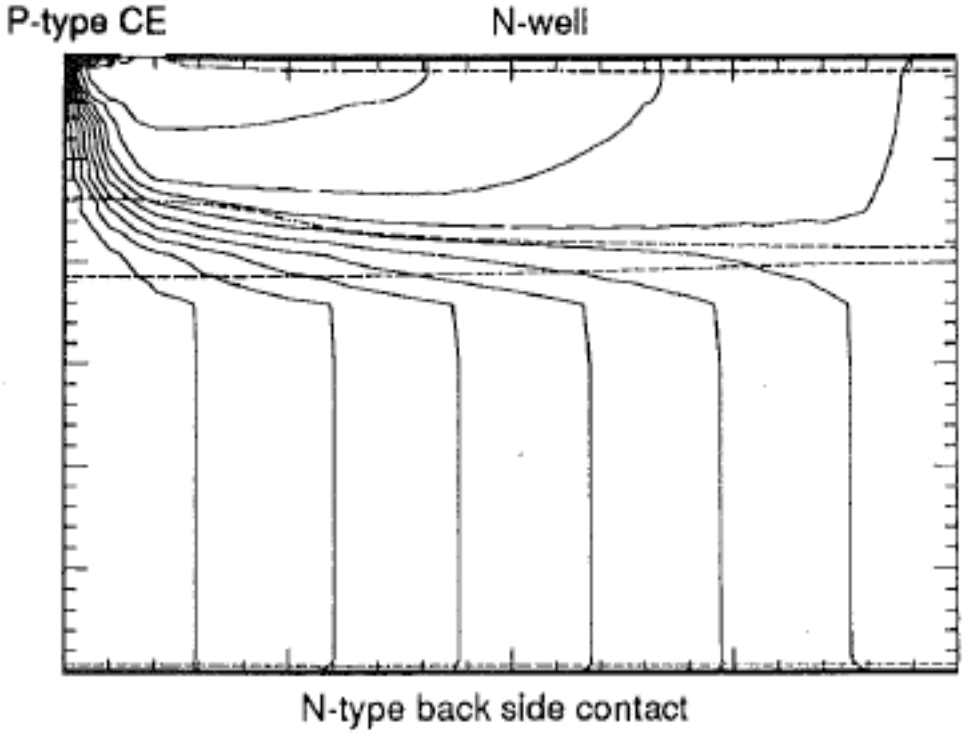


Vnwell at 4 V
to deplete

Less depletion at higher nwell biases (Vback still 55V) !

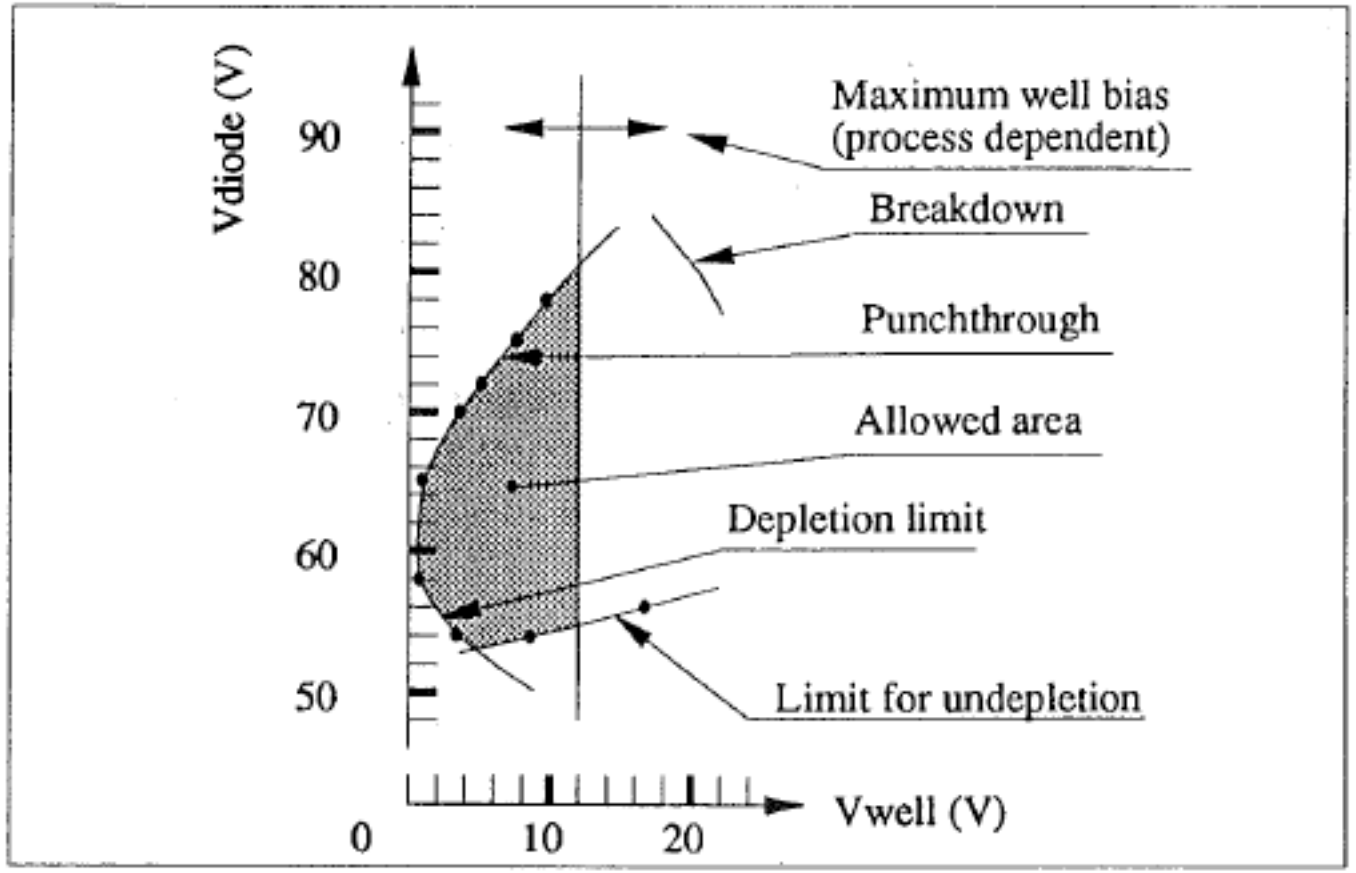


Vnwell at 20 V



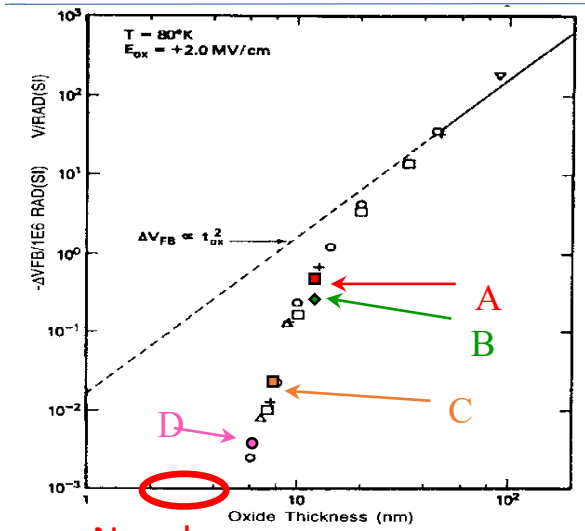
Vnwell at 30 V

Operating margins



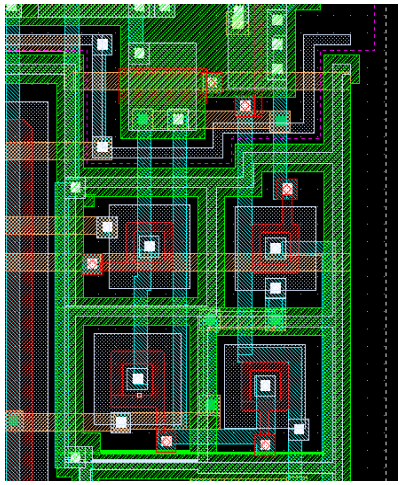
Similar now, but 3D TCAD and Monte Carlo simulations

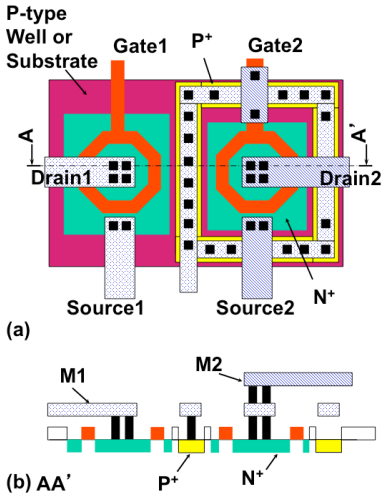
Circuit radiation tolerance: like standard CMOS



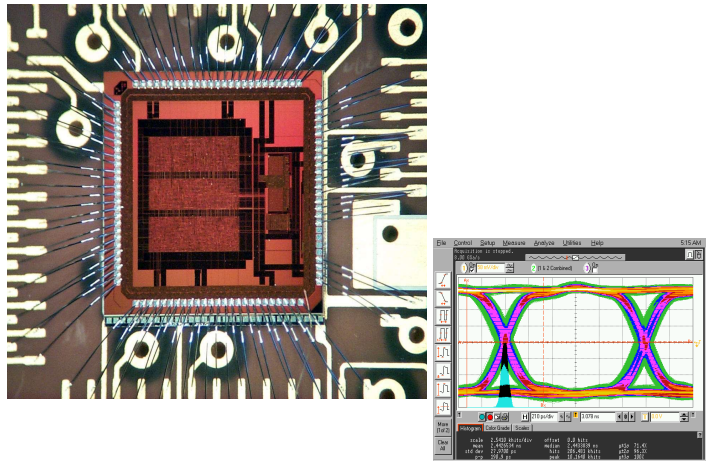
Now here

After N.S. Saks et al, IEEE TNS, Vol. NS-31 (1984) 1249





G. Anelli et al., IEEE TNS-46 (6) (1999) 1690



P. Moreira et al.
http://proj-gol.web.cern.ch/proj-gol/

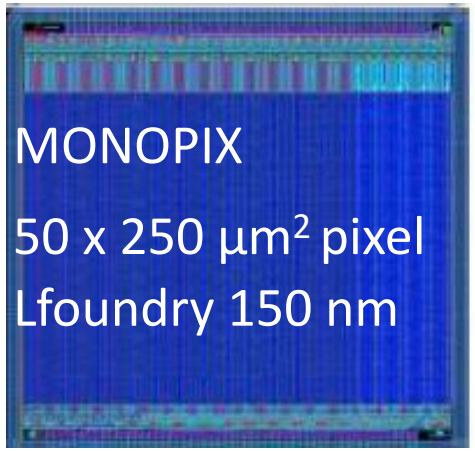
Total ionizing dose:

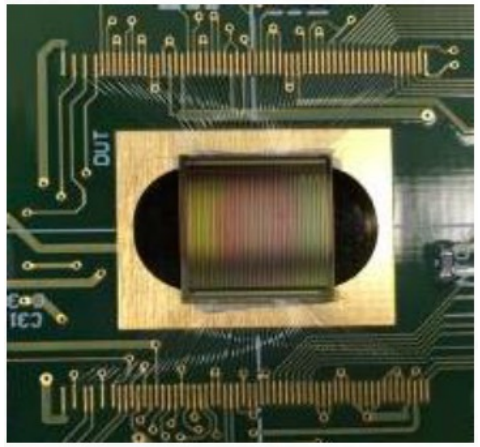
- Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
- In LHC enclosed NMOS transistors and guard rings in 0.25 µm CMOS to avoid large leakage current
- In deeper submicron enclosed geometry usually no longer necessary for leakage, but for small dimensions parasitic effects dominate e.g. from spacers, new gate dielectrics, **requires extensive measurement campaigns** F. Faccio et al. IEEE TNS-65 (1) 164, 2018,

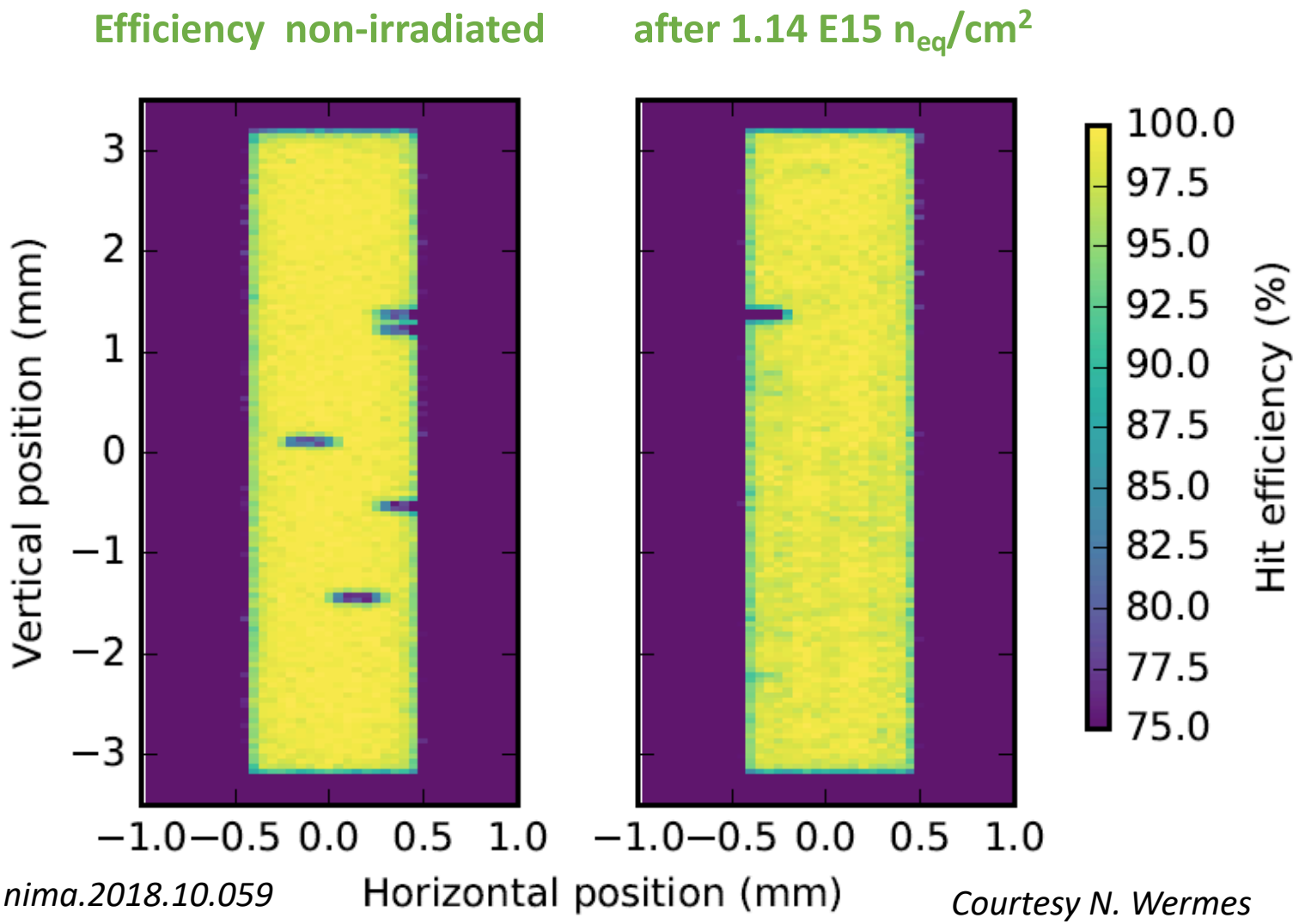
Single event effects:

- Single Event Upset : triple redundancy with majority voting (now special scripts S. Kulis)
- Latch-up not observed so far in LHC, but observed on MAPs at STAR, and in new technologies => **need attention in the design**

Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)







T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

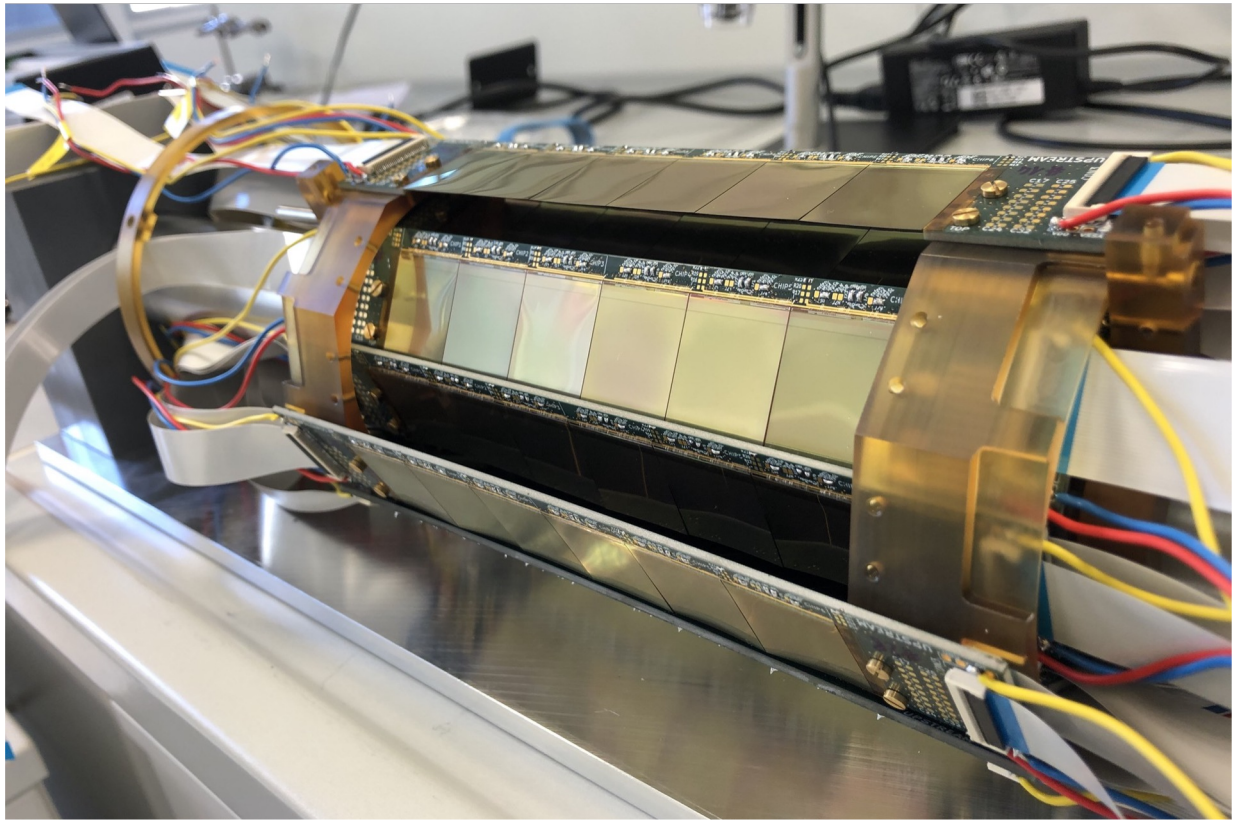
Courtesy N. Wermes

Other developments in same technology:

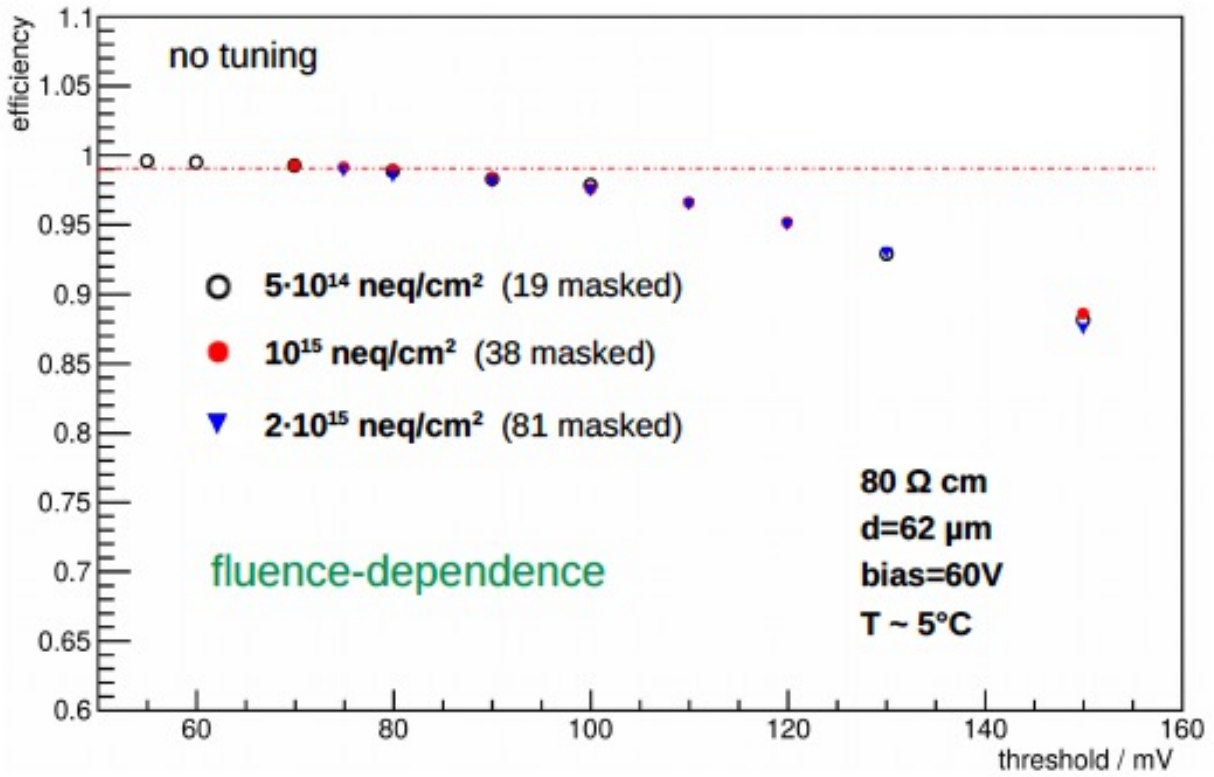
CACTUS Y. Degerli et al. doi:10.1088/1748-0221/15/06/P06011, VCI 2022, NIM A 1039 (2022) 167022

RD-50 E. Vilella et al. doi:10.22323/1.373.0019

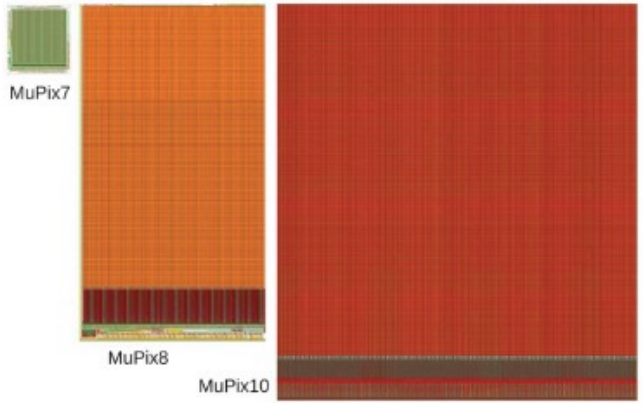
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)



MuPix vertex detector prototype



Courtesy I.Peric and A. Schoening

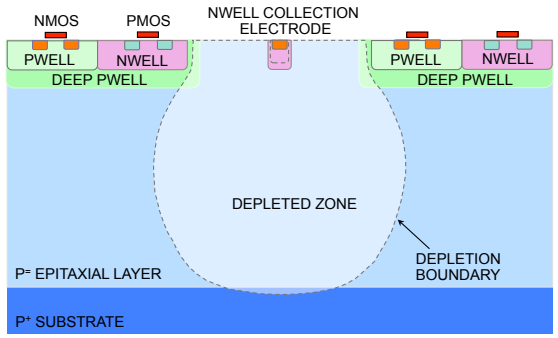


AMS/TSI 180nm, also used for ATLASPIX

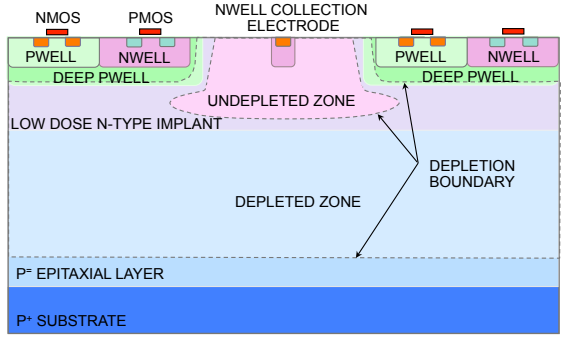
Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors

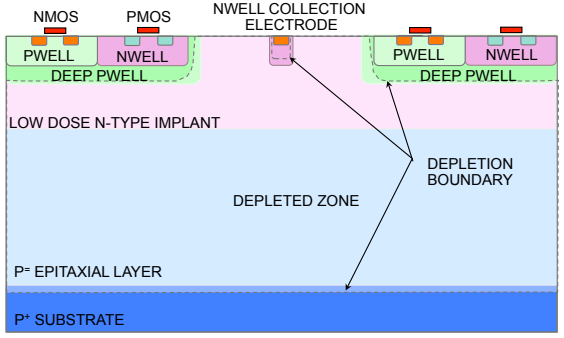
Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…



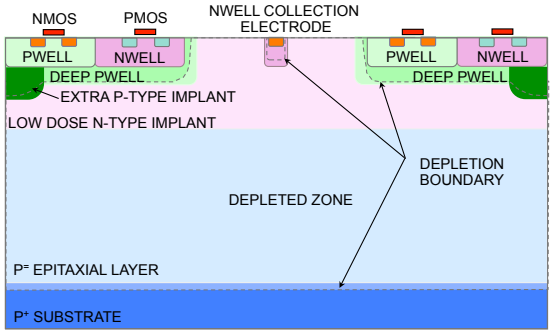
Standard, not fully depleted (ALPIDE)



Not fully depleted at low reverse bias



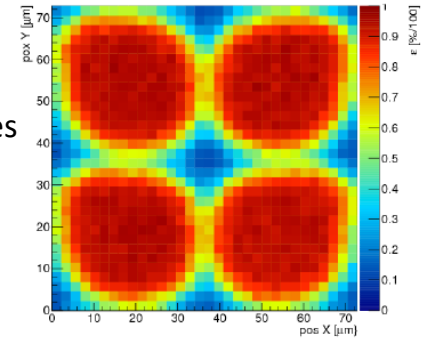
Depletion at higher reverse bias
(MALTA1, MONOPIX)



Further improvements by
influencing the lateral field

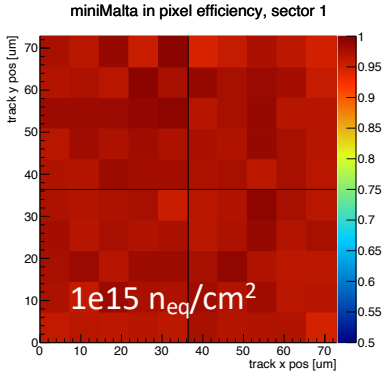
Additional implant for full depletion
=> order of magnitude improvement
Side development of ALICE for ALPIDE
NIMA 871 (2017) pp. 90-96
Triggered development in ATLAS
H. Pernegger et al, 2017 JINST 12 P06008

Efficiency drop at pixel edges
after irradiation
for 36.4 x 36.4 µm² pixel
needs improvement
E. Schioppa et al, VCI 2019



3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987



Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027…
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

Sensor optimization: Moving the junction away from the collection electrode

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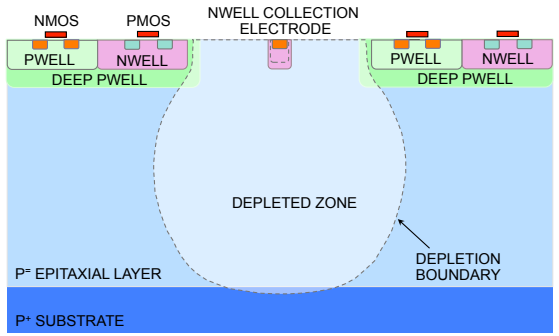
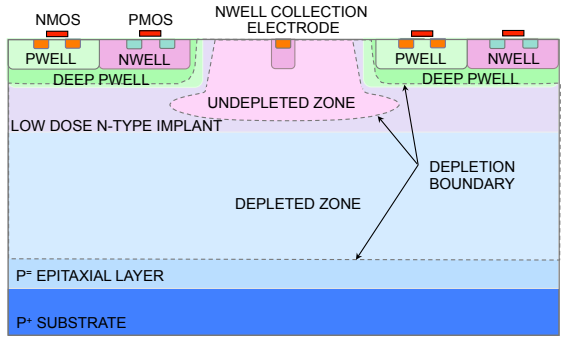
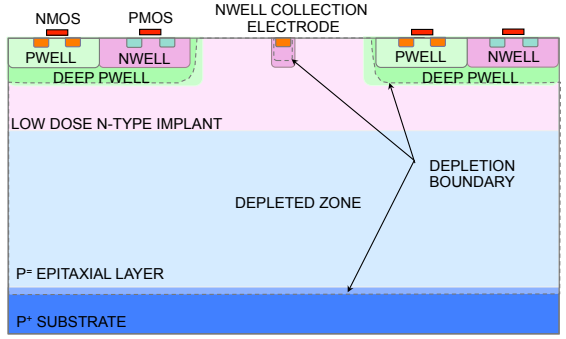


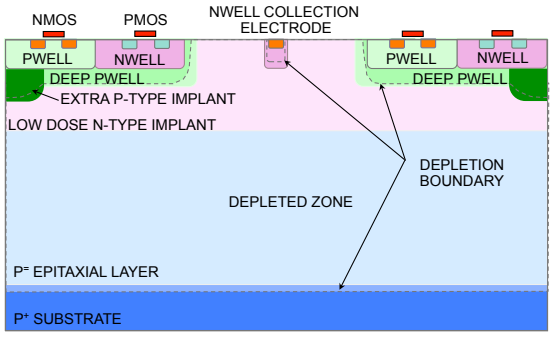
Standard, not fully depleted (ALPIDE)



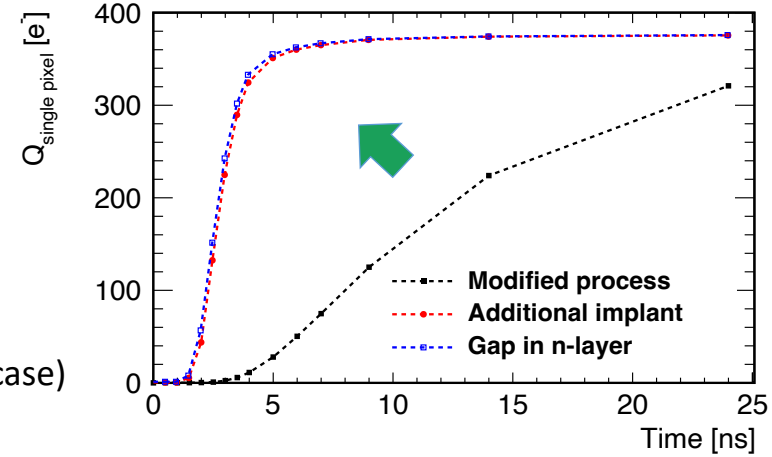
Not fully depleted at low reverse bias



Depletion at higher reverse bias
(MALTA1, MONOPIX)



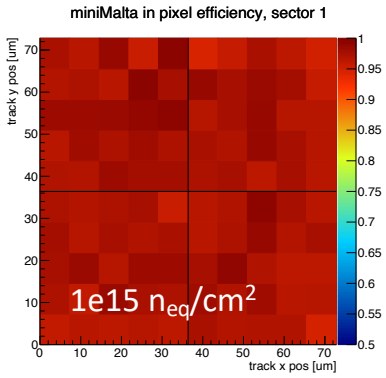
Further improvements by
influencing the lateral field



Hit in the pixel corner (= worst case)

3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987



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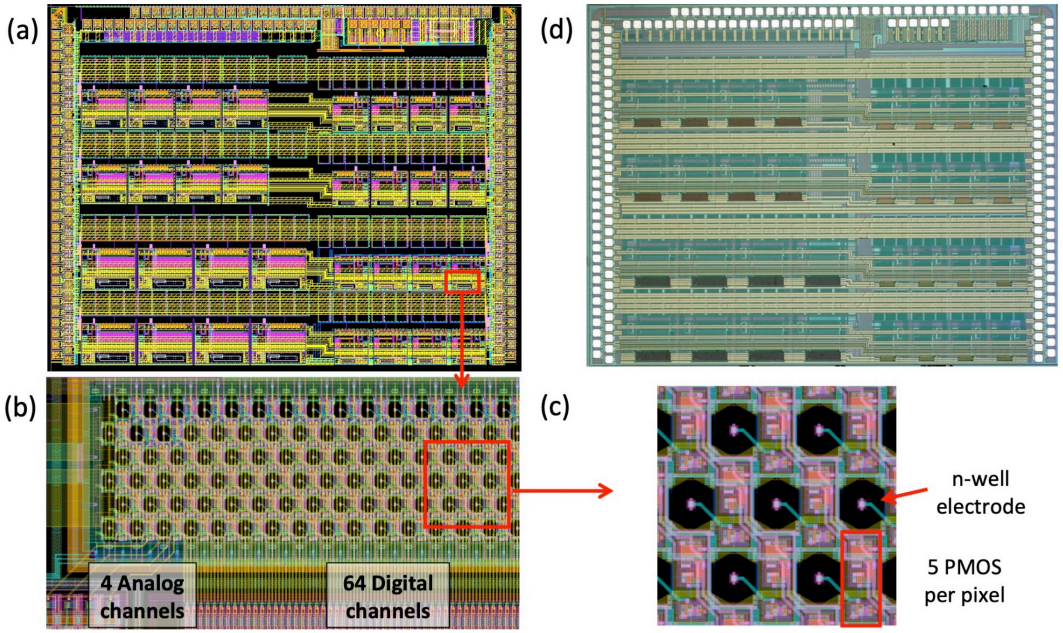
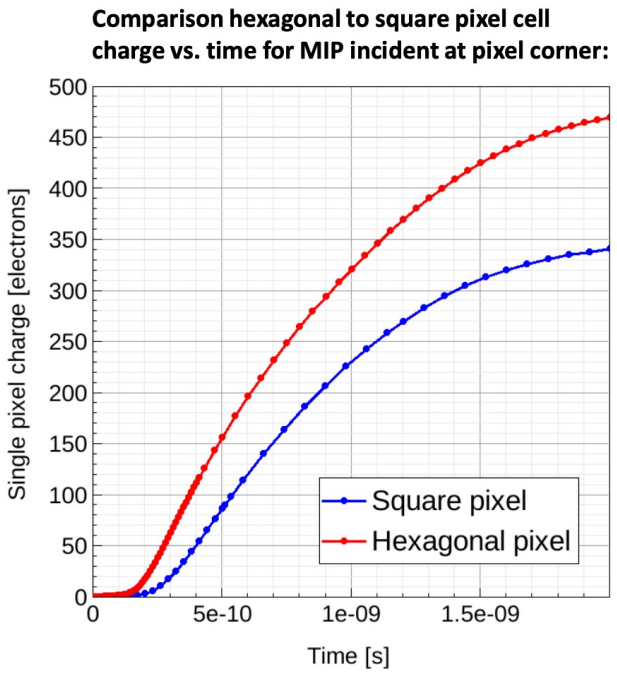
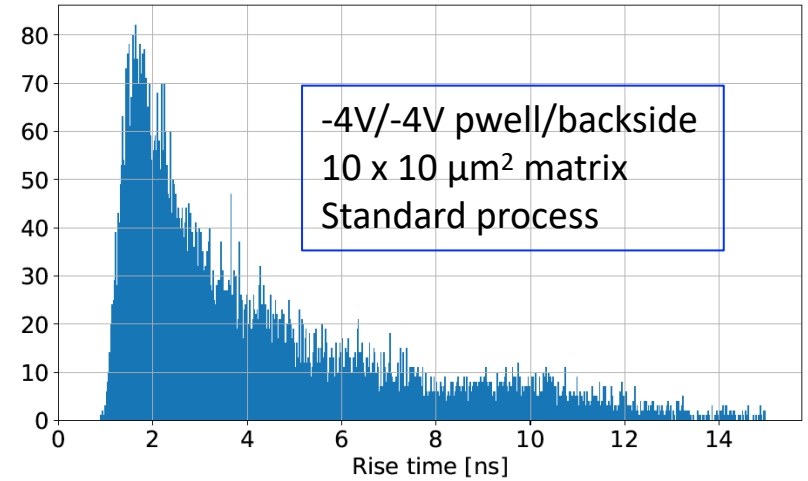
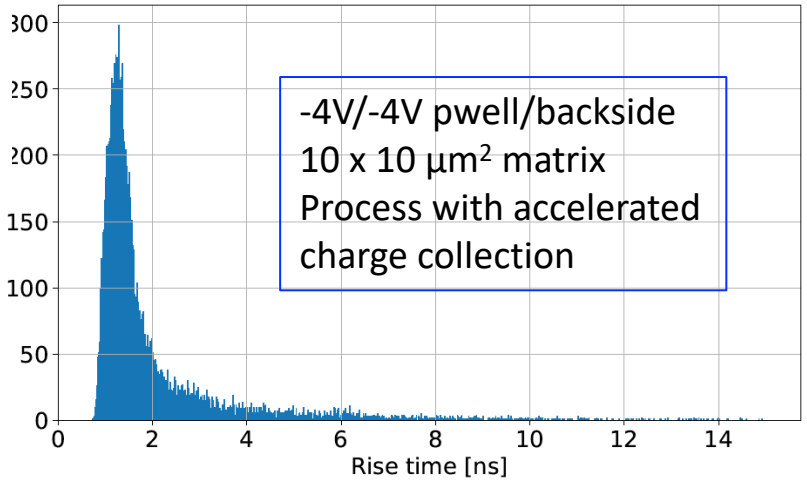
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

FASTPIX ATTRACT project: ^{90}Sr Risetime distributions









T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461 (ATTRACT: INFN, Ritsumeikan University and CERN)

E. Buschmann, D. Dannheim, K. Dort, M. Muenker

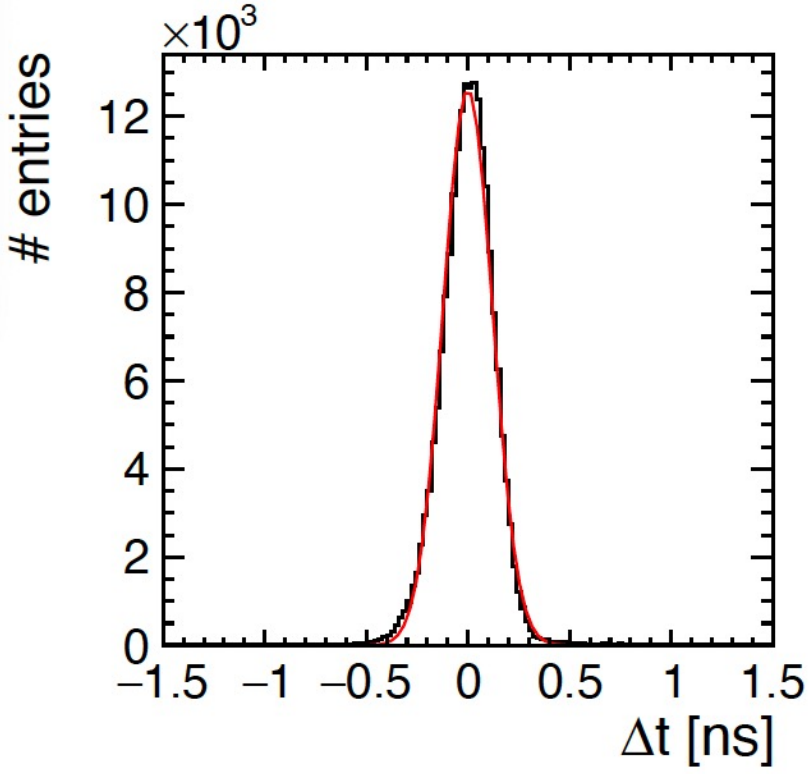
Direct relation between charge collection and process variant (TowerJazz 180nm)

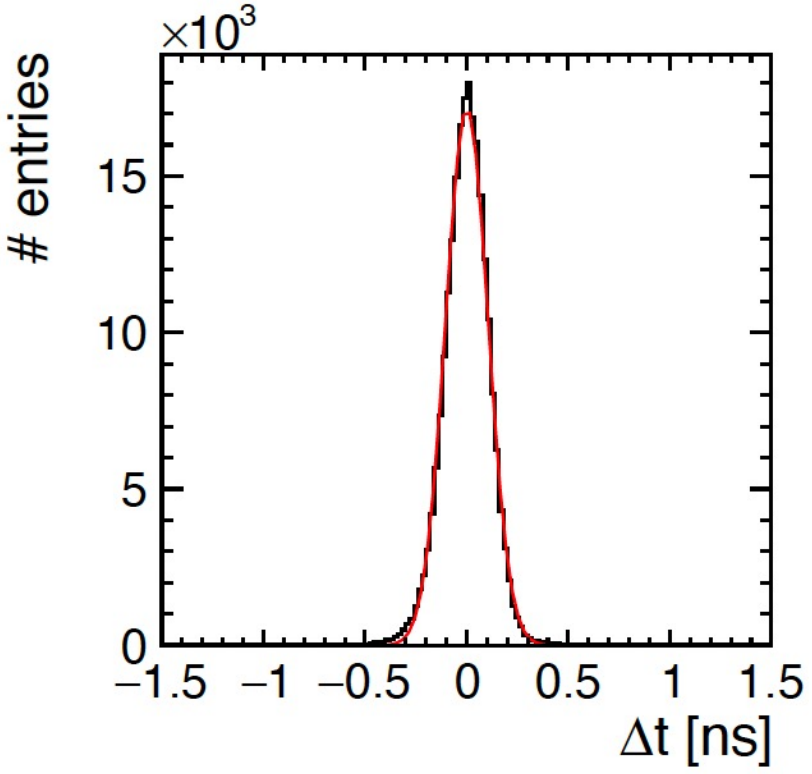
Significant impact even at very small pixel pitch

Hexagonal pixels

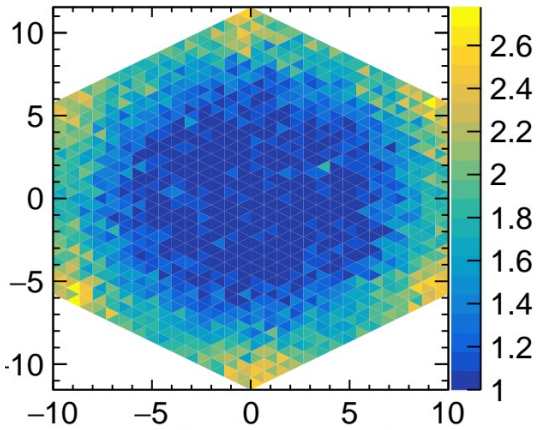
- better approximation of a circle
- charge sharing in the corners between 3 pixels instead of 4 -> more margin
- collection electrodes on hexagonal grid, circuit to remain on Manhattan layout

FASTPIX : time resolution (Cfr. Justus Braach et al)





Cluster size



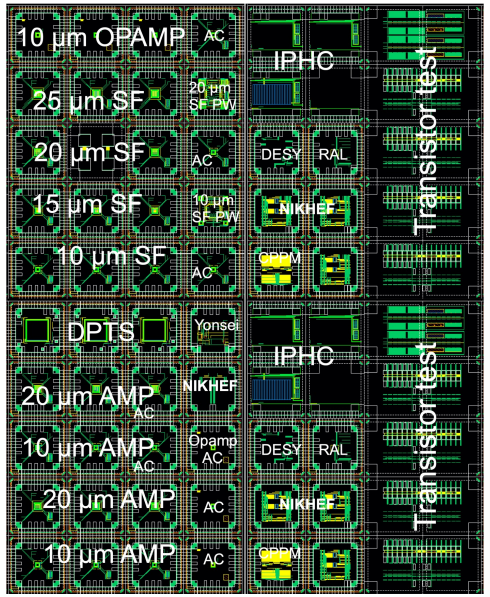
(a) Matrix 1, 10 µm pixel pitch at a threshold of 62 e. The distribution yields RMS = (140.7 ± 0.2) ps, $RMS_{99.7\,\%}$ = (128 ± 2) ps and $\sigma_{\text{fit, gaus}}$ = (121.5 ± 0.2) µm.

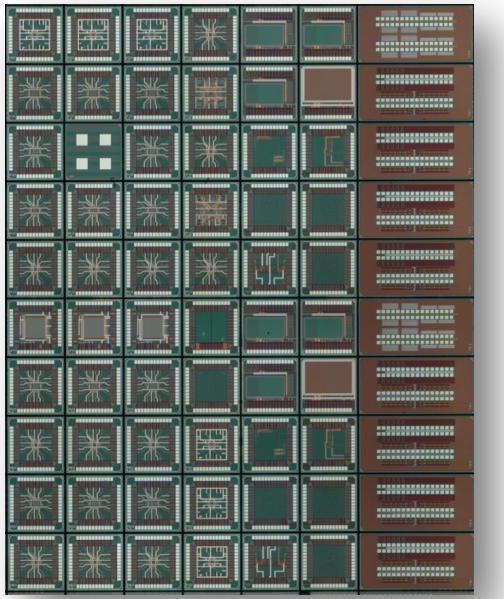
(b) Matrix 3, 20 µm pixel pitch at a threshold of 80 e. The distribution yields RMS = (138.2 ± 0.2) ps, $RMS_{99.7\,\%}$ = (109 ± 2) ps and $\sigma_{\text{fit, gaus}}$ = (104.4 ± 0.2) µm.

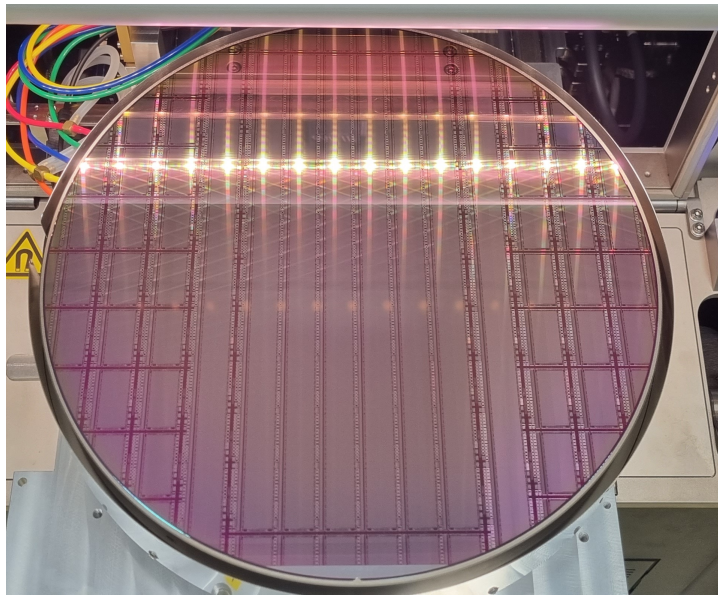
better time resolution at 20 micron pitch than at 10 micron !

Development of monolithic sensors for high energy physics in TPSCo 65nm ISC technology

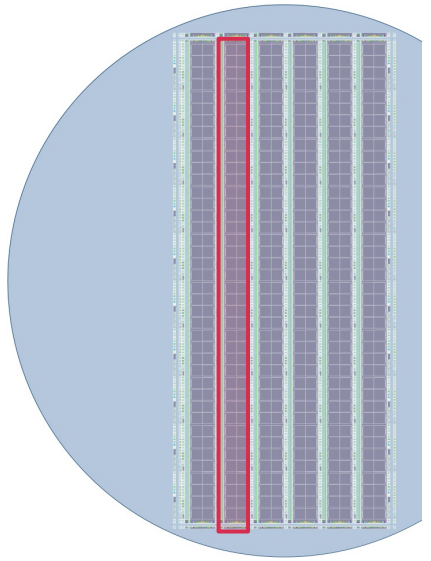
- CERN EP R&D (WP1.2 Monolithic Pixel Detectors) investigating sub 100 nm technologies for HEP
- Many contributors, strong synergy with ALICE ITS3 upgrade, very large measurement team (40-50 people)
- First technology selected TPSC 65 nm ISC, two submissions so far:







26cm long single silicon object



MLR1 (December 2020): 1.5 x 1.5 mm^2 test chips

Learn about the technology, characterize pixels, transistors and building blocks

ER1 (December 2022): 1.5 x 1.5 mm^2 test chips

Prove we can design wafer-scale stitched sensors

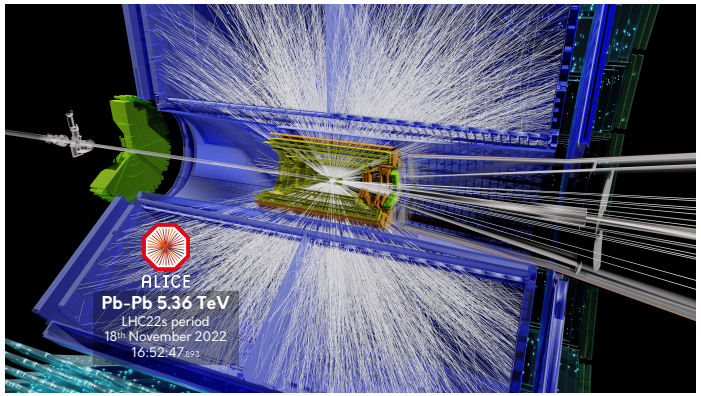
similar process modifications as in 180 nm, but more needed in 65 nm doi.org/10.22323/1.420.0001

Summary of WP1.2: Last EP R&D report: https://cds.cern.ch/record/2891650

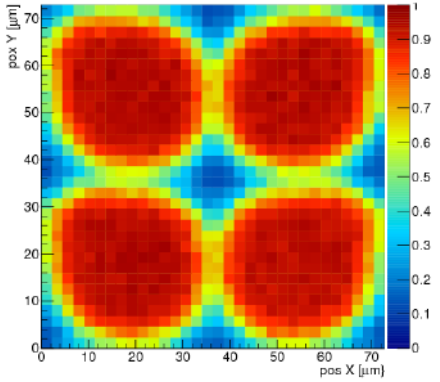
Pixel optimization for better margin: move junction away from the collection electrode for full depletion:
Better time resolution, radiation hardness and … efficiency, especially for thin sensors

EP R&D

in 180 nm



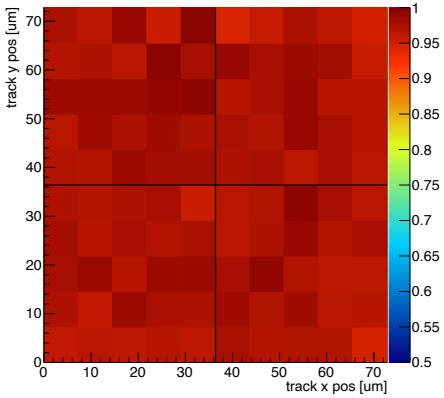
ALPIDE and ITS2 in ALICE (10 m^2)



E. Schioppa et al, VCI 2019

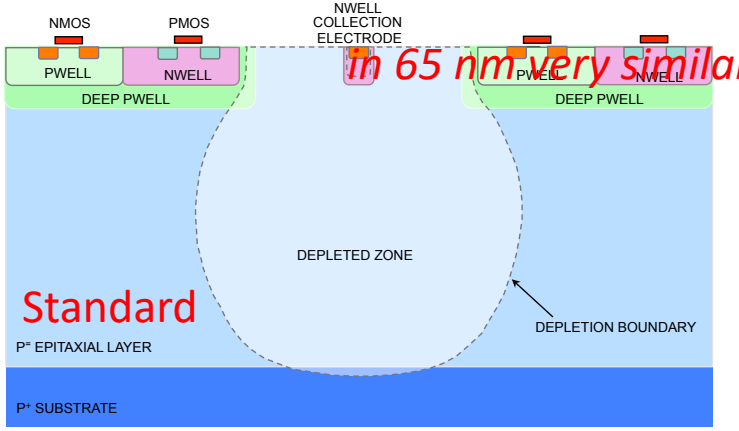
efficiency loss at
~ 10^{15} n_{eq}/cm^2

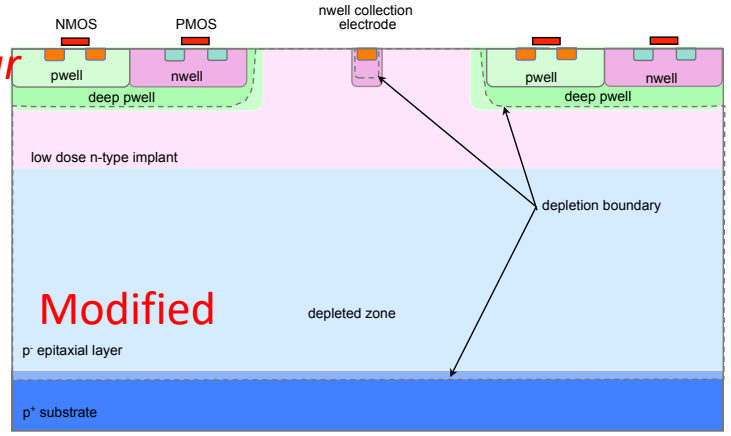
ALICE CLIC ATLAS EXPERIMENT STREAM



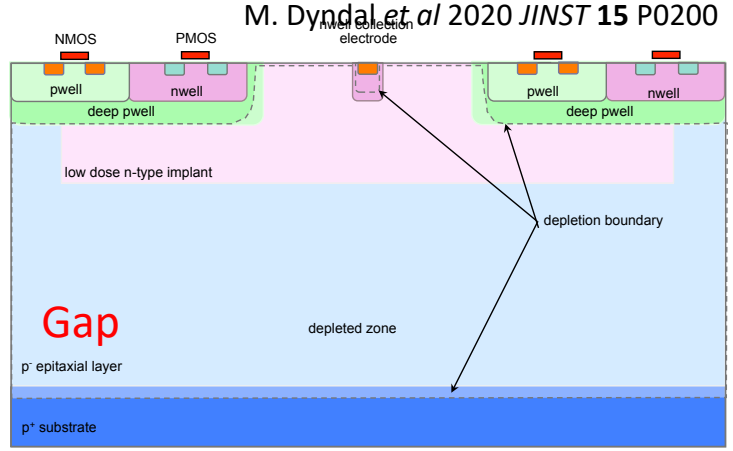
H. Pernegger et al., Hiroshima 2019,
M. Dyndal *et al* 2020 *JINST* **15** P0200

in 65 nm very similar





M. Munker et al.
https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

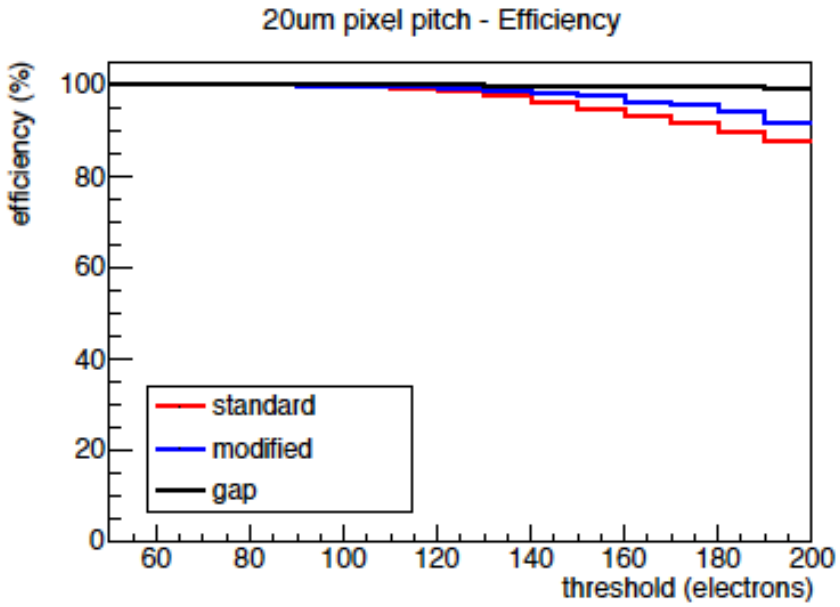
Charge sharing

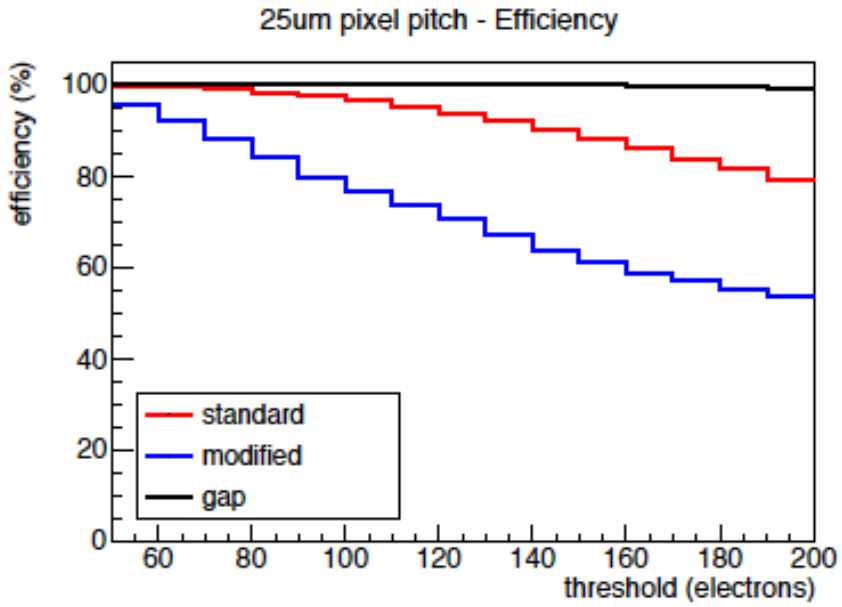
DOI: https://doi.org/10.22323/1.420.0001 (65nm)

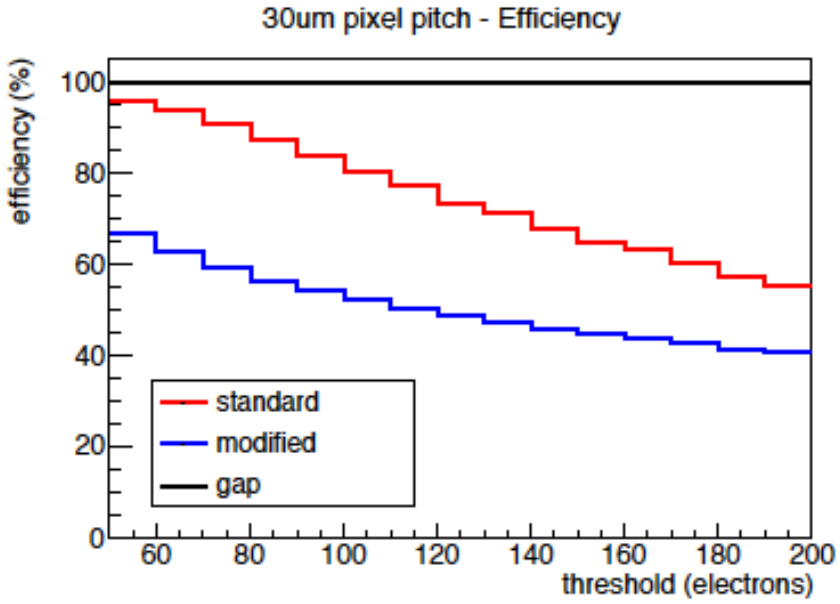
65 nm very similar, profited significantly from 10 years experience in 180 nm

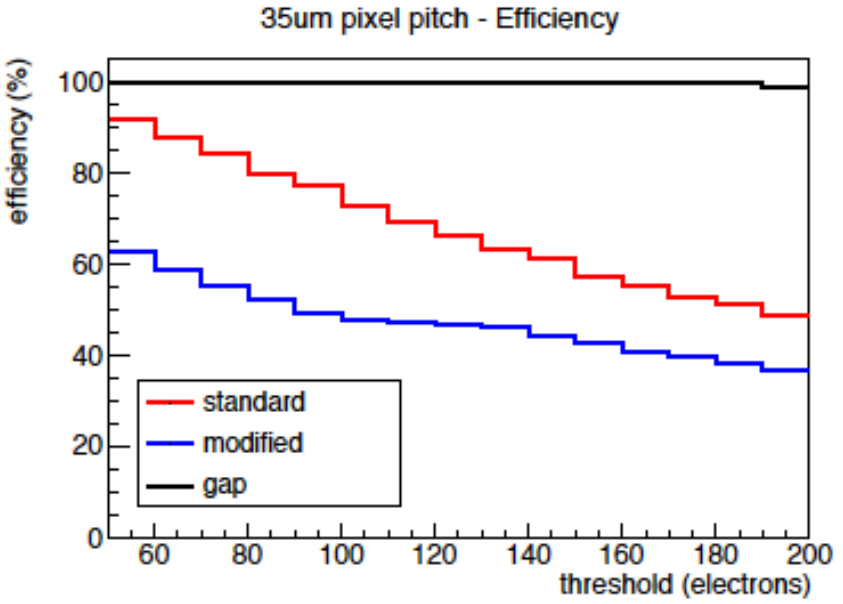
EP R&D WP1.2 with a very significant contribution from ALICE ITS3 team (large measurement team 40-50 people)

65nm: different pixel flavors at larger pixel pitches









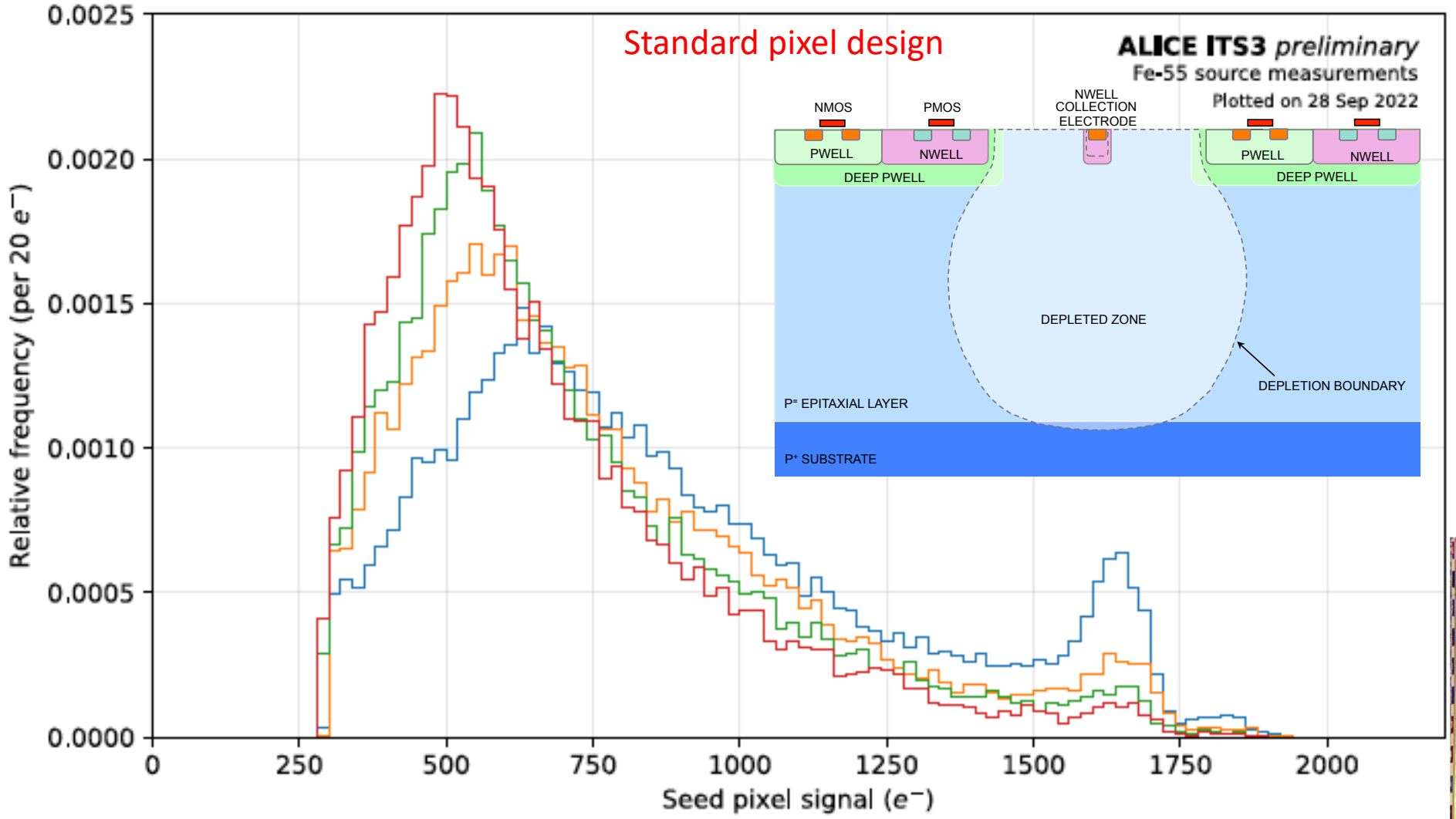
Simulations by J. Hasenbichler for MIPS

Charge sharing reduces the signal in a single pixel and reduces efficiency especially for larger thresholds.

Only the gap concentrates charge sufficiently to remain efficient for large pixel pitches

Pitch dependence for different variants ^{55}Fe

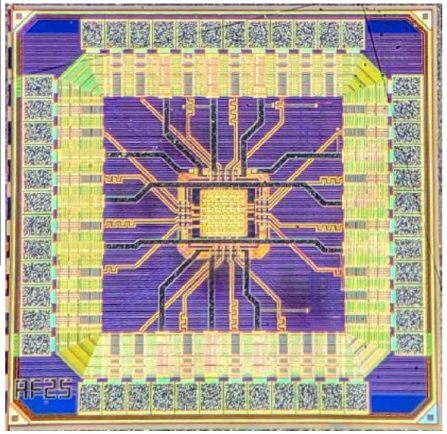
See also: I. Sanna IEEE NSS 2022



APTS SF
type: standard
split: 4
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

APTS SF

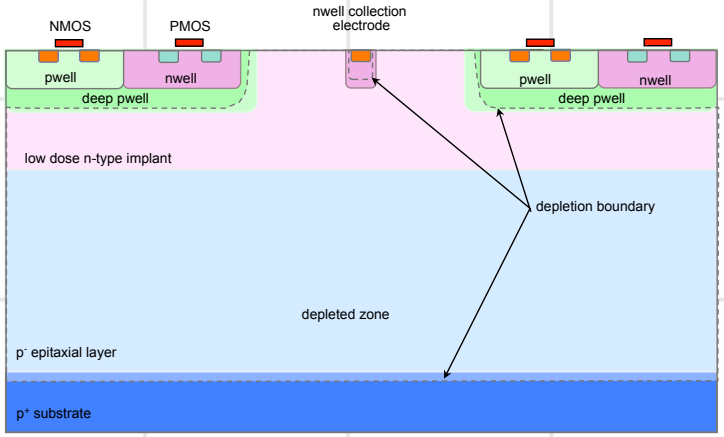


Pitch dependence for different variants ^{55}Fe

See also: I. Sanna IEEE NSS 2022

ALICE ITS3 *preliminary*
Fe-55 source measurements
Plotted on 28 Sep 2022

Modified pixel design



Relative frequency (per 20 e^-)

0.0025
0.0020
0.0015
0.0010
0.0005
0.0000

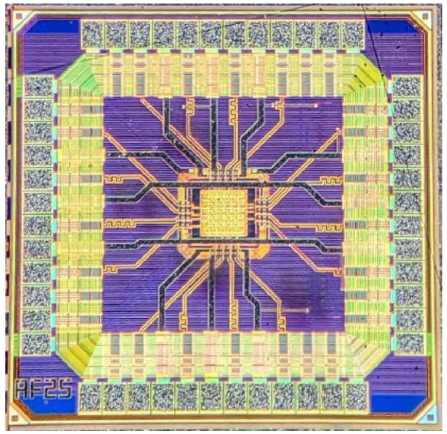
0 250 500 750 1000 1250 1500 1750 2000

Seed pixel signal (e^-)

APTS SF
type: modified
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$

pitch = 10 µm
pitch = 15 µm
pitch = 25 µm

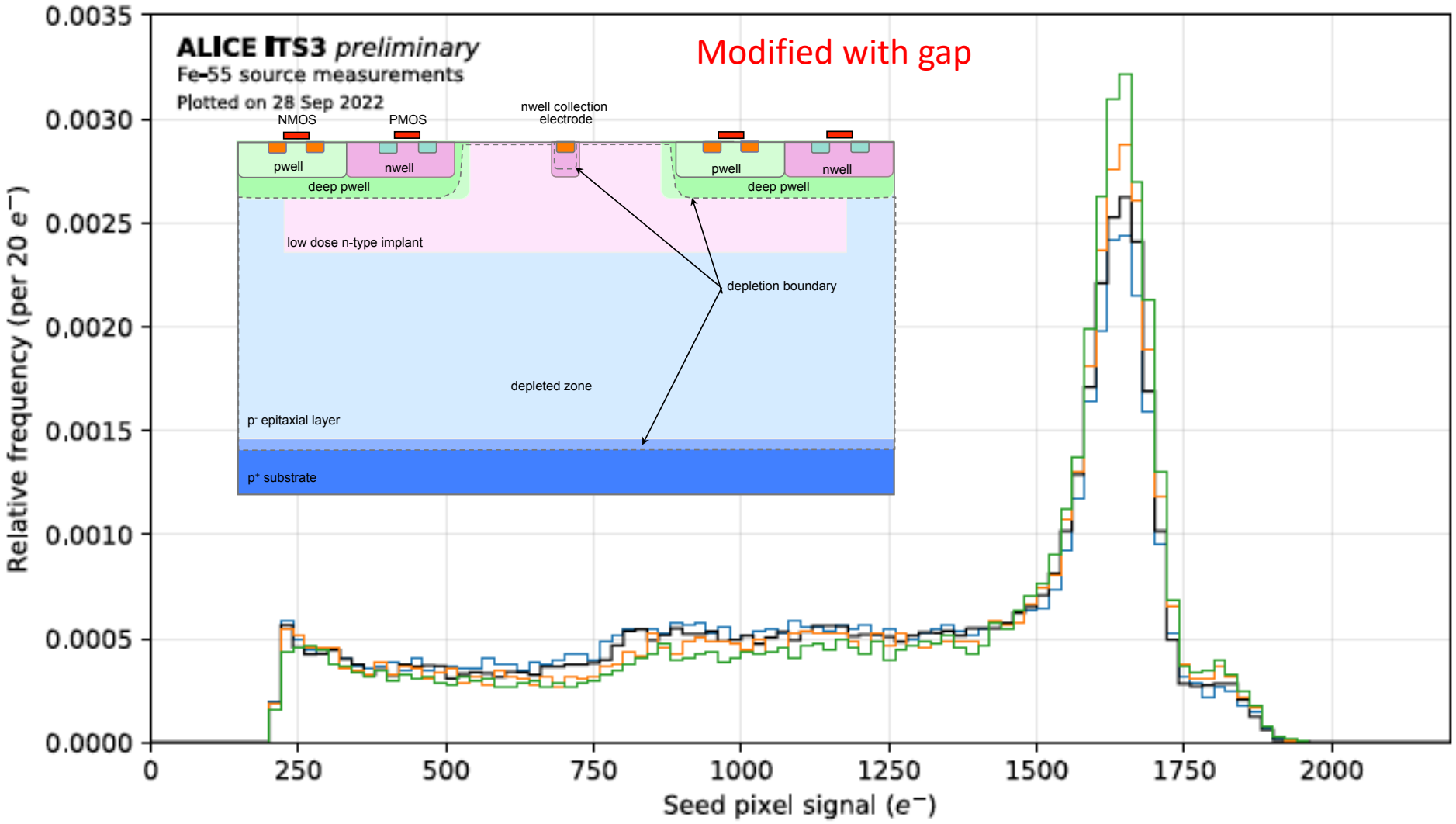
APTS SF



Pitch dependence for different variants ^{55}Fe

See also: I. Sanna IEEE NSS 2022

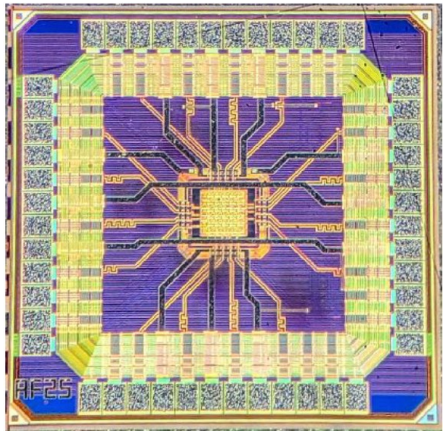
Remarkable result !



APTS SF
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

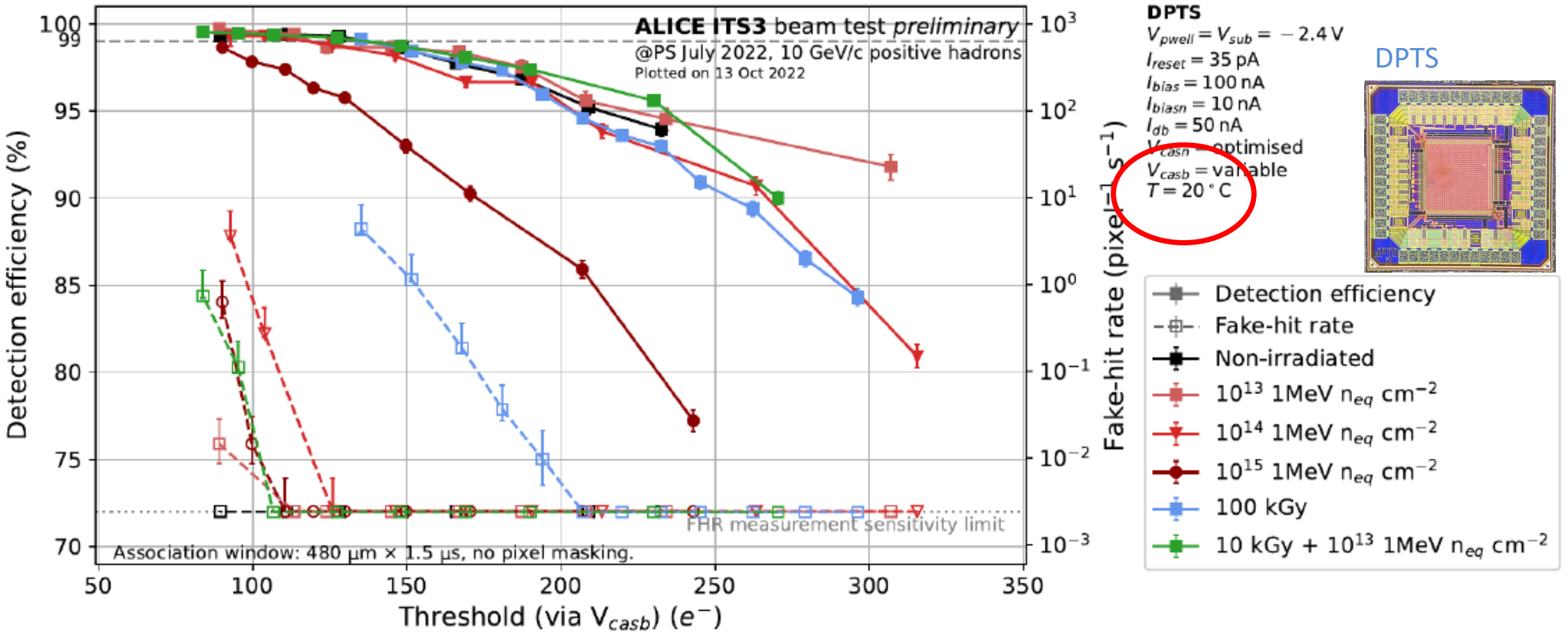
APTS SF



Sensor with gap is only variant conserving efficiency at larger pixel pitches

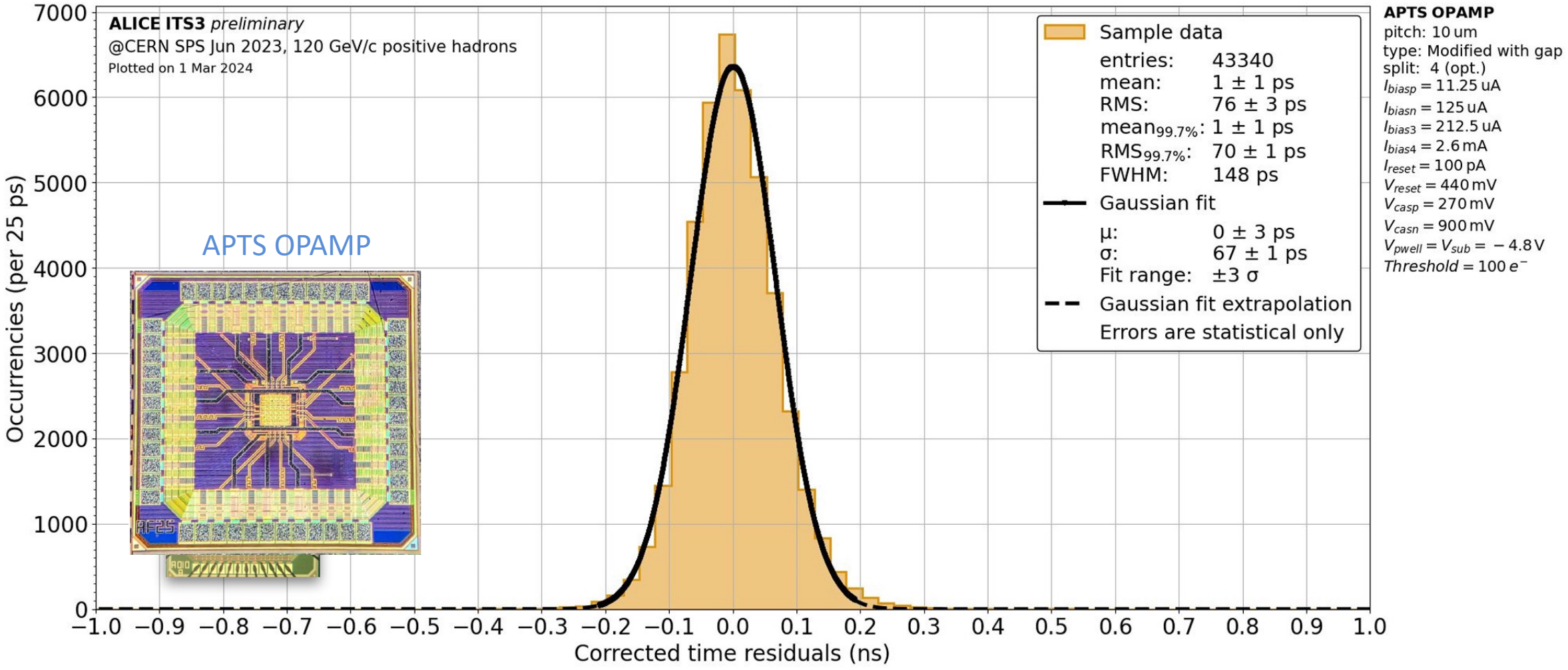
~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature

doi: 10.1016/j.nima.2023.168589



- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 µm^2 pixel (DPTS) including sensor optimization
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- KEY ACHIEVEMENT: 65nm ISC qualified for HEP, many features not yet explored (wafer stacking, special imaging devices…)

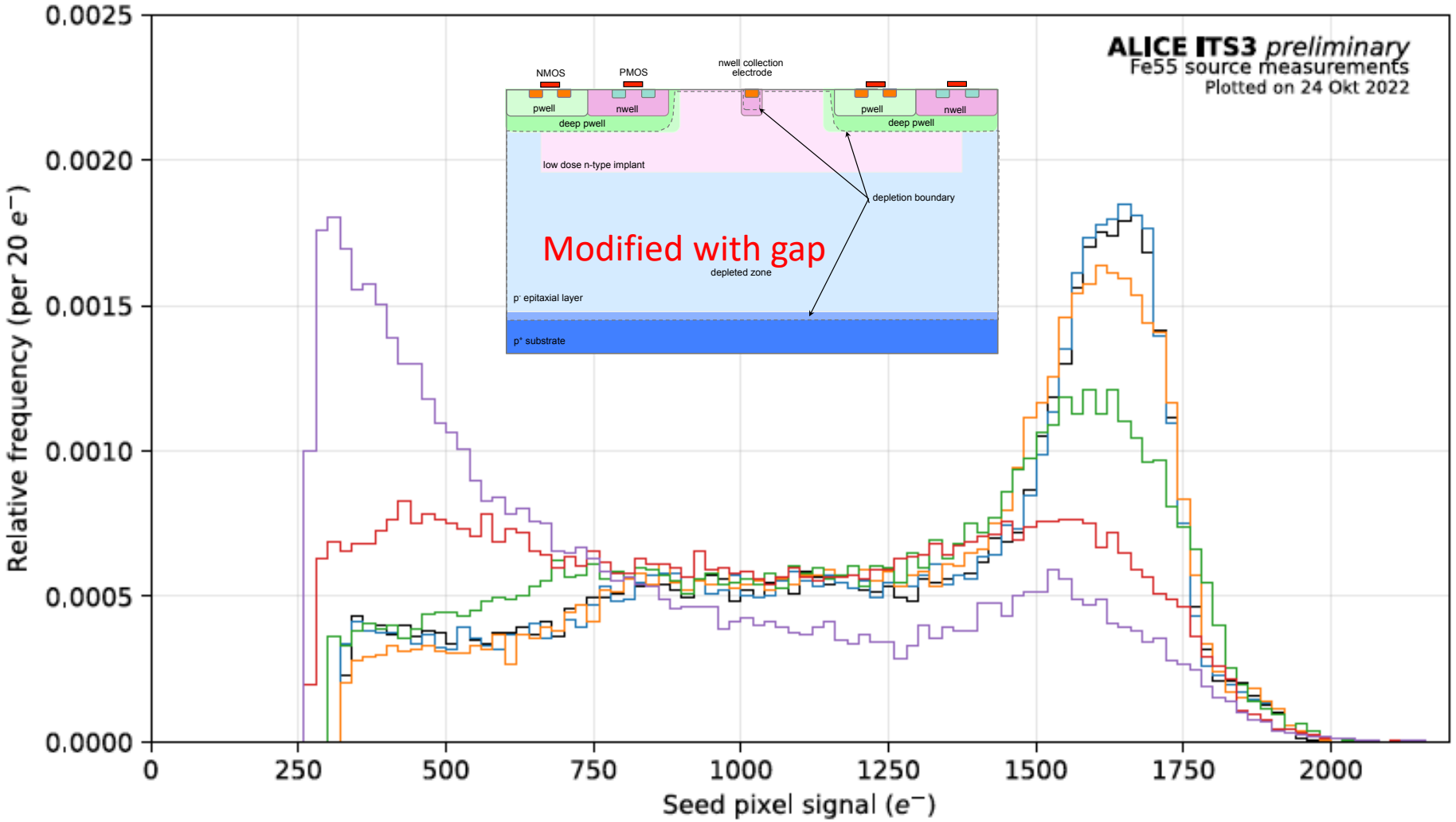
Sensor timing



Bong-Hwi, U. Savino et al. ULITIMA 2023, L. Aglietta, 16th Pisa conference on advanced detectors.

(180nm FASTPIX ~100 ps with time walk and cluster size correction, J. Braach et al. doi:10.48550/arXiv.2306.05938)

Irradiation results: exploring paths to higher fluences (I. Sanna et al.)

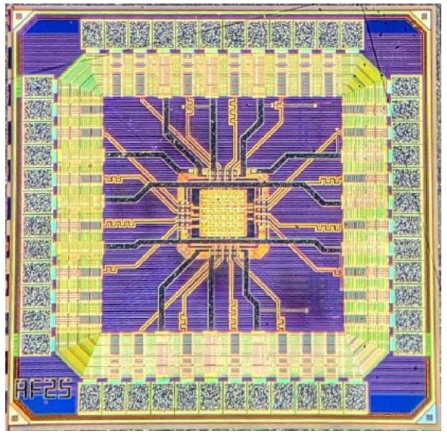


APTS SF
pitch: 15 µm
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 250\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0{,}5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$
temperature = 14 °C

Not irradiated
1e13
1e14
1e15
2e15
1e16

DPTS still efficient at RT

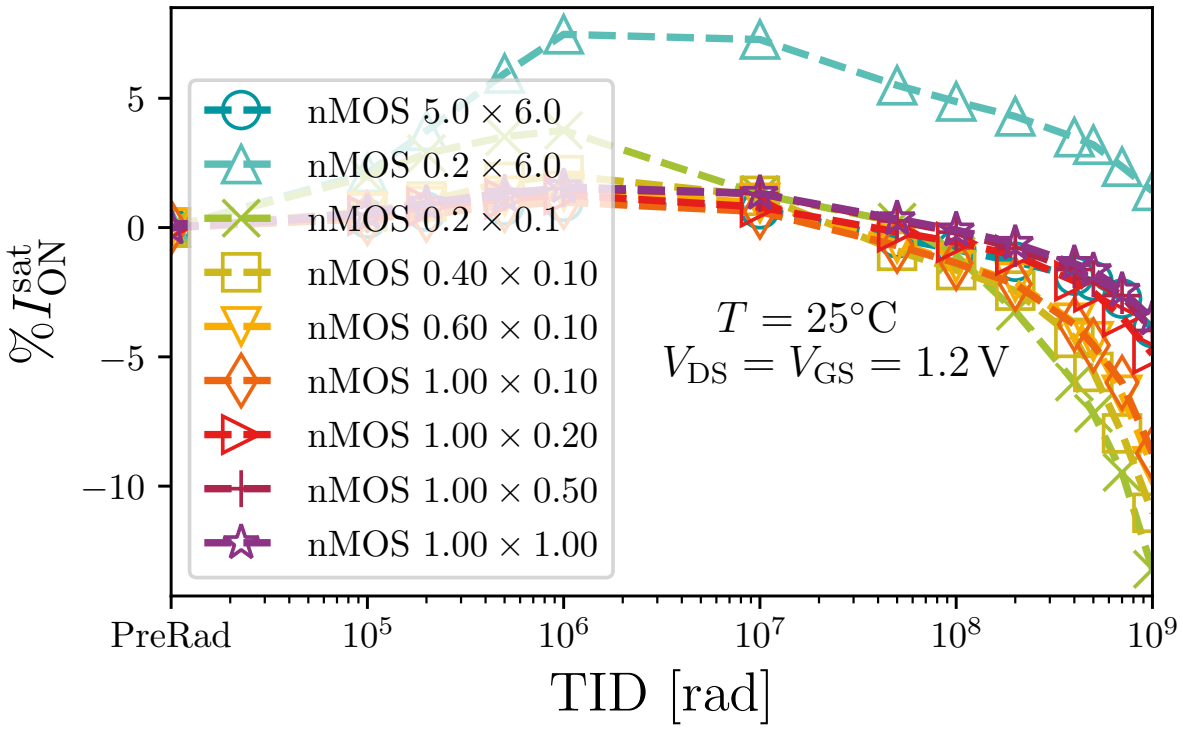
APTS SF

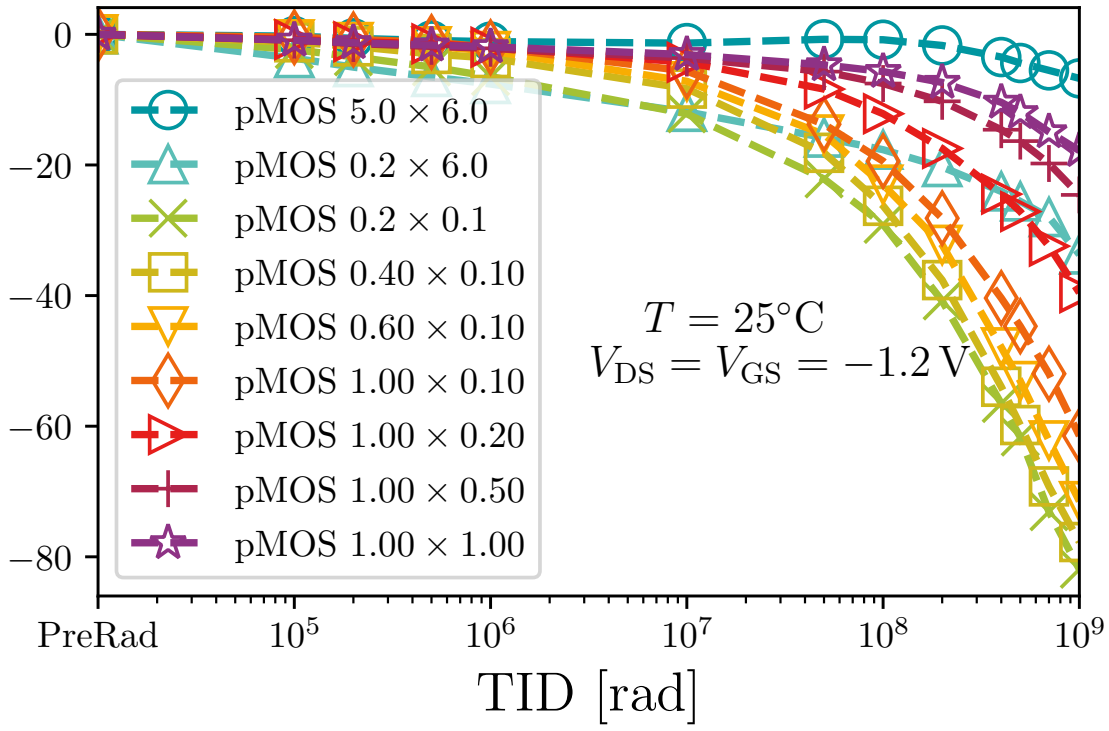


10^{16} n_{eq}/cm^2 will need cooling (needed for 10^{15} for 180 nm)

(C. Lemoine *et al* 2024 *JINST* **19** C02033)

Transistor radiation tolerance

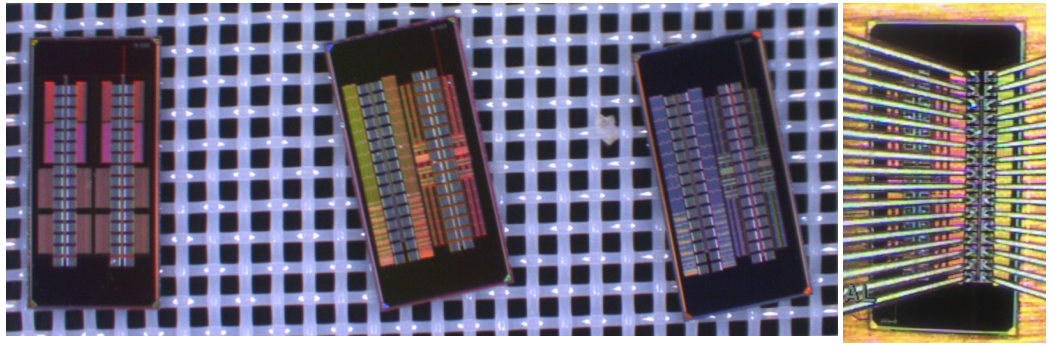




In line with other 65 nm technologies, no showstoppers.

Small size PMOS transistors degrade significantly after several hundred Mrad.

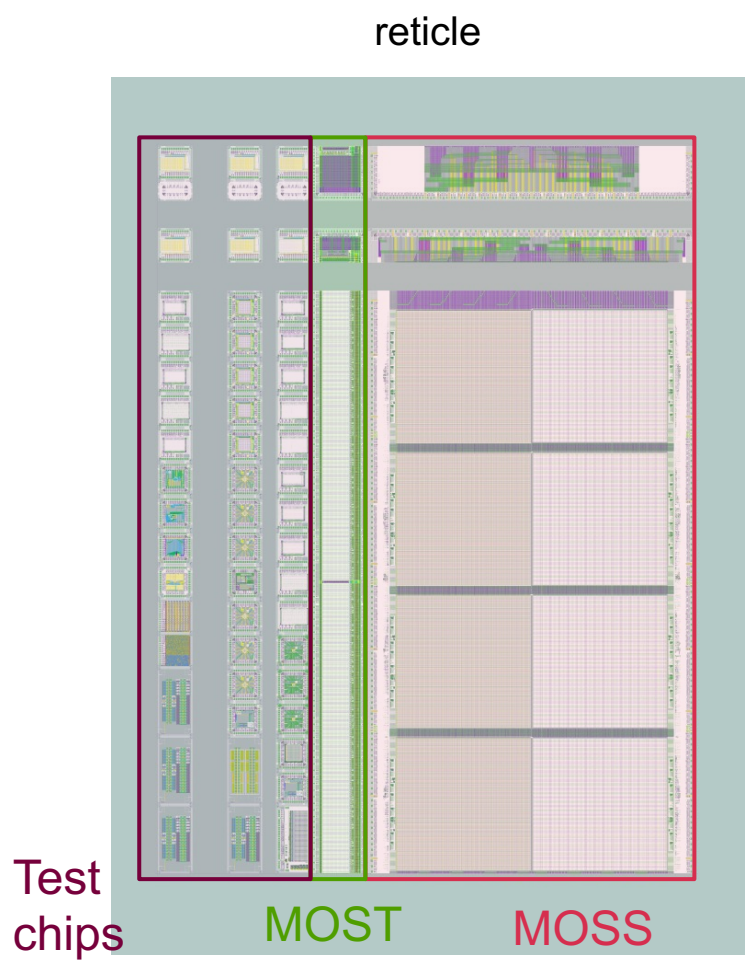
Caveat: modeling of transistors with significant reverse bias

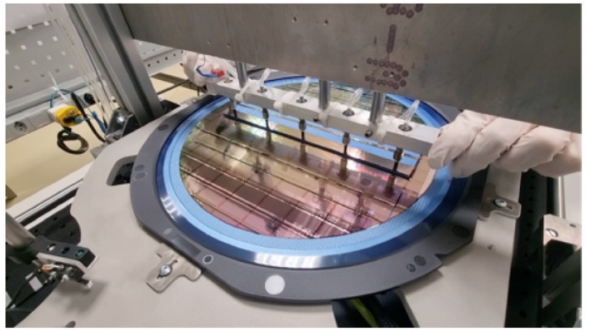


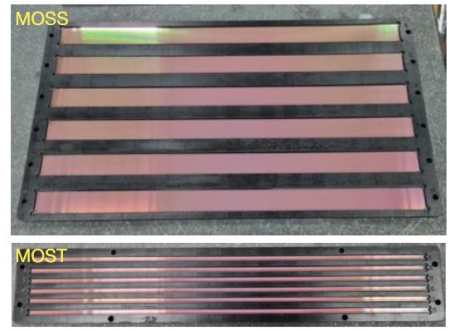
A. Dorda Martin et al. “Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias”. doi: 10.1088/1748-0221/18/02/C02036

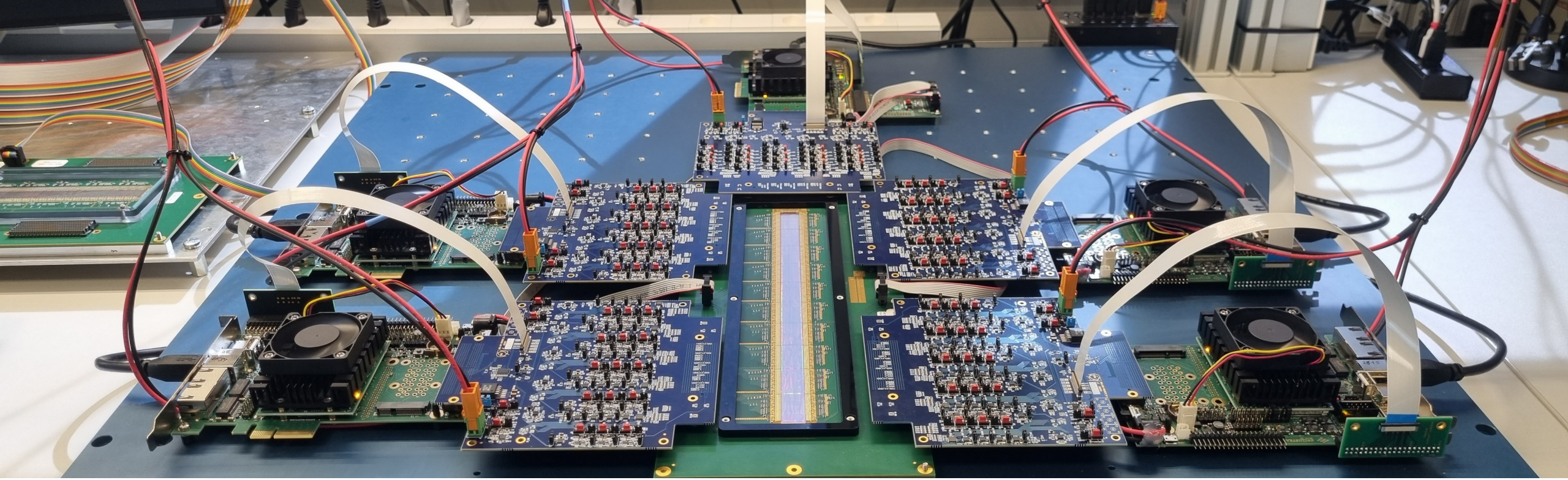
ER1 submission

- Two stitched sensor chips, 6 of each per wafer, digital on top design
  - MOSS chip (1.4 x 26 cm)
    - Conservative layout (DFM rules), Alpide-like readout scheme and 1/20 power segmentation
  - MOST chip (0.25 x 26 cm)
    - High local density with high granularity of power gating to mitigate faults, async hit driven readout
- 51 chiplets for prototyping blocks and pixel chips
  - PLL, pixel prototypes, fast serial links, SEU test chips, …
  - IPHC, NIKHEF, STFC, DESY, SLAC, INFN, CERN…
- Learn stitching methodology, wafer assembly and automated signoff (P.. Leitao et al.)
- Learn about yield, design for manufacturing (DFM) and defects masking
- Study power schemes, leakage, spread, noise and speed
  - Practical application: Alice ITS3 upgrade (see R. Ricci's presentation)
- Technology and support development
  - New metal stack: new I/Os, PDK, DDK, DRC rules
  - Custom DRC and LVS rule check, custom DFM standard library
  - Legal framework, nda …





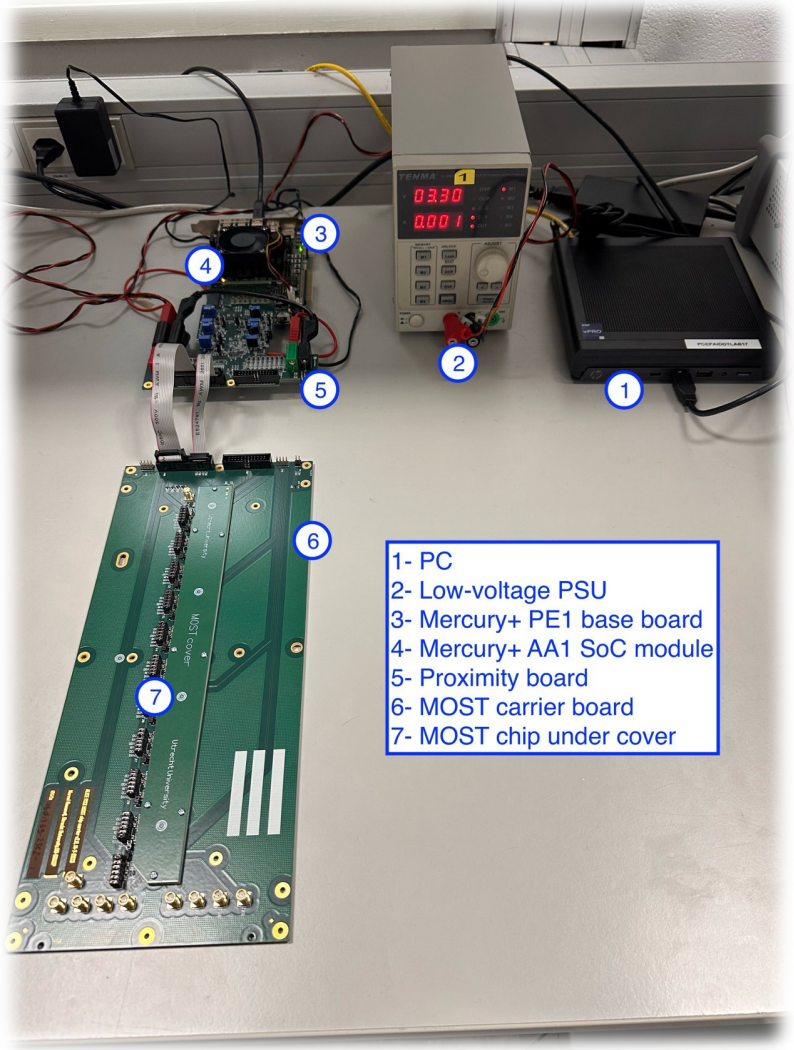


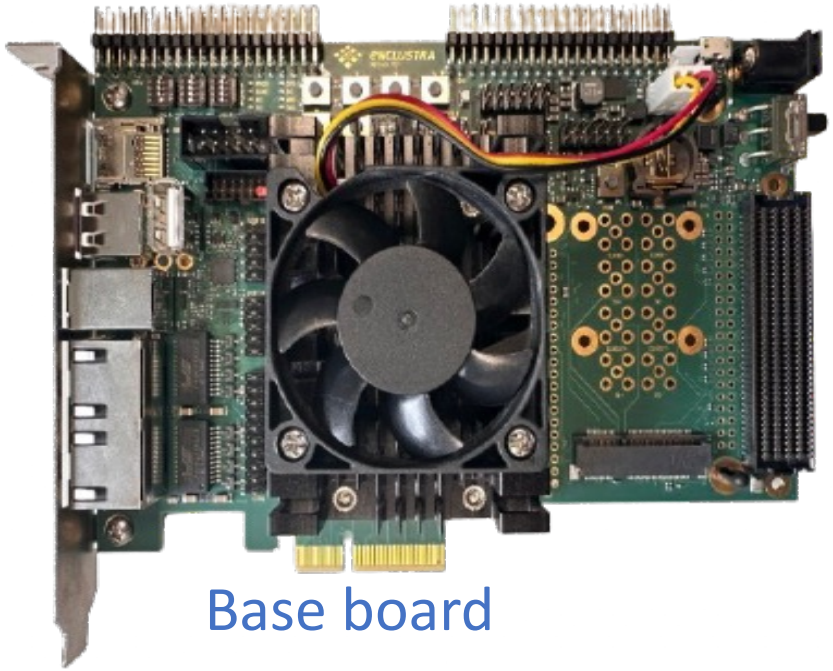


MOSS Functional Tests

- MOSS design fully functional
  - Design concepts and methodology validated
  - Block level yield and local defect rate under study
    - Faults probability seems negligible with respect to power shorts
  - No evidence of yield difference between the two layout densities
- Learnings and improvements to be employed in the ER2 engineering prototype (MOSAIX)

MOST test setup development





Base board

- Mercury+ PE1 base board
- Mercury+ AA1 SoC Module
- USB connection to PC
- FMC connection to Proximity board
- Needs FX3 + MOST firmwares

Proximity board

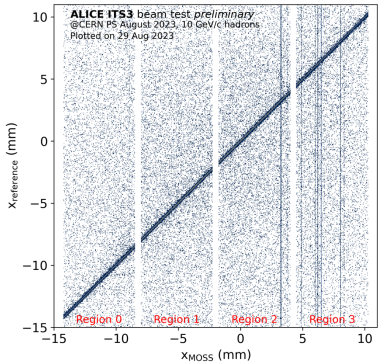
- 1 x DAC63004 for VDD supplies
- 2 x AD5668 for bias supplies
- 1 x AD7091R for current monitoring
- VDD regulators + Digital buffers
- FMC connection to base board

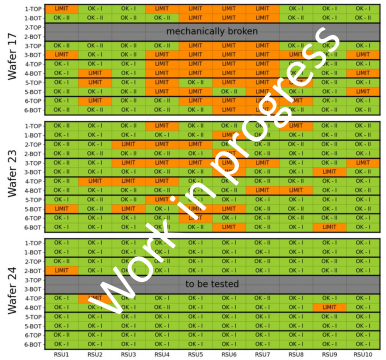
Documentation: • MOST Test-System and Hardware Wiki

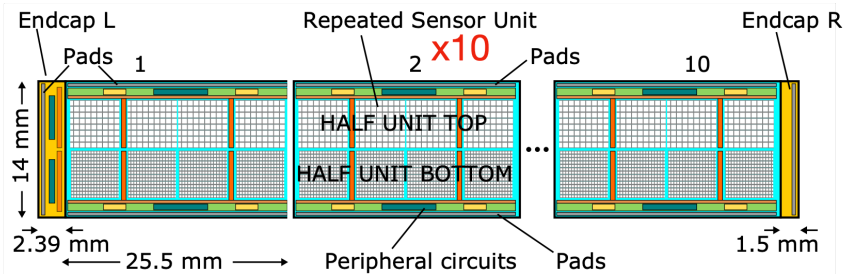
- Firmware/software development Younes Otarid (several elements from ALICE)
- Carrier and proximity board design (Marcel Rossewij Nikhef)

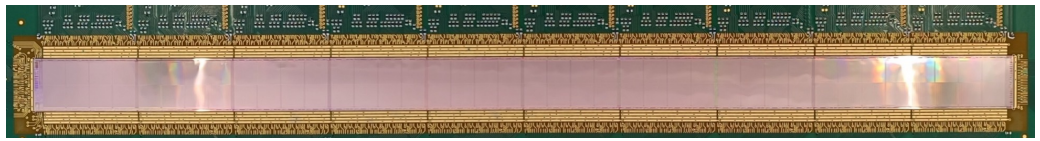
MOSS (25.9 cm x 1.4 cm)

- 10 repeated sensor units:
  - top half at 22.5 um pitch and bottom half at 18 um pitch,
  - each half powered completely independently with 4 conservatively designed submatrices -> many power domains
  - synchronous readout
- First operation in beam in August (D. Colella TIPP2023)
- Detection efficiencies and fake hit rates (M. Mager HSTD 2023)
- Intense effort on powering tests and yield investigations and more detailed characterization



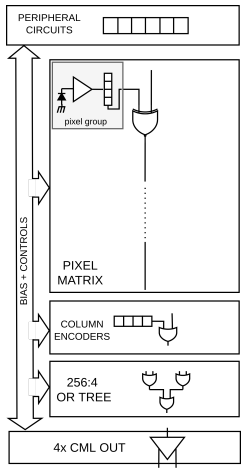


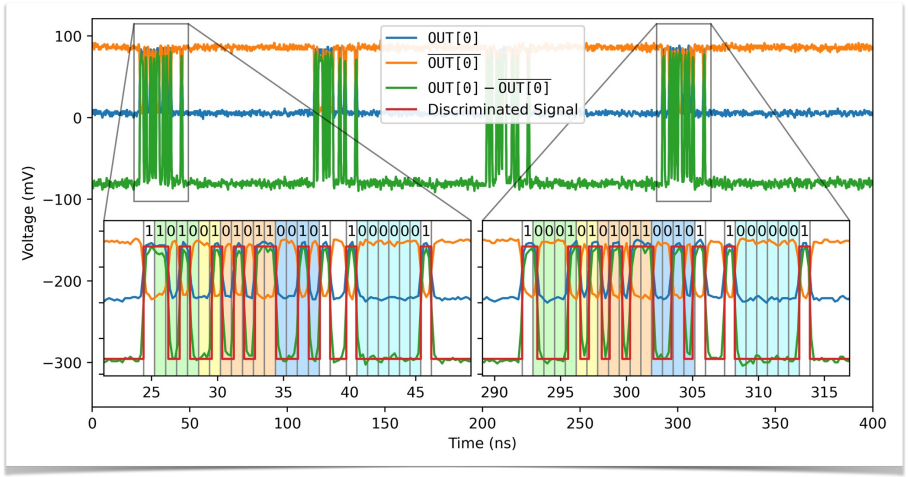




MOST (25.9 cm x 0.25 cm)

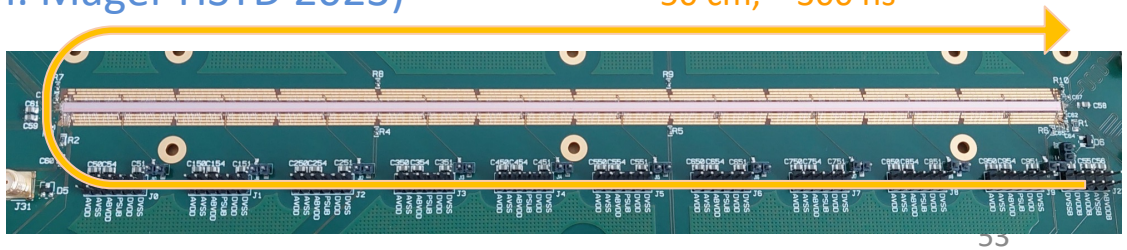
- 10 repeated sensor units:
  - 18 um pitch, very densely designed pixel matrix
  - Global power distribution + conservatively designed highly granular power switches to switch off faulty parts
  - Asynchronous, hit-driven readout, low power consumption + timing information
- Basic functionality established, detailed characterization ongoing.
- Pulsing signal and output signals at the end of the chip, round trip more than 50 cm, ~ 200 ns, with ~800 repeaters, all 256 signal lines functional.





(M. Mager HSTD 2023)

50 cm, ~ 300 ns

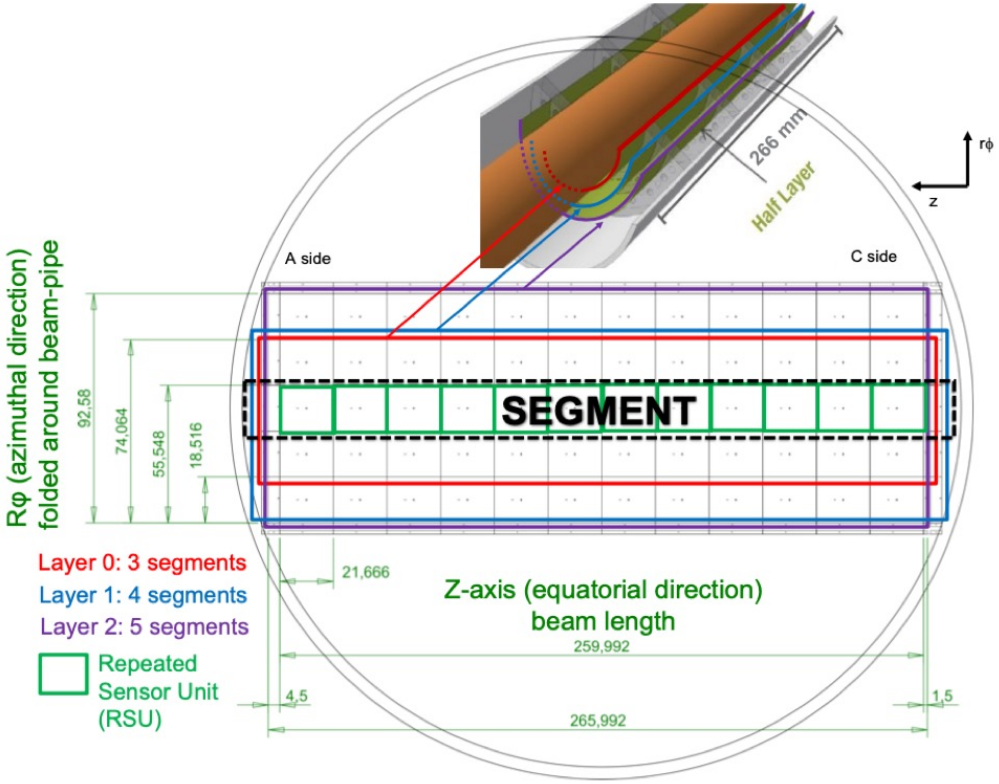


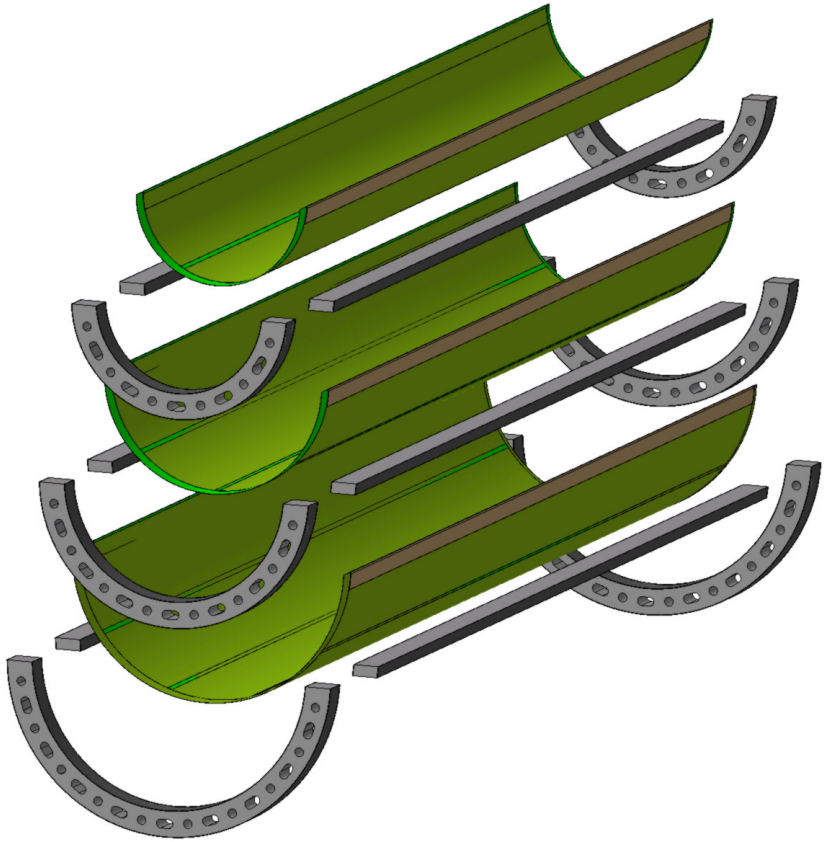
25.9 cm

NEXT STEP: ER2 engineering run: MOSAIX chip for ITS3

MOSAIX chip is being designed, submission in the fall.

- 12 repeated sensor units
- Learnings from MOSS and MOST on stitching are fed back into the design
- Use power switches with power granularity from 20 in MOSS to 144 per segment here
- 3, 4 and 5 segments for layer 0, 1 and 2, respectively





ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

ALICE 3 sensor specification estimates https://arxiv.org/pdf/2211.02491.pdf

LOI estimates, 24 MHz pp collision rate, $1/r^2$ – scaling					Hit Rate		Bandwidth					
	Layer	Radius (cm)	Surface (m2)	Pixels (1e6)	Hit Rate (1e6/cm^2/s)	Hit Rate (1e9/layer/s)	Hits (Gbit/s)	Noise (Gbit/s)	Total (Gbit/s)	Power (W)	NIEL (1 MeV n_eq/cm^2)	TID (Mrad)
Vertex Detector	0	0.5	0.016	160	94	17	274	1	275	13	9,00E+15	288
	1	1.2	0.038	380	16	7.3	117	2.4	119	32	1,60E+15	50
	2	2.5	0.079	790	3.8	3.6	57	5	62	66	3,60E+14	12
Middle Layers	3	3.8	0.29	120	1.7	1.8	28	0.7	79	175	1,60E+14	5
	4	7	0.55	220	0.48	1.2	18	1.4	43	131	4,60E+13	1.5
	5	12	0.94	370	0.16	0.8	13	2.4	27	224	1,60E+13	0.5
	6	20	1.6	620	0.058	0.6	9.9	4	19	374	5,60E+12	0.2
Outer Tracker	7	30	2.3	930	0.026	0.5	7.9	6	16	561	2,50E+12	0.08
	8	45	7.5	3000	0.012	0.6	9.6	19.1	33	1792	1,10E+12	0.04
	9	60	10	4.00E+03	6.50E-03	0.5	8.2	25.5	36	2389	6,30E+11	0.02
	10	80	13.3	5.30E+03	3.70E-03	0.4	6.8	34	42	3185	3,50E+11	0.01

	Vertex Detector	Middle Layers	Outer Tracker	ITS3	ITS2
Pixel size (µm^2)	*O(10 x 10)*	*O(50 x 50)*	*O(50 x 50)*	*O(20 x 20)*	*O(30 x 30)*
Position resolution (µm)	2.5	10	10	5	5
Time resolution (ns RMS)	100	100	100	100* / O(1000)	O(1000)
in-pixel rate (/ pixel / s)	100	100	100		
Fake-hit rate (/ pixel / event)	<1e-7	<1e-7	<1e-7	<1e-7	<< 1e-6
Power consumption (mW / cm^2)	70	20	20	20**	47 / 35***

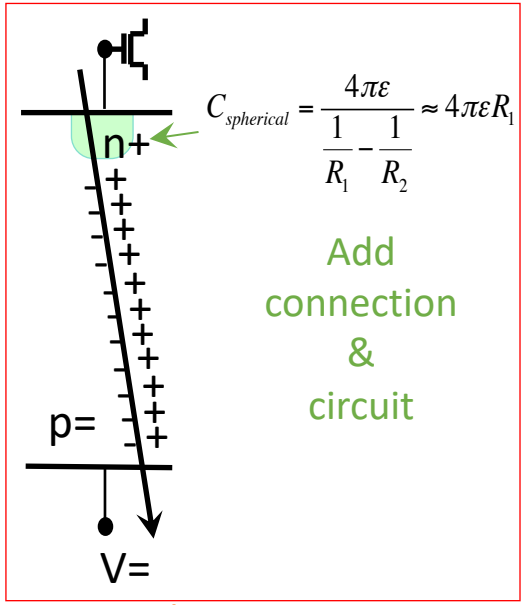
F. Reidt et al.

Need significant improvement in:

- Power-performance ratio, not only in front end, but also on and off chip data transmission, and architecture
- Radiation tolerance for inner layers

=> Observing convergence in sensor development targets, mostly common in the short term for different HEP applications, with longer term incremental R&D (L. Musa https://indico.cern.ch/event/994685/contributions/4181740/attachments/2193327/3707745/MUSA_ECFA_IS_2021FEB.pdf) see also D. Contardo

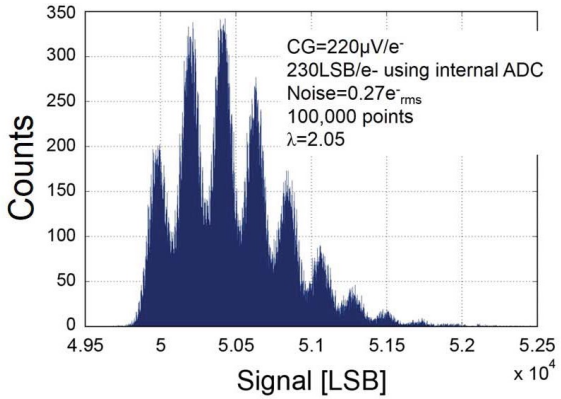
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

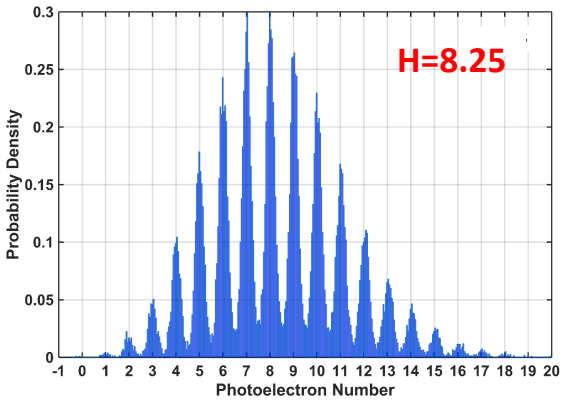
Add connection & circuit

M.W. Seo and S. Kawahito EDL 2015



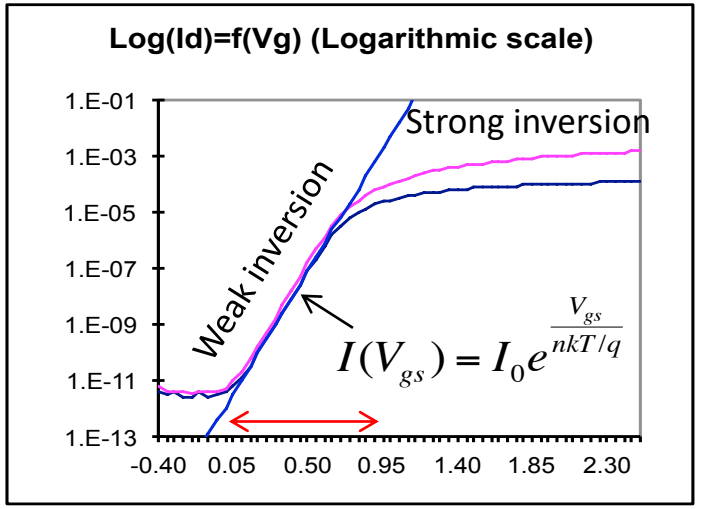
220 μV/e⁻ in 0.11 μm, C=0.73 fF

Ma, Masoodian, Wang, Fossum 2017



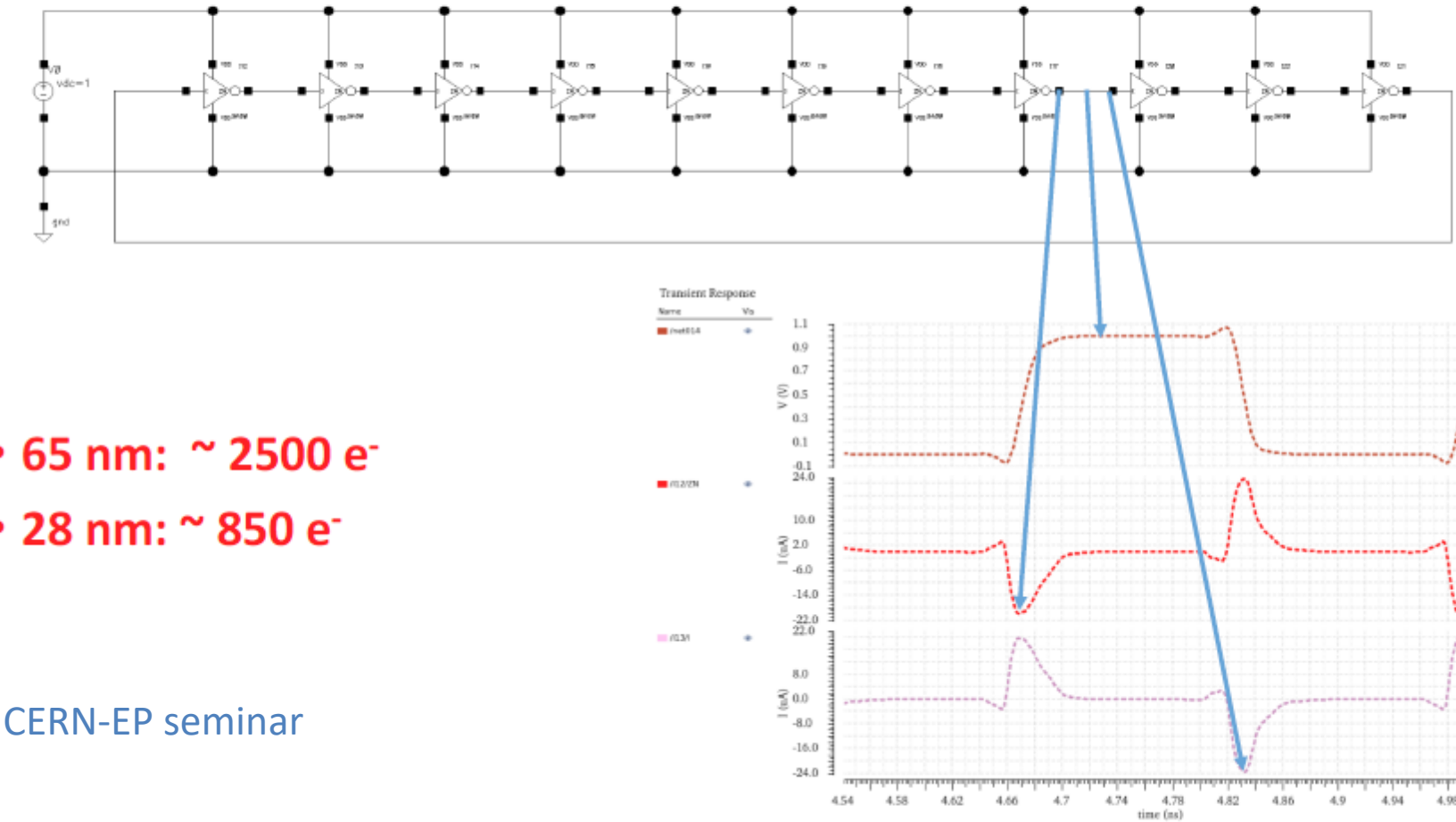
350 μV/e⁻ in 45 nm, C=0.46 fF

Non-linearity in weak inversion



- Q/C several 10's of mV in 180 nm
- "Conventional" approach
  - ITS3 estimate ~ 10-15 nW front end for about 10 mW/cm² (ALPIDE in 180nm ~ 40 nW), 5x area reduction
  - Increase power and speed for better timing, μW for < 1 ns F. Piro
- Reduce capacitance further, using:
  - tricks from imaging technology, at present not yet explored?
    - now very conventional nwell collection electrode…
    - Still need to extract signal charge from underneath the readout circuit !
  - deeper submicron: 2500 e- to switch inverter in 65 nm, 850 e- in 28 nm, 100 e- in 5 nm A. Marchioro 2019 CERN EP seminar
- Holy Grail: For Q/C > 400 mV, analog power consumption goes to zero.

How many electrons are needed to switch a logic gate ?



- **65 nm: ~ 2500 e⁻**
- **28 nm: ~ 850 e⁻**

A. Marchioro, 2019 CERN-EP seminar

Power consumption and voltage drops

Energy to transfer 1 bit to the periphery (assume line toggle, not step):

1 cm line at 1.8 V = CV^2 = 2 pF x $(1.8\ V)^2$ = **6.5 pJ** Lower VDD in deep submicron = 2 pF x $(1\ V)^2$ = **2 pJ**

Caveat: 2pF/cm can increase depending on line load…

- Digital power density proportional to activity level (hit densities…) and column height, but now leakage also important !!
- Voltage drops proportional to the square of the column height and power density
  - For constant power density (eg analog) voltage drops proportional to the square of the column height
  - Digital voltage drops for long distance in full CMOS proportional to the third power of the column height
  - Significant challenge for stitched devices, in addition to yield

Off-detector transmission:

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

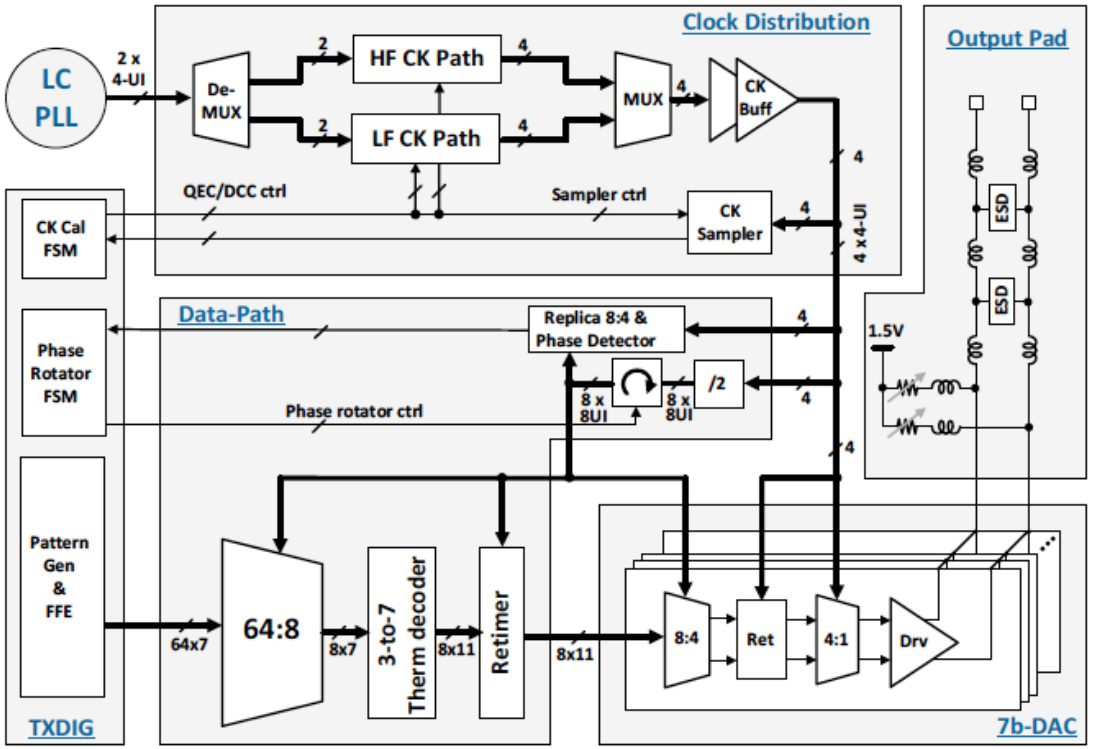
2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA

Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

INTEL, ISSCC2021, 224Gbps, PAM-4, 1.7 pJ/bit, 10 nm technology



State of the art: a few mW/Gbps, already earlier but also now at much higher bandwidths

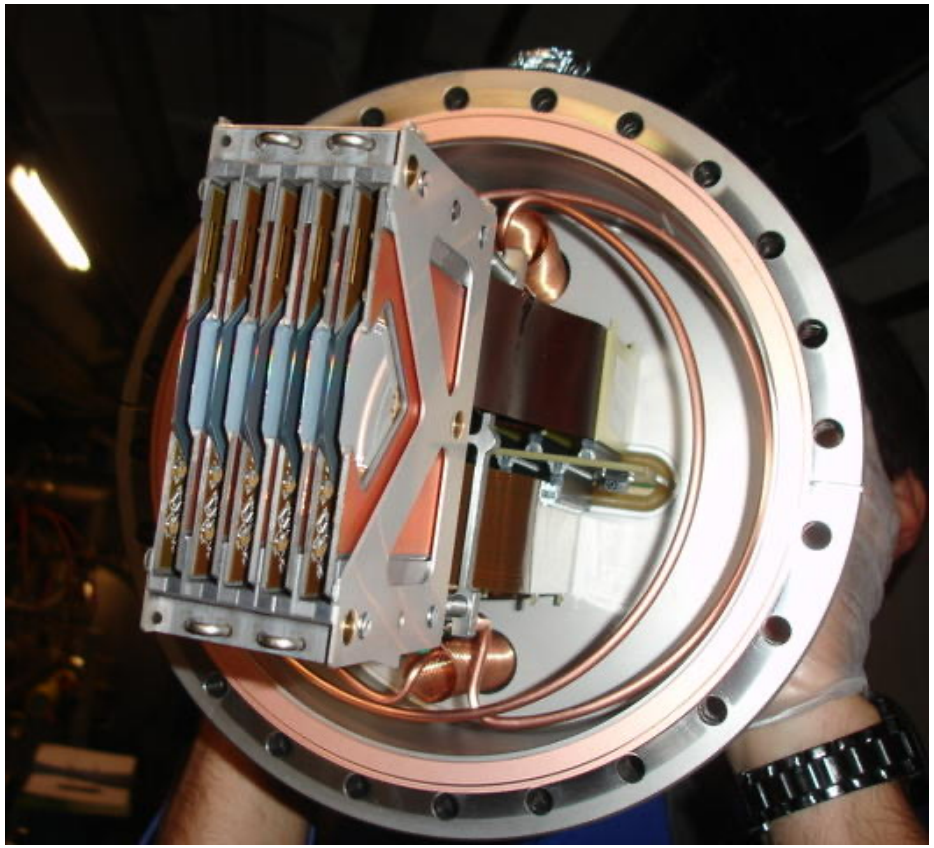
Significant circuit complexity

For HEP important penalty for SEU robustness due to triplication/larger devices…

Important: data concentration, physical volume for material budget, and technology

Low power is the key to low mass

- Cables, cooling etc… represent significant fraction of the material in the detector, and material in the tracker has to be minimized
- Limit for future upgrades
- Power consumed at CMOS voltages, so kW means kA

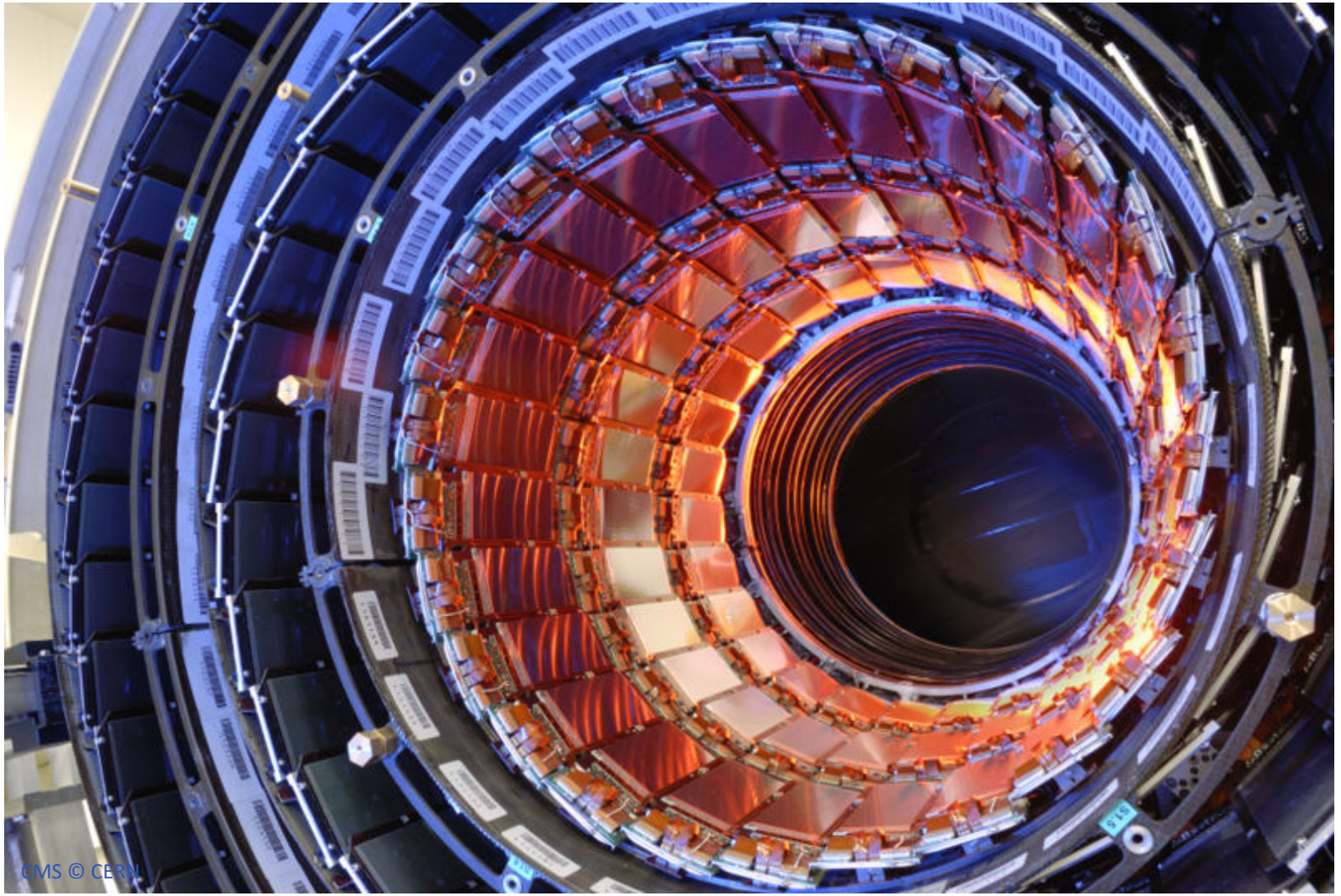


Example, currently installed at LHC:

Roman Pot in the TOTEM experiment:

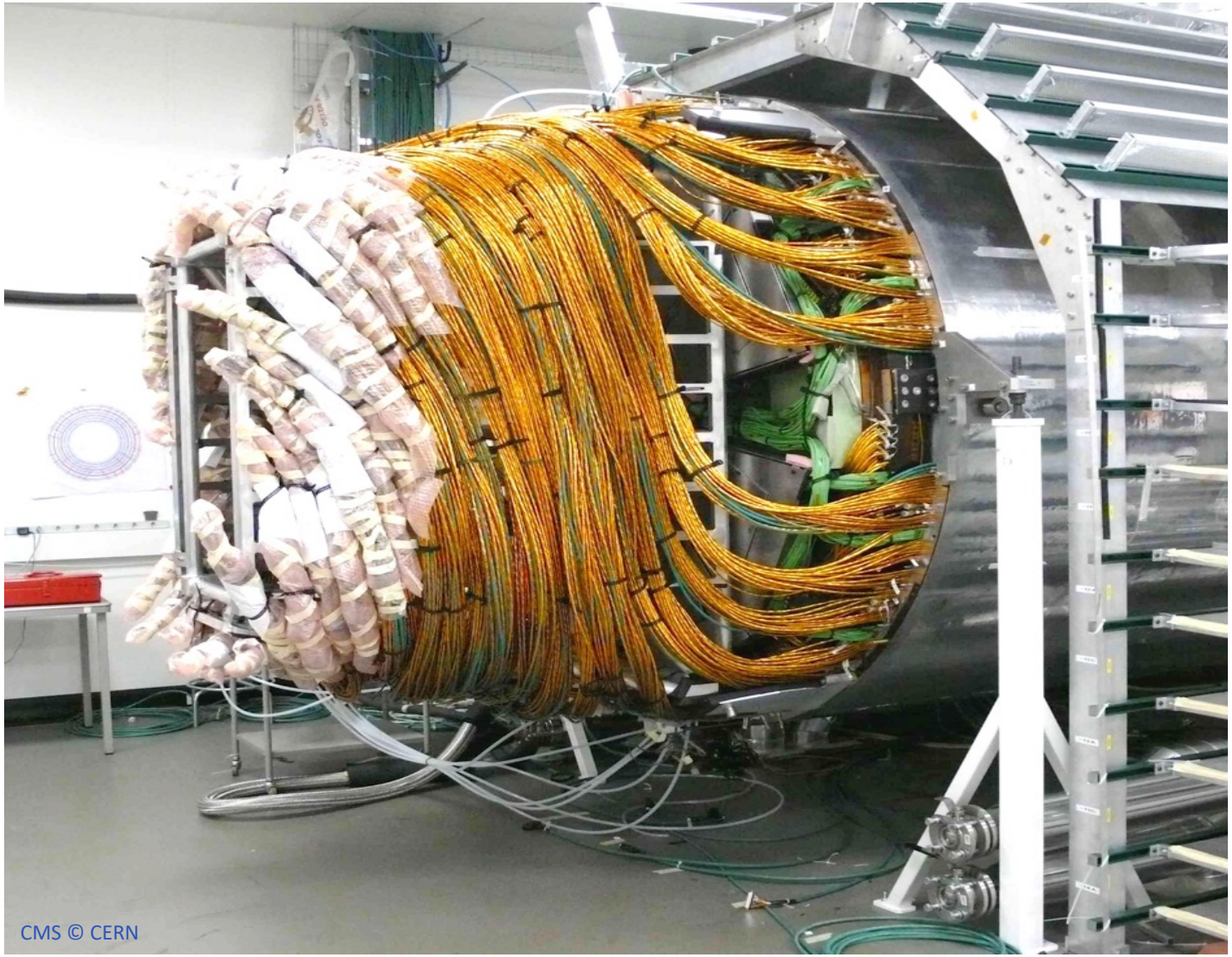
- ~ 6A @ 2.5 V
- ~100m 2x16mm^2 cable
- 26kg of Copper for ~ 15 W

THE CMS TRACKER before dressing



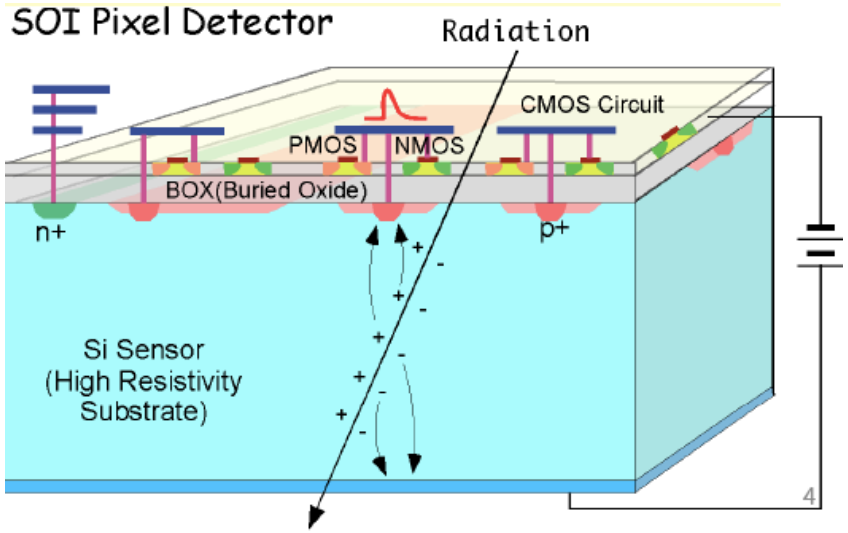
~ 200 m^2 of silicon strips

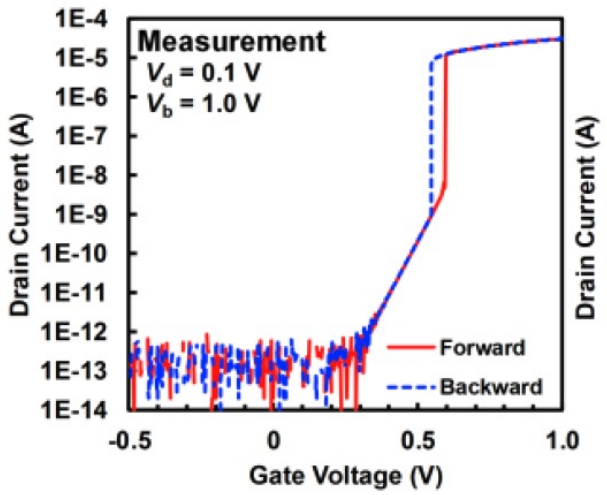
And after…

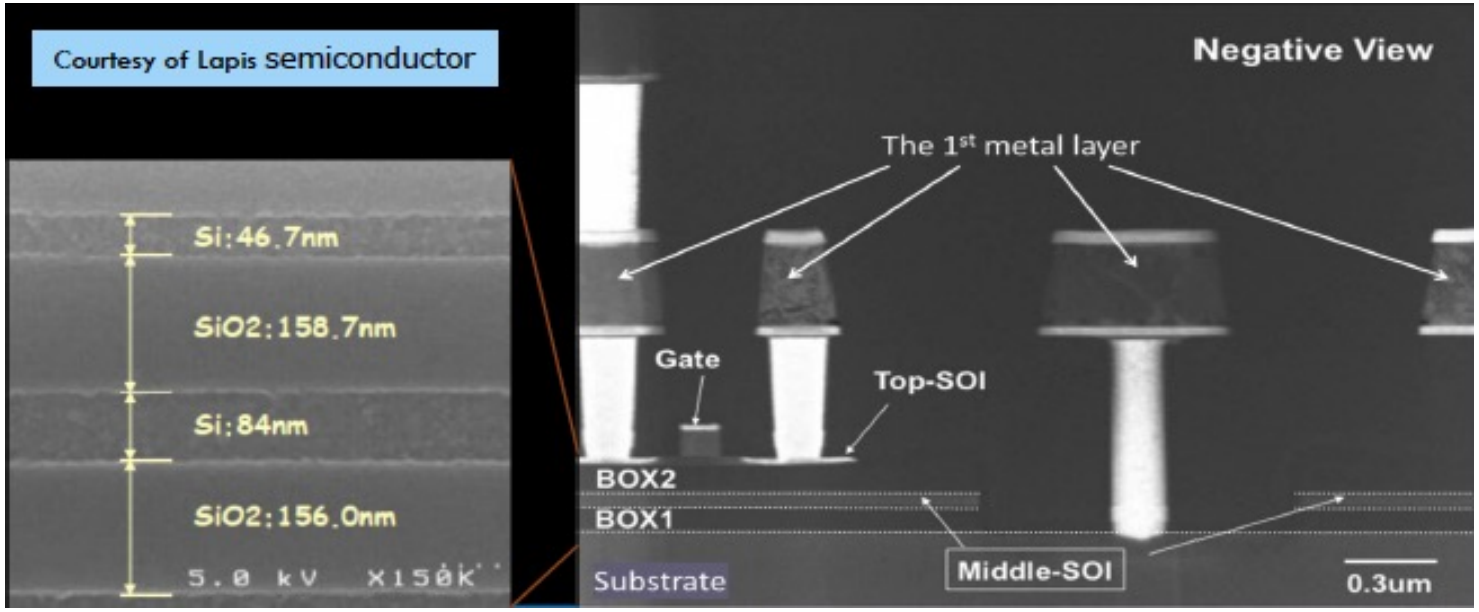


33 kW in the detector … and as much in the cables !

SOI development in Japan





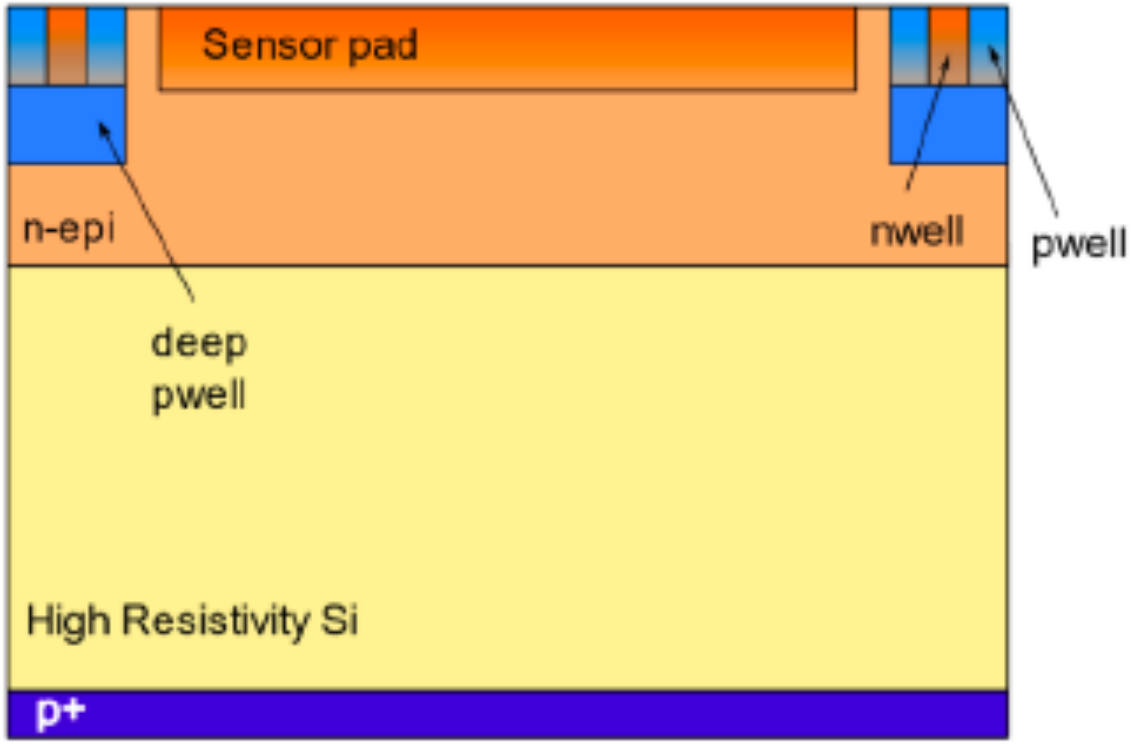


- Fully depleted 0.15 and 0.2 µm SOI technologies, impressive technology development
- Large user base, more than 20 MPWs so far in addition to dedicated runs
- Some freedom on sensor material
- BOX causes reduced radiation tolerance, several measures for improvement, like double box, see bottom left
- Also research on
  - steep slope transistors doi:10.1109/SISPAD.2019.8870519
  - pinned diodes doi:10.3390/s18010027
  - …
- Funded by Japan MEXT KAKENHI Grant-in-Aid for Scientific Research on Innovative Areas 25109001

Courtesy Y. Arai

Technology also used in presentation by Mizuki Uenomachi

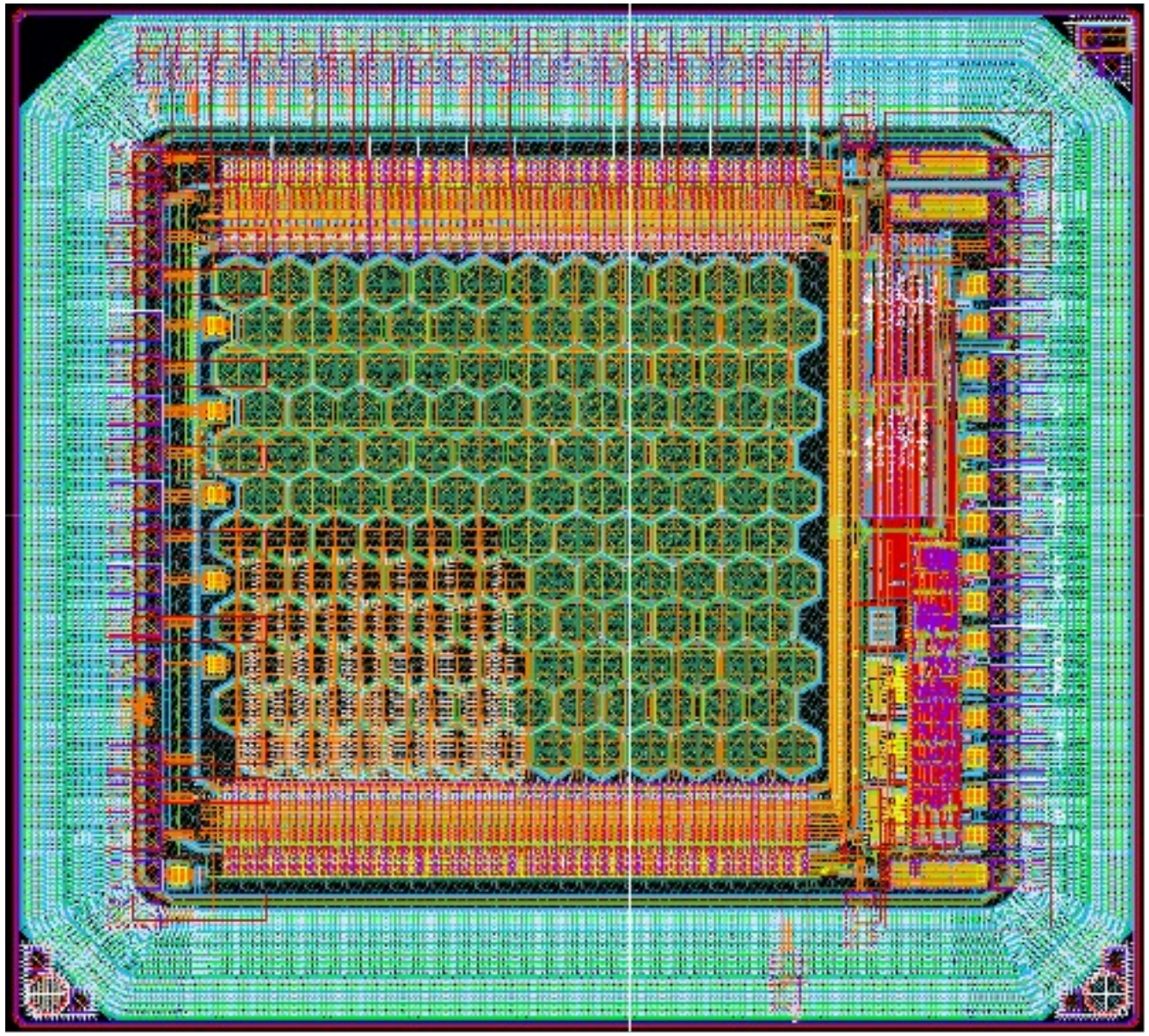
ARCADIA Sensor: LF 110 nm



L. Pancheri 2022
IEEE Transactions on Electron Devices
Vol. 67, No. 6, June 2020

- Depleted MAPS
- Developed in a collaboration between INFN and LFoundry
- 110 nm CMOS, 6 metal layers
- Adding gain layer (gain 10-20) to reach 20 ps resolution
  first results available, further optimizing gain.
- Prototypes
  - Pixel size: 250 x 100 μm^2
  - Diode area : 220 x 70 μm^2
  - Sensor capacitance: 127 fF
  - Electronics size: 280 x 8 μm^2
  - Active thickness: 50 μm^2
- Test beam campaign ongoing, results in Q4 2023

MONOLITH: SiGe BiCMOS development



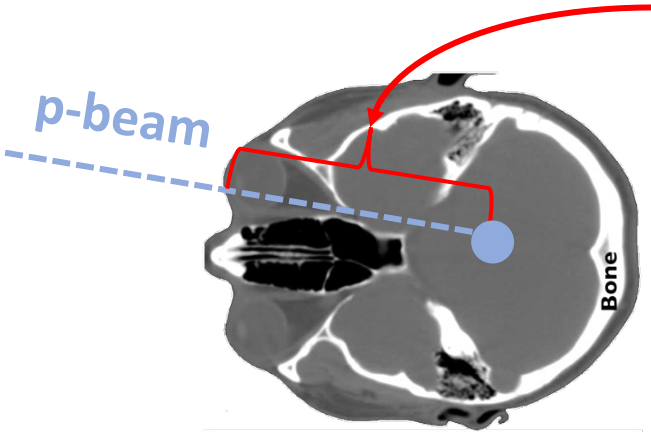
- Heterojunction Bipolar Transistor (HBT) gives cut-off frequencies otherwise only reached in more advanced CMOS technologies
- Large collection electrode hexagonal pixel arrangement
- Prototype without gain:
  - Full efficiency
  - ~ 20 ps time resolution without gain layer
  - Radiation tolerance 10^{16} n_{eq}/cm^2, also for the HBT !
- See presentation by Lorenzo Paolozzi

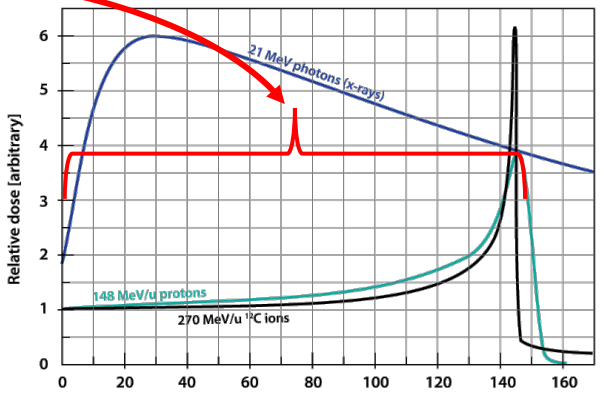
Courtesy G. Iacobucci

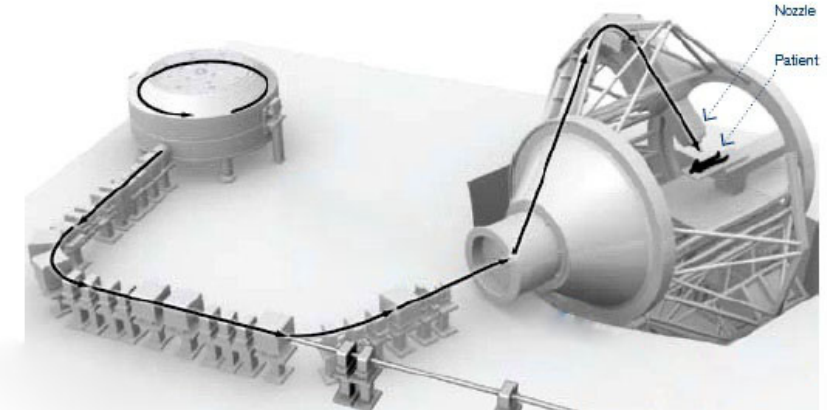
From medical imaging to medical tracking: Proton therapy and proton CT

Cfr. D. Rohrich and P. Giubilato

Energy tuning proton beam better than 0.5 % requires proton CT rather than X-ray CT (too poor tissue density resolution)

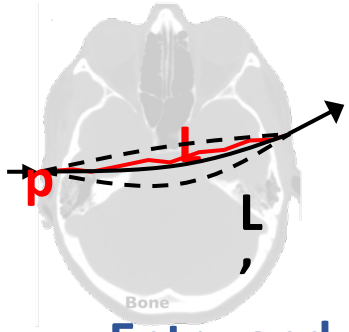






courtesy of P.Giubilato

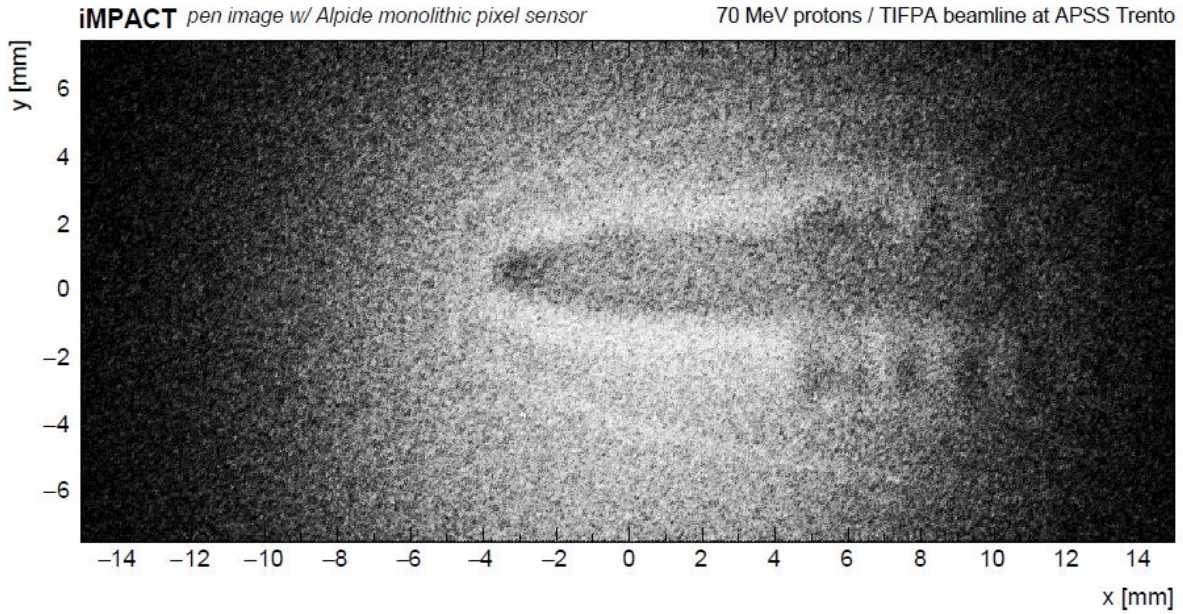
Proton true trajectory



Energy measurement

Entry and exit points + angle

Most Likely Path calculation



Demonstration with ALPIDE chip

Need at least 10^9 proton tracks (entry and exit + most likely path) and 10s of minutes with state of the art detectors.

Gaining time requires detectors which do not yet exist

- After years of R&D monolithic sensors for HEP move to CMOS MAPS with complex in-pixel circuitry in mainstream CMOS technology, but requirements for HEP are not completely identical to those for visible light imaging, and some technology flexibility can still be beneficial.

- Circuit radiation tolerance as for standard CMOS, which naturally evolved towards significant tolerance with some caveats.

- 10 years of experience with 180 nm enabled fast qualification of the 65 nm technology for HEP and the exploration of wafer-scale sensors for ITS3, opening perspectives for other projects like ALICE3. Some foundry flexibility has allowed greatly improved sensor timing, radiation tolerance and operating margin based on general principles applicable to different technologies.

- Large collection electrode sensors provide extreme radiation tolerance and more uniform sensor timing but exhibit large input capacitance.

- Decreasing technology feature size or special imaging sensor features can increase the voltage excursion on a small collection electrode and ultimately reduce analog front end power to zero and allow precision timing.

- The increasing complexity of Monolithic Active Pixel Sensors requires digital-on-top design techniques and verification by a team of expert chip designers, and sensor optimization and simulation by device/TCAD/Monte Carlo experts.

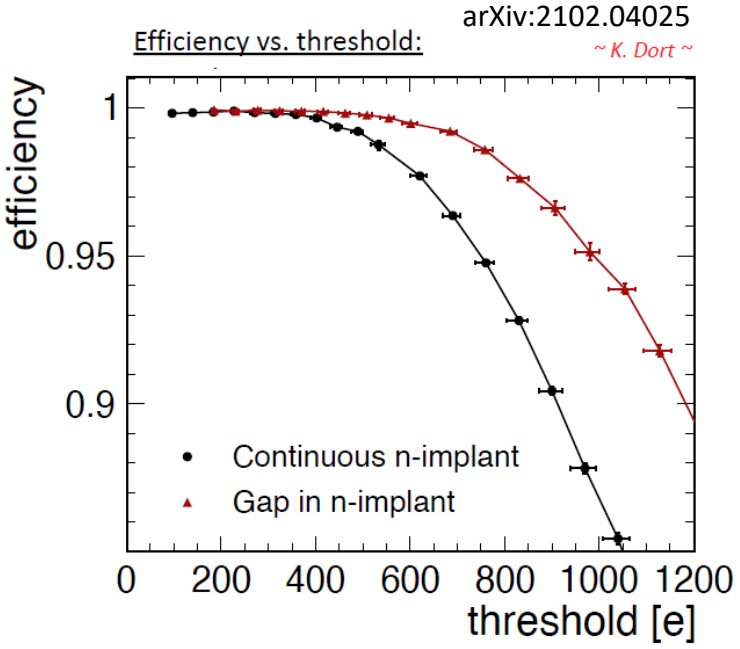
- 3D wafer stacking now allows the connection of a readout wafer to a detector wafer, and deliver the fully finished diced assemblies to the customer. This reduces the distinction with hybrid sensors, but provides opportunities well beyond with multiple connections within each pixel and stacking of even more than two wafers.

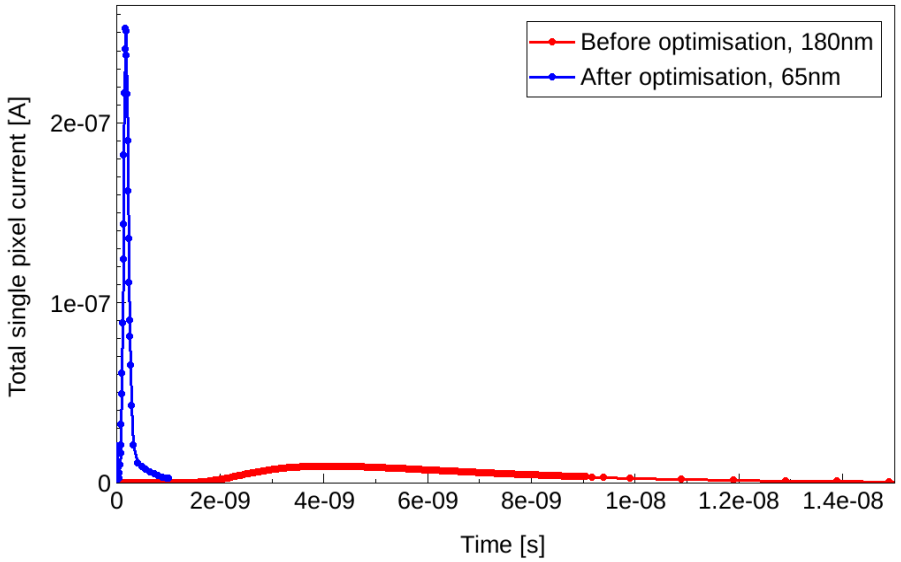
- Unprecedented integration in electronics systems continues to be driven by the computation needs of AI. Stitching and wafer stacking brings pixel pitches around 10 um within reach. The circuitry on a monolithic sensor allows the mitigation of local, otherwise fatal defects for large, even wafer-scale sensors. Efficient volume test, assembly, and mounting, together with significant progress towards lower power densities and on-chip resistive drops, will be enablers for large area detectors, and this for practically all applications in HEP.

- CMOS monolithic sensors will become widely applied in HEP, in tracking, calorimetry and timing detectors. Non-negligible MAPS production volumes within HEP should allow our community to impact not only the quality of its own measurements, but also society in general, with access to the most advanced technologies.

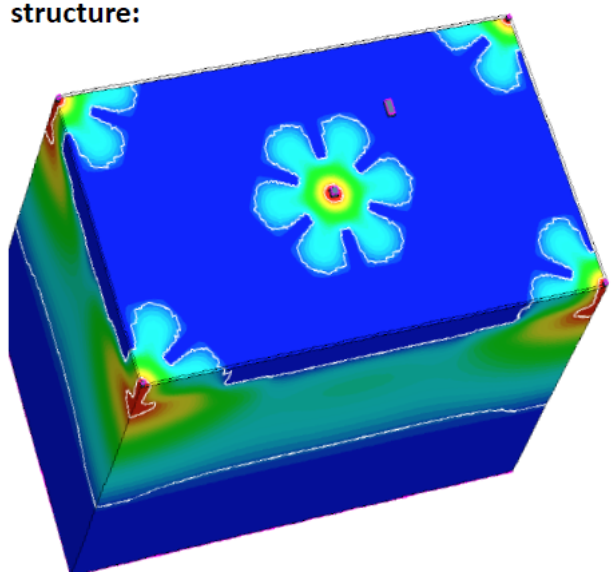
THANK YOU !

Process optimizations for small collection electrode





Example of complex 3D TCAD structure:



- Efficiency improvement is not only simulated but also measured, even before irradiation (see top left: efficient operating window is almost doubled)
- The optimization over different pixel pitches and flavors, and technologies has improved the timing by several orders of magnitude. Simulations of even more complex structures bring peak-to-peak variations in the order of 50 ps at the moment
- These techniques have now been applied to several chips, and technologies and are generally applicable.

See M. Muenker's CERN EP detector seminar