GBT-FPGA Interface

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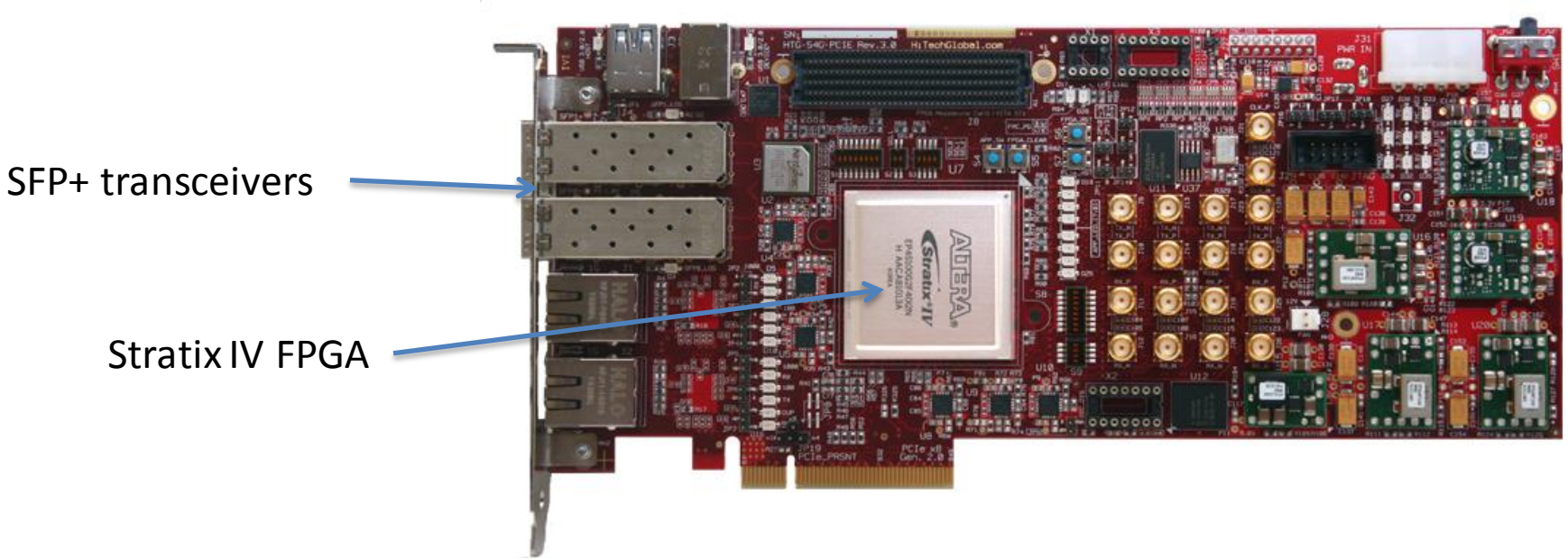
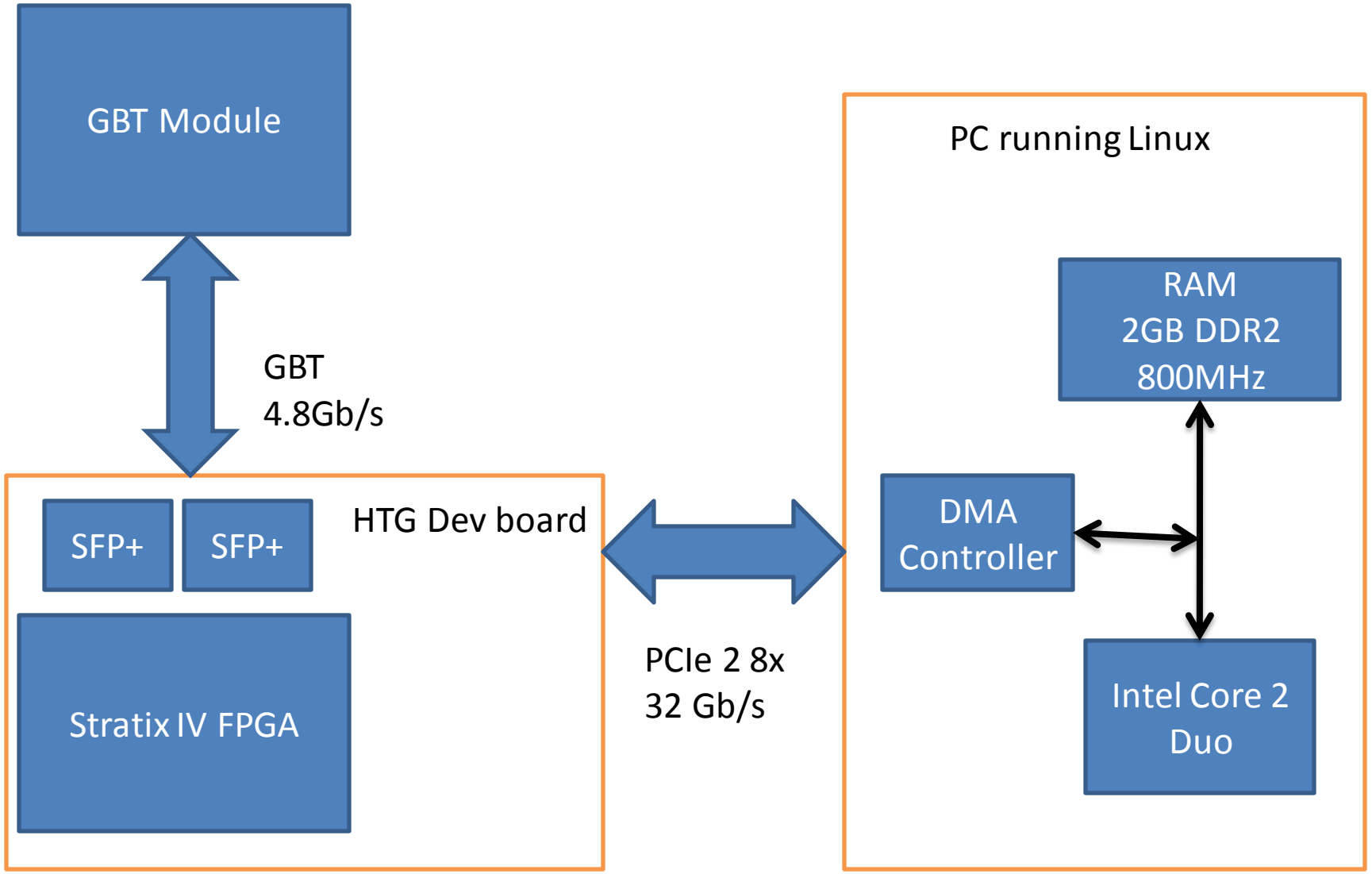
GBT

- New radiation tolerant ASIC for bidirectional 4.8 Gb/s optical links to replace current timing, trigger, and control system of LHC experiments
- Will be required when luminosity increases since the amount of data will also increase
- GBT modules located at detectors

FPGA

- Counting room electronics don't need to be radiation hard
- Implement transceiver using commercial FPGA
- High Tech Global board with Altera Stratix IV FPGA and two SFP+ transceivers.

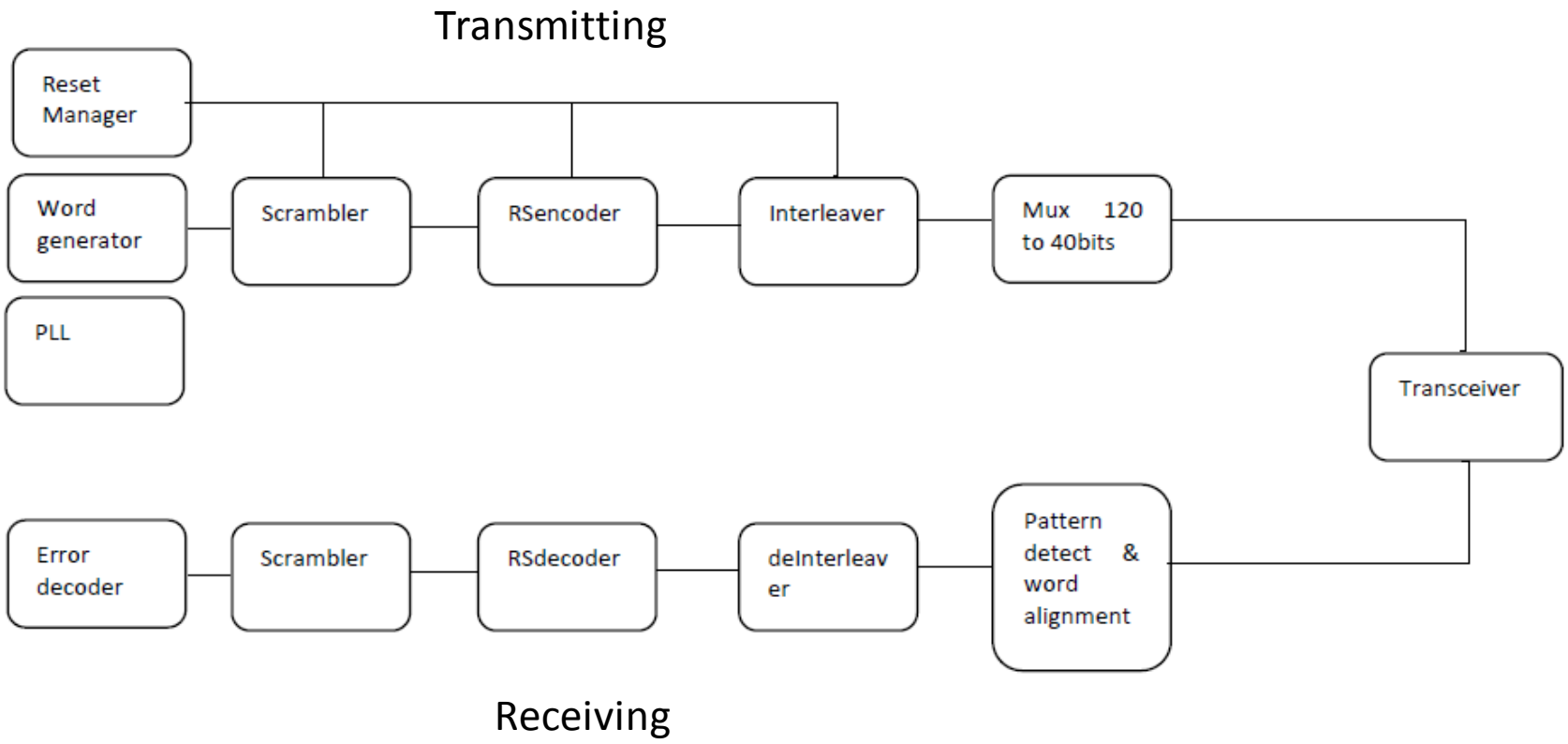



GBT Module
GBT
4.8Gb/s
SFP+
SFP+
HTG Dev board
Stratix IV FPGA
PCIe 2 8x
32 Gb/s
PC running Linux
RAM
2GB DDR2
800MHz
DMA
Controller
Intel Core 2
Duo

What I've done since last time

- I've been modifying a linux driver
  - Changing configurations in driver to match those of the PCI IP core in the FPGA
  - Updating code for newer kernel
- Testing GBT interfacing code through internal loopback
  - Make sure process of receiving and transmitting data using GBT protocol is working on FPGA end
  - Debugging using LEDs and maybe simulations

GBT Serialization-Deserialization Procedure



What I need to do

- Fix problems with the linux DMA driver and modify it to allow board to read/write to memory through PCIe bus
- Interface with GBT module using SFP+ transceiver
- Run tests to verify speed and accuracy of GBT module