Update on R&D efforts at NISER for ALICE FoCal

ALICE-STAR-India Meeting

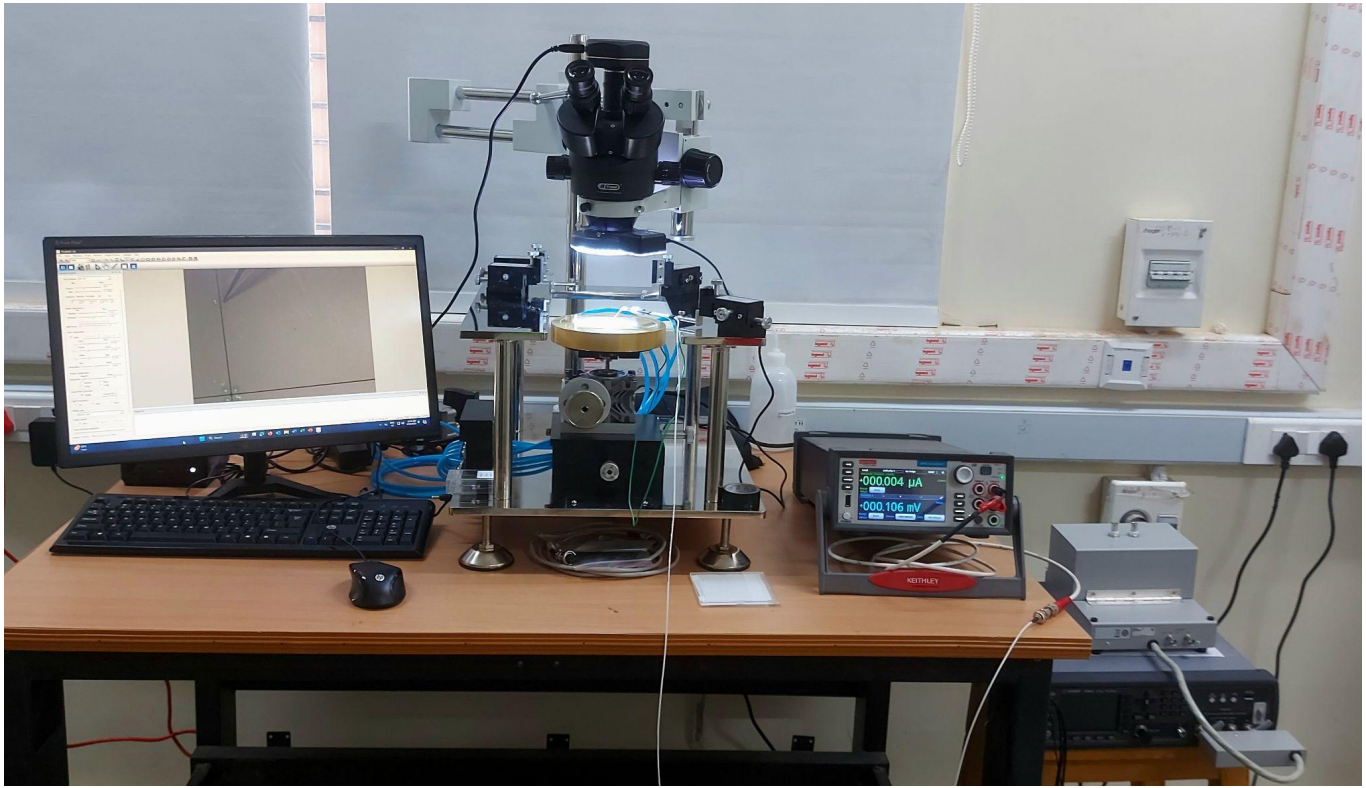
IoP Bhubaneswar, 26 June 2024

https://indico.cern.ch/event/1411351/contributions/6013991/

Outline:

- Previously reported in ALICE -India meeting at Jammu Univ. (Nov. 2023):
  - n-type Si pad array detectors fabricated at BEL, Bangalore, India
  - IV tests results are fine ~ 90% pads show leakage current < 10 nA/pad cell
  - Performance test results using LED and Sr90 source at NISER lab
    - refer article https://arxiv.org/abs/2406.08144
  - PS, CERN test beam experiment results
    - refer article https://arxiv.org/abs/2403.13394
- Progress in last six months
  - Mostly worked on completion of above two papers
  - Assembled basic probe station in clean room at NISER
  - Status of single pad PCB development in India
  - Update on multilayer test setup and its DAQ

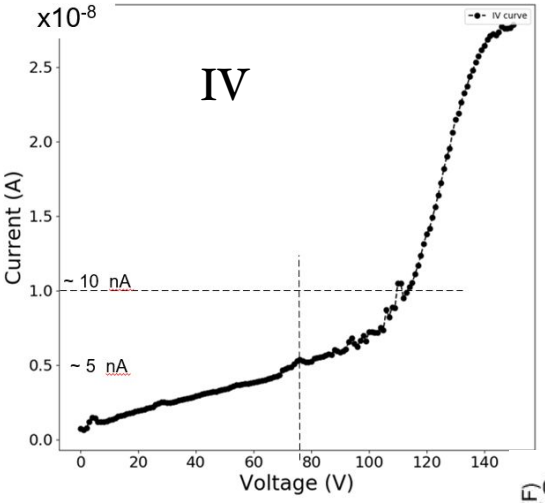
Basic probe station @ NISER



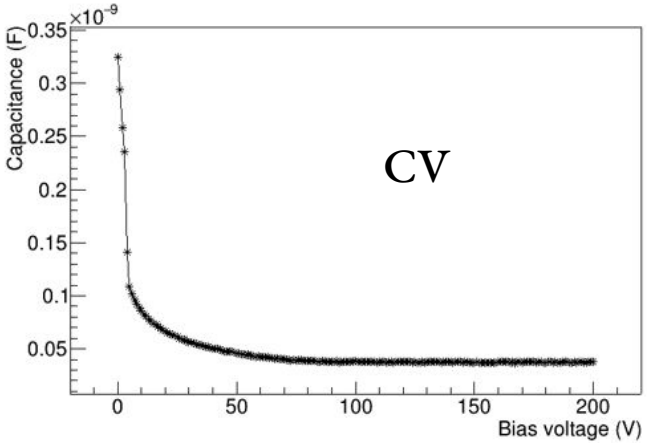
Assembled basic Si-detector wafer/die probe station:
Ready to perform IV/CV of single pad cell, work in progress for IV/CV of Si pad array

Basic probe station @ NISER: ongoing

Probe station with dark box
in clean room (class 1000)

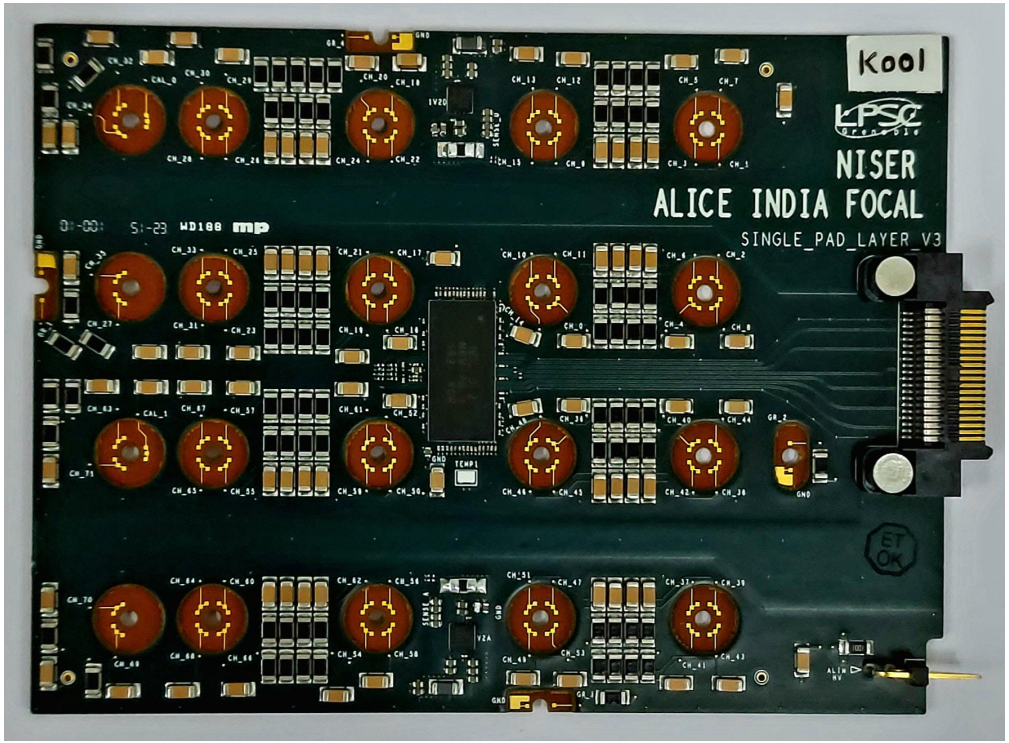


Typical IV and CV plots
Of single pad cell on the die

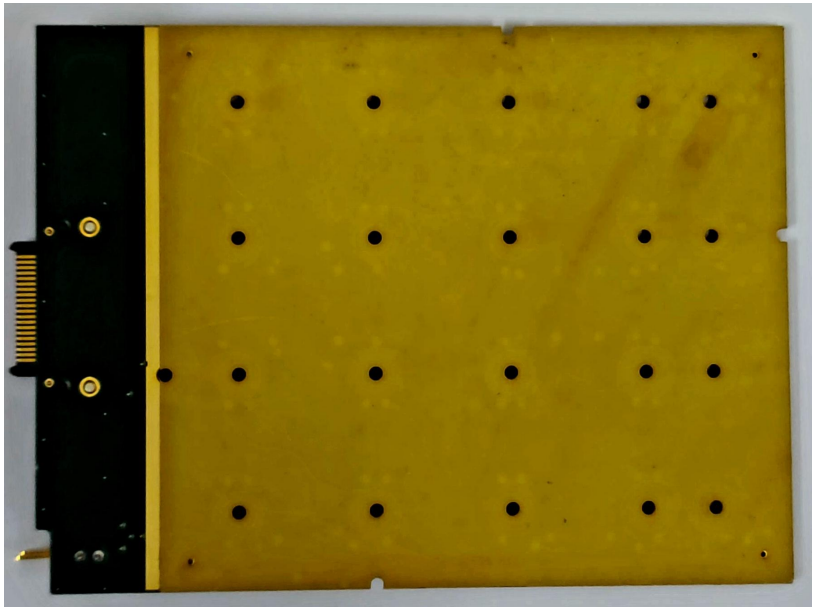


Update on Single pad array PCB: LPSC, Grenoble design

Front view: 8 cm x 11 cm



Back view

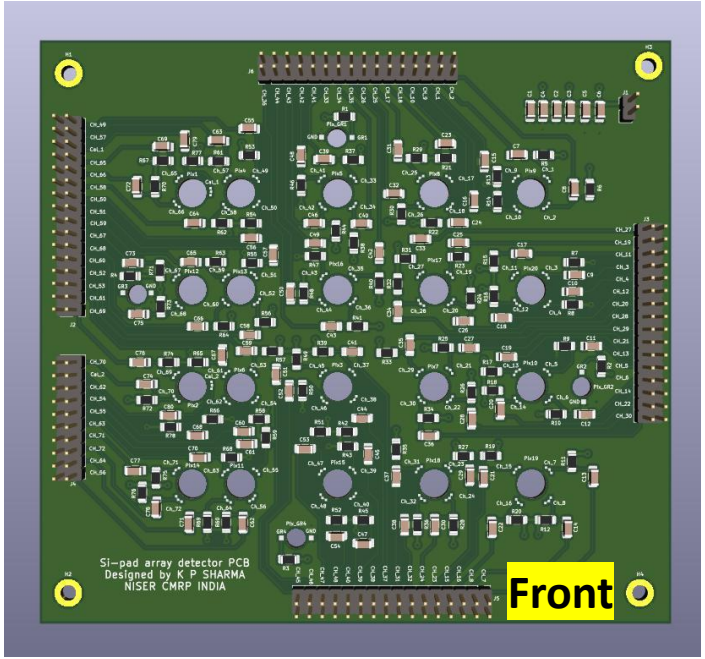


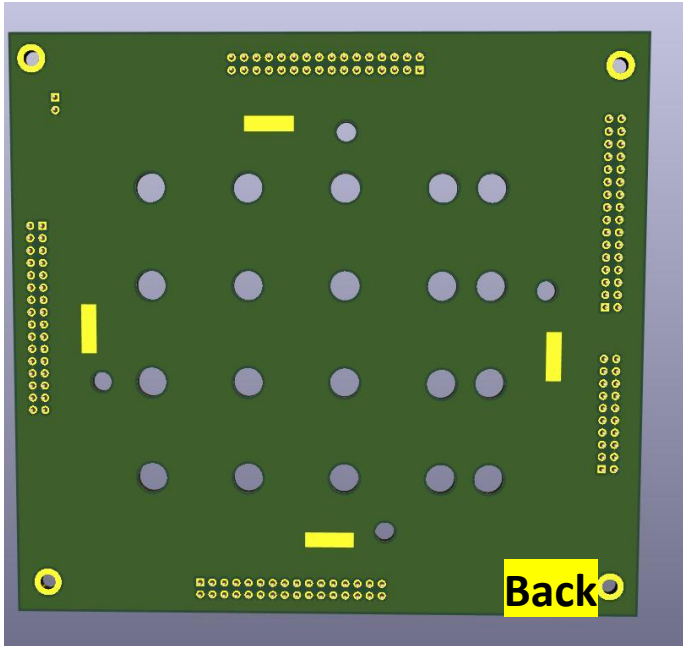
Si pad array detector readout PCB fabricated, 3 assembled and tested, its working as it should.

(Thanks to Kirti, Micropack Private Limited and KHMDL, Bangalore, India)

Update on Single pad array PCB: NISER design

Designed another PCB @NISER: Test detector with other Readout electronics, monitor IV/CV of individual Si pad cell, gain uniformity, cross-talk study etc.

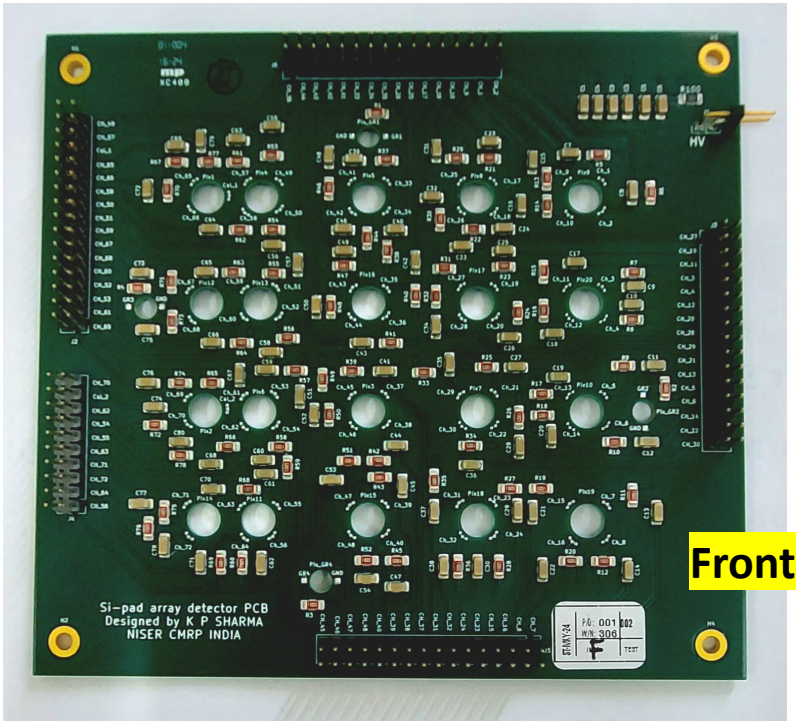


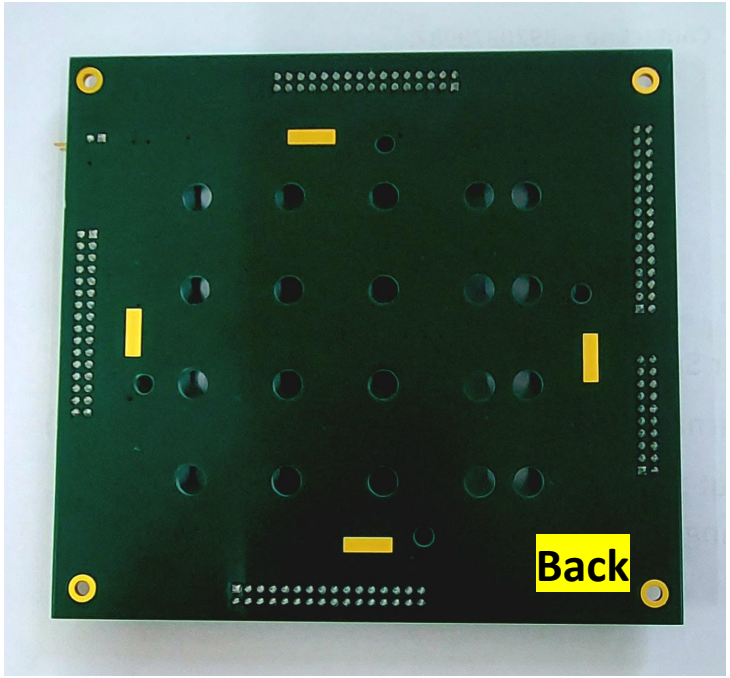


PCB designed by Mr. Kirti Prakash Sharma (NISER)

Update on Single pad array PCB: NISER design

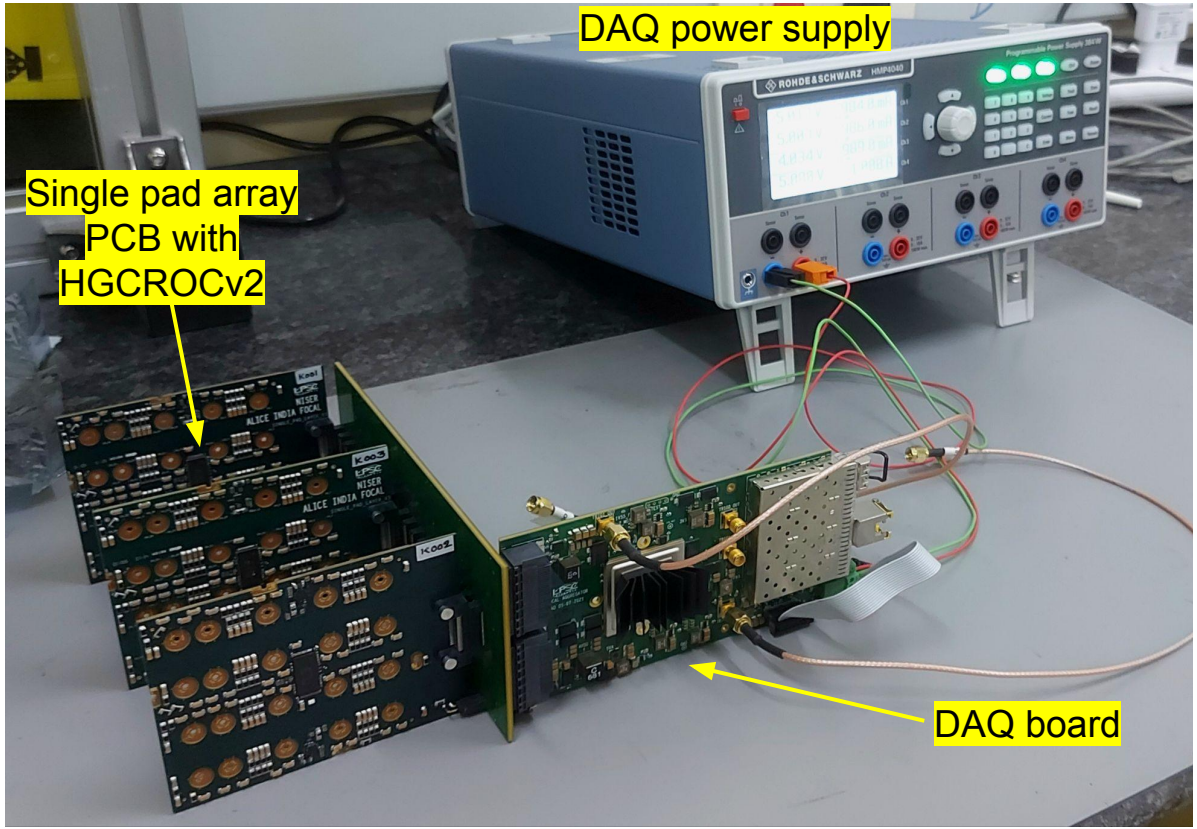
Another single pad array PCB received in May 2024:
jig production and die attached should be complete by Sept. 2024





PCB designed by Mr. Kirti Prakash Sharma (NISER)

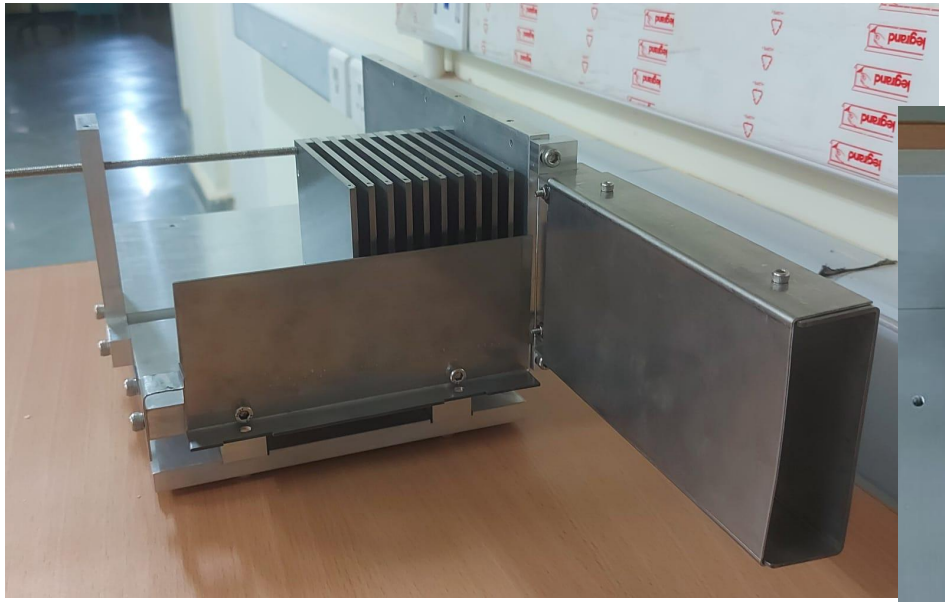
Multiple Si pad array readout setup: work in progress



Will take some time Since, there is no user manual/documentation

Multi-Layer Test setup under preparation @ NISER Si lab

Mechanical setup ready for use



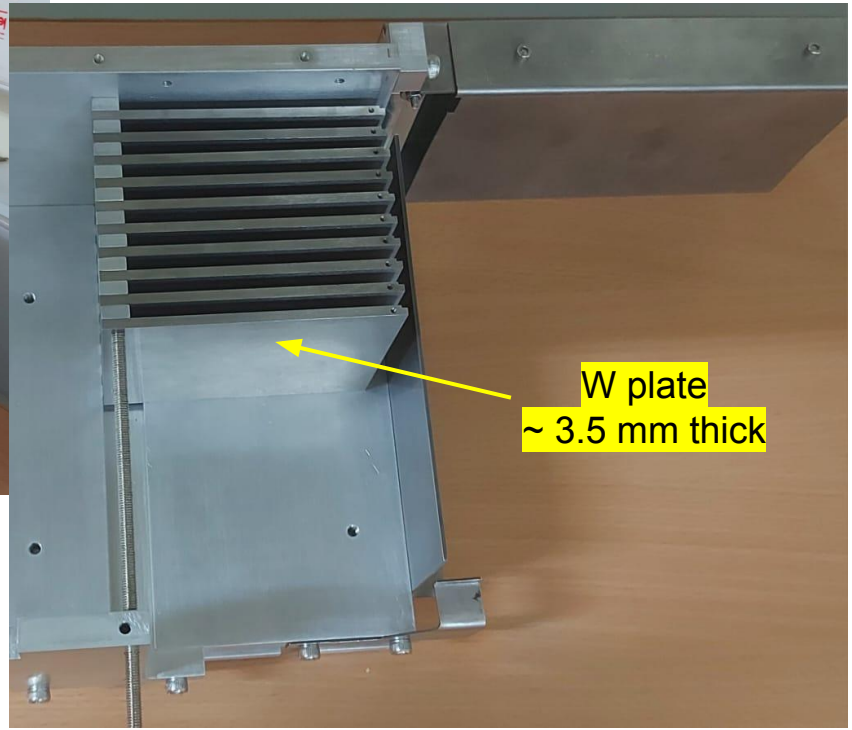


Photo of setup at NISER Si lab,

Parts made at Central workshop NISER

Summary

- Performance testing of n-type Si detector at NISER test lab done using LED and Sr90 source,
  - refer article https://arxiv.org/abs/2406.08144
- Successful detector test experiment using GeV energy e- and Pion beams at PS, CERN
  - refer article https://arxiv.org/abs/2403.13394
- Assembled basic probe station in class-1000 clean room and ready for use
  - work ongoing to make it semi-automated - for 72 pad array
- 25 PCB fabrication and component assembly near completion:
  - assembled and successfully tested 3 PCBs, they working well
- Adaptation of data acquisition system for single n-type Si detector done
  - Working on layered Si-W setup - DAQ setup ongoing
  - Mechanical setup and 20 tungsten plates are ready

NISER groups interests to contribute in FoCal project:

- P-type pad array design and development, and fabrication with Indian Si -fab.
- Wafer level IV/CV tests using semi-automated probe station at NISER
- Detector test: LED, radioactive sources and test beam at CERN
- Electronics development and fabrication in collaboration with Indian industry
- Detector module assembly and testing at NISER
- Participate in the final detector system integration and related tests.

Thank you!

NISER FoCal Group

Sawan
(PhD Student)

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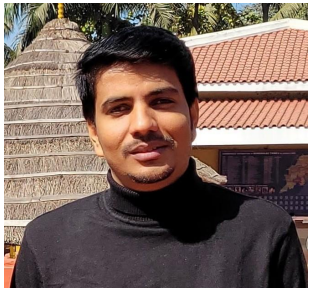
(Project Assistant)



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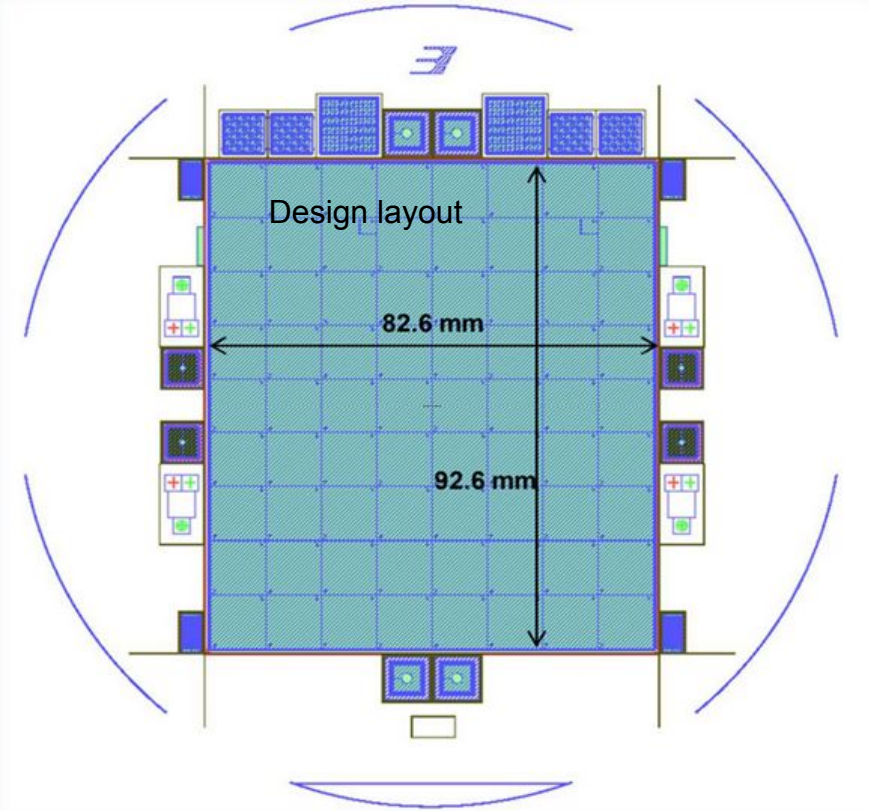
Backup:

n-type 8x9 Si pad array detector: Design & Wafer



High resistivity (~7kohm.cm), ~325 um thick Si wafer