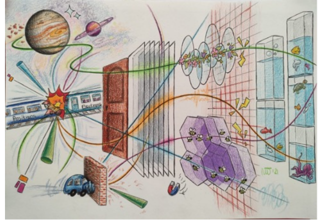
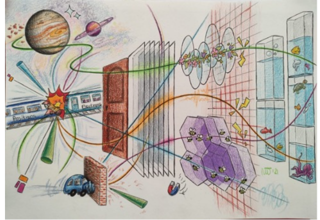


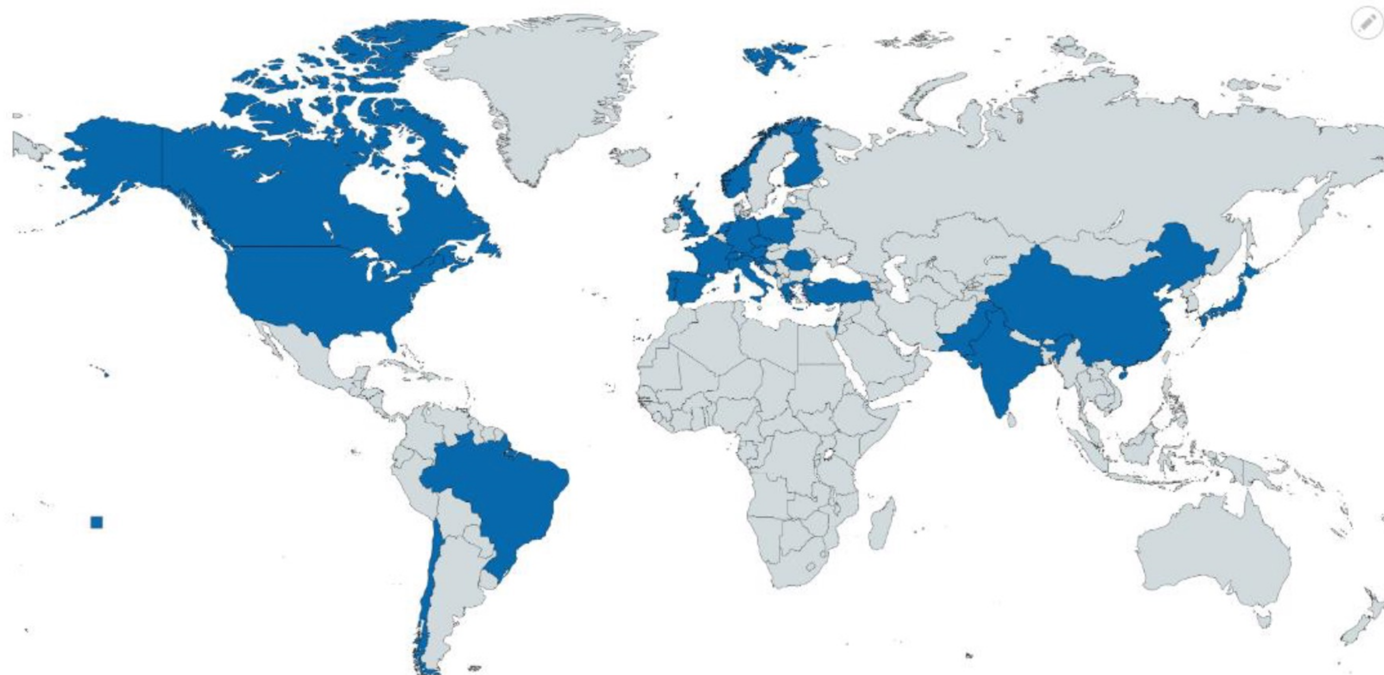
Interconnect and device fabrication technologies

G. Calderini (LPNHE Paris), D. Dannheim (CERN), F. Huegging (Bonn)



Evolution of the DRD3 Collaboration

DRD3



132 institutes registered
537 people on the mailing list

https://drd3.web.cern.ch/institutes

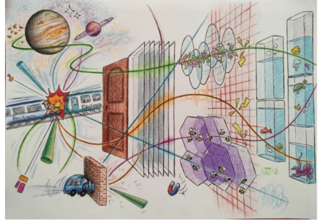
The DRD3 Collaboration has evolved a lot in the last year

A number of new Institutes joined

Structure of WGs is now more clear

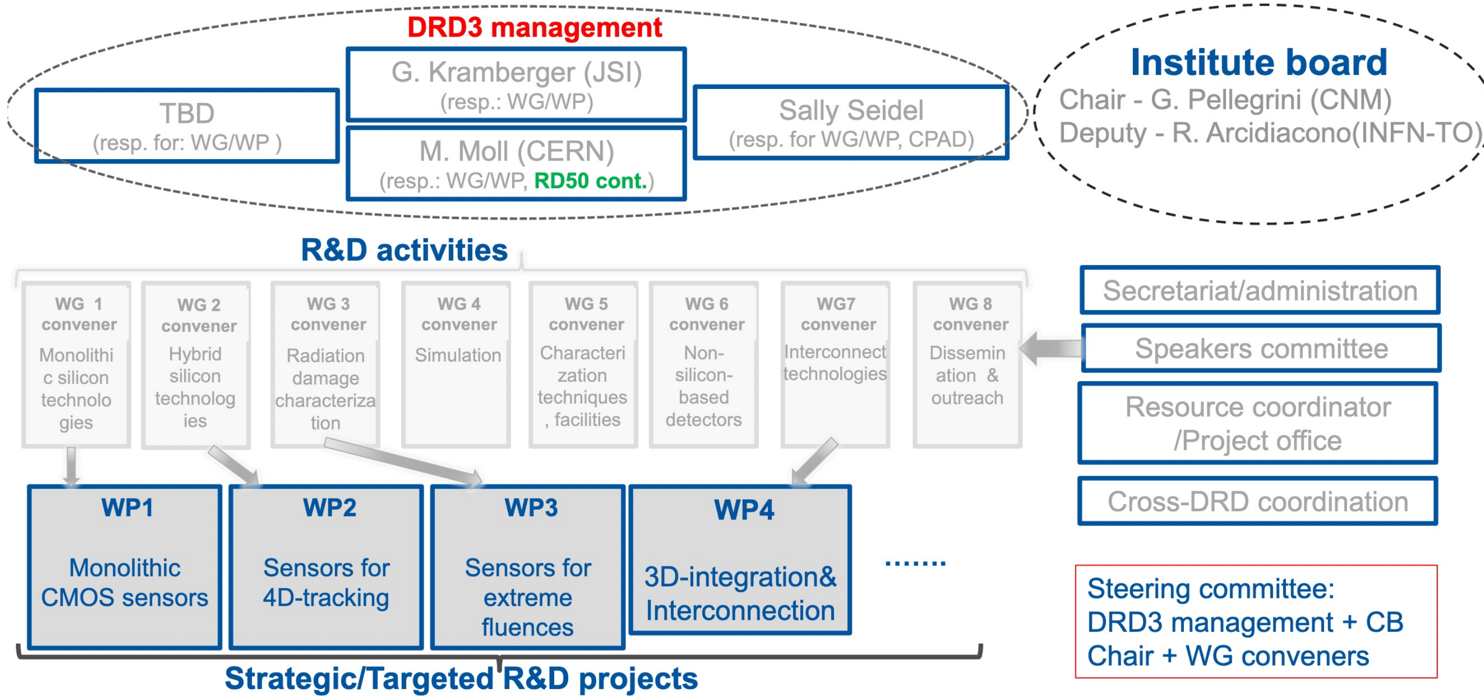
An Institute Board and Management Structure is in place

Progressing towards a DRDC approval



Evolution of the Collaboration

DRD3

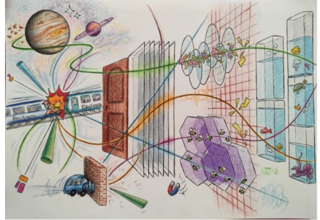


WG7 has a strong association with the Interconnection WP

The idea is to organize the activities as formal tasks inside the WP

Everybody interested in interconnections is welcome to deposit a EoI to allow us with the organisation

We will try to build aggregation of groups on a number of projects



WP4/WG7: Interconnections

DRD3

Interconnections are a strong point of future detector and electronics development

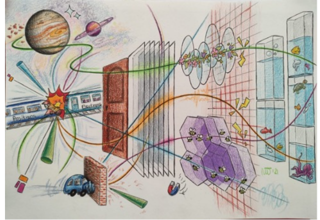
Gaseous	DRDT 1.1	Improve time and spatial resolution for gaseous detectors with long-term stability
	DRDT 1.2	Achieve tracking in gaseous detectors with dE/dx and dN/dx capability in large volumes with very low material budget and different read-out schemes
	DRDT 1.3	Develop environmentally friendly gaseous detectors for very large areas with high-rate capability
	DRDT 1.4	Achieve high sensitivity in both low and high-pressure TPCs
Liquid	DRDT 2.1	Develop readout technology to increase spatial and energy resolution for liquid detectors
	DRDT 2.2	Advance noise reduction in liquid detectors to lower signal energy thresholds
	DRDT 2.3	Improve the material properties of target and detector components in liquid detectors
	DRDT 2.4	Realise liquid detector technologies scalable for integration in large systems
Solid state	DRDT 3.1	Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
	DRDT 3.2	Develop solid state sensors with 4D-capabilities for tracking and calorimetry
	DRDT 3.3	Extend capabilities of solid state sensors to operate at extreme fluences
	DRDT 3.4	Develop full 3D-interconnection technologies for solid state devices in particle physics
PID and Photon	DRDT 4.1	Enhance the timing resolution and spectral range of photon detectors
	DRDT 4.2	Develop photosensors for extreme environments
	DRDT 4.3	Develop RICH and imaging detectors with low mass and high resolution timing
	DRDT 4.4	Develop compact high performance time-of-flight detectors
Quantum	DRDT 5.1	Promote the development of advanced quantum sensing technologies
	DRDT 5.2	Investigate and adapt state-of-the-art developments in quantum technologies to particle physics
	DRDT 5.3	Establish the necessary frameworks and mechanisms to allow exploration of emerging technologies
	DRDT 5.4	Develop and provide advanced enabling capabilities and infrastructure
Calorimetry	DRDT 6.1	Develop radiation-hard calorimeters with enhanced electromagnetic energy and timing resolution
	DRDT 6.2	Develop high-granular calorimeters with multi-dimensional readout for optimised use of particle flow methods
	DRDT 6.3	Develop calorimeters for extreme radiation, rate and pile-up environments
Electronics	DRDT 7.1	Advance technologies to deal with greatly increased data density
	DRDT 7.2	Develop technologies for increased intelligence on the detector
	DRDT 7.3	Develop technologies in support of 4D- and 5D-techniques
	DRDT 7.4	Develop novel technologies to cope with extreme environments and required longevity
	DRDT 7.5	Evaluate and adapt to emerging electronics and data processing technologies
Integration	DRDT 8.1	Develop novel magnet systems
	DRDT 8.2	Develop improved technologies and systems for cooling
	DRDT 8.3	Adapt novel materials to achieve ultralight, stable and high precision mechanical structures. Develop Machine Detector Interfaces.
	DRDT 8.4	Adapt and advance state-of-the-art systems in monitoring including environmental, radiation and beam aspects
Training	DCT 1	Establish and maintain a European coordinated programme for training in instrumentation
	DCT 2	Develop a master's degree programme in instrumentation

Solid state	DRDT 3.1	Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
	DRDT 3.2	Develop solid state sensors with 4D-capabilities for tracking and calorimetry
	DRDT 3.3	Extend capabilities of solid state sensors to operate at extreme fluences
	DRDT 3.4	Develop full 3D-interconnection technologies for solid state devices in particle physics

They have a critical role in the development of detectors and electronics

Sensor-FE, Tier to tier, multiple stacks

Interconnections for modules, interconnection for characterization



WP4/WG7: Interconnections

DRD3

Activity of the WP4/WG7 will be organized around axes (Research Goals)

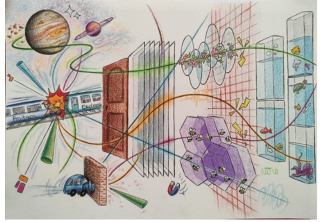
RG 7.1: Yield consolidation for fast interconnection technologies

RG 7.2: Demonstration of in-house process for single dies and pixel interconnections for a range of pitch (down to < 30 μm)

RG 7.3: Development of maskless post-processing for classical bumping interconnection technologies

RG 7.4: Development of wafer-to-wafer approach in presently advanced interconnection technologies

RG 7.5: Development of VIAS in multi-tier sensor/front-end assemblies



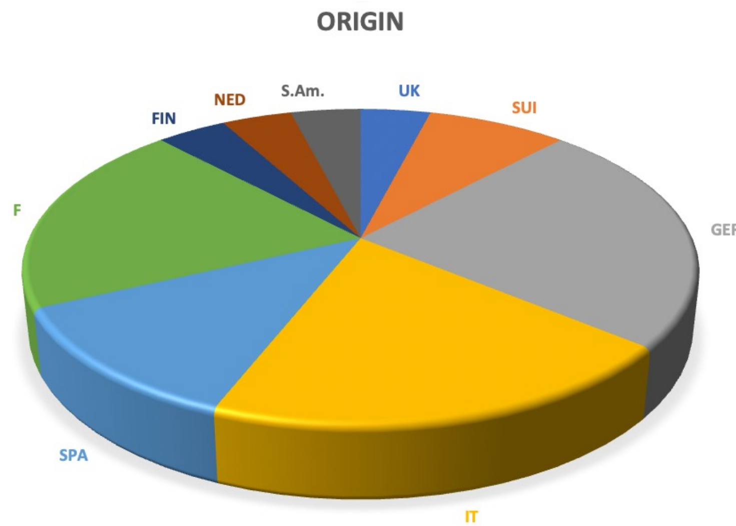
Interest in the community

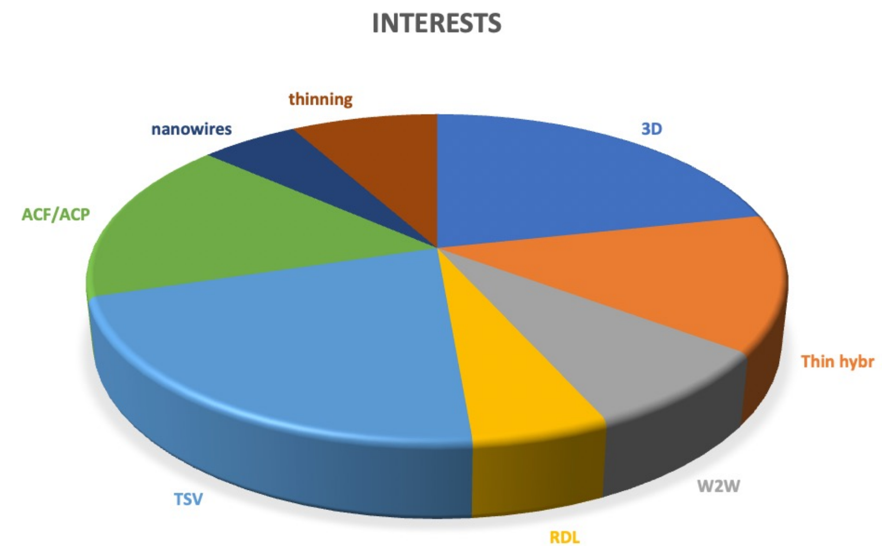
DRD3

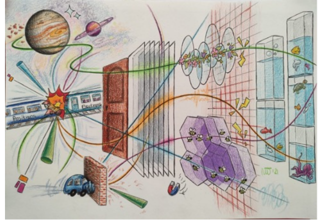
- New version of the EoI slides from institutes are still flowing in (on 16/5 we have 10)

- For reference: at the time of last year workshop:

- 35 groups / 85 questionnaires already interested and planning to have resources
- Among them 25 gave some specific information
- 15-20 FTE already declared







Strong interplay with DRD7

TSV, RDL -> 6 institutes
3D, direct wafer bonding -> 3 institutes
ACF/ACP -> 2 institutes

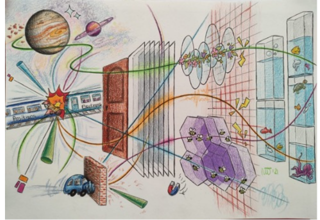
Statistics from interconnection interests inside the “Emerging technologies, DRD7.5”

Yes
No
35,3%
64,7%

17 answers

- CERN
- KIT and DESY
- FNAL
- UniBarcelona
- ITAINNOVA Instituto Tecnologico de Aragon)

ITAINNOVA
FNAL
CERN
UniBarcelona
DESY
KIT



Todays' session and June Collaboration Meeting

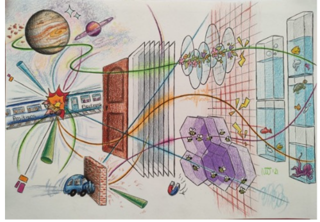
DRD3

Today:

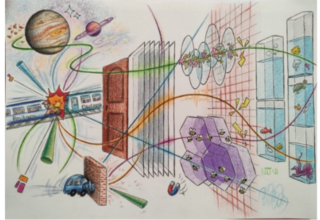
- Introduction and analysis of interests
- Quick overview of the main WP4 axes
  - Fast Interconnections for R&D
  - In-house interconnection technologies
  - Interconnection technologies via specialized vendors
- Discussion with present groups

Collaboration meeting: June 17-20th

- Thematic presentations centered on WP4 projects



Different stages and technology levels



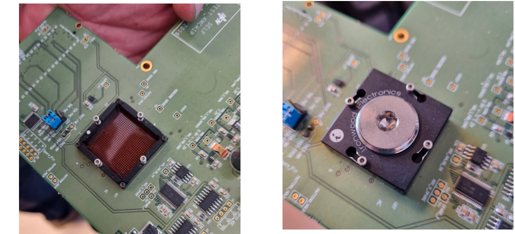
I – Maskless connections

DRD3

Testing and fast connections: not only to have a cheap way to test objects but also for fast prototyping

Application possible even for temporary connection

(Temporary connections already widely used in testing / characterization)



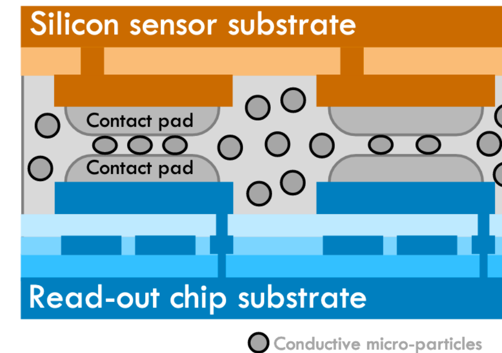
ATLAS AM chips test setup

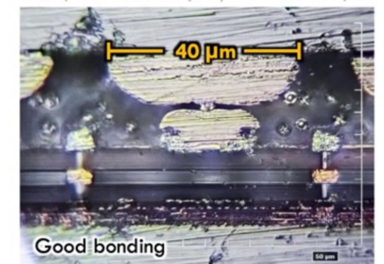
Permanent maskless connections (for example ACF/ACP)

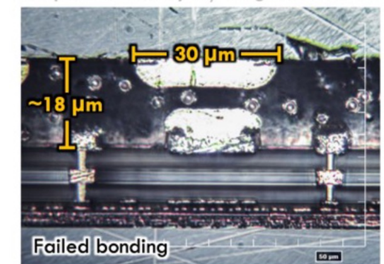
Maskless, in house technology for plating/interconnect

Allows for cheap interconnection
Quick turnaround time

- Wafer and device level connection
- Module to flex interconnections







Research goals:

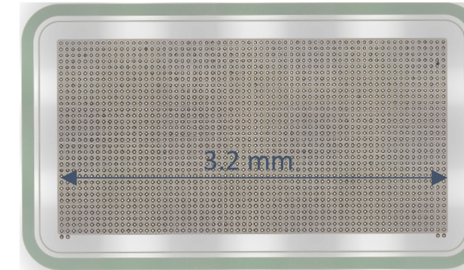
RG 7.1 Yield consolidation for fast interconnections
RG 7.2 Demonstration of in-house process for single dies and pixel interconnections for a range of pitches (down to < 30µm)
RG 7.3 Development of maskless post-processing for classical bump-like interconnection technologies

I – Maskless connections: status and plans

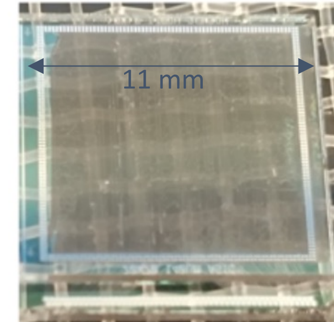
Recent progress by CERN EP R&D WP 1.3, Geneva Univ., Medipix, LPNHE Paris, FBK, ESRF, Univ. Pisa:

- Plating
  - Systematic optimisation of ENIG processing parameters
    → Uniform plating with ~10 µm ± 0.5 µm height down to 50 µm pitch
- Hybridisation
  - Proof-of-concept ACF hybrids with Timepix3, SPHIRD, ALTIROC3, TimeSpot
  - Confirmed low resistance of ACF/ACP micro-particle connections using FBK/LPNHE chain devices
- Module integration
  - Adhesion tests and module bonding with ACF, gold studs, nano wires for MALTA2 and test structures
  - Multi-module flex PCB produced; functional demonstrator with chip-to-chip data transfer for 4 MALTA
- Plans for EP R&D phase II (2024-2028) / DRD3
  - Further **exploration** of innovative interconnect + module-integration technologies
  - **Reliability testing** (thermal cycling, irradiations)
  - **Scalability** towards large-area applications, integration of **optical links**

ENIG plating on SPHIRD Si sensor

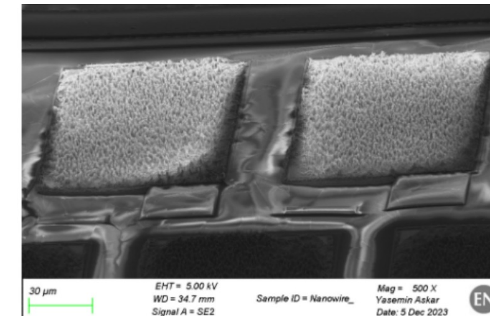


Chain device for resistance meas.

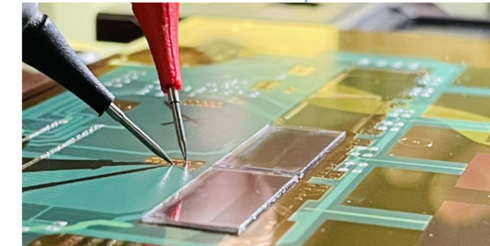


18 µm ACF – resistance measurement

Nano wires on MALTA2 pads



ACF-bonded 4-chip module



II - More advanced bumping / bonding interconnections

DRD3

Different technological level

This needs today RTO or industry

Vendors busy with upgrade productions

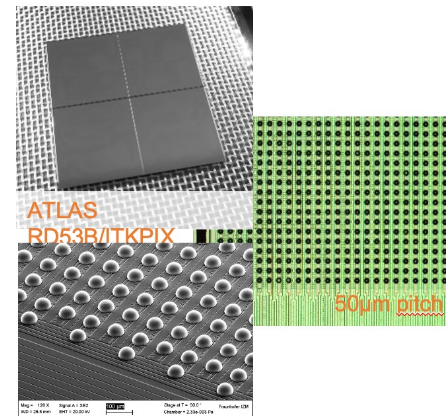
Move part of process to laboratories

Different features from different technologies can address specific complex issues

- small pitch
- process-temperature constraint
- electrical properties (current, C)
- connection flow (wafer-wafer, device-wafer)

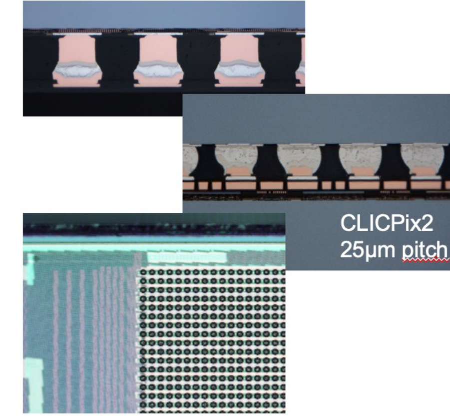
Examples of interconnection technologies provided by IZM

Fine pitch bumping



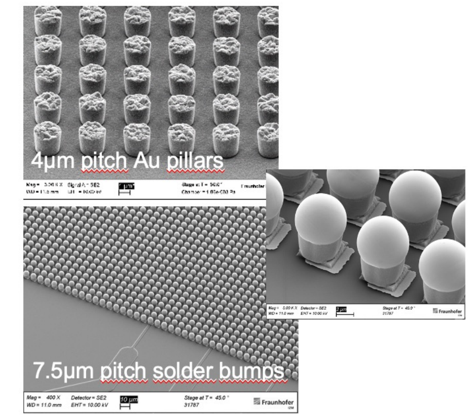
- Pitch 100…50µm
- Bump size: 50…25µm
- Material: Solder bumps, pillar bumps with solder cap

µ-bumping



- Pitch 50…20µm
- Bump size: 25…12µm
- Material: Solder bumps, pillar bumps

Sub-10µ-pitch



- Pitch 10…2 µm
- Bump size: 6…1µm
- Material: pillar bumps, metal pins

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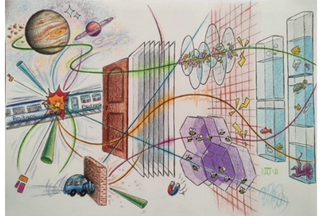
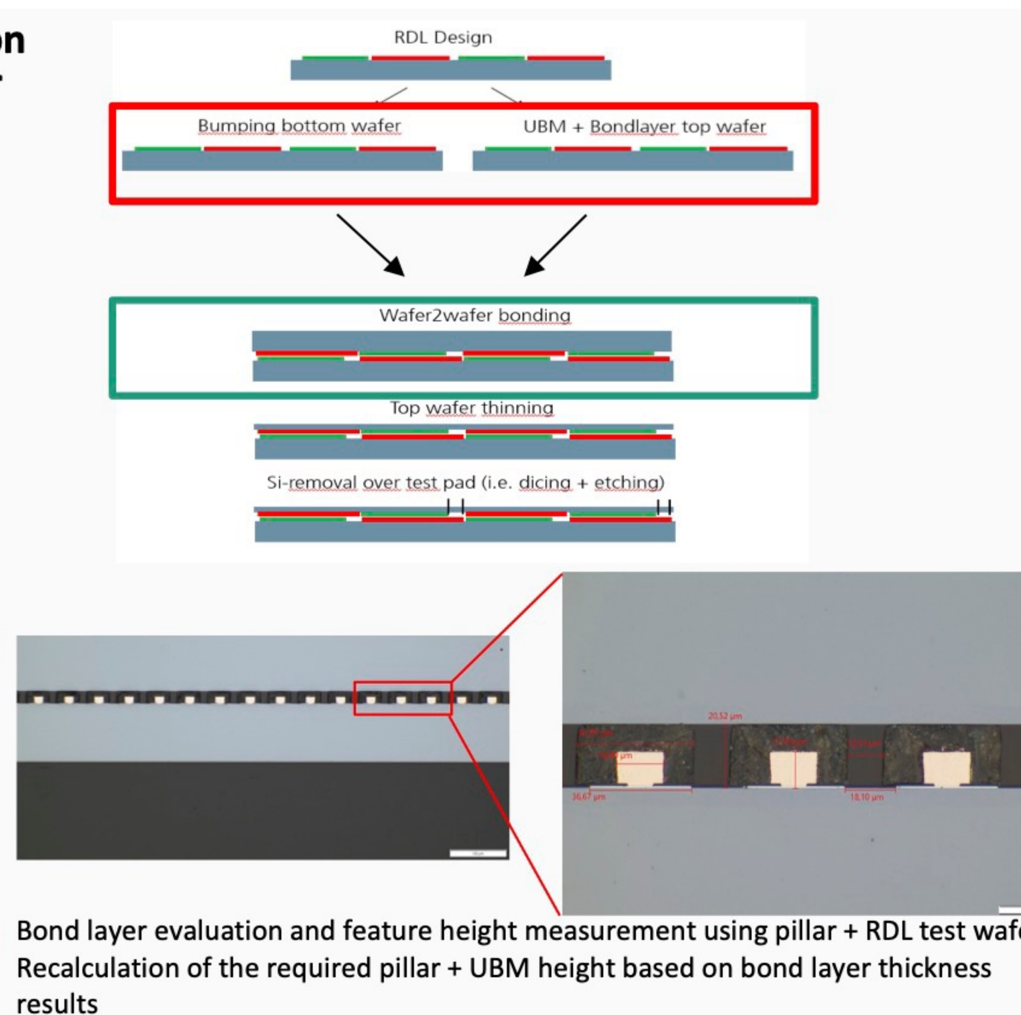


II - W2W BONDING PROCESS DEVELOPMENT

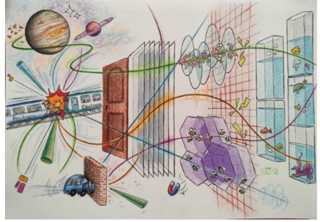
DRD3

Recent work at Bonn University in collaboration with IZM

- **WP1: Design development and manufacturing of process qualification wafer, design preparation of functional TIMEPIX3 and DMAPS sensor wafer**
  - 1.1 Definition of technological approach for ultra-thin low-mass hybrid pixel detectors
  - 1.2 Process qualification design including test structures
  - 1.3 Fabrication of process development wafer
  - 1.4 Design and mask preparation for TIMEPIX3 readout electronics and DMAPS active sensor wafer
- **WP2: Wafer bonding and thinning process**
  - Bonding material evaluation and process
- **WP3: Wafer bonding with capacitive coupled IOs and conductive IOs**
- **WP4: Backside wafer process with TSV-etching and backside metallisation process**
- **Next steps:**
  - Processing of daisy chain test layout setup wafer
  - Evaluation of full process chain (bonding, thinning, silicon etching)
  - Electrical conductivity test of daisy chain test structures



Bond layer evaluation and feature height measurement using pillar + RDL test wafe
Recalculation of the required pillar + UBM height based on bond layer thickness results



III - 3D and vertical integration

DRD3

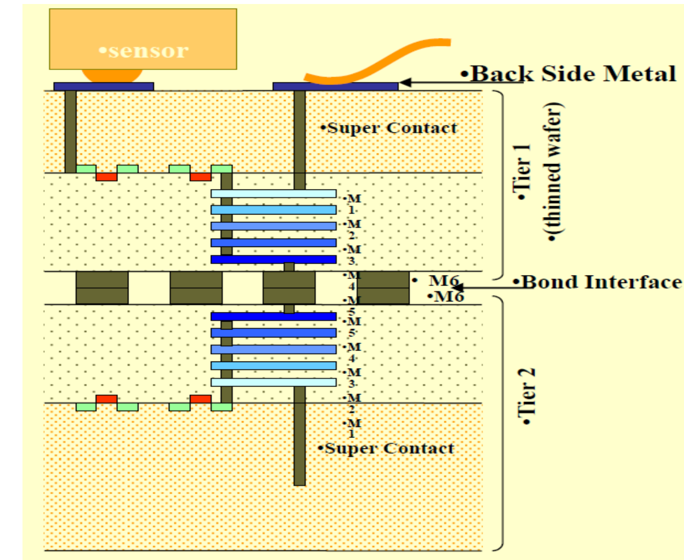
Via industry
it will profit of commercial drive

Stack to match digital/analog
many reasons to do so

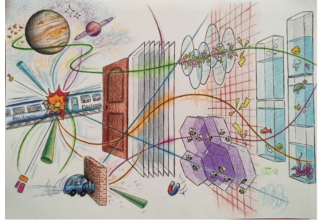
Could allow complex communication between different connected devices

Allow to contact/power/read a lower layer through an upper one

Multi-tier, mixed-technology



This is at the interface with DRD7: institutes/groups interested?



Wrap-up

DRD3

Interconnections are essential point of all hybrid sensor-FE technologies

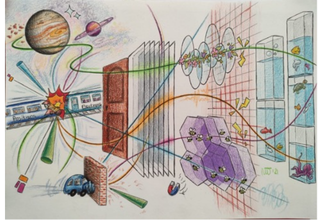
Different levels:

- Cheap temporary (for test) or permanent connections
- Fast connections for prototyping: short turn-around
- More advanced - partially in-house - process to address specific constraints (small pitch, temperature)
- Complex interconnection process via RTOs/industries

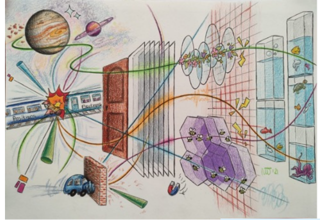
For monolithic technologies, interconnections are necessary for multi-tier extensions. Here, important applications also for module-to-flex interconnections

Strong link with electronics (DRD7): importance of interface definition

Groups interested in the above activities should work proactively to help us to build up the WP4 collaborative projects in view of the June DRD3 Collaboration Meeting



DRD3



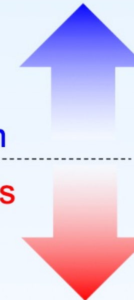
Strong interplay with DRD7

3D integration & high density interc. (5)

ECFA European Committee for Future Accelerators | DRDT 7.5 Emerging Technologies

Please describe the topics you (and/or your group) would like to participate in?

- Integration of single photon sensor and readout chip (*UniBarcelona*)
- Characterisation of 3D stacks, with focus on irradiation studies (*CERN*)
- Power consumption, heat, combine analogue, digital and photonic functions (*CERN*,



Test and characterization

Developments of TSV, TGV, RDL and 3D ICs

- Edgeless IC design (*FNAL, KIT*)
- High-density integration sensor, electronic & photonic ICs (*KIT, DESY*)
- 3D integration of silicon photonics and Electronic IC using TGV and TSV (*CERN, KIT*)
- Development of detector modules concepts for 3D stacked MAPS with redistribution layers (*CERN*)
- Design and prototyping of chip/sensor/interconnect assemblies focusing on low mass, powering, heat dissipation, signal integrity, and electromagnetic compatibility (EMC) (*ITTAINOVA*)
- 3D Tools for LVS and DRC; partitioning of functions across layer stack (*FNAL*)

ECFA DRDT 7.5 Kick-off 13