Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

CaR Board v1.5

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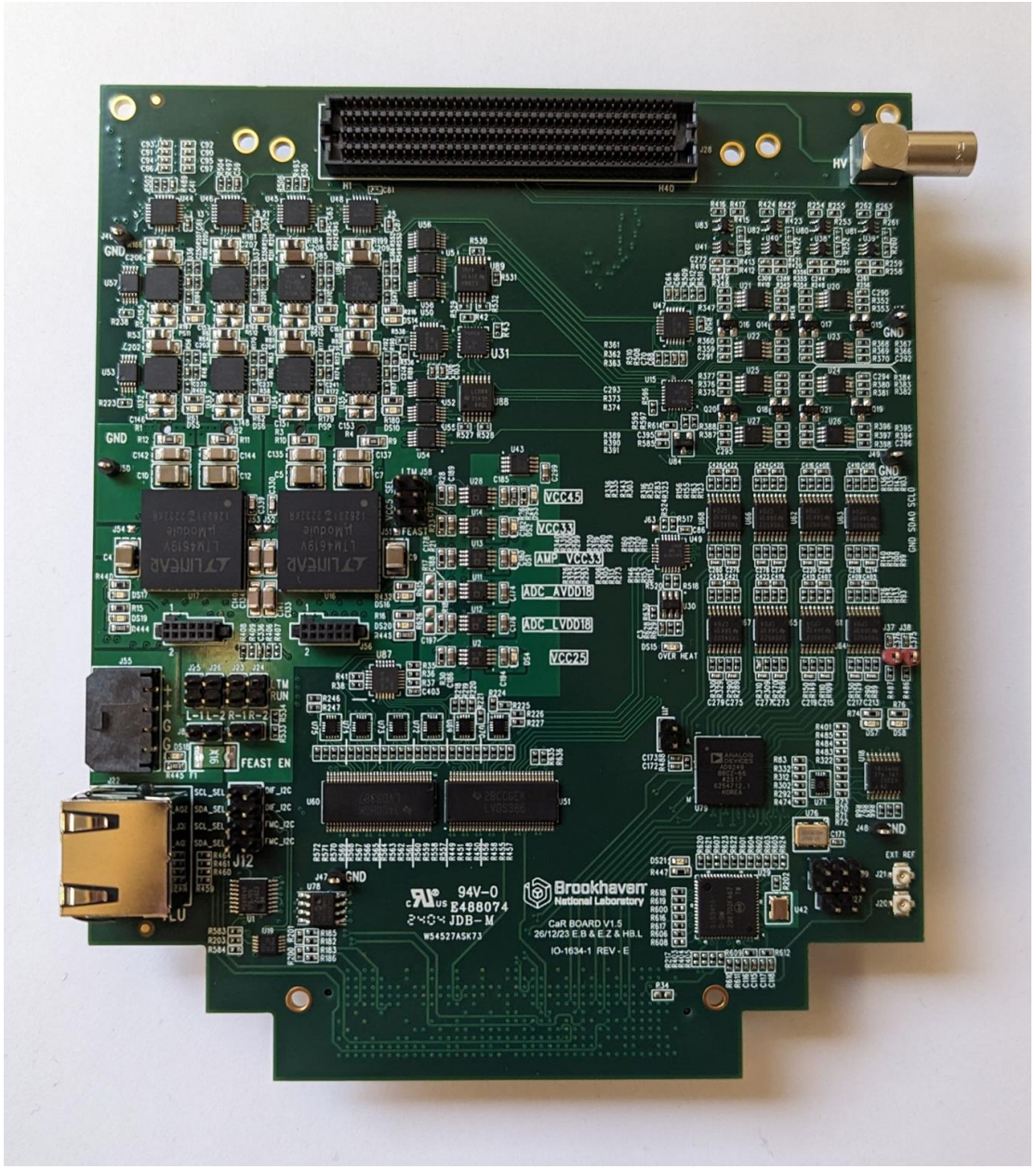
Carboard V1.5

- Slightly updated version of V1.4 to replace obsolete parts and fix a few minor issues
- Interim solution before V2 is ready
- Have 5 boards assembled
- 1 shipped to CERN and 1 to Fermilab

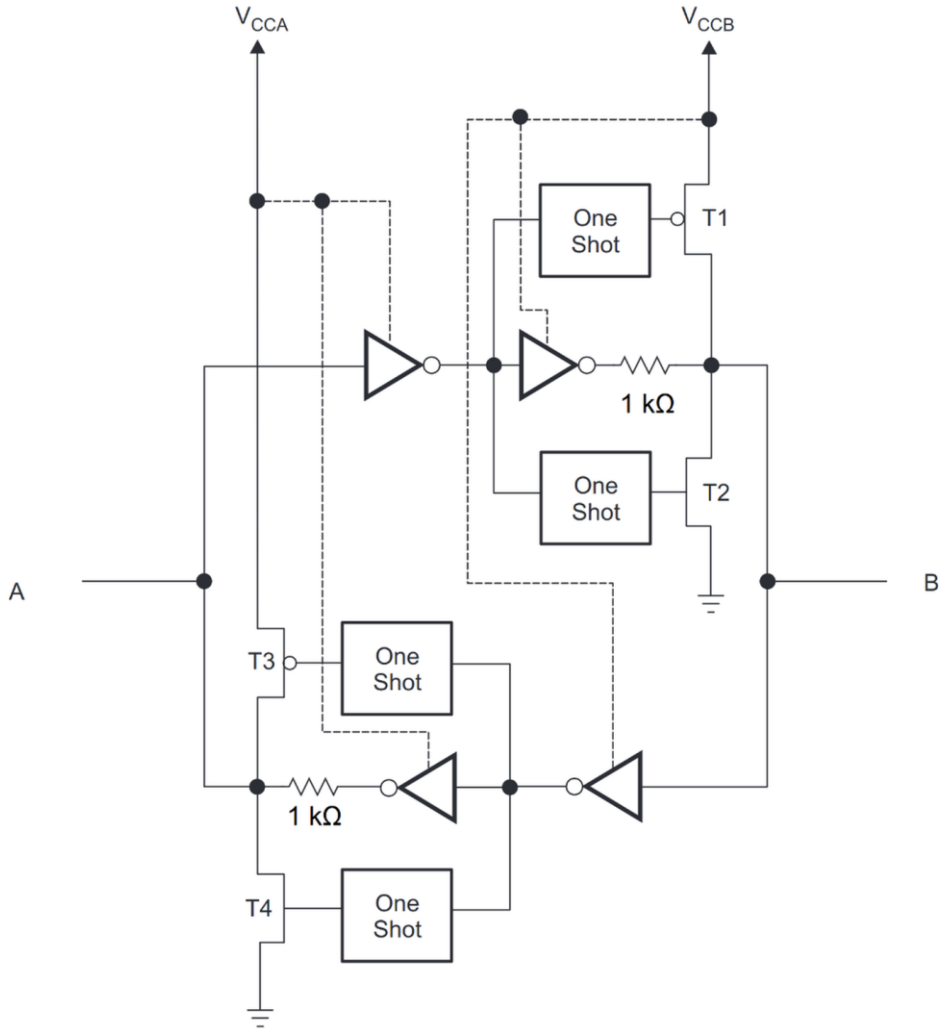


Changes from V1.4

- Replaced obsolete I2C to SPI bridge
- Replaced level shifters for CMOS I/O
- Changed 2 resistors to set identical gain on all ADC channels
- Reconnected power rails on U89 which got disconnected in V1.4
- Reconnected enable pin on U51
- Inverted polarity of overheat LED
- Misc cleanup of layout and schematic

Level Shifters

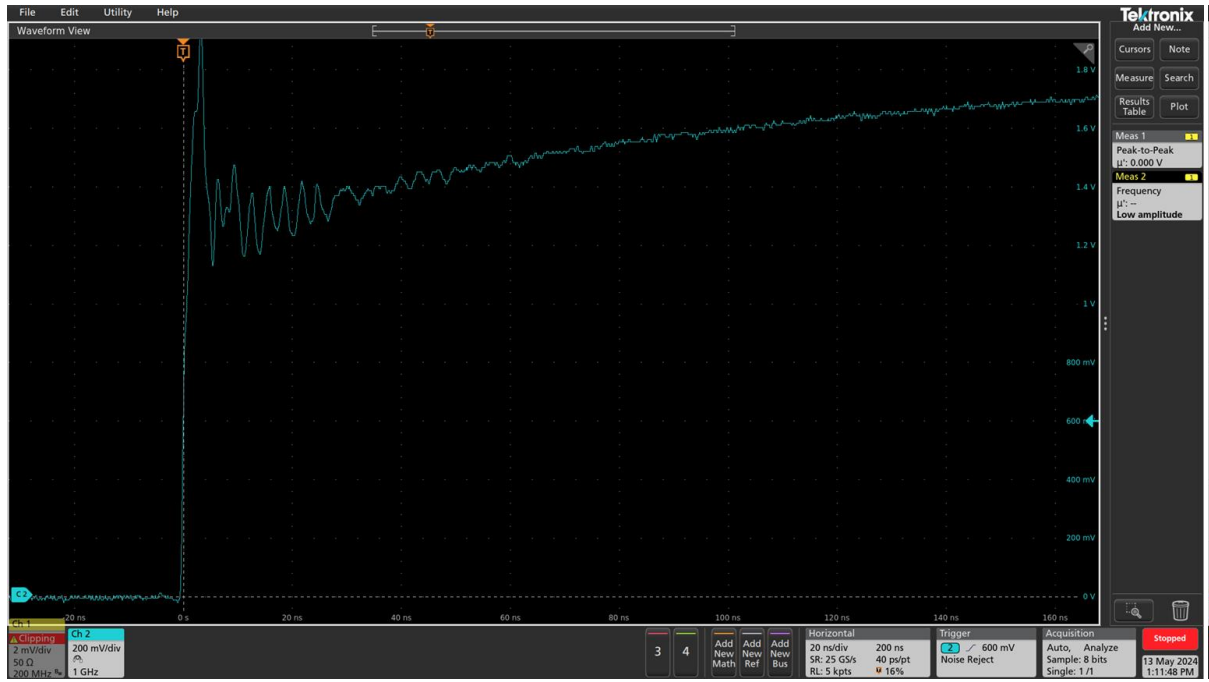
- Bidirectional level shifters for CMOS signals on V1.4 cause distortions and ringing, especially when driving long cables
- Replaced bidirectional TXB0304 with unidirectional 74AVCT245GU and added series termination
- Not yet tested with long FMC cable



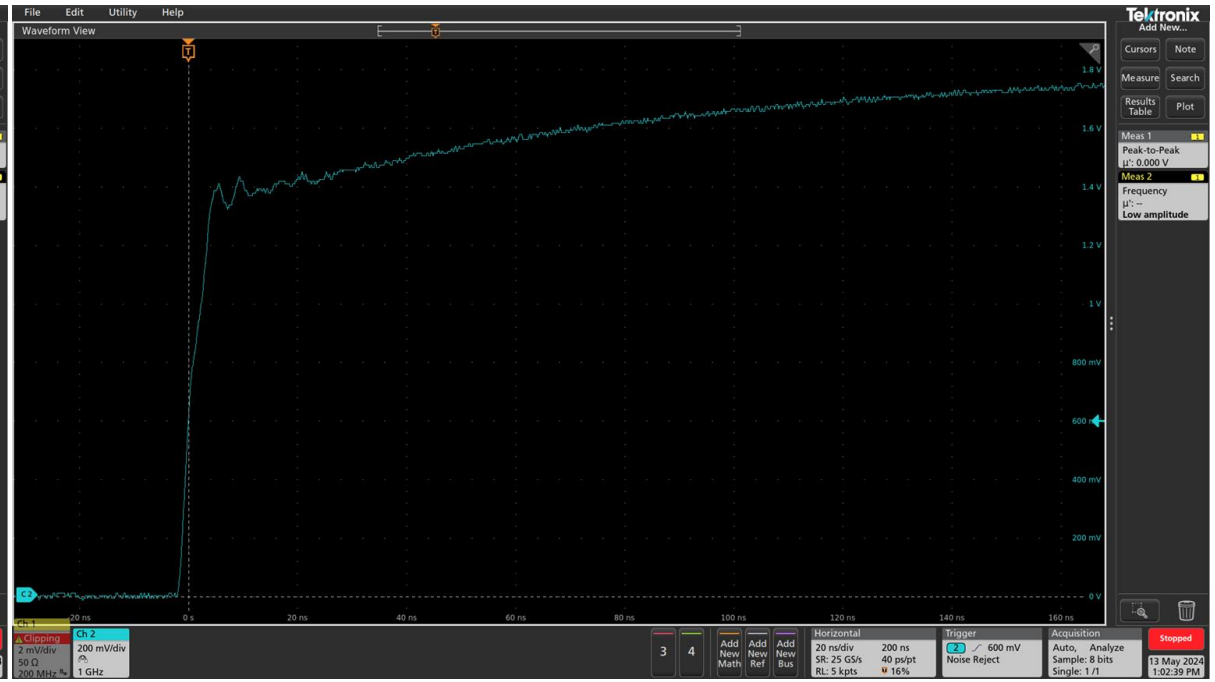
Testing: Level Shifters

Rising edge, breakout board without cable:

V1.3



V1.5



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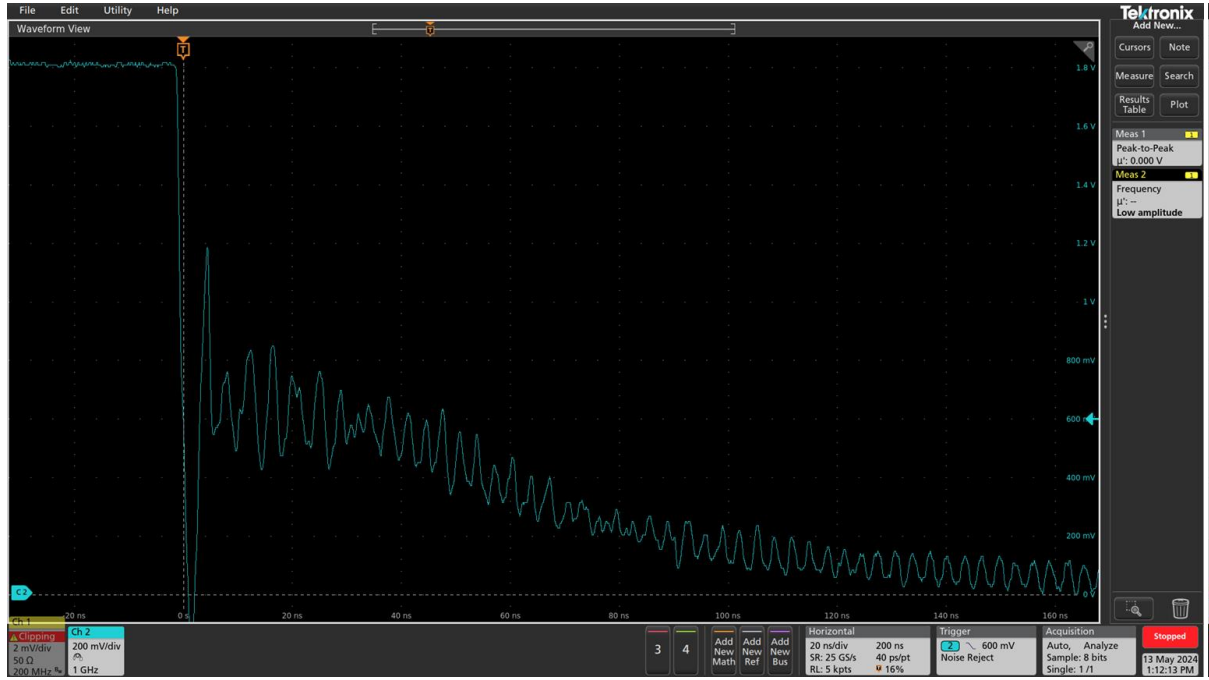
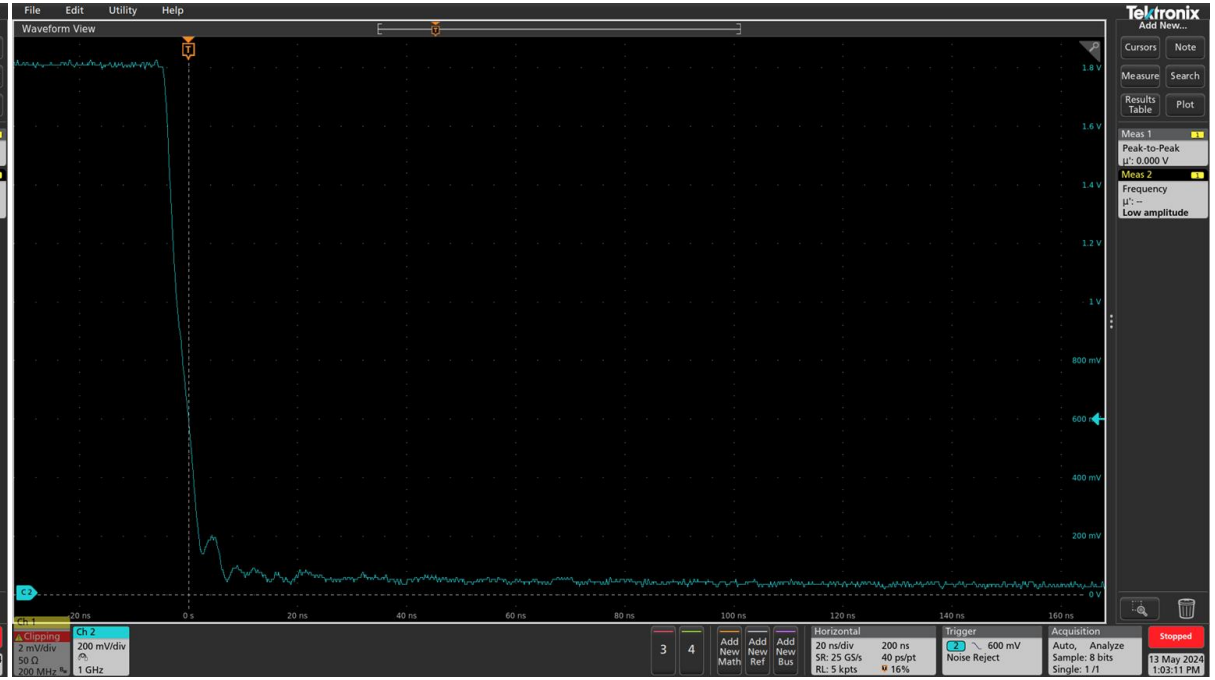
Testing: Level Shifters

Falling edge, breakout board without cable:

V1.3



V1.5



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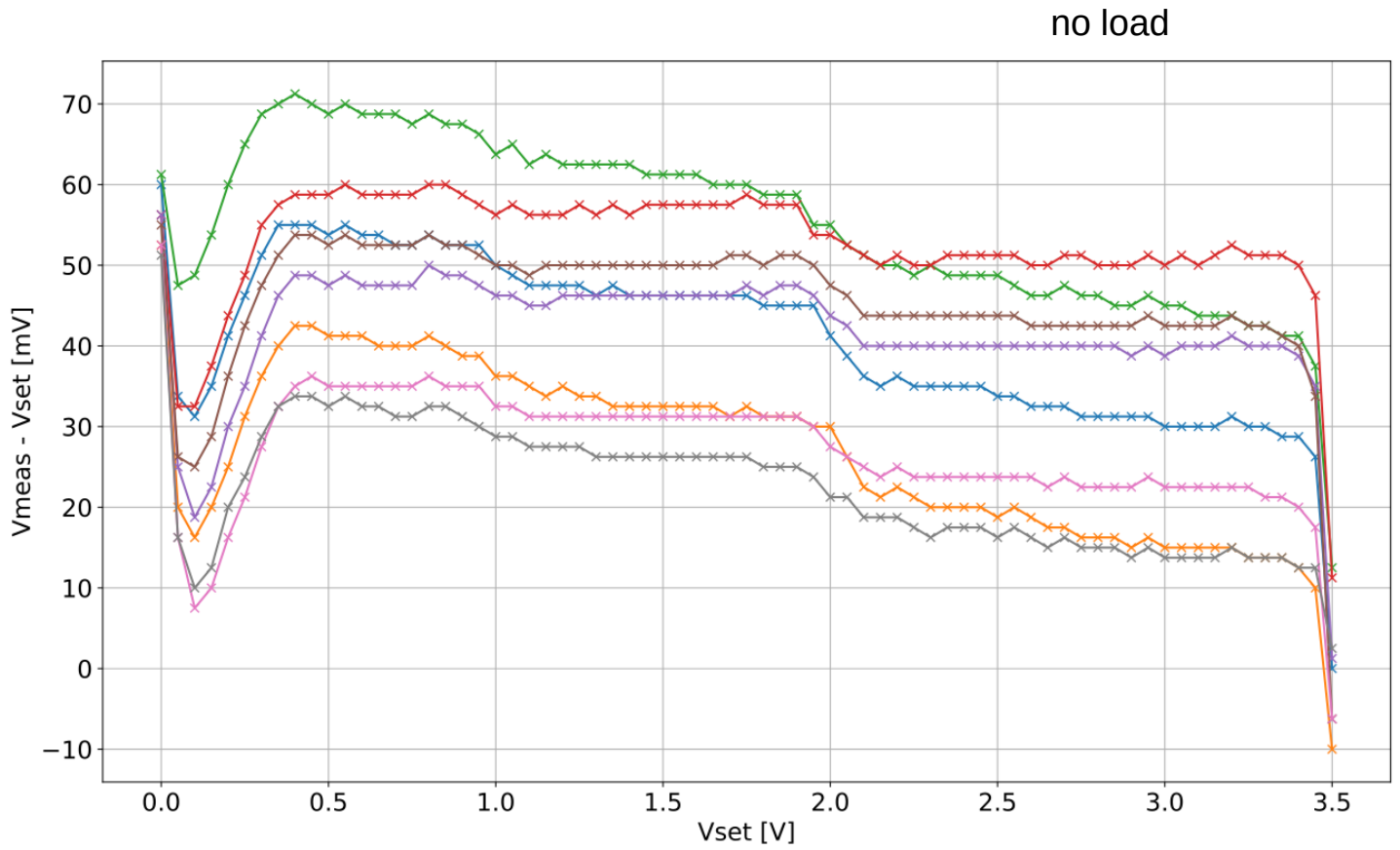
Testing: Power Supplies

- Testing the 8 adjustable power supply channels
- Measured voltage is 30mV - 60mV above set voltage
- Mostly linear between 0.5V and 3.4V
- Found error in current monitoring for negative values



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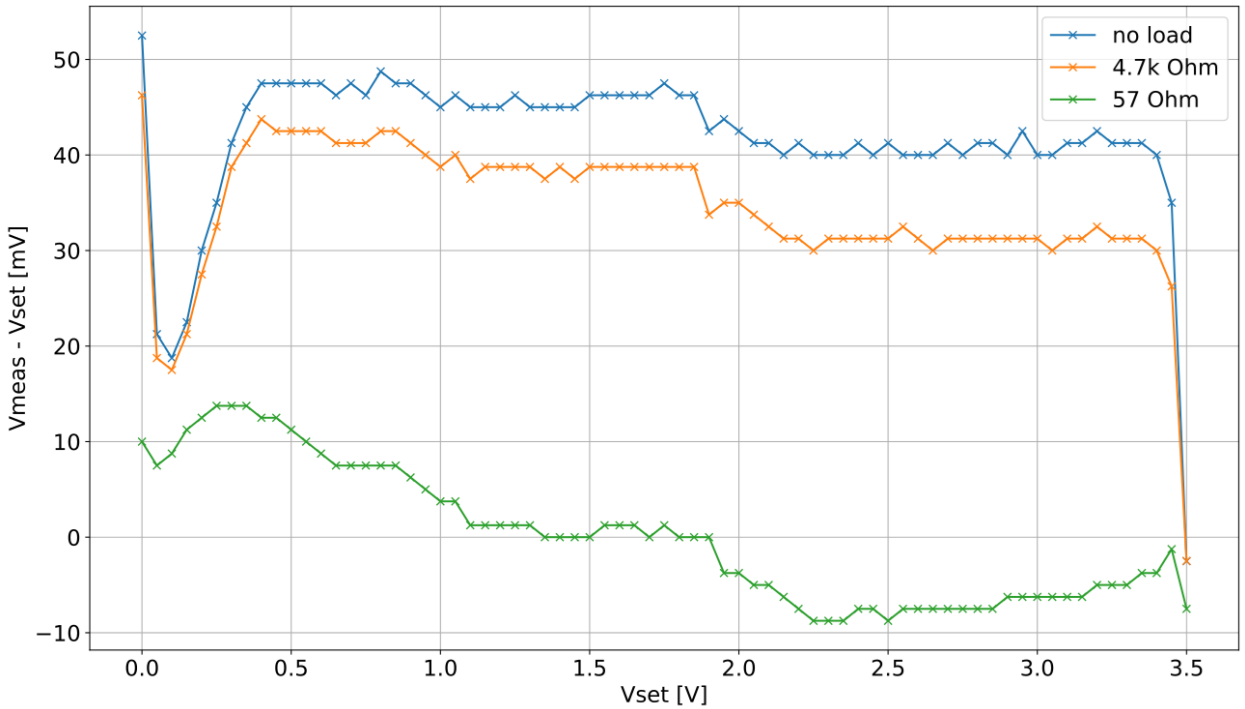
Testing: Power Supplies

- Deviation seems to be caused by load regulation of TPS74401 at low currents
- Improves with higher load

Board 2 channel 1



$\Delta V_{OUT(\Delta IOUT)}$ Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA	0.013	%/mA
	50 mA ≤ I_{OUT} ≤ 3.0 A	0.03	%/A

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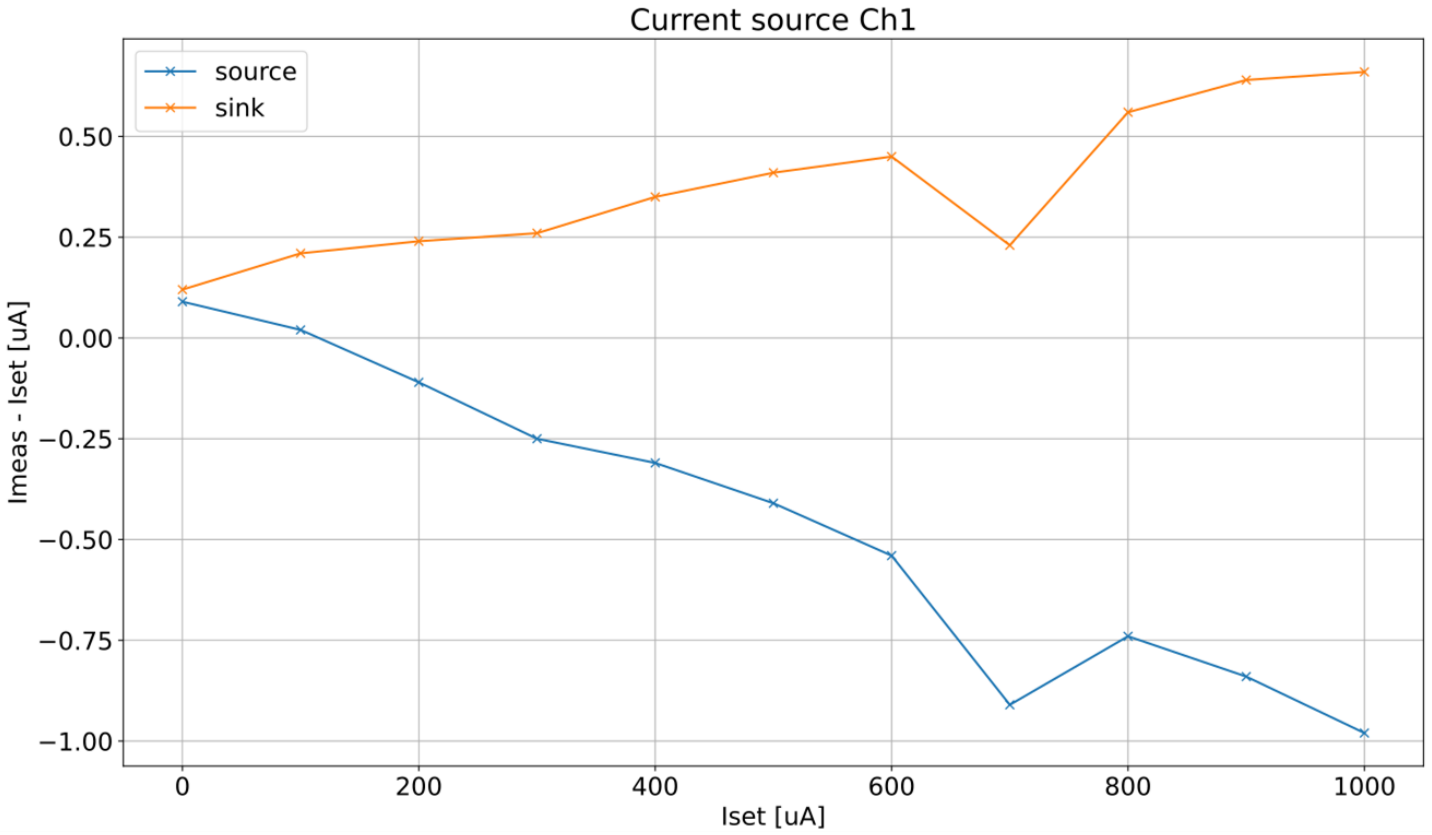
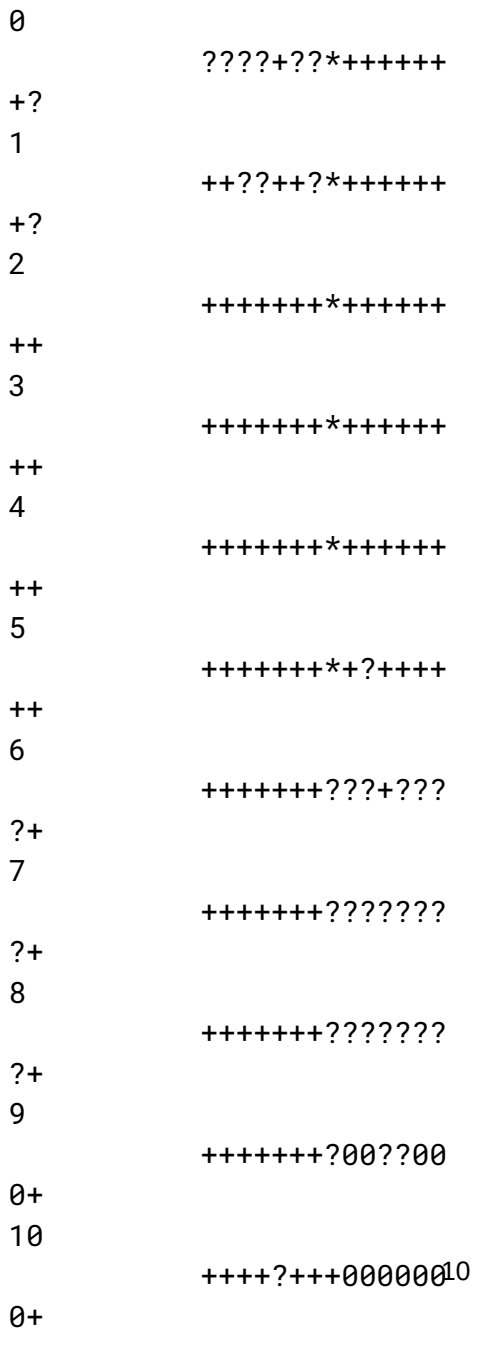
Testing: Current Sources

- Found error in calculation: currents were off by a factor of 1.024
- Mostly linear with a dip at 700uA
- Gain error of about 0.5uA/mA (sink) and 1uA/mA (source)
- Not tested more channels yet, resistors in current source are only 1%



Testing: 16 Ch ADC AD9249

- Replaced obsolete I2C to SPI bridge SC18IS602B with SC18IS606
- Used for SPI interface on AD9249 ADC
- Software compatible but has different pinout
- Testing SPI communication and receivers on FPGA by doing a phase scan:
  - ADC is configured to send test pattern, received data is checked for different phase settings
  - Works as expected, very similar results to V1.4



Conclusions

- Updated V1.4 to fix (most of the) known issues
- Tested the first 3 boards and verified the changes
- A few peculiarities (i.e. power supplies) remain, which will be addressed in the development of the V2 CaR board