ASIC developments for the AMBER MM experiment

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AMBER collaboration

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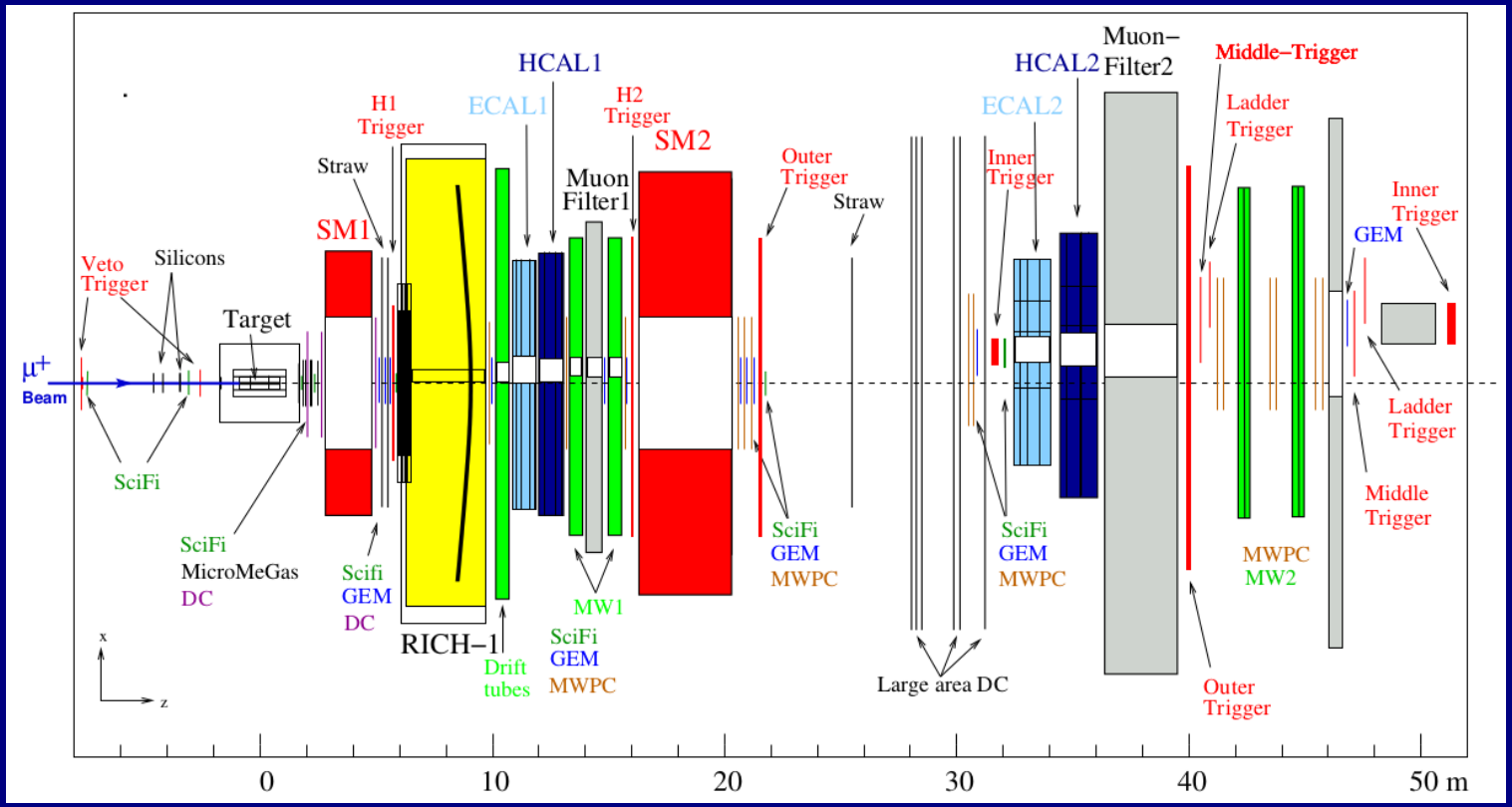
AMBER MM ASIC project

- New development for the MicroMegas detector of the AMBER experiment
- Possibly compatible also with straw detectors
- Moderate timing resolution (1-2 ns or better)
- Analog Front-End : custom development
  - inspired to VMM[(1)] and Tiger[(2)] designs
- Back-end : same as the ToASt ASIC[(3)]
  - silicon proven
  - save time in terms of design and test set-up development

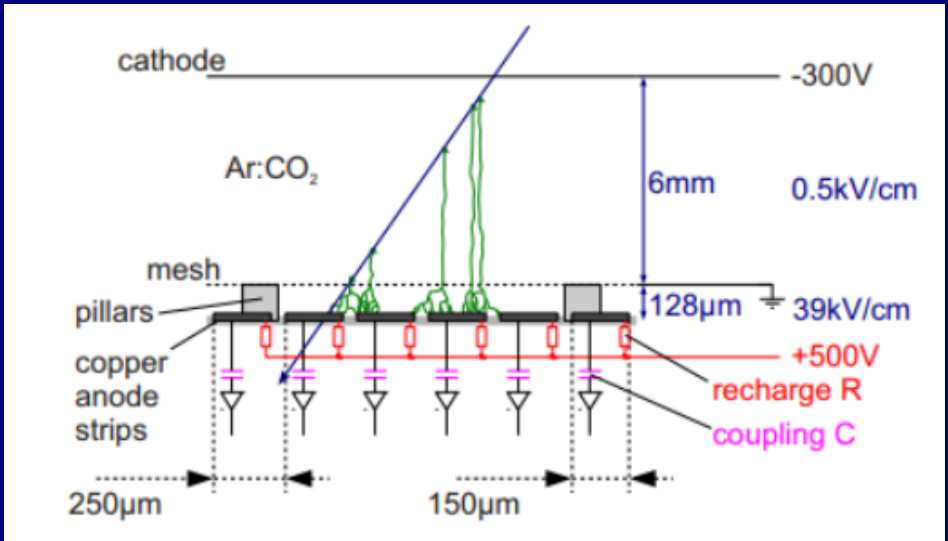
[(1)] *G.De Geronimo et al.*, The VMM3a ASIC,
IEEE Trans. Nucl. Sci., vol. 69, no. 4, Apr. 2022
[(2)] *A.Rivetti et al.*, TIGER: A front-end ASIC for timing and energy measurements with radiation detectors,
Nucl. Instrum. Meth., A 924, pp. 181-186, 2016
[(3)] *G.Mazza et al.*, A 64 channels ASIC for the readout of the silicon strip detectors of the PANDA micro-vertex detector,
J. Instrum., vol. 18, C01020, Jan. 2023

AMBER experiment



- COMPASS spectrometer as starting point
- Several detectors being upgraded
- New detectors added
- 3 MWPC stations will be replaced with Micro-Mega detectors → new design
- MM under development

AMBER MM



First prototype

- Active area: 6.8×6.8 cm^2
- Amplification gap: 128 μm
- Conversion gap: $\sim$5 mm
- Strips width: 400 μm
- Pitch: 550 μm
- Holes: 45×45 μm^2
- Wires diameter: 18 μm

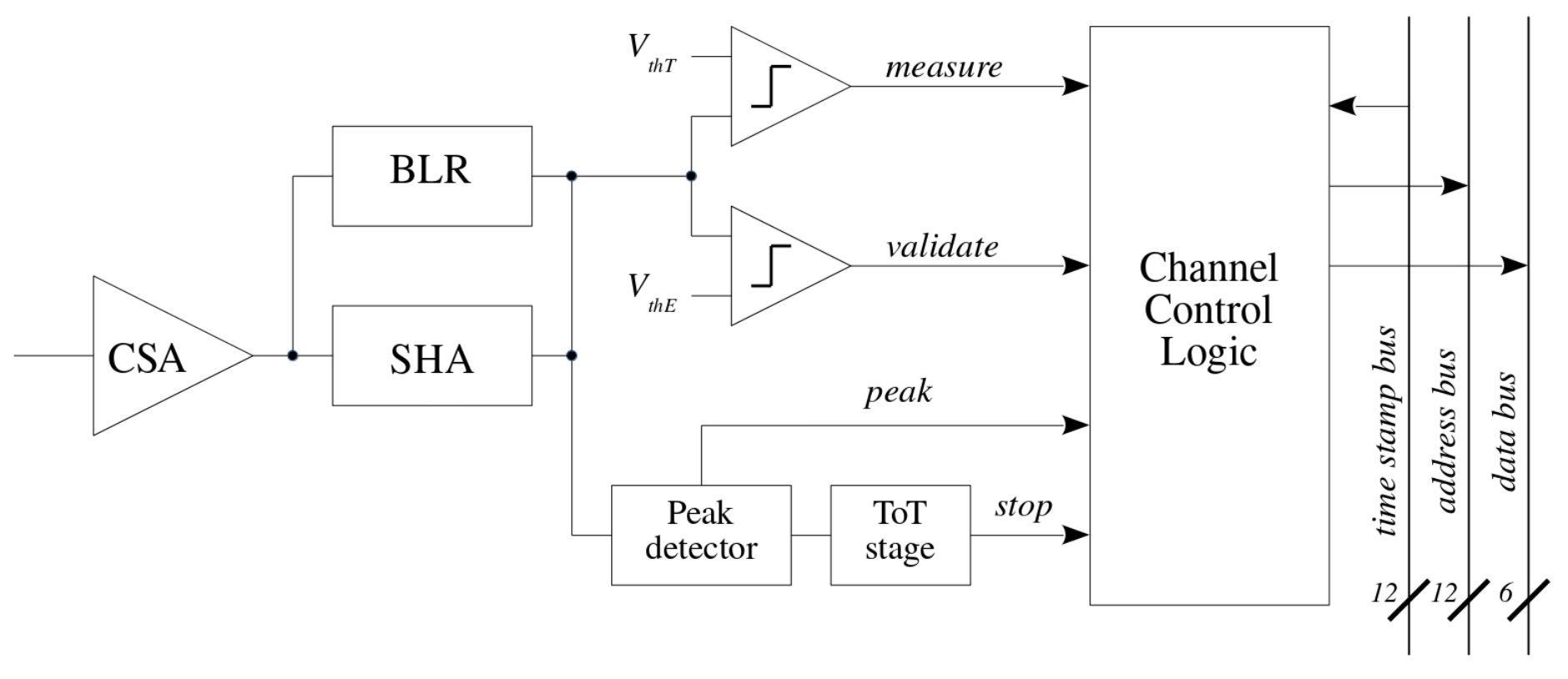
...work in progress...

Note : detector and ASIC developments have to go in parallel

Specifications

Detector	MM	Straw	
Channels/ASIC	64	64	
Power/channel	$\leq$5	$\leq$10	mW
Input capacitance	$\leq$150	20-100	pF
Input charge	1-100	1-1000	fC
Input impedance	*tbd*	*tbd*	Ω
Max rate	$\leq$2	$\leq$0.18	MHz
Peaking time	150	75-150	ns
Time resolution	1-2	$\leq$1	ns
Charge resolution	*tbd*	10	bits
Gain	10	1	mV/fC
ENC @10 pF	500-1000		e^-
ENC @150 pF	1000-2000		e^-
ENC @60 pF		3000	e^-
Threshold range	*tbd*	0-15	fC
Clock frequency	200	200	MHz

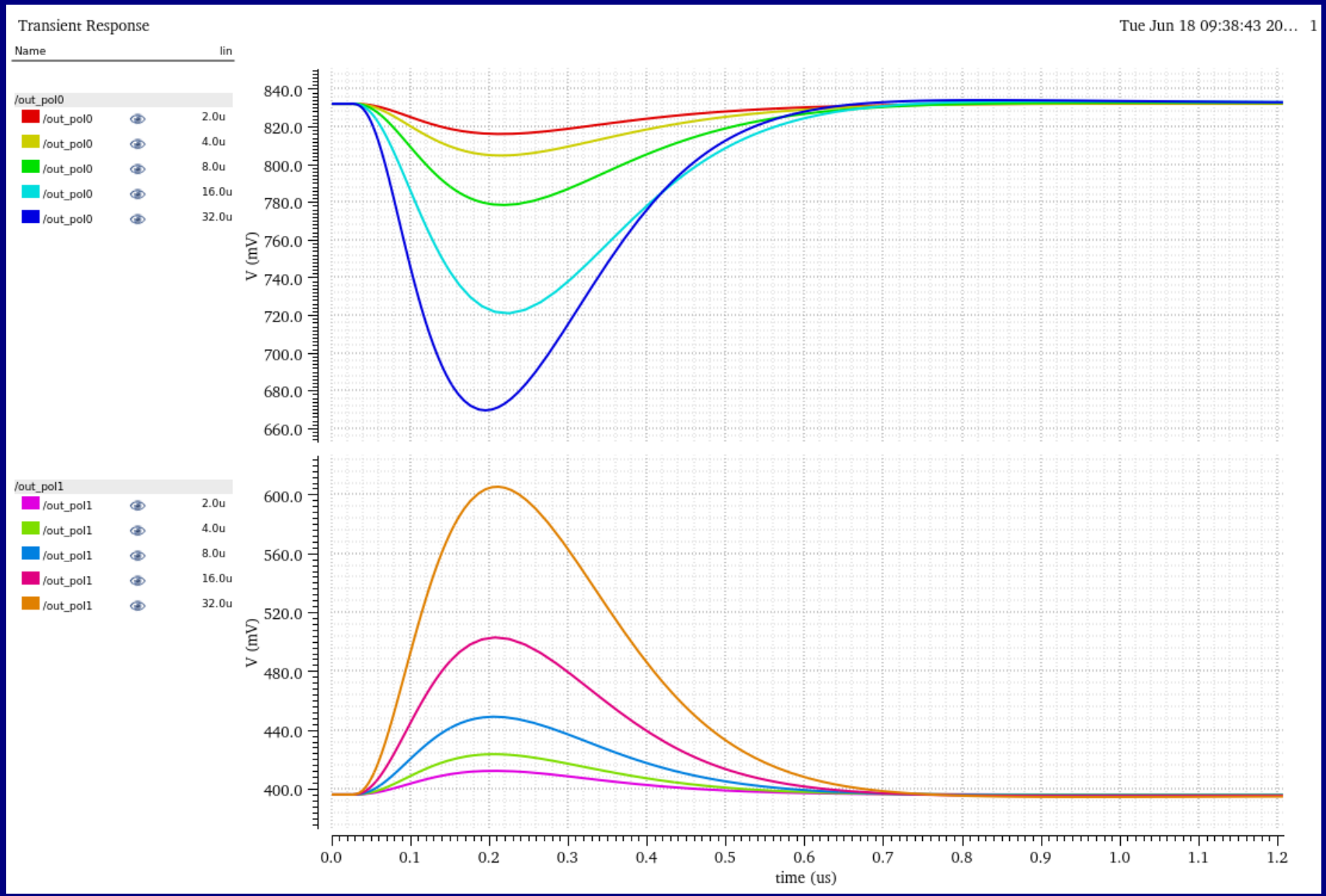
Analog channel architecture



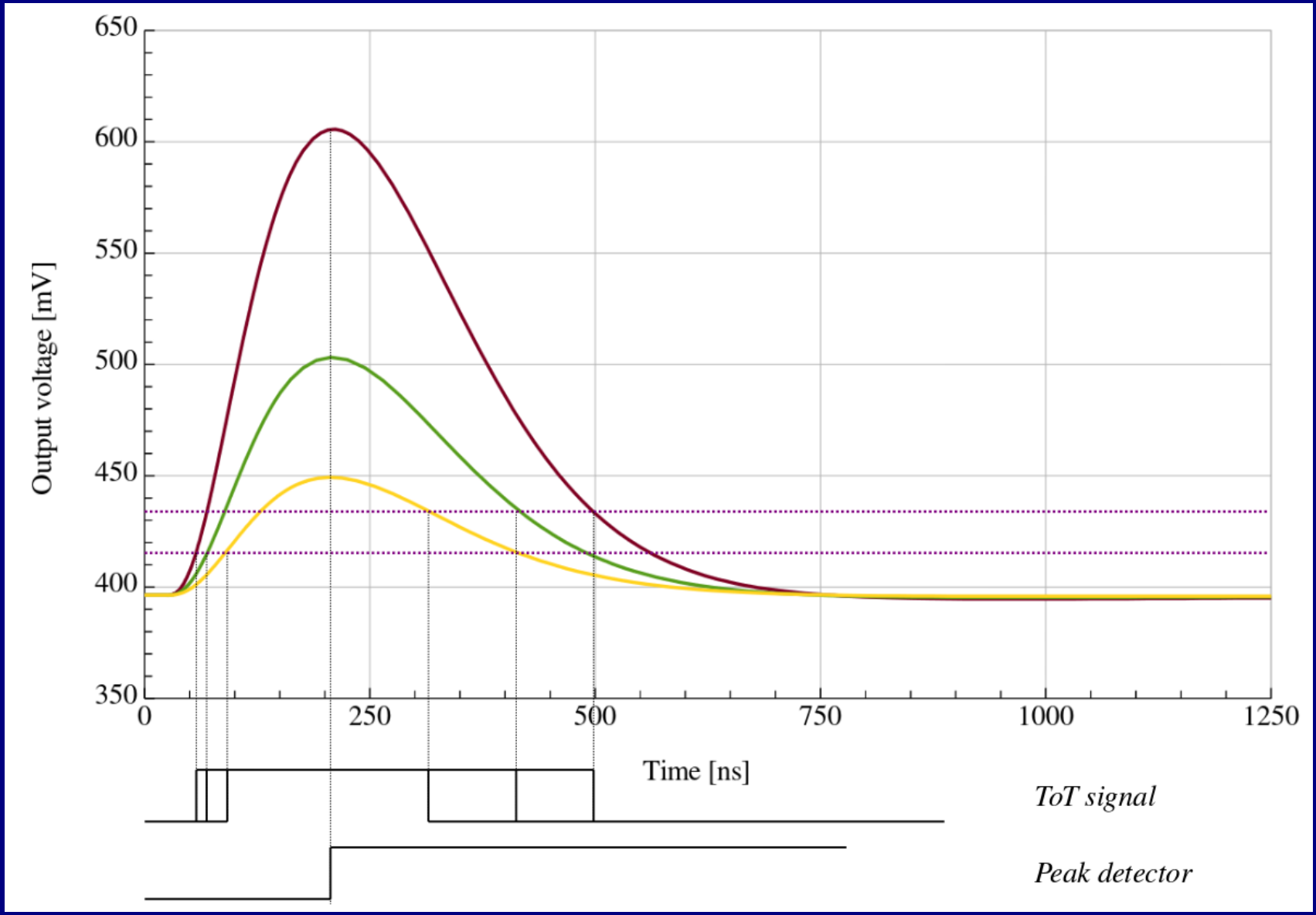
Analog front-end

- Charge Sensitive Amplifier
  - Two gains : 1 and 10 mV/fC
  - Possibility to accept inputs from both polarities
- Shaper
  - 3^{rd} order, one real and two cc poles
  - Programmable peaking time
- Double threshold signal detection
  - Lower threshold for time measurement, higher threshold for validation
- Peak detector signal
- Peak holder for charge measurement (via ToT)
- Linear ToT measurement under evaluation

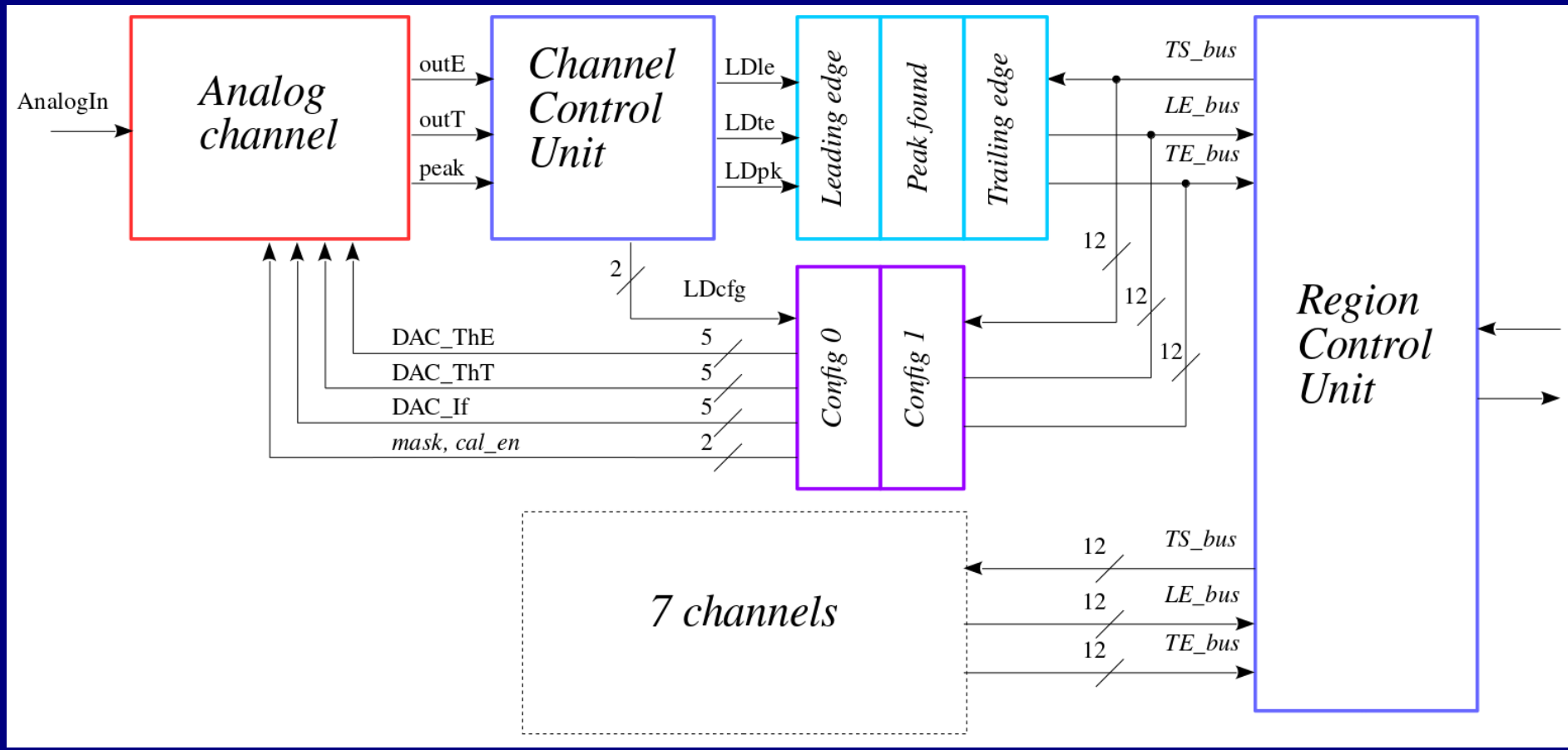
CSA+Shaper simulations



Signal detection



Full channel architecture

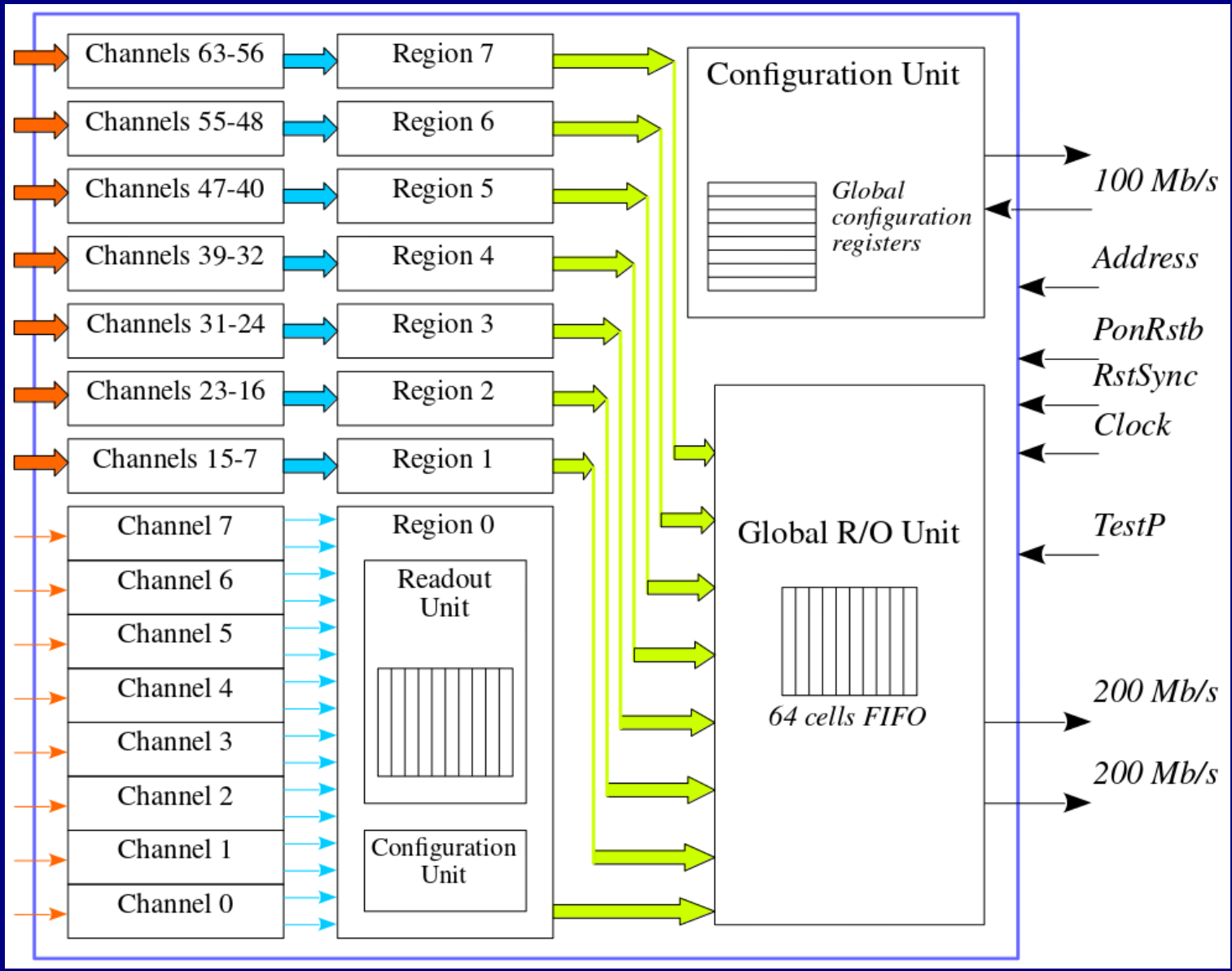


- Common time stamp distributed to all channels
- 3 data register for time acquisition
- 2 configuration registers
- Threshold and discharge current fine tuning

Time measurement

- Time resolution set by clock frequency
  - 200 MHz $\rightarrow$ 1.44 ns r.m.s.
- ToT-based charge measurement for time walk correction
- Option for second version
  - Channel or region-level 8-tap delay line
  - Delay controlled by a global DLL
  - Time resolution 180 ps r.m.s.
- Studies ongoing real signals
  - Problem of multiple ionization
  - Detector-FE co-design

ASIC architecture



Readout scheme

- Event driven (no trigger)
- Time of arrival order is different from time of readout
- Events are divided in frames
  - Frame duration : full cycle of the time-stamp counter
  - Event readout order does not correspond to event time of arrival
  - Events in a given time frame are not time-ordered
  - Events belonging to the same time-stamp counter cycle are transmitted in the same frame
- Continuous data transmission *(sync words when no data available)*

Output data format

- Data output in 32 bits words over 200 Mb/s serial links
- It can be configured to use 1 or 2 links
- Frame lenght : 20.48 μs at 200 MHz
- Data within a frame are packed within a frame header and a frame trailer
- Frame header contains chip id and frame number
- Frame trailers contains the number of valid samples and CRC

Packet type	Header 1 *1 bit*	Header 2 *3 bit*	Data *28/31 bits*
Header	1	010	ChipId[6:0] Reserved[12:0] FrameN[7:0]
Trailer	1	101	DataCnt[11:0] CRC[15:0]
Sync	1	000	1100 1100 1100 1100 1100 1100 1111
Data	0	Region[2:0] Channel[2:0] Le[11:0] Pk[5:0] Te[6:0]	

Control unit

- Serial link at 1/2 of the master clock frequency
- Input : 16 bits command
- Output : 16 bits data
- Address :
  - $\mathrm{a_B}$: broadcast address
  - $\mathrm{a_6 a_5 a_4 a_3 a_2 a_1 a_0}$: chip address
- Three types of registers :
  - Global Control Registers (GCR)
  - Region Control Registers (RCR)
  - Channel Control Registers (CCR)

Control data format

Function	**Data** 4 bits	**Op code** 12 bits
Chip Select	1101	$01a_B a_6 a_5 a_4 a_3 a_2 a_1 a_0 00$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000 r_2 r_1 r_0 0 c_2 c_1 c_0 a_0$
Register select (region)	0100	$0000 r_2 r_1 r_0 1 a_3 a_2 a_1 a_0$
Register select (global)	0100	$00010 a_6 a_5 a_4 a_3 a_2 a_1 a_0$
Register write	0101	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
Reserved for config output	1000	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$

Reset management

- Asynchronous power-on reset : for start-up only
- Synchronous, pulse lenght encoded reset :
  - 1 clock cycle reset pulse : ignored
  - 2 clock cycles reset pulse : time stamp counter and Tx units reset
  - 3 clock cycle reset pulse : ignored
  - n$\geq$4 clock cycles reset pulse : global reset
- "Short" synchronous reset used for time stamp synchronization at the system level

Conclusions

- A new ASIC for the readout of MicroMegas detectors, currently under design
- Custom developed analog FE
- Two gains, 10 mV/fC and 1 mV/fC
- Provides ToA, peak position, ToT
- Digital BE from a silicon-proven design (ToASt)
- Submission foreseen for 2H2024