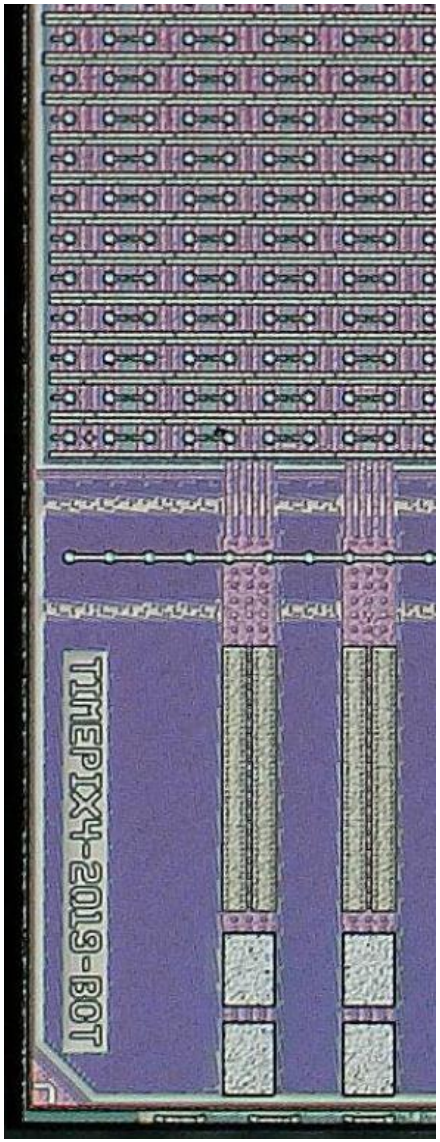


Timepix4 and pixel ASIC design challenges

X. Llopart,
On behalf of the Medipix4 Collaboration

19th June 2024

Timepix3 → Timepix4

Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging capabilities

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable [8.3% dead area] 256 x 256	4-side buttable [0.5% dead area] 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	**33%**
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	**6x**
TOT energy resolution			< 2KeV	< **1Kev**	**2x**
Time resolution			1.56ns	**195.3125ps**	**8x**
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	≤163.84 Gbps (16x @10.24 Gbps)	**32x**
Target global minimum threshold			<500 e^-	<500 e^-	

Medipix4 Collaboration

- **Medipix4 Collaboration is set to provide the next generation of Medipix4 family chips (Medipix4 and Timepix4):**
  - Agreement signed on May 2016
  - 20 collaboration members
- **Timepix4 (2019)**
  - 65nm technology
  - Pixel matrix of 512 x 448 pixels (55 x 55 μm^2)
  - Particle identification and tracking (Data-driven and zero suppressed) → up to 10.8 kHz/pixel
  - Sub-ns time binning → ~195ps
  - X-ray Imaging (full frame based with CRW sequential readout)
  - Energy resolution → ~1 KeV (FWHM, Si)
- **Medipix4 (2022)**
  - 130nm technology
  - Pixel matrix of 320 x 320 (75 x 75 μm^2) or 160 x 160 (150 x 150 μm^2)
  - Charge Summing architecture:
    - Dynamic range → to 140 KeV
    - Count Rate → to 10^8 ph/mm^2/s
    - Energy resolution < 2.2 KeV (FWHM, CdTe, CSM @ 60 KeV)
  - 2 thresholds @75 µm pixel or 8 thresholds @150 µm
- **Both chips have a 4-side buttable architecture:**
  - Periphery integrated inside the pixel matrix
  - Prepare for readout using TSV (Through-Silicon-Vias)
  - Larger ASICs

- **CEA, Paris, France**
- **CERN, Geneva, Switzerland**
- **DESY, Hamburg, Germany**
- **Diamond Light Source, England, UK**
- **IEAP, Czech Technical University, Prague, Czech R.**
- **IFAE, Barcelona, Spain**
- **JINR, Dubna, Russian Federation**
- **NIKHEF, Amsterdam, The Netherlands**
- **University of California, Berkeley, USA**
- **University of Canterbury, Christchurch, New Zealand**
- **University of Geneva, Switzerland**
- **University of Glasgow, Scotland, UK**
- **University of Houston, USA**
- **University of Maastricht, The Netherlands**
- **University of Oxford, England, UK**
- **INFN, Italy**
- **LNLS, Brazil**
- **CSNS, China**
- **PNRI, Philippines**
- **University of Tennessee, USA**

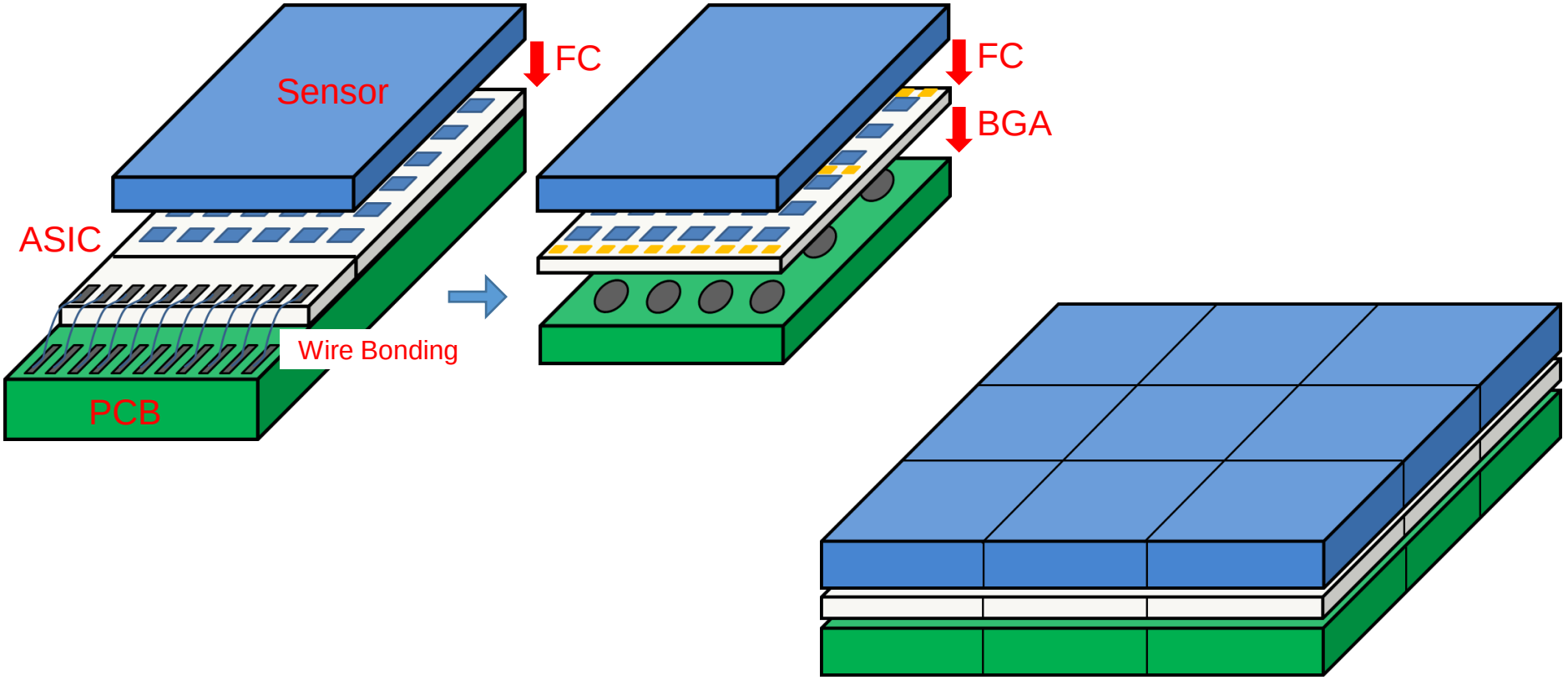
Potential Timepix4 applications

- **Particle-Tracking applications**:
  - HEP:
    - Very high-rate pixel telescope
    - Sensor studies (sub 100psrms time resolutions)
    - Beam gas interaction (PS SPS/LHC?)
    - AeGIS/ASACUSA
    - ATLAS background rad monitor and TRD detector
    - MOEDAL
    - GEMPIX / large area TPC
    - Test vehicle for next gen LHCb-VELO with tens of ps time resolution
  - Time-of-flight mass spectrometry
  - Neutron time-of-flight imaging
  - Radiation monitors
  - Electron microscopy
  - X-ray and powder diffraction
  - Compton camera for medical diagnostics
  - Sub-pixel resolution imaging
  - Gamma and neutron imaging for nuclear industry and Homeland Security

- **Frame-based imaging applications**:
  - X-ray imaging in synchrotrons with extreme high rates > 10^9 particles/mm^2/s

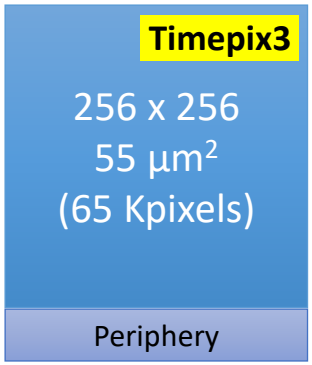
- 20th Anniversary Symposium on Medipix and Timepix
  - https://indico.cern.ch/event/782801/

4-side buttable pixel arrangement

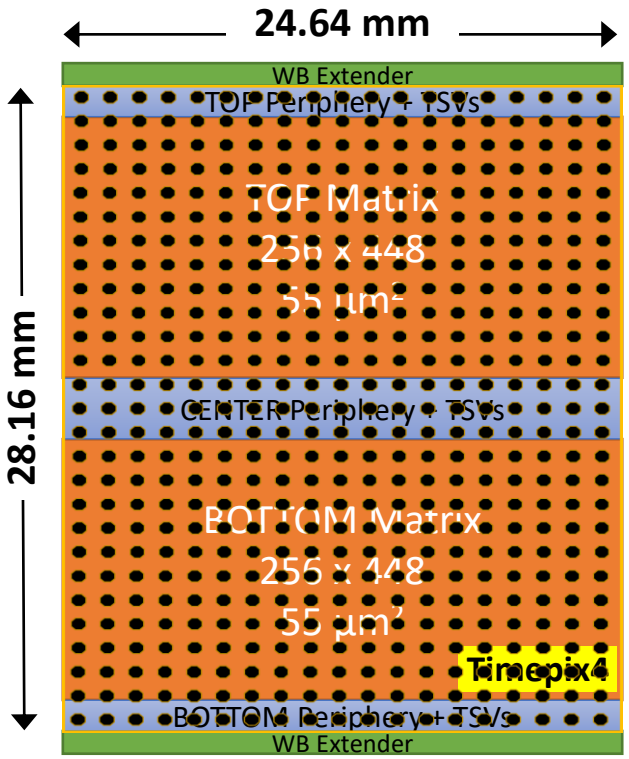


- Target to build **large area detectors** by combining smaller modules
- The through-silicon vias (TSVs) is the key technology for this paradigm shift

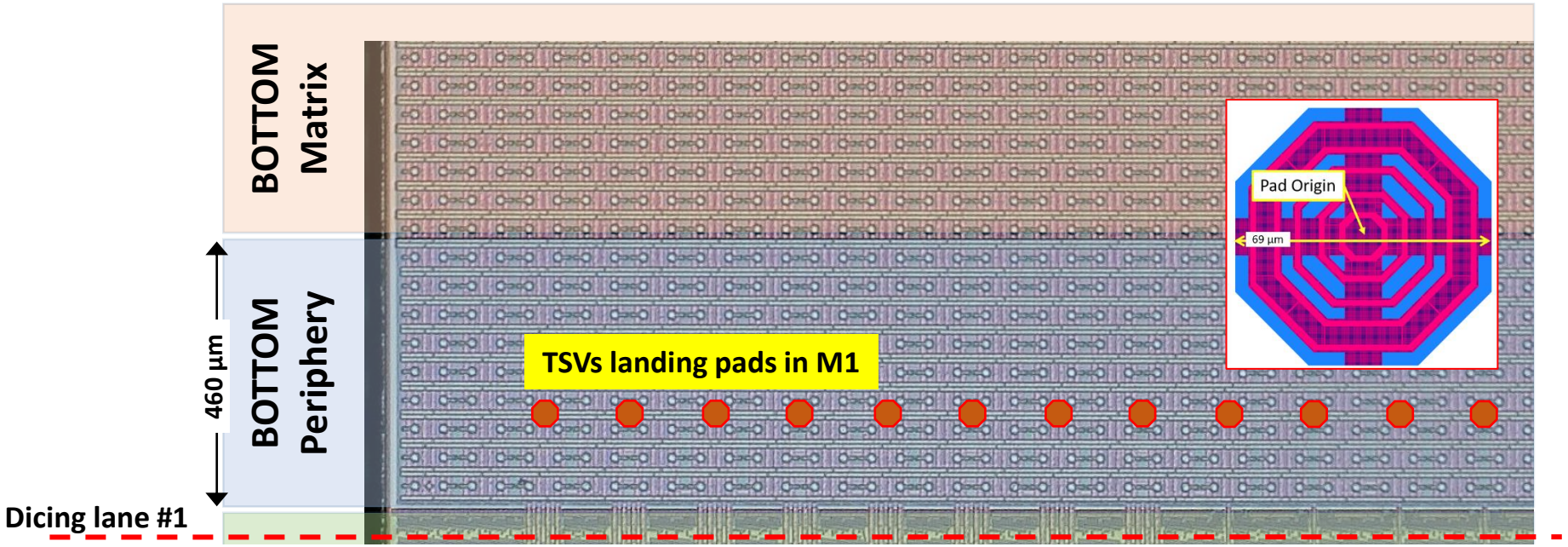
Timepix4 arrangement



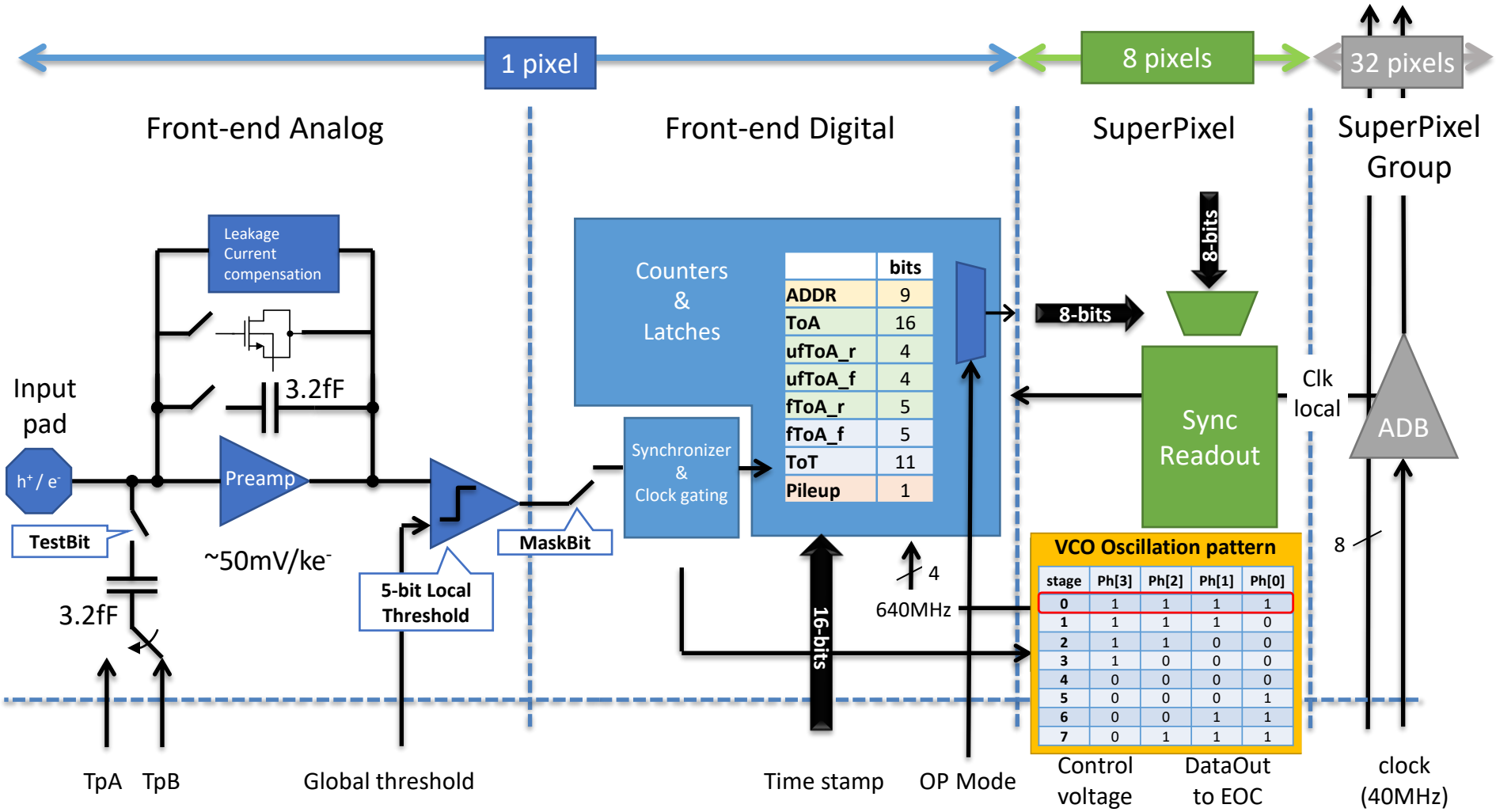
- 512 x 448 of 55 x 55 µm pixels
  - 2 Matrices (TOP and BOTTOM)
- 3 peripheries with TSV (Through-Silicon-Vias):
  - TOP, BOTTOM (TSV, WB): Data Readout (16x 10.24 Gbps Serializers)
  - CENTER (TSV): Analog Blocks (DACs, ADC, Band-Gap…)
- On-chip bump to pixel redistribution layer (RDL):
  - Pixel matrix pixels are shorter (51.4 µm) than sensor pixels (55 µm)
  - Equalized Cin for all pixels → ~46 fF increase for a 460 µm periphery
- Edge peripheries include 1mm Wire Bond Extender
- Dicing options:
  - With WB (Wire-Bonds Extenders): 29.96 mm x 24.7 mm
    - **>93.7%** active area (28.16mm x 24.64mm)
  - Without WB (TSV Only) : 28.22 mm x 24.7 mm
    - **>99.5%** active area (28.16mm x 24.64mm)
    - Through Silicon Vias (TSV) requires post processing at wafer level to create TSV and on the ASIC back sides RDL + BGA pads



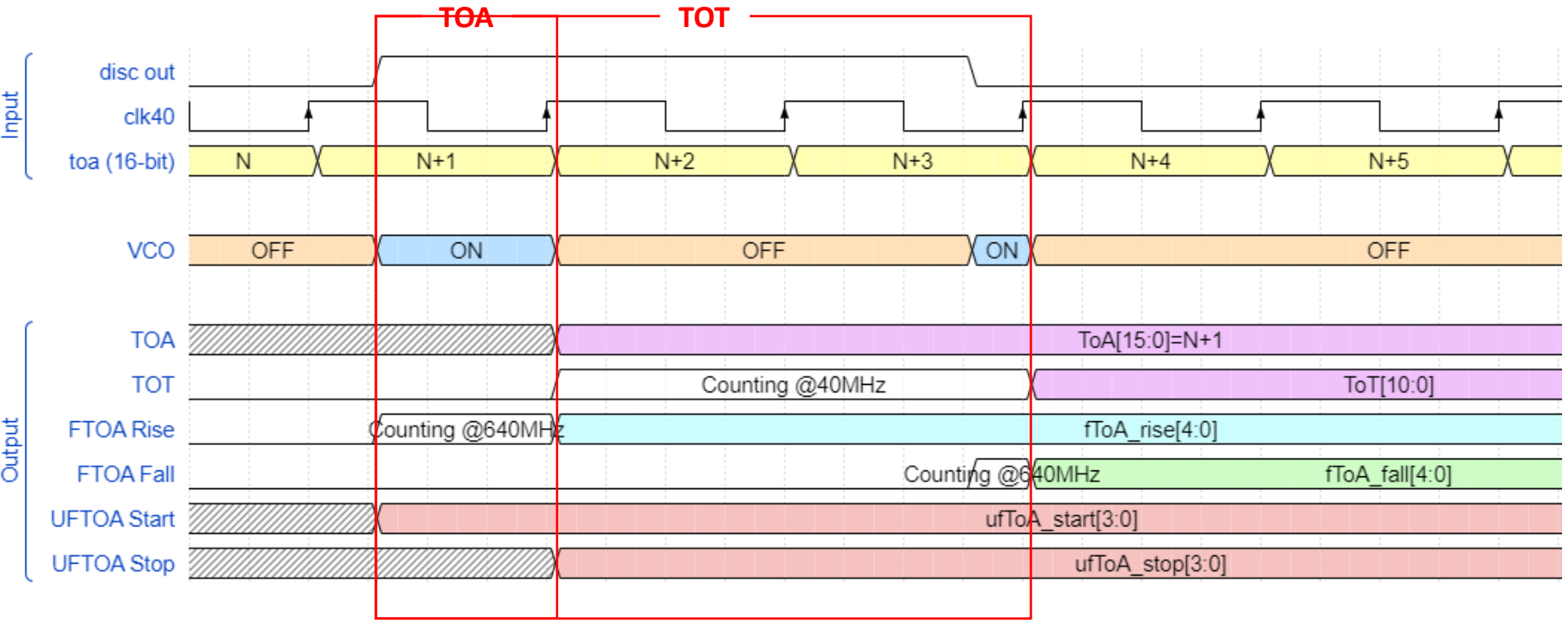
Timepix4 Bottom left detail



Timepix4 Pixel Schematic



Pixel Operation in TOA & TOT [DD]



SPEC: Packet specifications ToA/ToT				
Name	**Width**	**MSB**	**LSB**	**Bits**
Top	1	63	63	[63:63]
EoC	8	62	55	[62:55]
SP	6	54	49	[54:49]
Pixel	3	48	46	[48:46]
ToA	16	45	30	[45:30]
ufToA_start	4	29	26	[29:26]
ufToA_stop	4	25	22	[25:22]
fToA_rise	5	21	17	[21:17]
fToA_fall	5	16	12	[16:12]
ToT	11	11	1	[11:1]
Pileup	1	0	0	[0:0]

Address: 18 bits

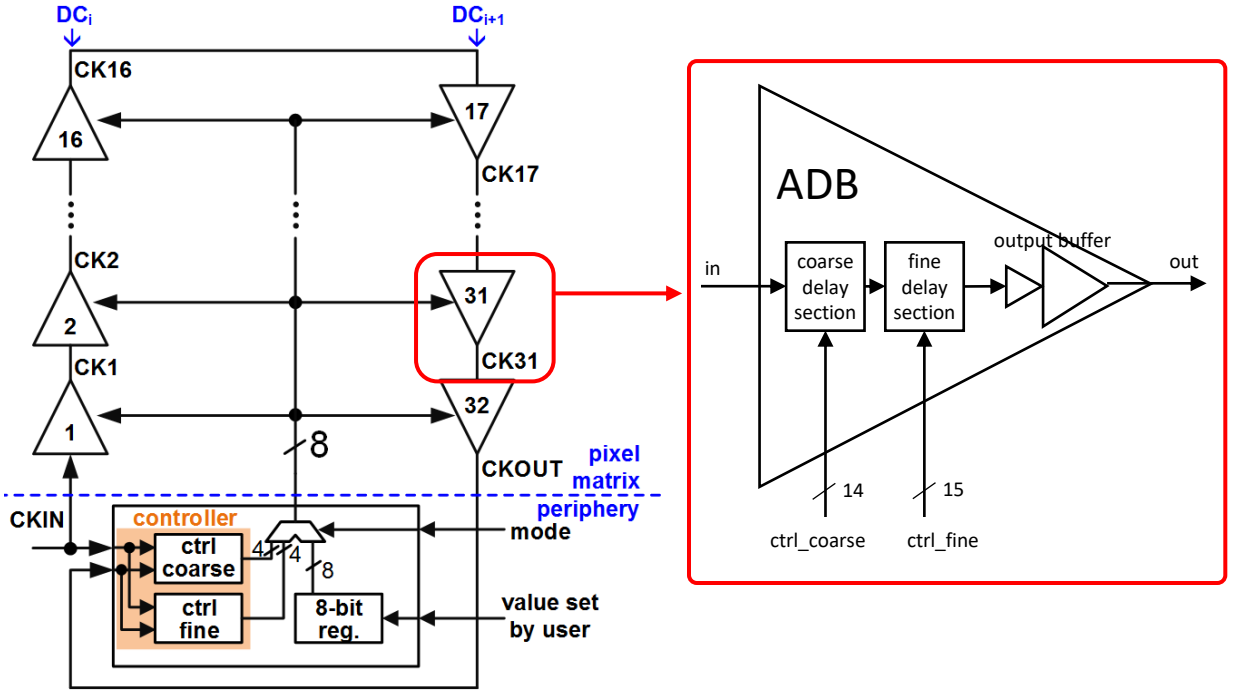
Time: 29 bits
(LSB=195ps @VCO=640MHz)

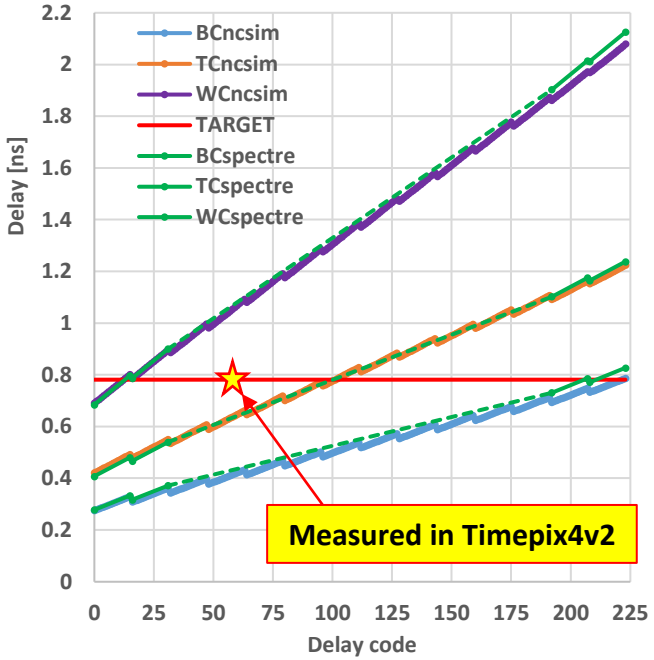
Energy: 21 bits
(LSB=1.56ns@VCO=640MHz)

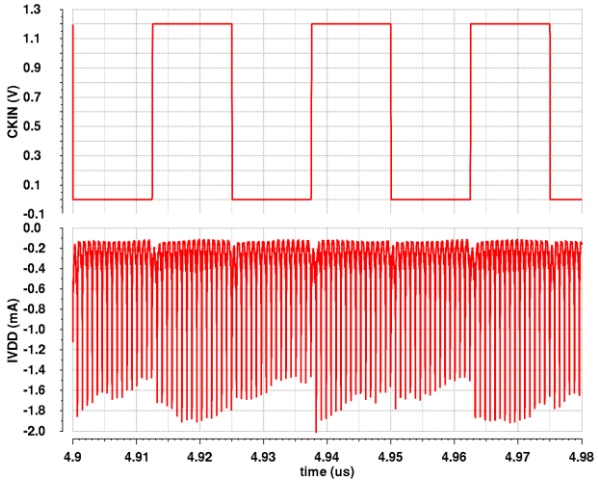
Full digital double column DLL

[448 dDLL: 224 Top Matrix and 224 Bottom Matrix]

iWoRID 2018
X. Llopart et al 2019 JINST 14 C01024



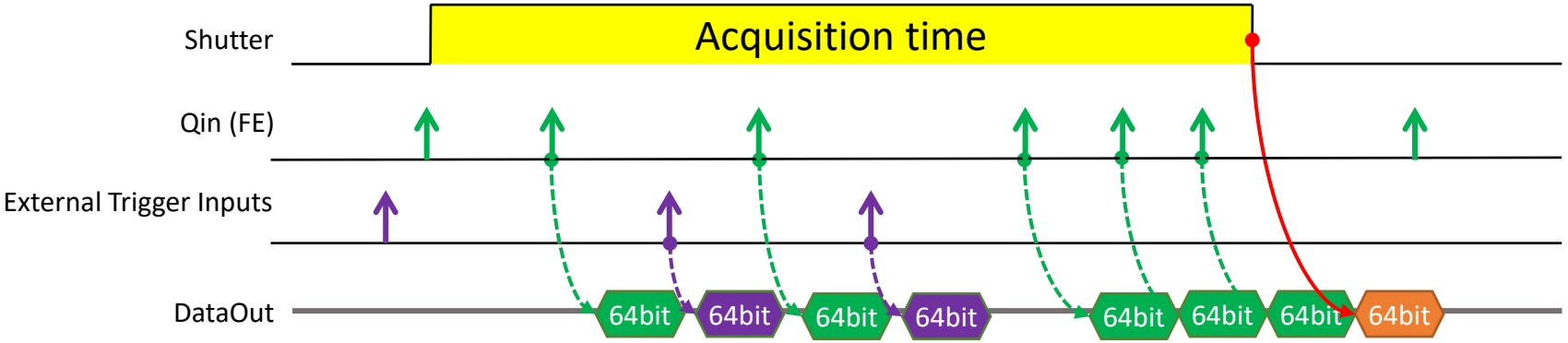




- Timepix3 ~100mW/cm^2 @40MHz clock with **~1.2ns skew**
- Timepix4 ~23 mW/cm^2 @40MHz clock with a **100ps$_{rms}$**
  - ~100 mW/cm^2 measured when adding local pixel clock distribution
- Dynamic digital power consumption is distributed across the clock period

Timepix4 Readout Modes : Data-Driven

- Zero-suppressed continuous data-driven
  - Output bandwidth from 40 Mbps (2.6 Hz/pixel) to 160 Gbps (10.8 KHz/pixel)
  - Uses Aurora 64b/66b standard encoding communication protocol
- 4 External Trigger Inputs to synchronize/align external signals with data



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ToT	11	11	1	[11:1]
Pileup	1	0	0	[0:0]

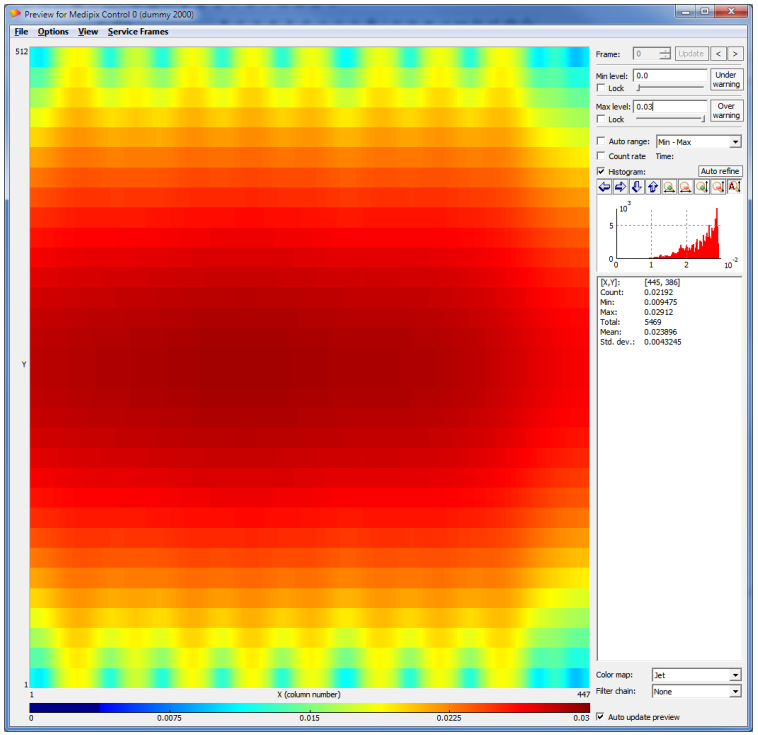
Address: 18 bits

Time: 29 bits

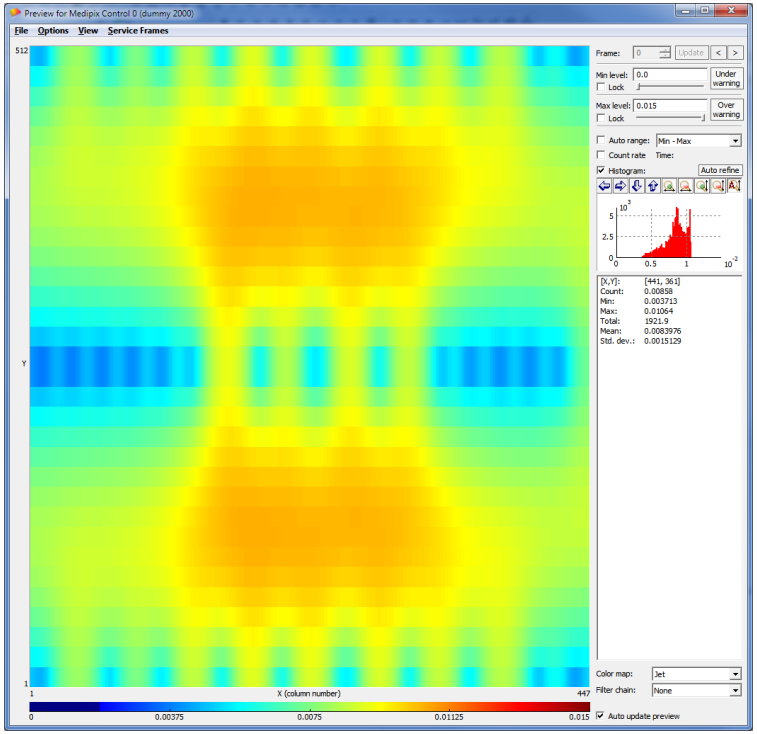
Energy: 21 bits

Analog (static) power supply distribution

	Total I (chip)		2 WB	3 TSV
Nominal Analog Power [10 µA/pixel]	**~2300 mA**	V_{drop} [VDDA-GNDA]	19.6 mV	6.9 mV
		Imax pad	60 mA	57 mA
Low Analog Power [1 µA/pixel]	**~230 mA**	V_{drop} [VDDA-GNDA]	1.96mV	0.69mV
		Imax pad	6 mA	5.7 mA



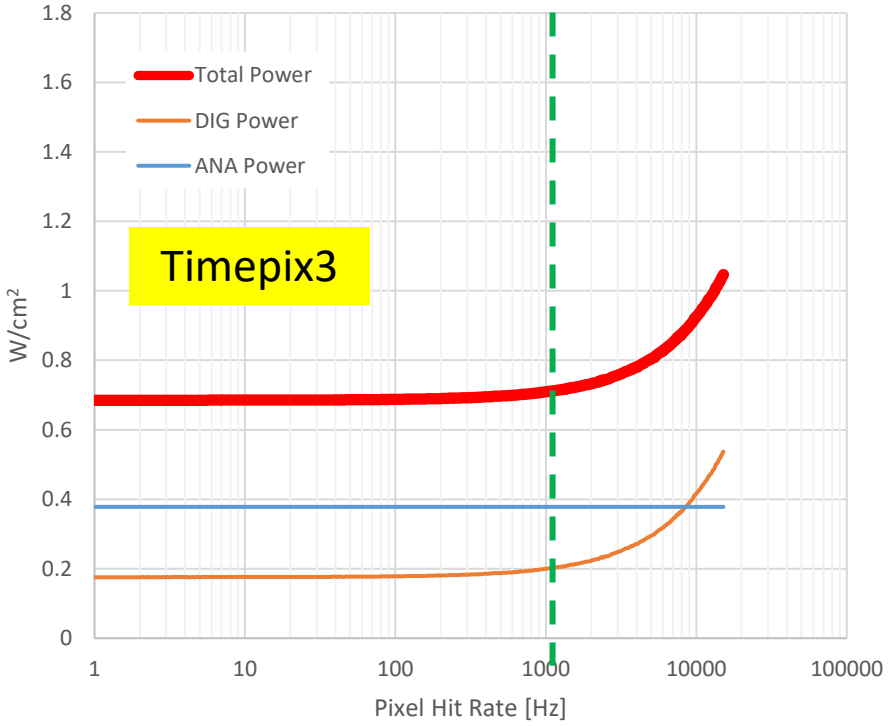
2 WireBonds

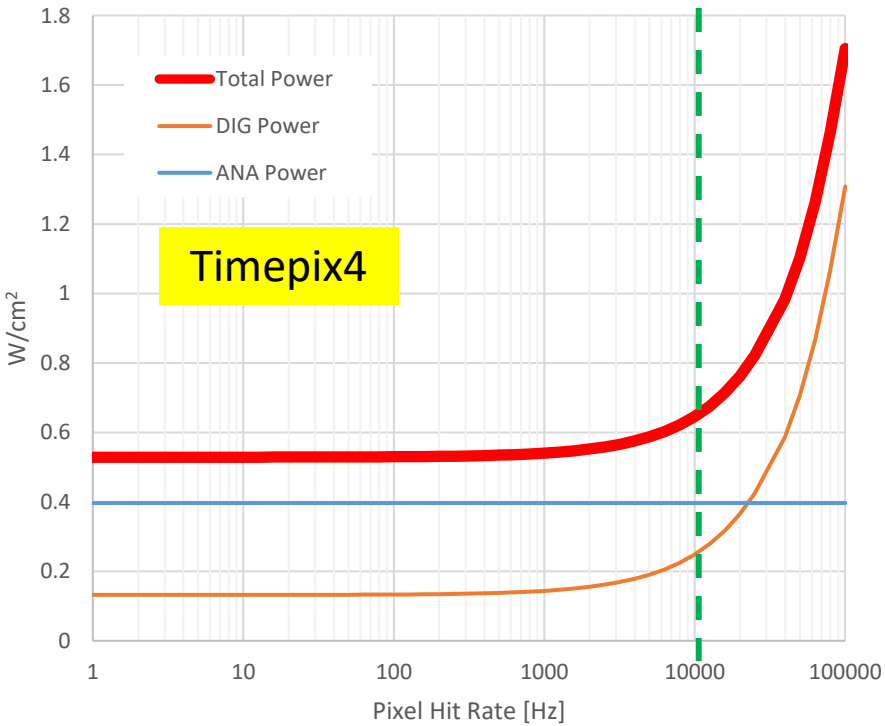


3 TSV

Digital (dynamic) Power Consumption
[Data-Driven]

- Power consumption density is ~20 % less than Timepix3:
  - Digital power consumption 25% less
    - Improved clock distribution (dDLL)
    - 130nm → 65nm
  - Analog consumption is ~5% more
    - Minimize jitter → < 50ps
    - Compensate increase in input capacitance





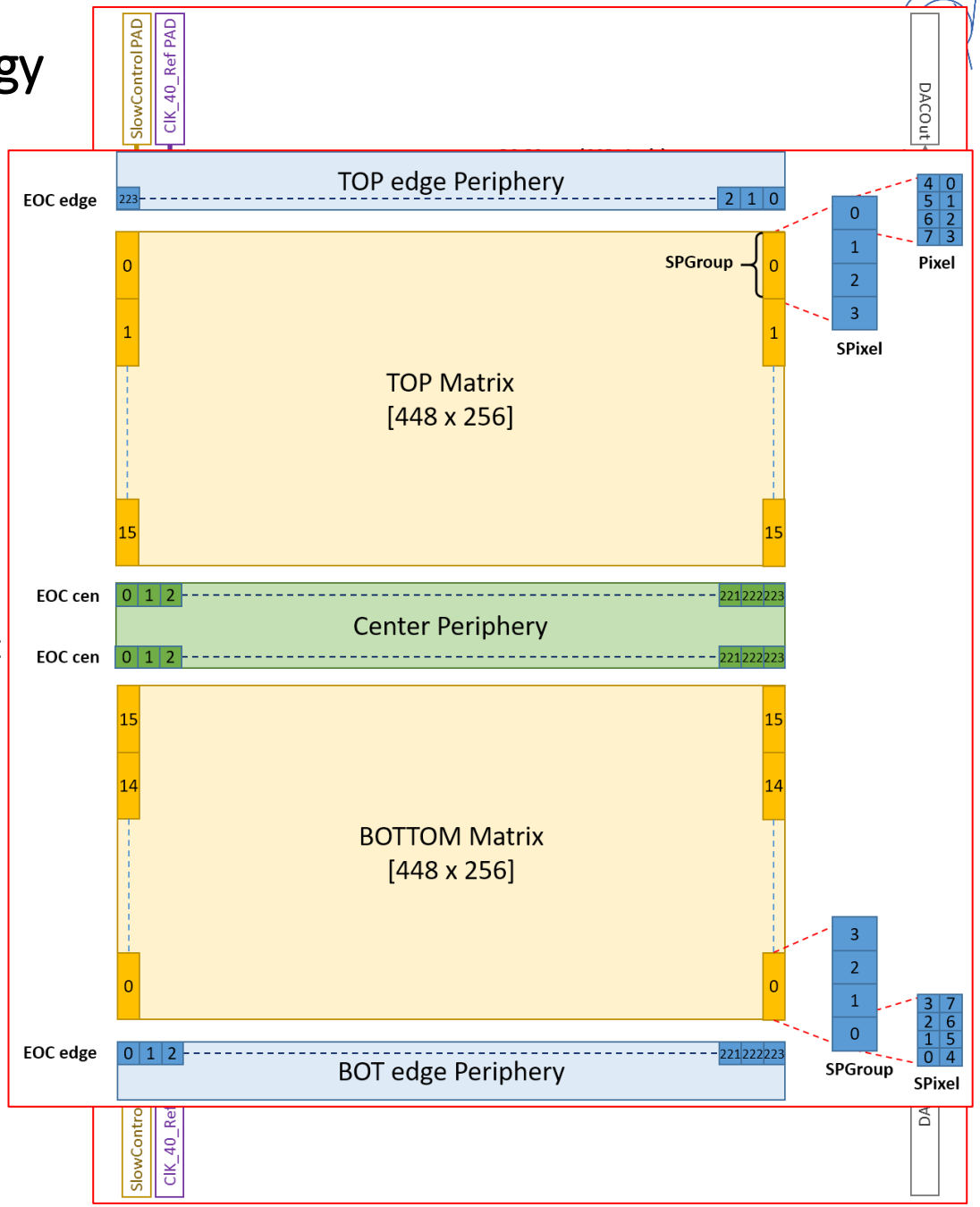
Timepix4 Design Strategy

- Digital on top design methodology
  - Top level design partition:

Timepix4_TOP	
	Timepix4EdgePeriphery (x2)
	Timepix4CentrePeriphery
	edge_routing_analog (x2)
	edge_routing_digital (x2)
	PixelMatrix (x2)

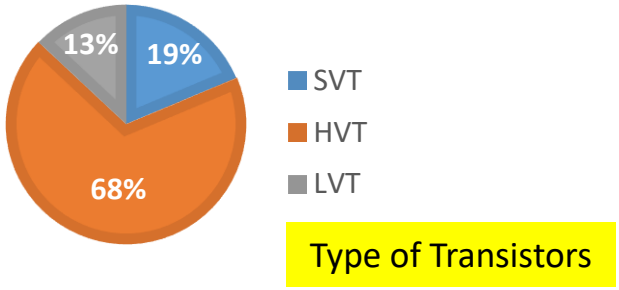
  - Designs partitions are connected by abutting macro blocks → No routing at top level

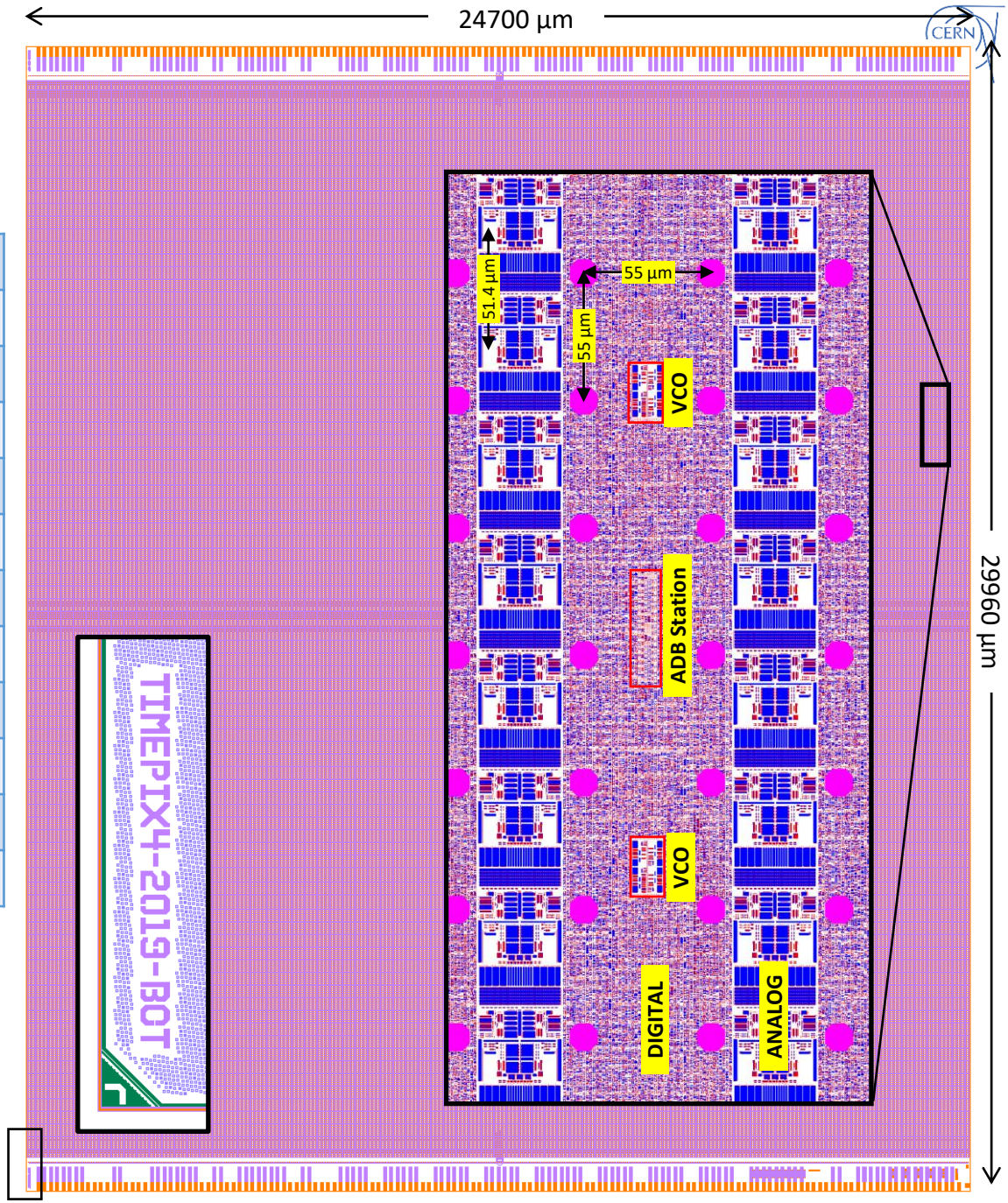
- Benefit of this approach clearly visible towards the end of the project:
  - Full chip LVS in ~2h
  - Full chip (with filling) DRC in ~5h
  - Full chip functional regression verification in <24h → with few complete columns



Timepix4v0 (November 2019)

Pixel size	55 x 55 µm
Array	512 x 448
Pixels	229376
aPLL	19
aDLL	16
10.24 Gbps serializers (Nikhef)	16
On-pixel VCO (Nikhef)	28672
dDLL Columns	448
Biasing DACs	13
ADC (IFAE)	1
Transistors in pixel	~6000
Transistors in chip	~1.5 bn





Timepix4 submissions

Q4 2019

Timepix4v0

~17 FTEE
Full mask engineering run

6 wafers received

Chip is operational

1) Excess noise coupling from peripheries to FE
2) 640 MHz clock in edge peripheries
3) VCO not oscillating at nominal frequency

Q3 2020

Timepix4v1

4 BEOL masks changed

Small test VCO chip

6 wafers received

1) Improved RDL shielding in peripheries
2) 640MHz in peripheries recovered

1) VCO not oscillating at nominal frequency

Q2 2021

Timepix4v2

4 FEOL + 4 BEOL masks changed

19 wafers received

1) TDC and High speed links working as expected
2) Further improvement in RDL shielding in peripheries

Chip at its final version

Q3 2022

Timepix4v3

2 BEOL masks changed

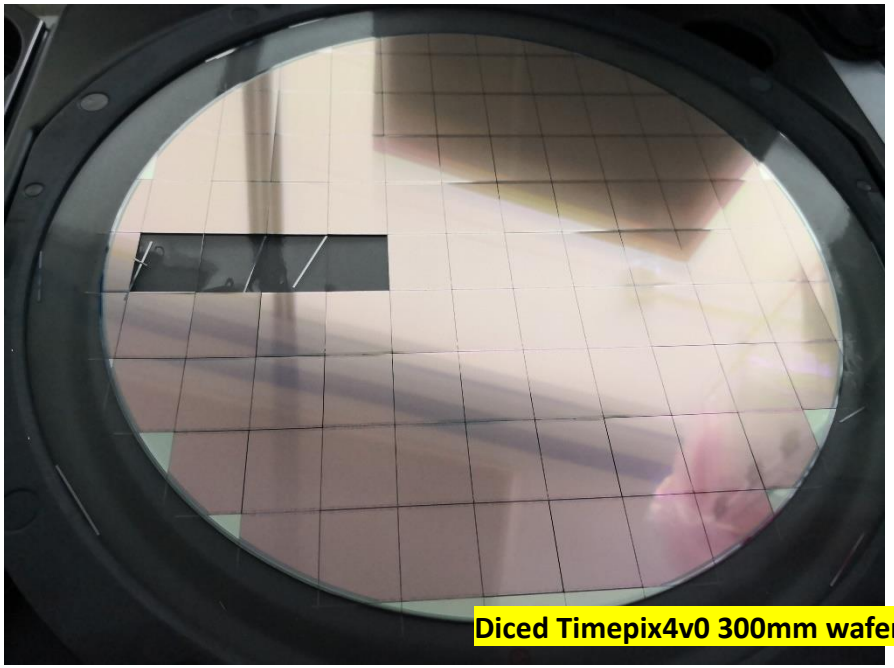
25 wafers received

1) Larger IO Pads

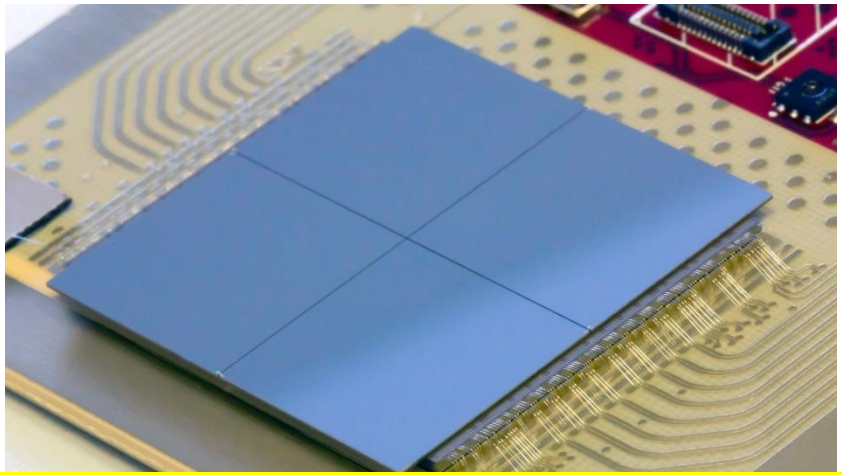
Chip at its final version

Timepix4 on Silicon

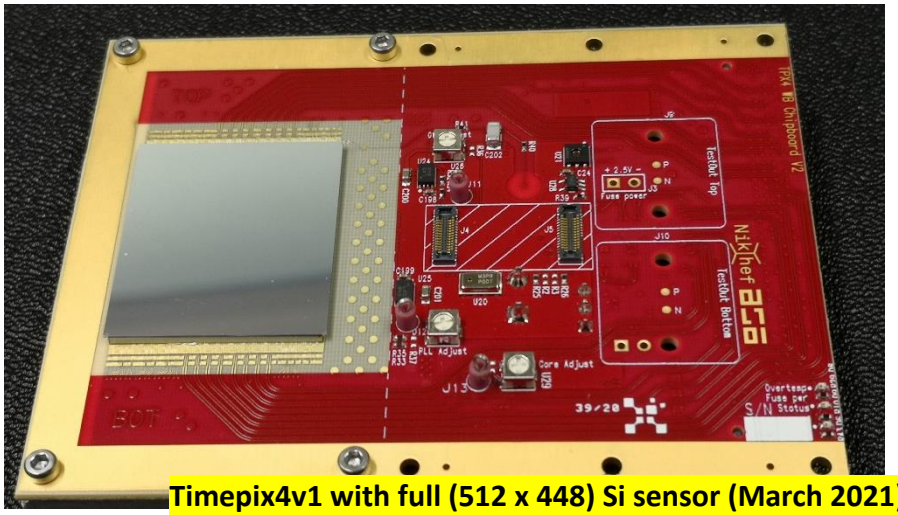
- First Timepix4v0 devices became available on the beginning of 2020 → chip debugging/characterization delayed by COVID19
- SPIDR4 readout system (Nikhef) used as a DAQ for initial chip debugging
- Testing of Timepix4 using the Wire Bond connections



Diced Timepix4v0 300mm wafer

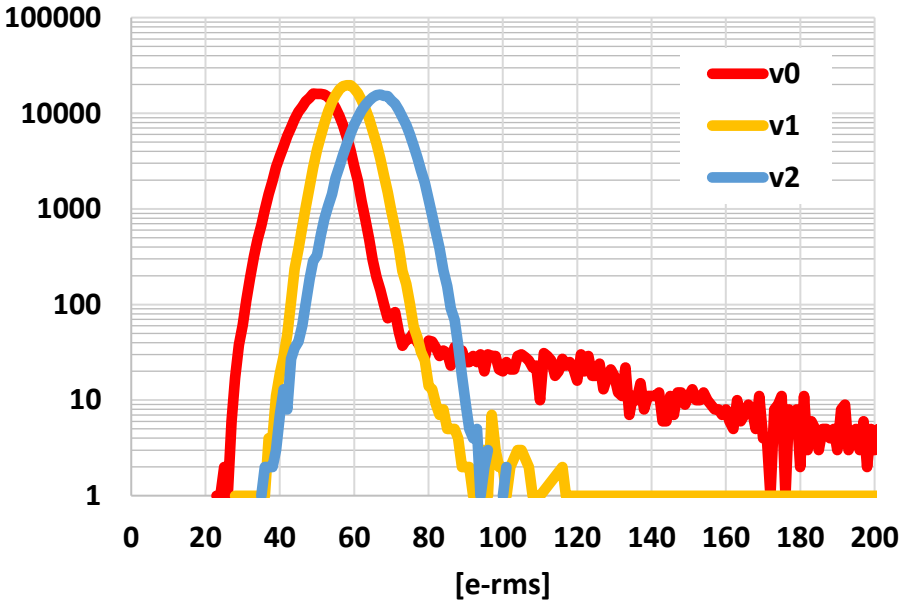


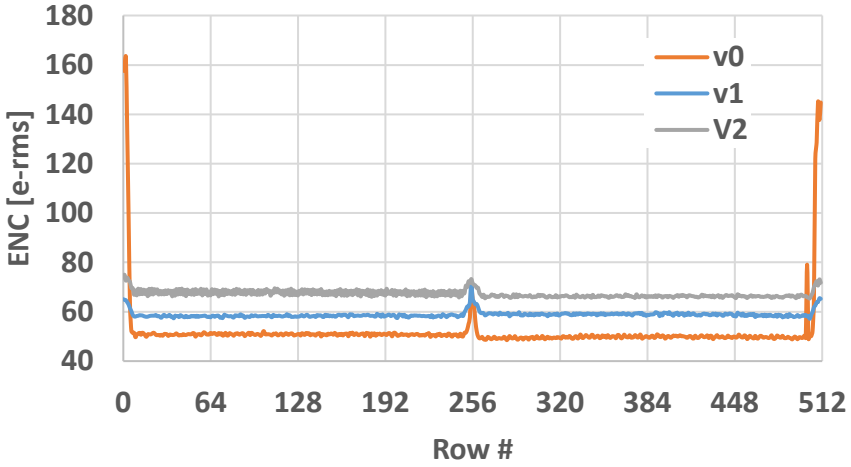
Timepix4v0 with 4x300 µm (256x256) edgeless Si sensor (August 2020)

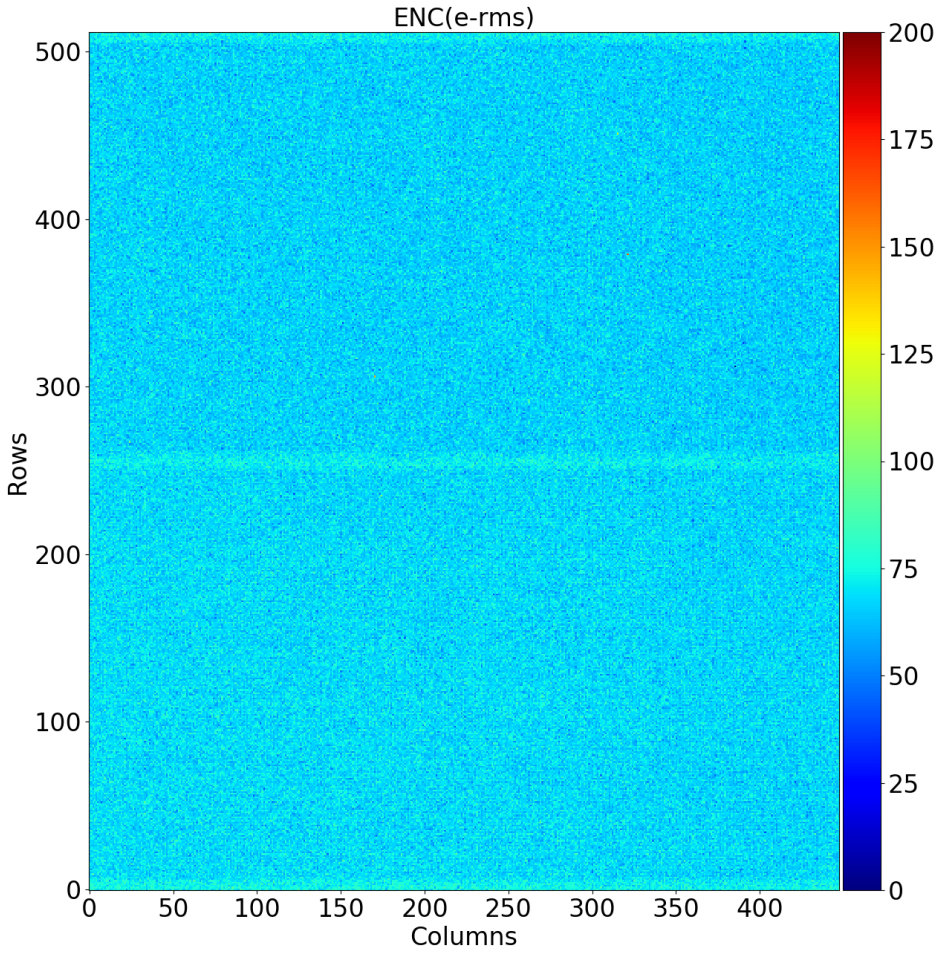


Timepix4v1 with full (512 x 448) Si sensor (March 2021)

Timepix4v0, v1 and v2 ENC

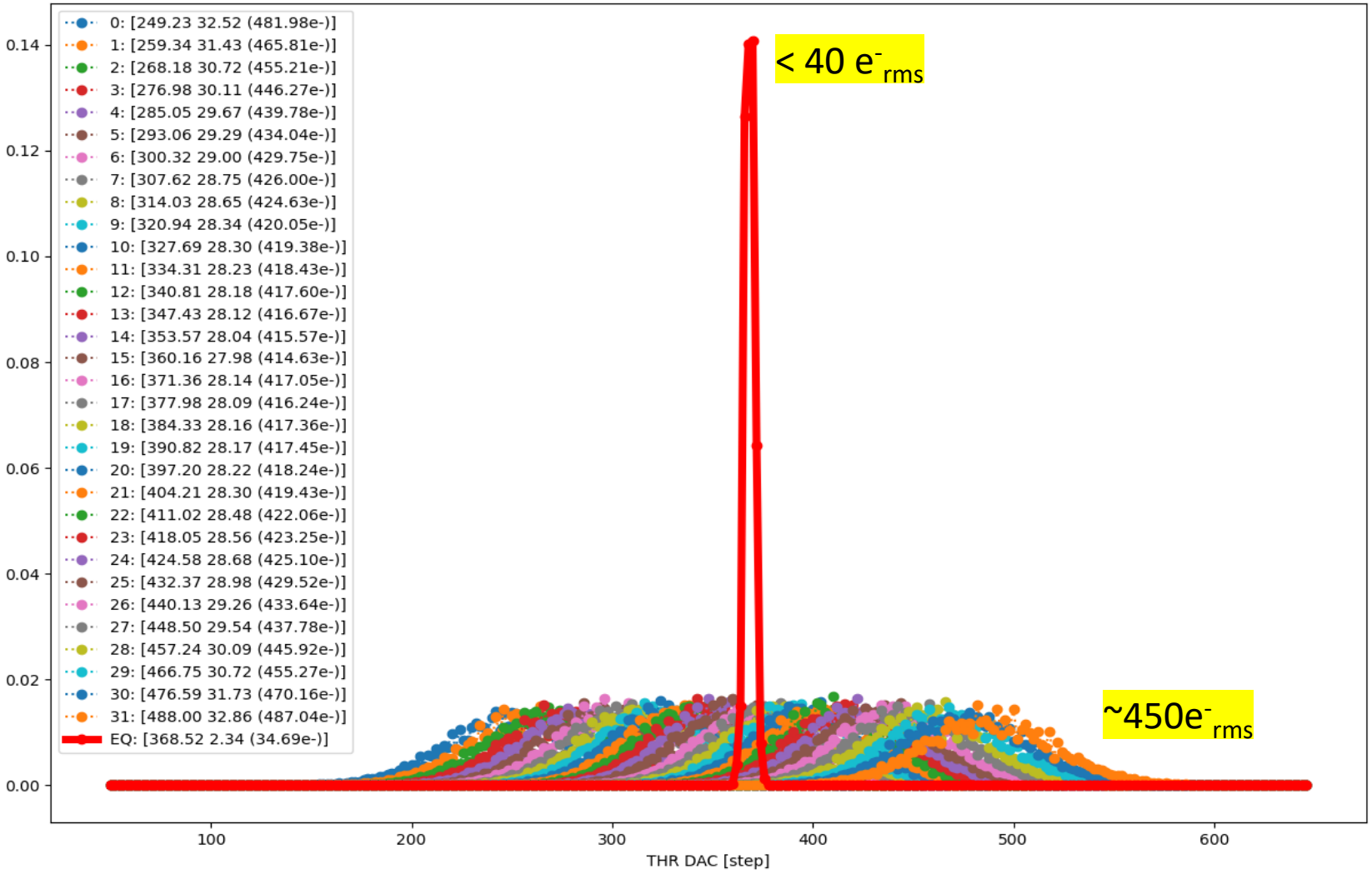






With a Si sensor the noise slightly increase ~3e$^-$ / pixel

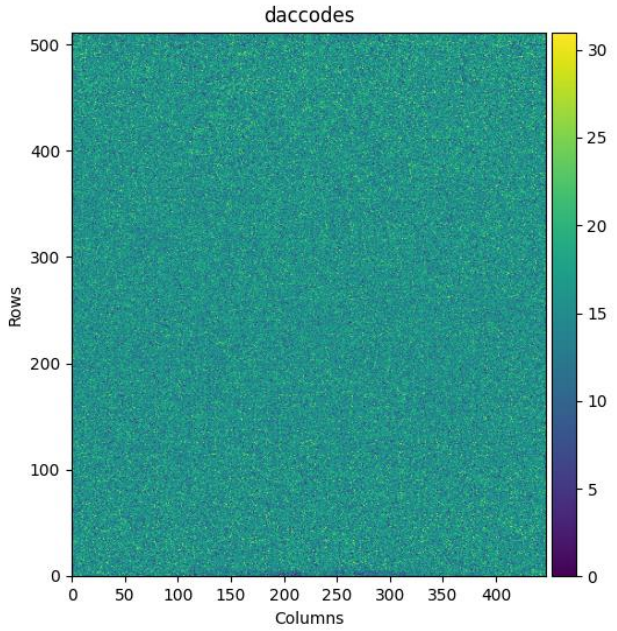
Timepix4v0 equalization

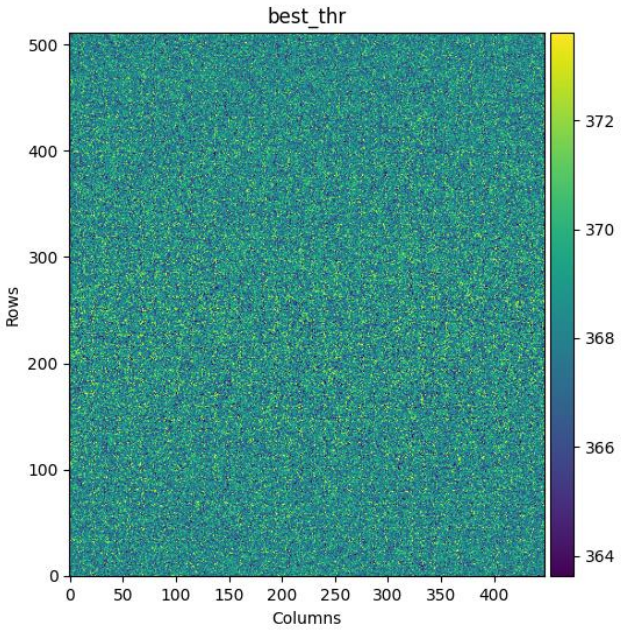


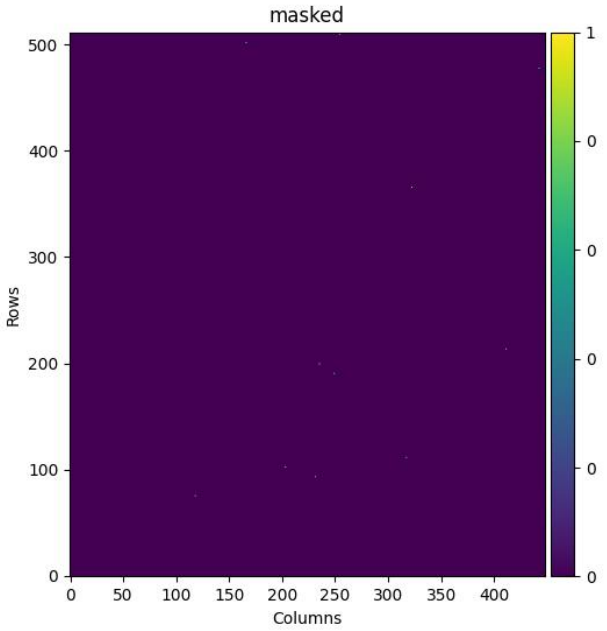
Equalization matrix

[PC24bit mode, e- collection high gain]

- All pixels responding (448x512)
- 11 pixels masked
- No observable systematic across matrix



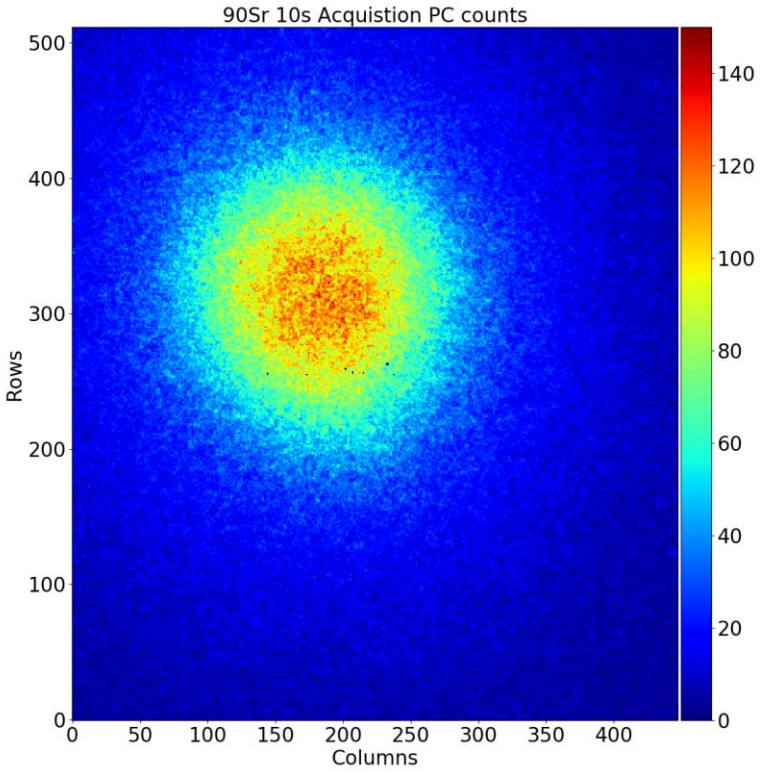




Timexpix4v1 in Data-Driven mode

[Thr=800e- with ~120 pixels masked]

- Timepix4v1 running at 2 x 2.56 Gbps links: 77 MHits/s
- ~6.1M packets received without errors: ~610 KHits/s

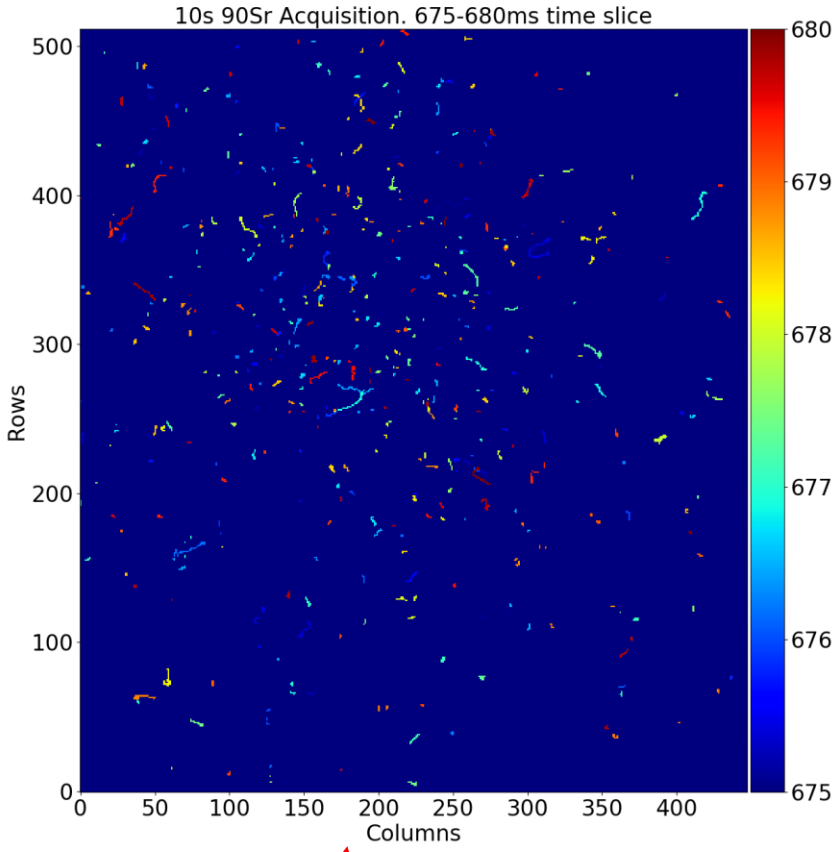


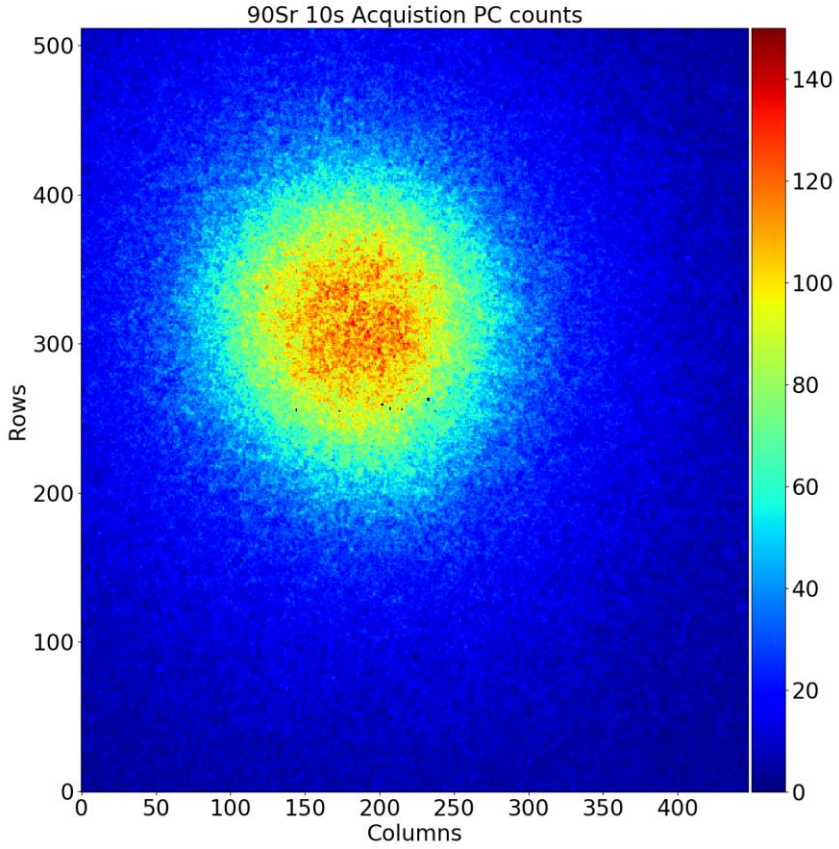
10s ^{90}Sr source
Photon Counting reconstruction

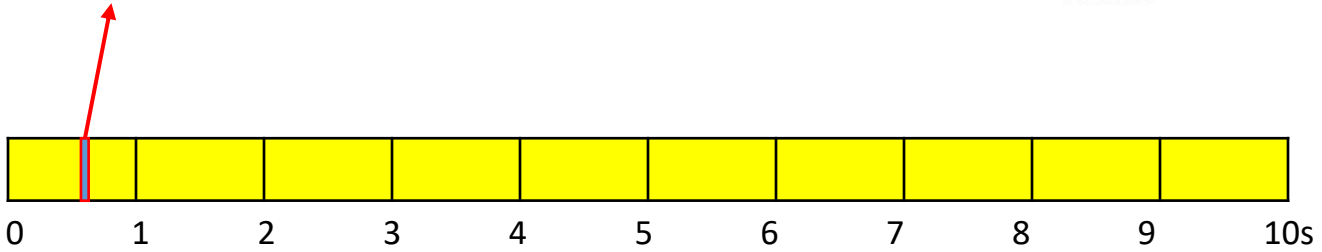
```
174579: SHUTTER_RISE T 36515
174580: top=1 eoc=5b pixnr=1fc toa=c9fe uftoa-sta/sto=1,f ftoa-f/r= 2, d tot=  0 pileup=0
174581: top=1 eoc=5b pixnr=1ff toa=c9ff uftoa-sta/sto=7,f ftoa-f/r= b, 4 tot=  1 pileup=0
174582: HEARTBEAT T 36870 (diff=1025)
174583: HEARTBEAT T 37895 (diff=1025)
174584: top=1 eoc=cd pixnr= ef toa=da1d uftoa-sta/sto=1,f ftoa-f/r= 6,15 tot= 14 pileup=0
174585: HEARTBEAT T 38920 (diff=1025)
174586: HEARTBEAT T 39945 (diff=1025)
174587: top=1 eoc=53 pixnr= cb toa=d622 uftoa-sta/sto=e,f ftoa-f/r= d, f tot=  8 pileup=0
174588: top=1 eoc=53 pixnr= d7 toa=d622 uftoa-sta/sto=c,1 ftoa-f/r= c, 6 tot=  0 pileup=0
174589: top=1 eoc=53 pixnr= d2 toa=d623 uftoa-sta/sto=0,e ftoa-f/r= 4, 4 tot= 10 pileup=0
174590: top=1 eoc=52 pixnr= cf toa=d622 uftoa-sta/sto=0,f ftoa-f/r= 6, f tot= 13 pileup=0
174591: top=1 eoc=53 pixnr= d0 toa=d623 uftoa-sta/sto=0,1 ftoa-f/r=10, 4 tot= 19 pileup=0
174592: top=1 eoc=52 pixnr= d4 toa=d623 uftoa-sta/sto=e,f ftoa-f/r=10, 3 tot= 2b pileup=0
174593: top=1 eoc=53 pixnr= d1 toa=d623 uftoa-sta/sto=0,f ftoa-f/r= 6, 5 tot= 15 pileup=0
174594: top=1 eoc=53 pixnr= d6 toa=d623 uftoa-sta/sto=0,7 ftoa-f/r= b, 5 tot= 3e pileup=0
174595: top=1 eoc=54 pixnr= d2 toa=d623 uftoa-sta/sto=0,f ftoa-f/r= 8, 4 tot= 51 pileup=0
174596: HEARTBEAT T 40970 (diff=1025)
174597: top=1 eoc=3b pixnr=14d toa=f0d6 uftoa-sta/sto=3,f ftoa-f/r=12,11 tot=  a pileup=0
174598: top=1 eoc=3b pixnr=147 toa=f0d6 uftoa-sta/sto=0,f ftoa-f/r= 1, 7 tot= 1a pileup=0
174599: top=1 eoc=3b pixnr=14c toa=f0d6 uftoa-sta/sto=3,8 ftoa-f/r= 5,11 tot= 22 pileup=0
174600: top=1 eoc=92 pixnr=1ef toa=f148 uftoa-sta/sto=1,3 ftoa-f/r= 9, d tot=  1 pileup=0
174601: top=1 eoc=94 pixnr=1f2 toa=f158 uftoa-sta/sto=1,f ftoa-f/r=10,14 tot=  1 pileup=0
174602: top=1 eoc=93 pixnr=1f5 toa=f148 uftoa-sta/sto=f,1 ftoa-f/r=15, 4 tot=  6 pileup=0
174603: top=1 eoc=92 pixnr=1f0 toa=f148 uftoa-sta/sto=e,f ftoa-f/r= 7, f tot=  7 pileup=0
174604: top=1 eoc=94 pixnr=1f7 toa=f148 uftoa-sta/sto=0,e ftoa-f/r= 8, 7 tot=  8 pileup=0
174605: top=1 eoc=94 pixnr=1f8 toa=f148 uftoa-sta/sto=3,f ftoa-f/r=14, 8 tot=  8 pileup=0
174606: top=1 eoc=93 pixnr=1f1 toa=f148 uftoa-sta/sto=e,f ftoa-f/r= a, 9 tot= 14 pileup=0
174607: top=1 eoc=92 pixnr=1ea toa=f148 uftoa-sta/sto=3,c ftoa-f/r= 6, a tot= 1f pileup=0
174608: top=1 eoc=93 pixnr=1fd toa=f148 uftoa-sta/sto=f,f ftoa-f/r= 3, 7 tot= 17 pileup=0
174609: top=1 eoc=94 pixnr=1f3 toa=f148 uftoa-sta/sto=1,f ftoa-f/r= a, 9 tot= 19 pileup=0
174610: top=1 eoc=92 pixnr=1f4 toa=f148 uftoa-sta/sto=f,f ftoa-f/r=12, f tot= 1c pileup=0
174611: top=1 eoc=94 pixnr=1fd toa=f148 uftoa-sta/sto=3,f ftoa-f/r= a, 4 tot=  8 pileup=0
174612: top=1 eoc=93 pixnr=1f6 toa=f148 uftoa-sta/sto=e,8 ftoa-f/r= a, 9 tot= 18 pileup=0
174613: top=1 eoc=94 pixnr=1f9 toa=f148 uftoa-sta/sto=7,1 ftoa-f/r= 2, 8 tot= 16 pileup=0
174614: top=1 eoc=93 pixnr=1fe toa=f148 uftoa-sta/sto=f,0 ftoa-f/r=15, 4 tot= 13 pileup=0
174615: top=1 eoc=94 pixnr=1fc toa=f148 uftoa-sta/sto=3,0 ftoa-f/r= 0, 8 tot= 27 pileup=0
174616: top=1 eoc=92 pixnr=1eb toa=f148 uftoa-sta/sto=3,f ftoa-f/r= 7,11 tot= 4c pileup=0
174617: HEARTBEAT T 41995 (diff=1025)
174618: top=1 eoc= 8 pixnr=  0 toa=f674 uftoa-sta/sto=1,f ftoa-f/r= 2, a tot= 13 pileup=0
174619: top=1 eoc= 7 pixnr=  5 toa=f674 uftoa-sta/sto=e,8 ftoa-f/r= 8, 6 tot= 1c pileup=0
174620: top=1 eoc= 7 pixnr=  4 toa=f674 uftoa-sta/sto=e,f ftoa-f/r= 9, d tot= 37 pileup=0
174621: top=1 eoc=3d pixnr=1a0 toa=f7a5 uftoa-sta/sto=7,f ftoa-f/r= 5,13 tot=  1 pileup=0
174622: top=1 eoc=3d pixnr=1a2 toa=f7ac uftoa-sta/sto=e,f ftoa-f/r= c,16 tot= 1b pileup=0
174623: top=1 eoc=3d pixnr=1a1 toa=f7ac uftoa-sta/sto=e,1 ftoa-f/r= c,13 tot= 2d pileup=0
174624: HEARTBEAT T 43020 (diff=1025)
174625: top=1 eoc=a7 pixnr=181 toa=fd24 uftoa-sta/sto=0,f ftoa-f/r=13,12 tot=  f pileup=0
174626: top=1 eoc=a8 pixnr=182 toa=fd25 uftoa-sta/sto=0,f ftoa-f/r=14, 5 tot= 13 pileup=0
174627: top=1 eoc=a7 pixnr=185 toa=fd25 uftoa-sta/sto=7,f ftoa-f/r= 5, 1 tot= 13 pileup=0
174628: top=1 eoc=a7 pixnr=182 toa=fd24 uftoa-sta/sto=0,f
174629: top=1 eoc=a7 pixnr=186 toa=fd25 uftoa-sta/sto=7,8
```

Raw Data-Driven data

Previous data with 5ms time slices

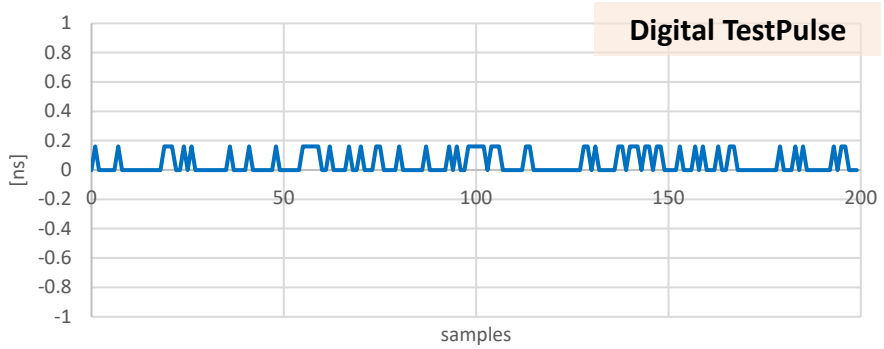


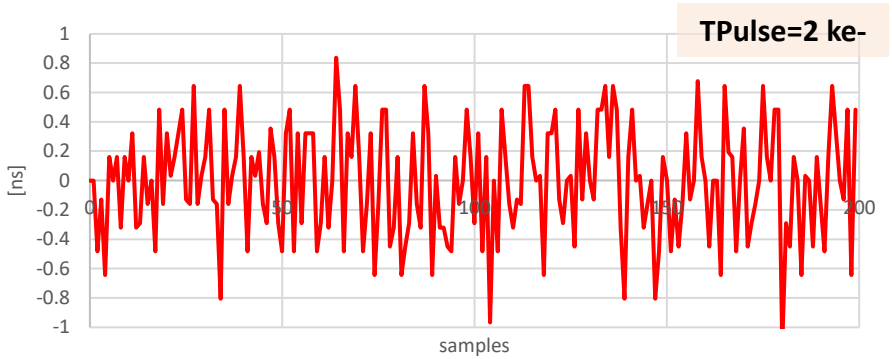


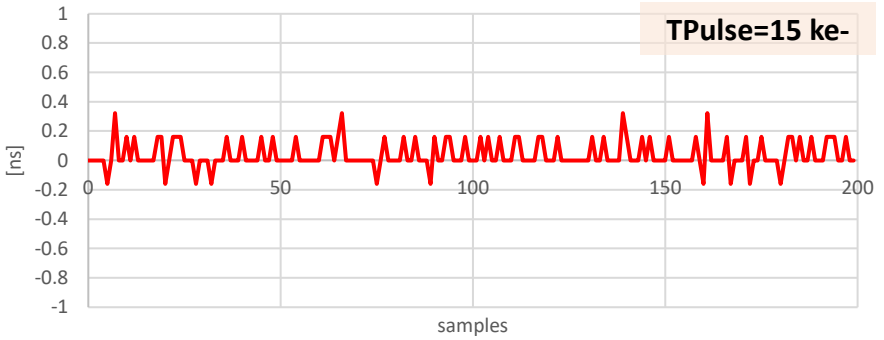


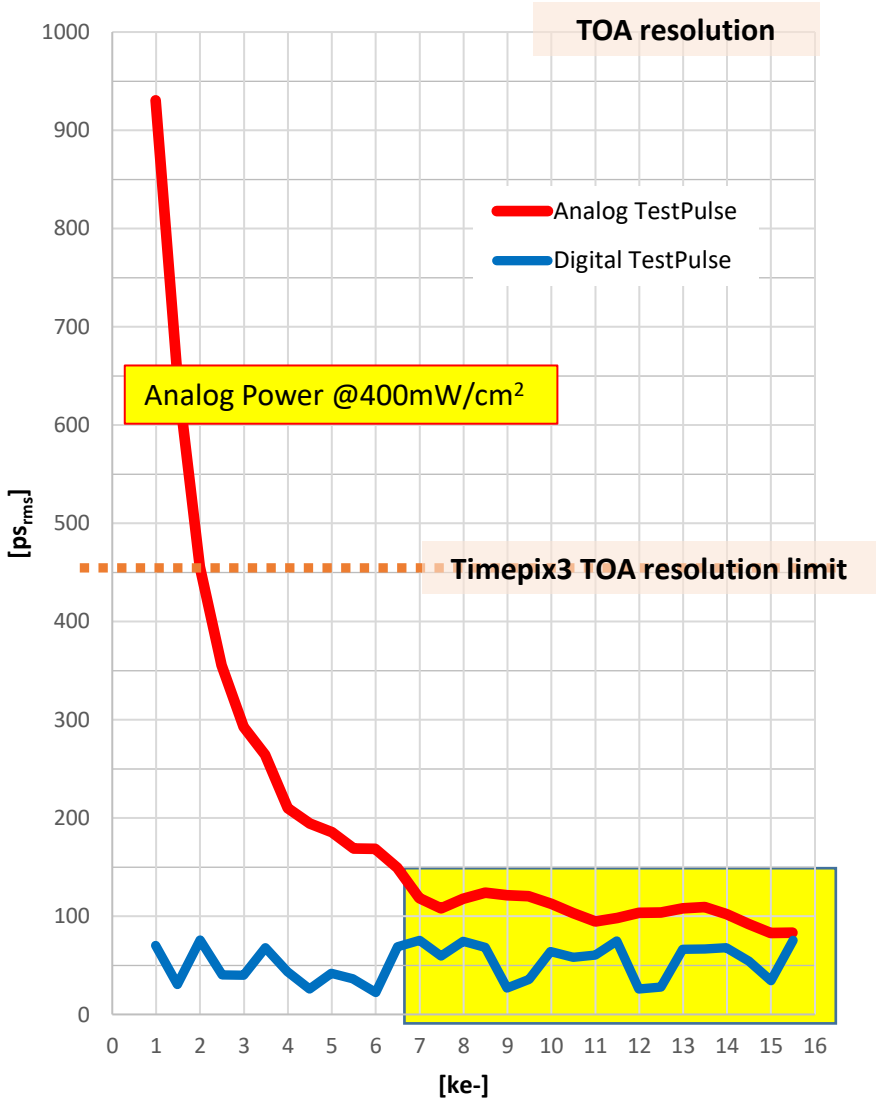
TOA Resolution – Timepix4v0

[TOA-TOT, 1 pixel, 10000 samples, HG e-]



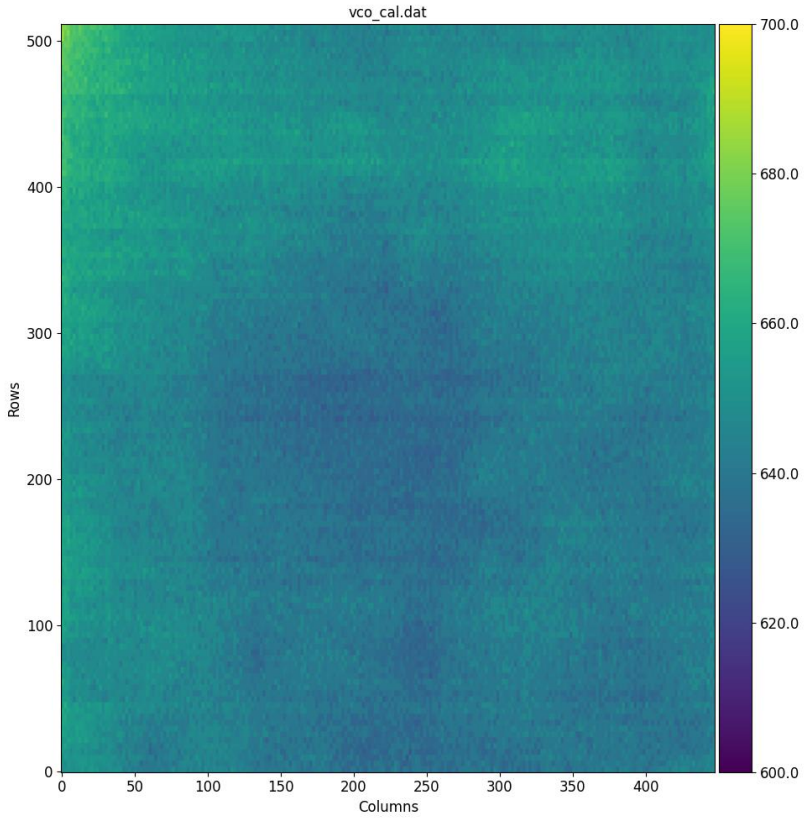


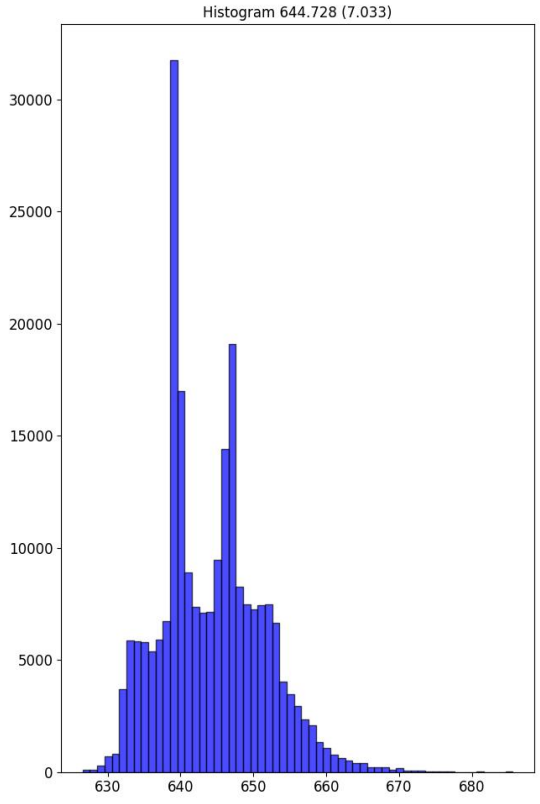




Timepix4 2D VCO distribution

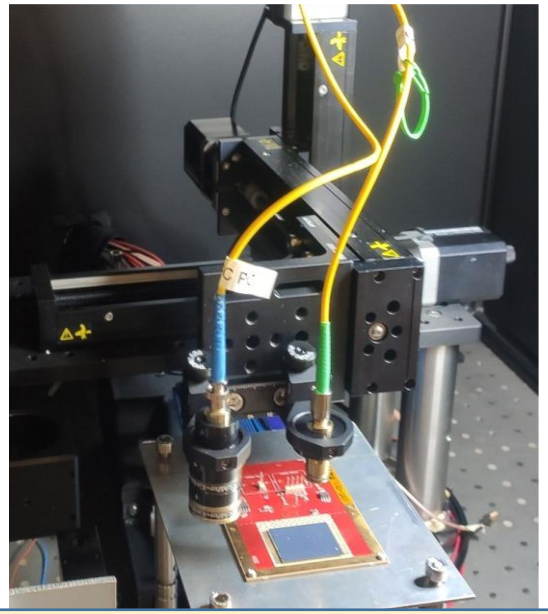
- Measured VCO oscillation frequency in Timepix4 using on chip Test Pulse circuitry
- Most of measured dispersion across chip due to power supply distribution (VCO design sensitivity of 1MHz/mV)
- VCO Calibration is required to get to the designed time resolution (~60psrms)
- Large improvement expected with TSVs





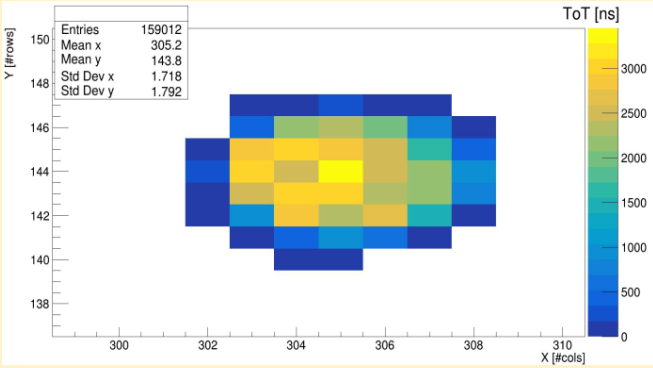
Timing resolution measurements of Timepix4V2 assembly with picosecond laser setup

- Setup:
  - Timepix4v2 bonded to a 100 µm n-on-p Si detector:
    - Biased at -150 V
    - Metallization with holes pattern
  - Pulsed Diode Laser PDL 800-B:
    - 1060 nm
    - Trigger simultaneously sent to laser and Timepix4 Trigger input



- Measurement:
  - After TOT timewalk correction and VCO calibration:
    - **Single pixel resolution** of **111 ± 1 ps**
    - **Cluster timing resolution** of **σ_{ToAAvg} = 49 ± 1 ps**

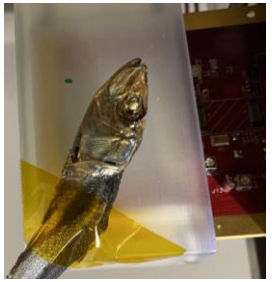
Preliminary!!!



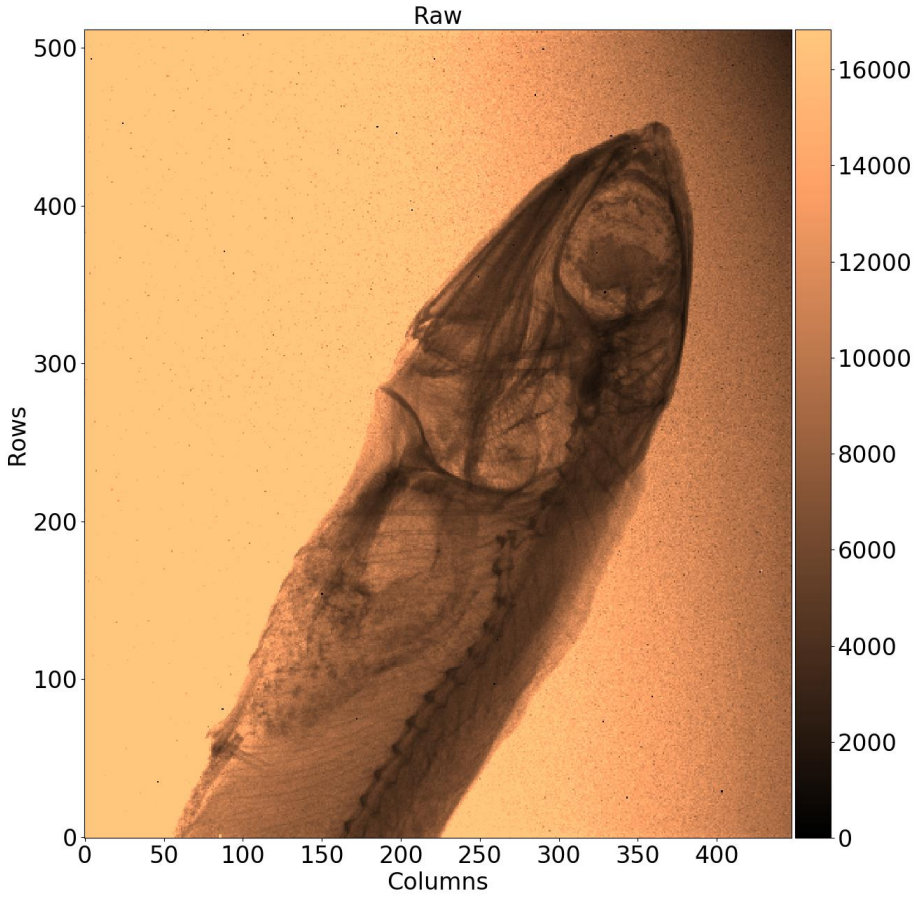
- σ = 1.4 pixel = 77 µm
- most of the charge is released in 4-5 pixels
- Wide range of released charge covered

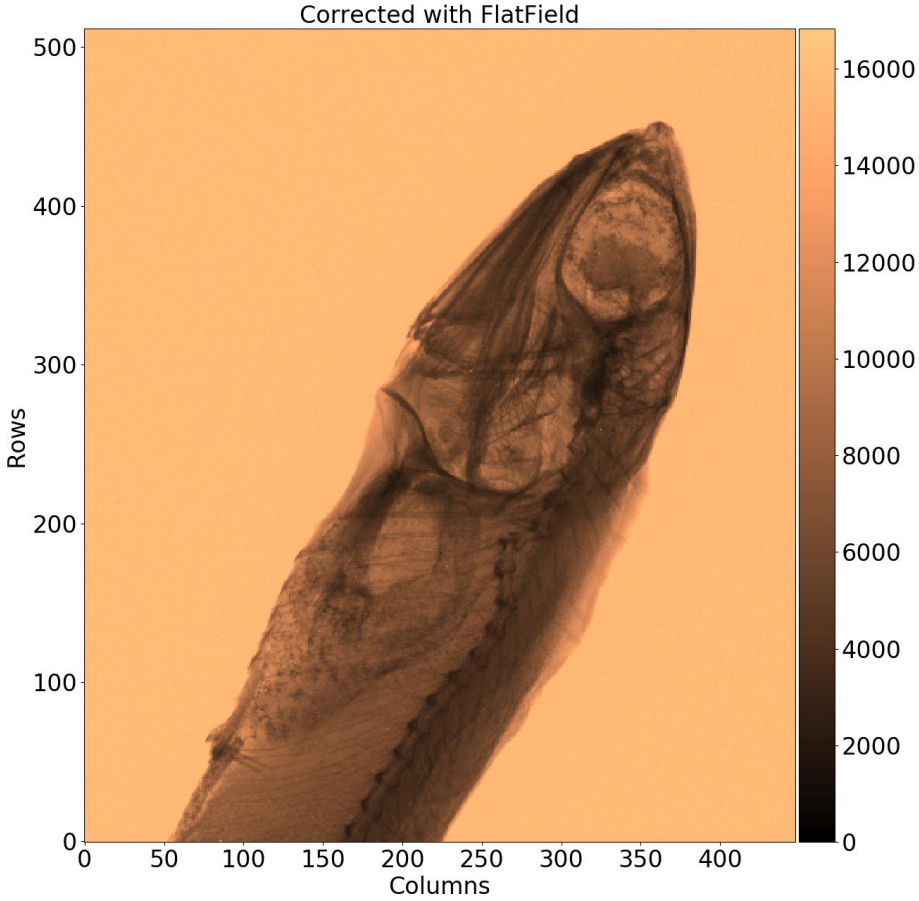
R.Bolzonella (INFN Ferrara)

Timepix4v1 with 300 µm Si Sensor Full sensor
[CRW 16-bit Frame Based mode, Thr ~1 ke-]



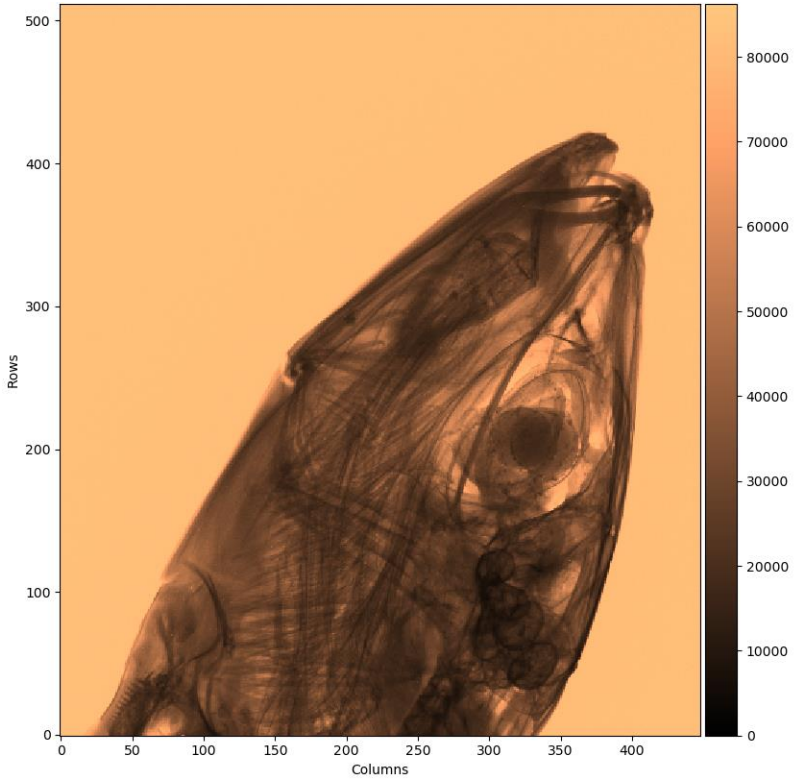
- 2s acquisition X-ray source, Cu target @30kVp
- 20 Flatfield acquisition used for correction
- Excellent bumping! Only 6 unconnected pixels (99.997% good pixels)

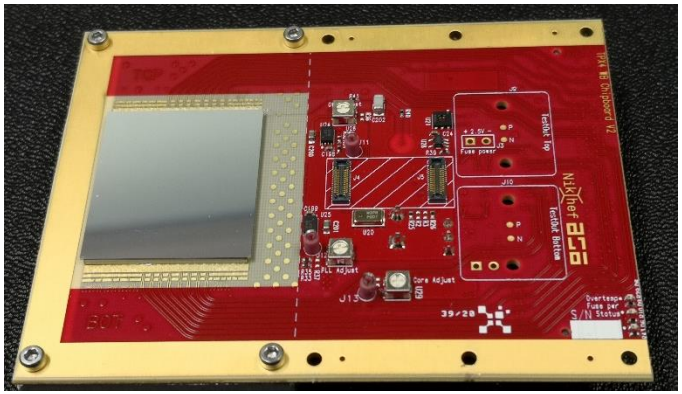




Conclusions

- **Timepix4** is the new particle-tracker and photon counting hybrid pixel detector designed with the support of the **Medipix4 collaboration**:
  - Large area hybrid pixel detector with **6.94 cm^2** sensitive area
  - 4-side buttable with **<0.5% dead area**
  - TOA: **23-bit dynamic range (1.6ms) with 195 ps LSB → 60ps$_{rms}$**
  - TOT: **15-bit dynamic range with ~200 e$^-$rms resolution**
  - PC: **8-bit or 16-bit CRW up to 5*10^9 hits/mm^2/s**
  - Readout: **Up to 160 Gbps readout bandwidth**
  - **Very configurable architecture** to accommodate many different applications
  - https://iopscience.iop.org/article/10.1088/1748-0221/17/01/C01044

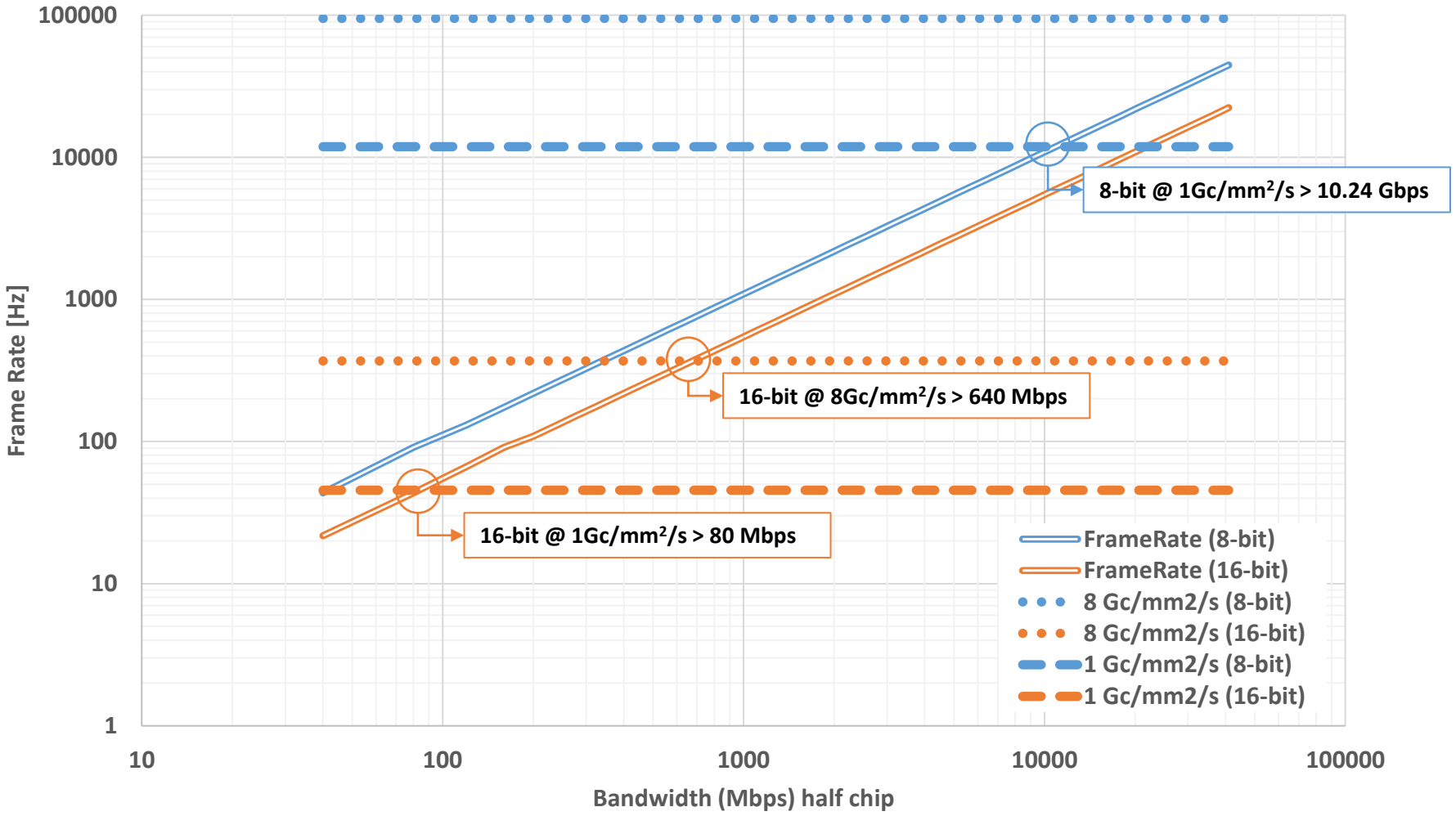




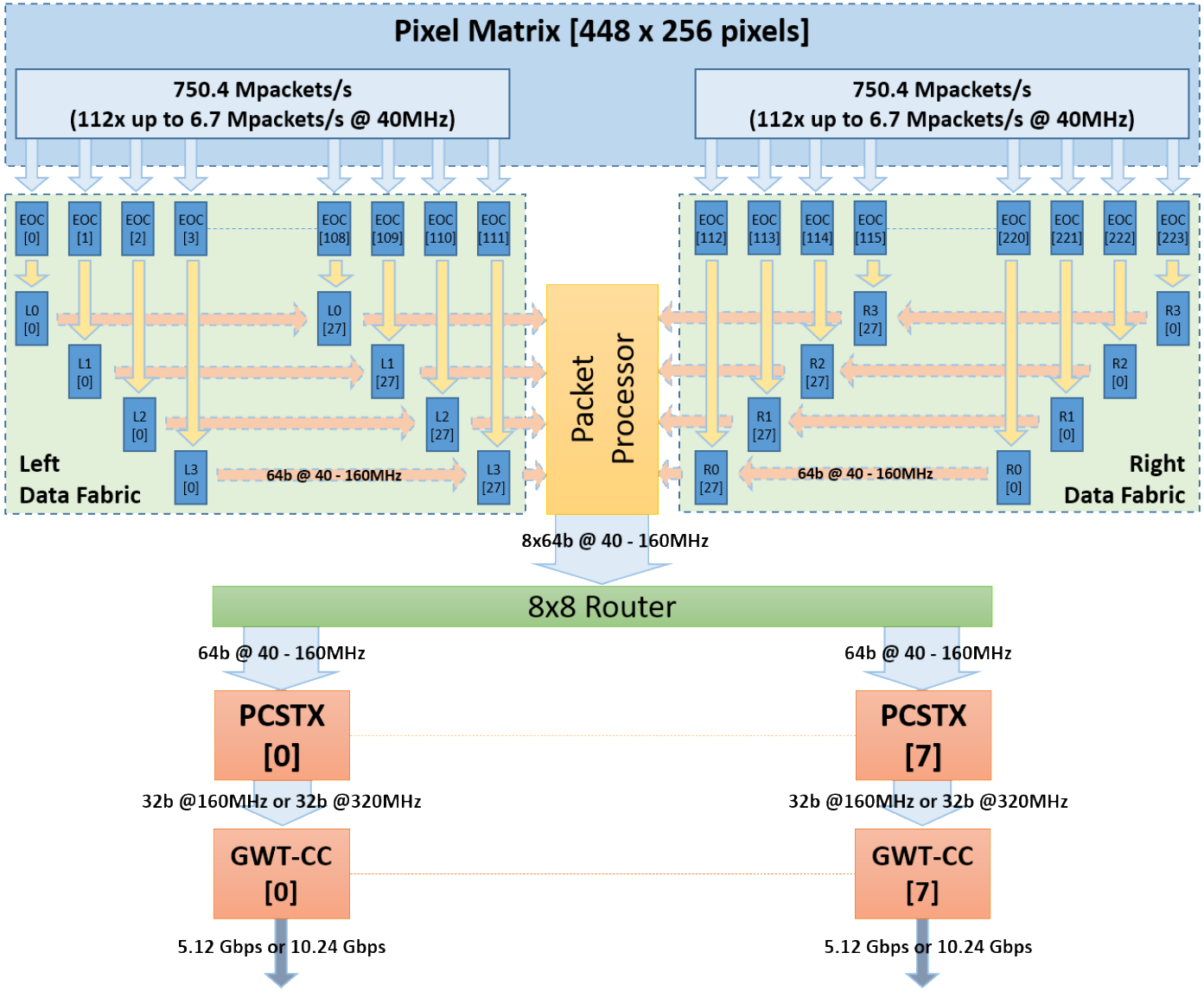
- **LA-Picopix** (https://cernbox.cern.ch/s/lko9y9zZNUGCHT3): Large area < 30ps$_{rms}$ particle tracking detector with on-chip clustering support, data-driven readout and 100Gbps output bandwidth → Q4/2025

SPARE

Frame Based CRW:
[Minimum output bandwidth before counter overflow]



Timepix4 edge peripheries

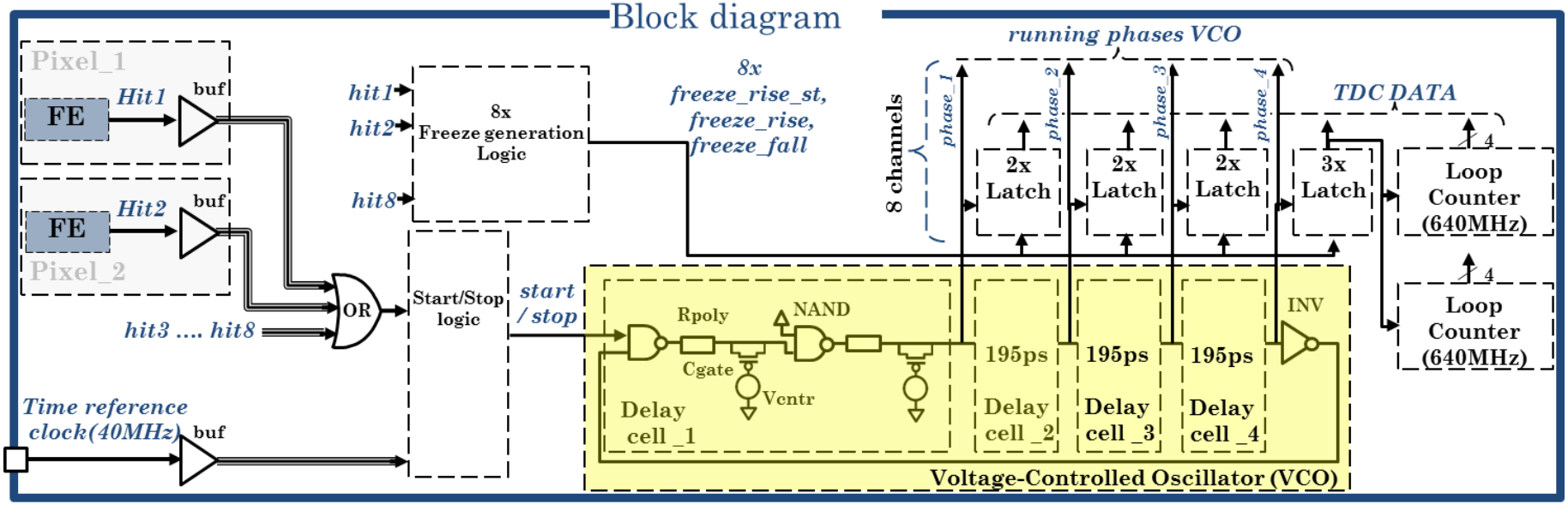


On-Pixel TDC

- Full digital Superpixel TDC implementation:
  - VCO:
    - full-custom designed (as in Timepix3) and characterized using Liberate
    - 640 MHz nominal frequency with 4-bit frequency adjustment (~40MHz range)
    - Nominal consumption ~600 µW (enabled)
  - Full digital integration with the rest of digital pixel

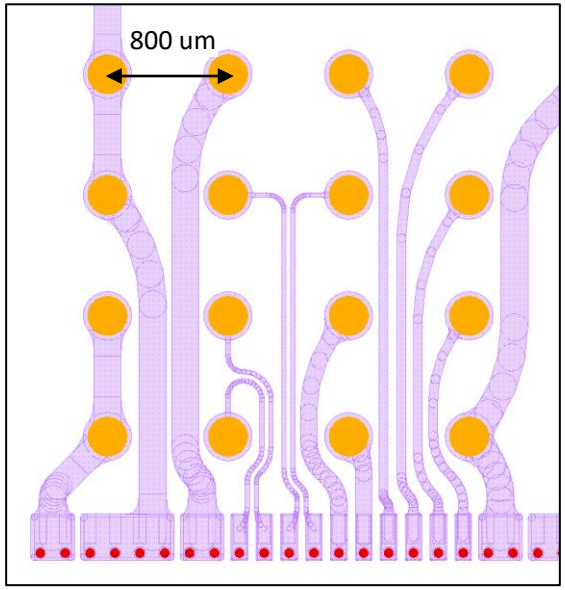
VCO Oscillation pattern

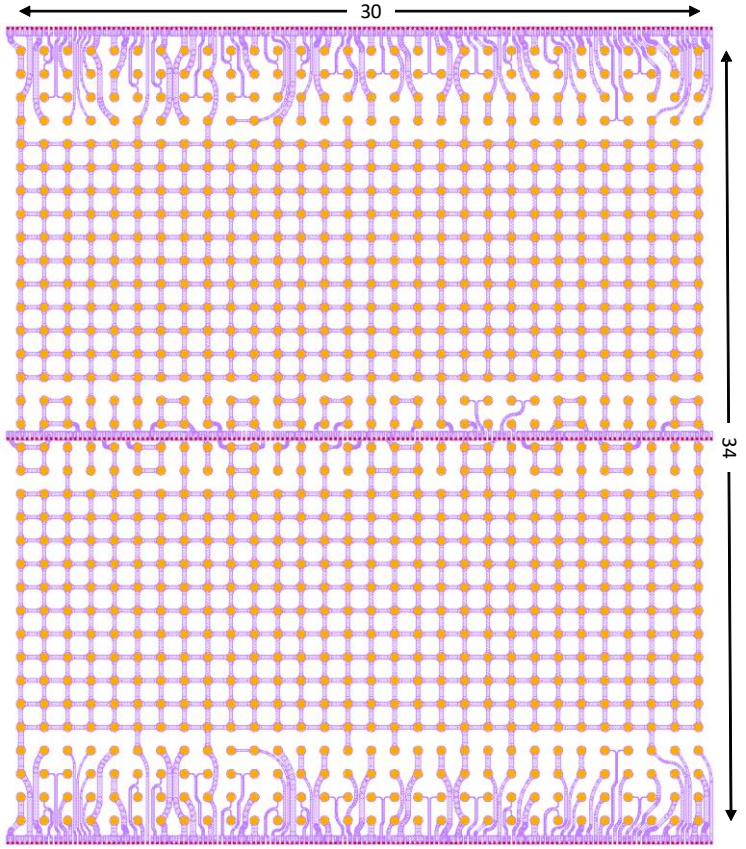
stage	Phase[3]	Phase[2]	Phase[1]	Phase[0]
0	1	1	1	1
1	1	1	1	0
2	1	1	0	0
3	1	0	0	0
4	0	0	0	0
5	0	0	0	1
6	0	0	1	1
7	0	1	1	1



TSV processing with Timepix4

- First Timepix4 TSV post-prcessing started in Q42021 with IZM
- Timepix4 to be interfaced through a 30x34 BGA array
- First samples expected by Q1-2 2023

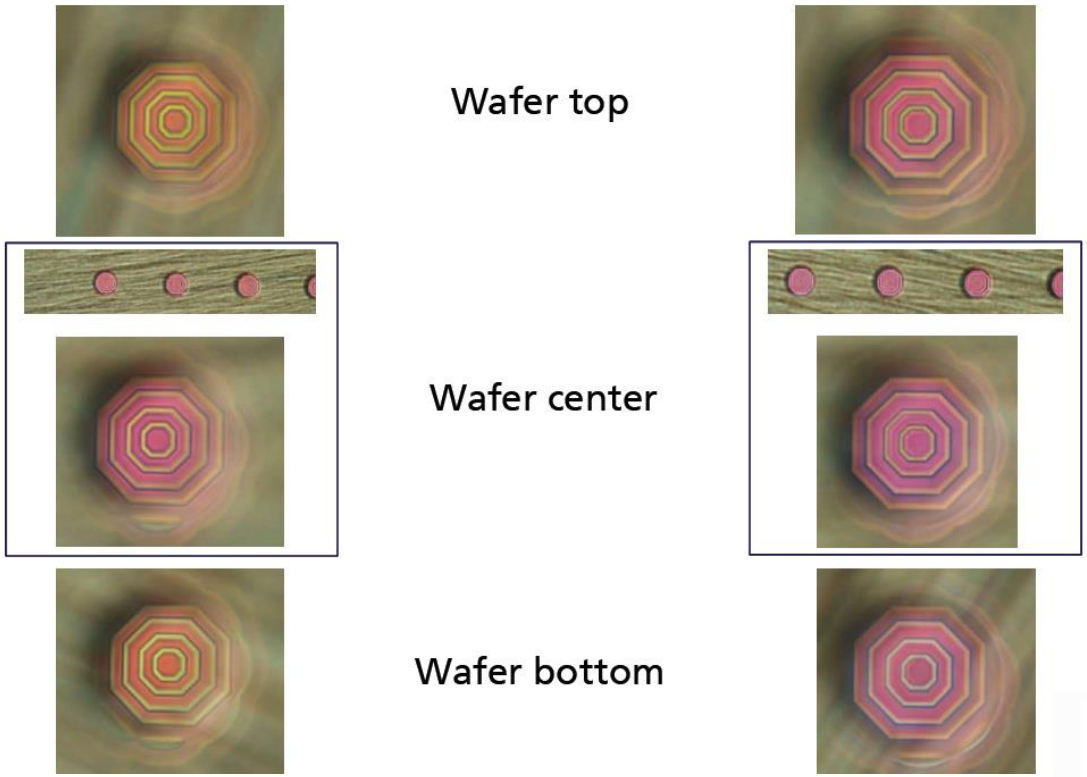




TIMEPIX4 wafer backside: TSV silicon etch

TIMEPIX4.0

TIMEPIX4.1

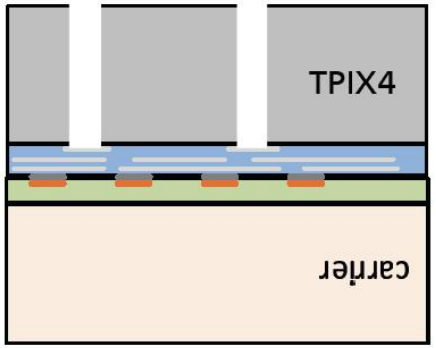


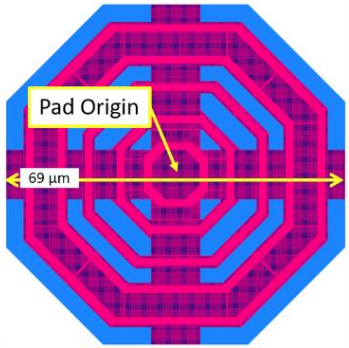
Wafer top

Wafer center

Wafer bottom

- TSV after Si etch
- view into TSV: M1 landing pad magnification 500x

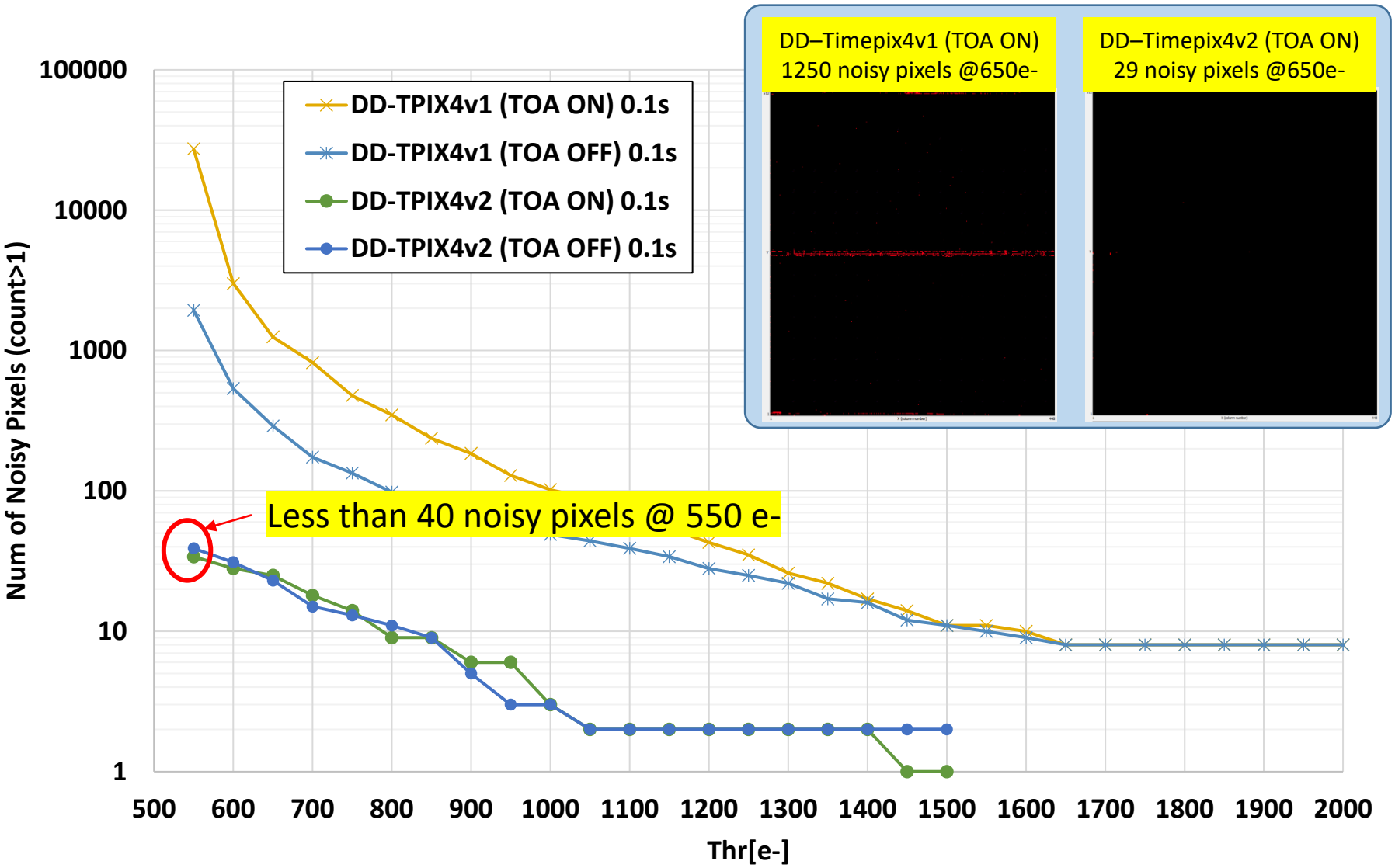




Thomas Fritzsch, Wafer Level System Integration

Timepix4v1 and v2: Number of Noisy pixels (>1 count)

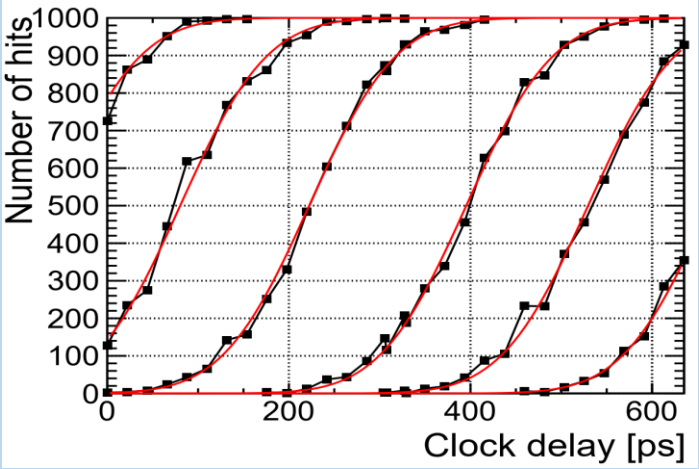
Data-Driven mode [DD]



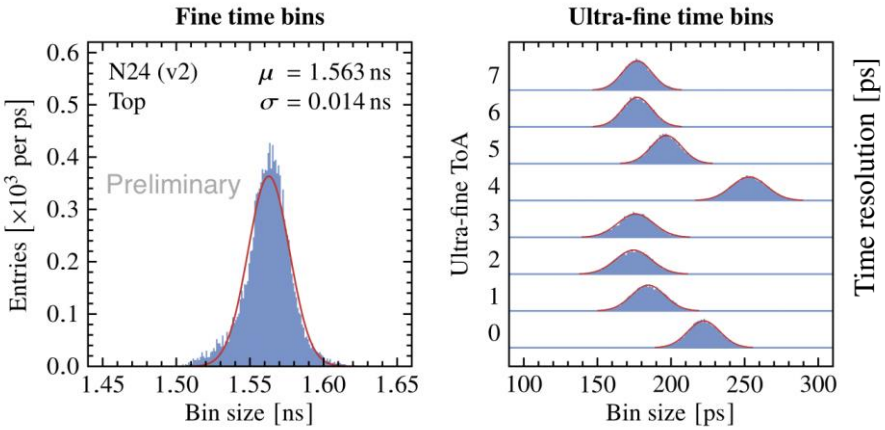
Timimg performance with Test Pulse measurements

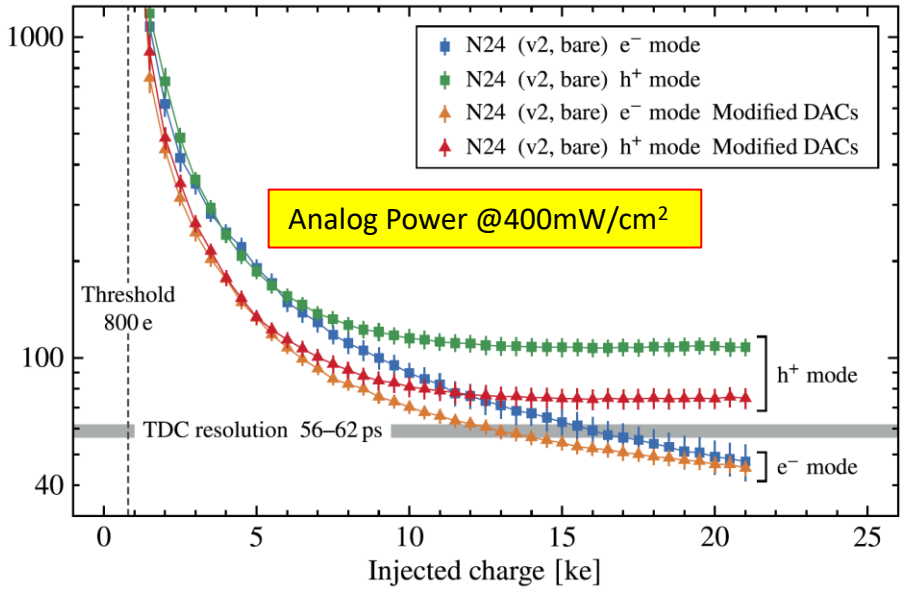
- Timepix4v2
- Using DDLL in bypass mode:
  - Controlled delay step of ~5.1ps
- Test on first 4 rows of pixels of both edges
- Allows for precise UFTOA measurement

K. Heijhoff (Nikhef)



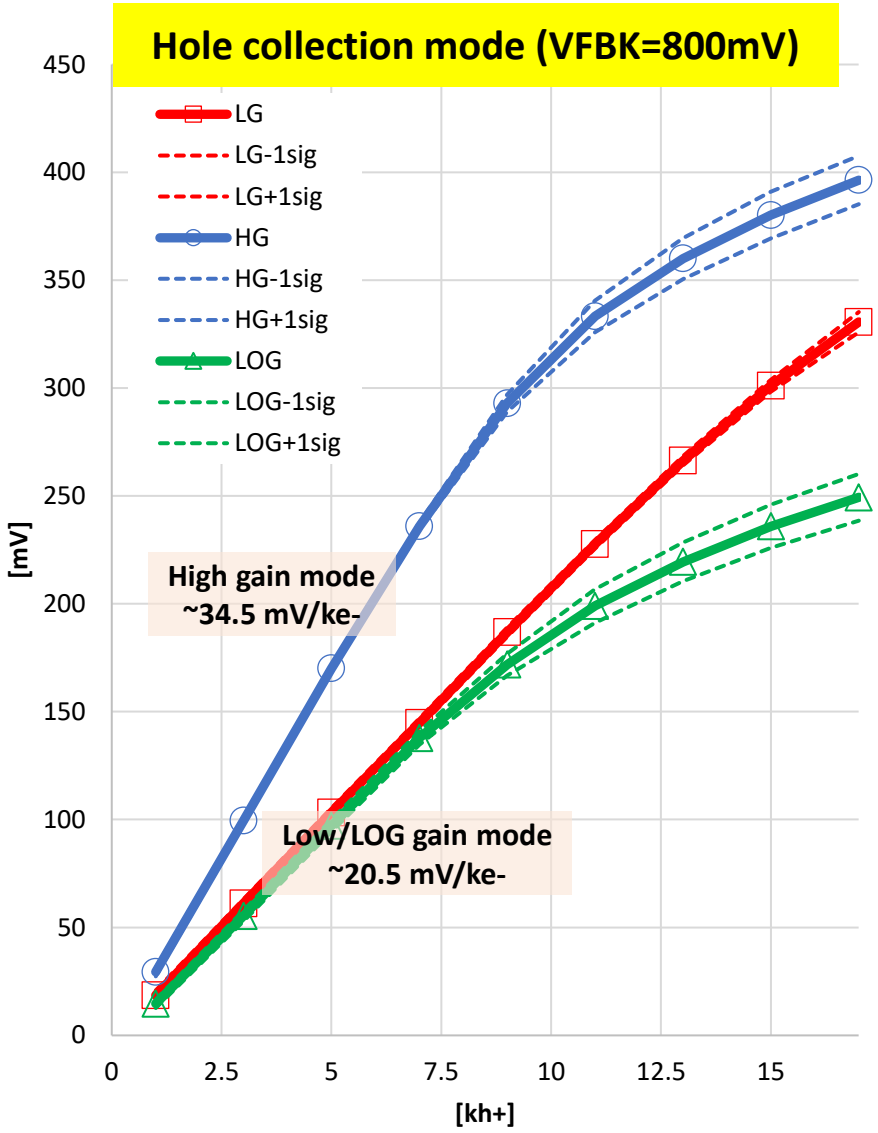
UFTOA bins shows a small non uniformity at bin 4 and 0

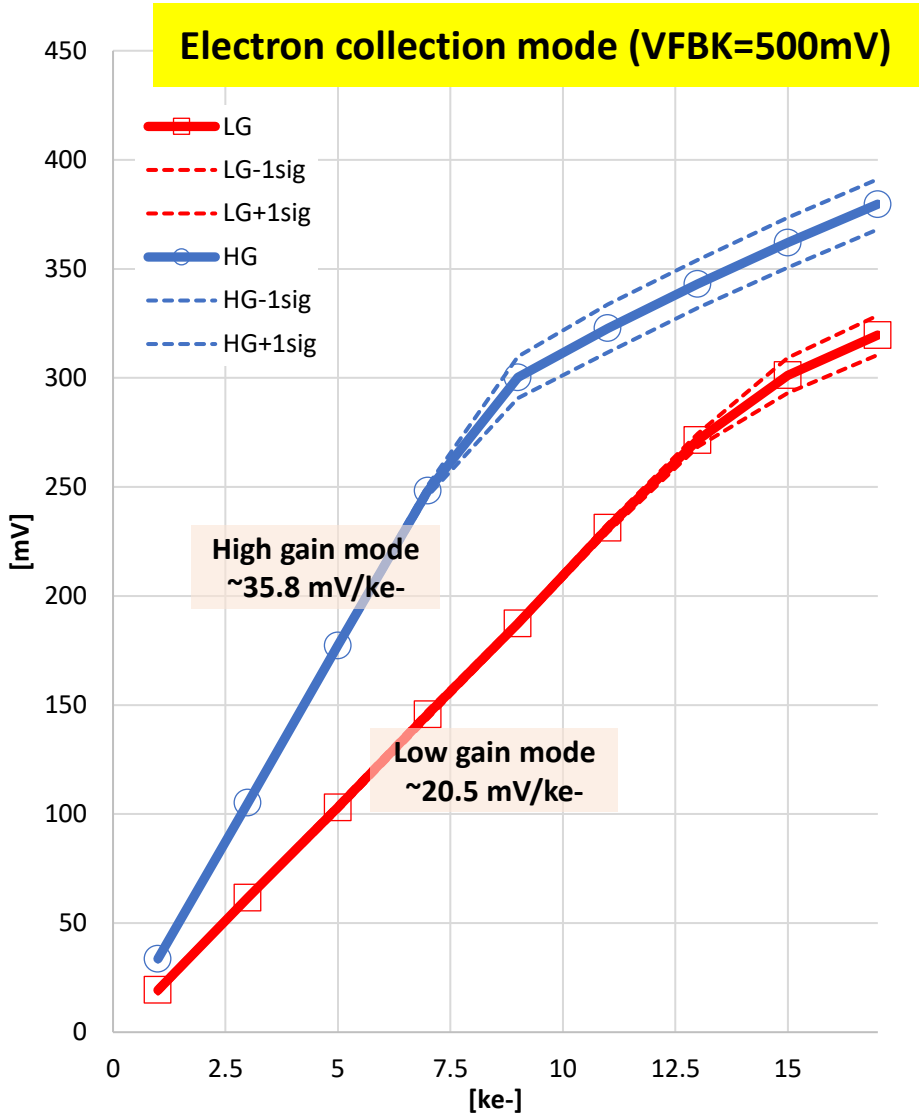




Gain slopes for different FE Gain

[TOA-TOT, ~200 pixels]

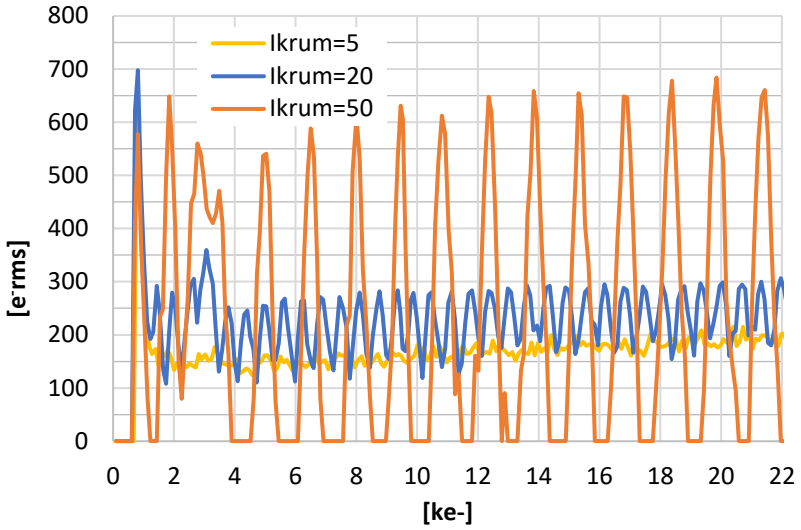


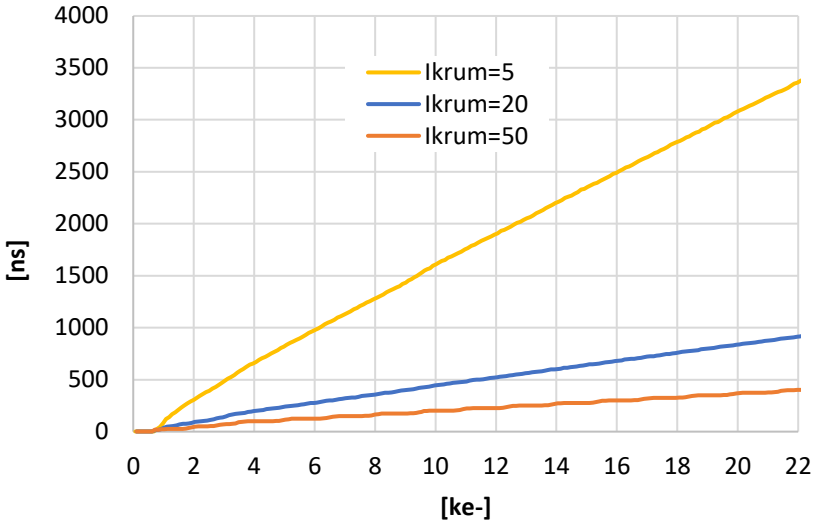


TOT Resolution

[Data-Driven 1 pixel, average of 200 events/TP, HG e-]

TOT (Timepix3)





TOT-HD (Timepix4)