ASIC design challenges
with a focus on precise timing

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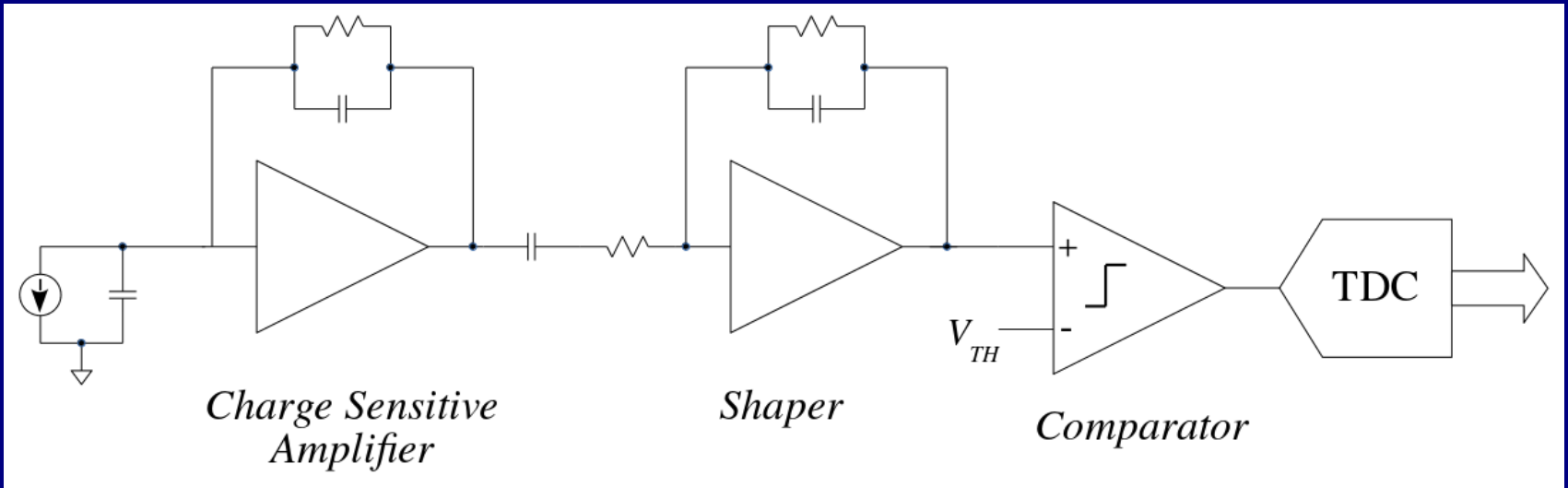
Basic techniques for timing measurements

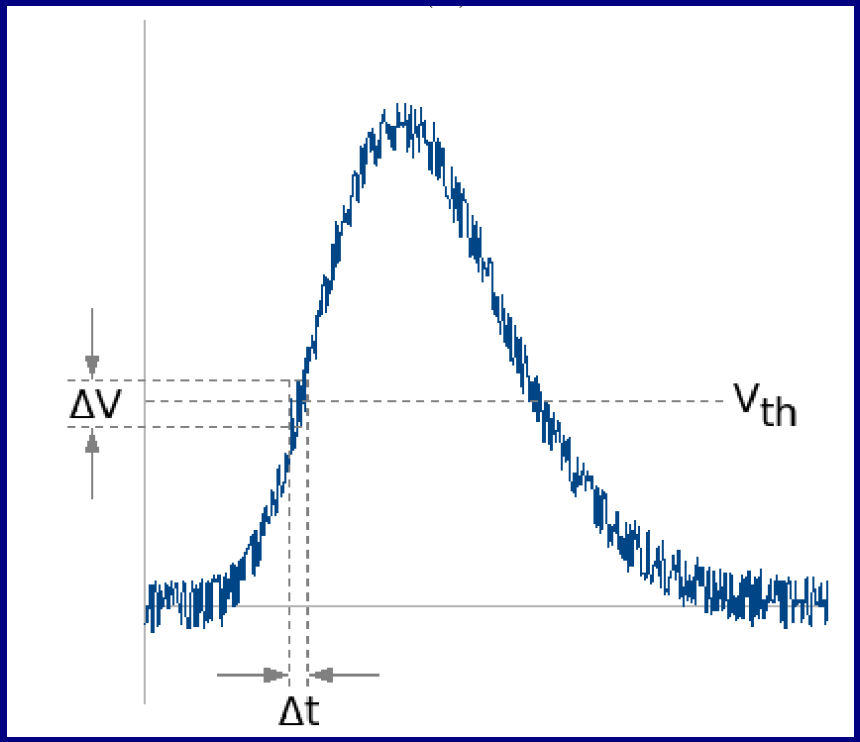
- Single sampling
  - Simpler system
  - Lower power
  - Lower data throughput
  - Requires time walk compensation
  - Requires pile-up management
- Multiple sampling
  - Digital post-processing
  - Provides both time and charge informations
  - Possibility to remove common noise
  - Requires high performance ADC

Timing systems: single sample



- The sensor signal is usually amplified and shaped
- A comparator generates a digital pulse
- The threshold crossing time is captured and digitized by a TDC
- TDC can be embedded on the front-end chip or external
- Timing is derived from a single sample

Time jitter - single sampling



$$\sigma_T = \frac{\sigma_V}{\frac{\Delta V(t)}{\Delta t}}$$

$$\frac{\Delta V(t)}{\Delta t} \approx \frac{V}{t_r} \rightarrow \sigma_T = \frac{t_r}{SNR}$$

$$t_r \propto \frac{1}{BW}, SNR \propto \frac{1}{\sqrt{BW}}$$

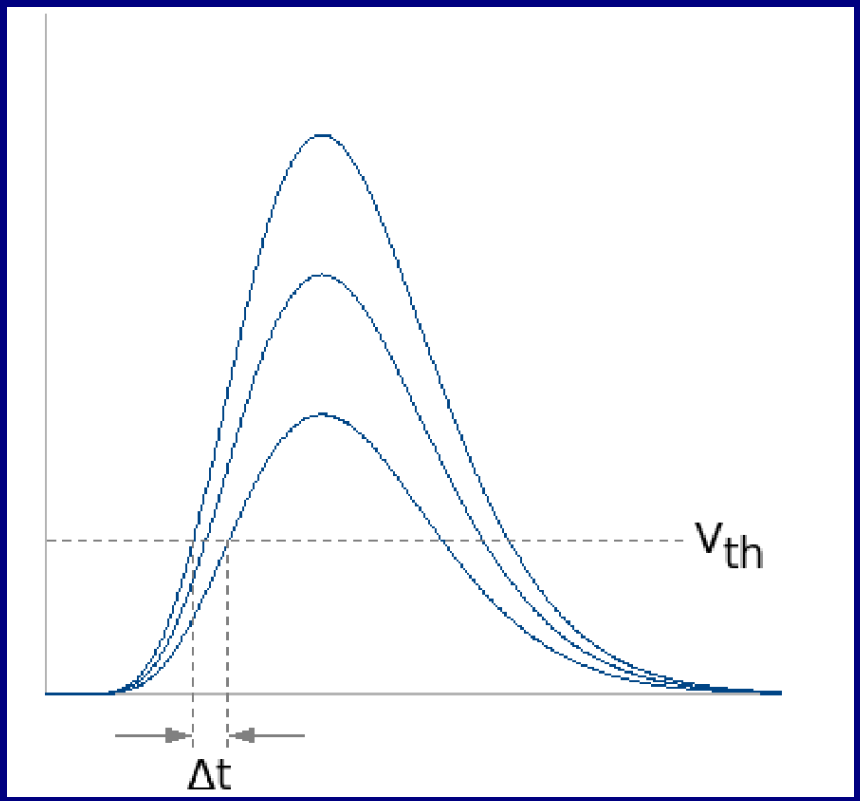
$$\sigma_T \propto \frac{1}{\sqrt{BW}}$$

- The front-end rise time should be matched to the sensor collection time

$$t_r = 1\ ns, SNR = 10 \rightarrow \sigma_T = 100\ ps$$

$$t_r = 40\ ns, SNR = 20 \rightarrow \sigma_T = 2\ ns$$

Time walk

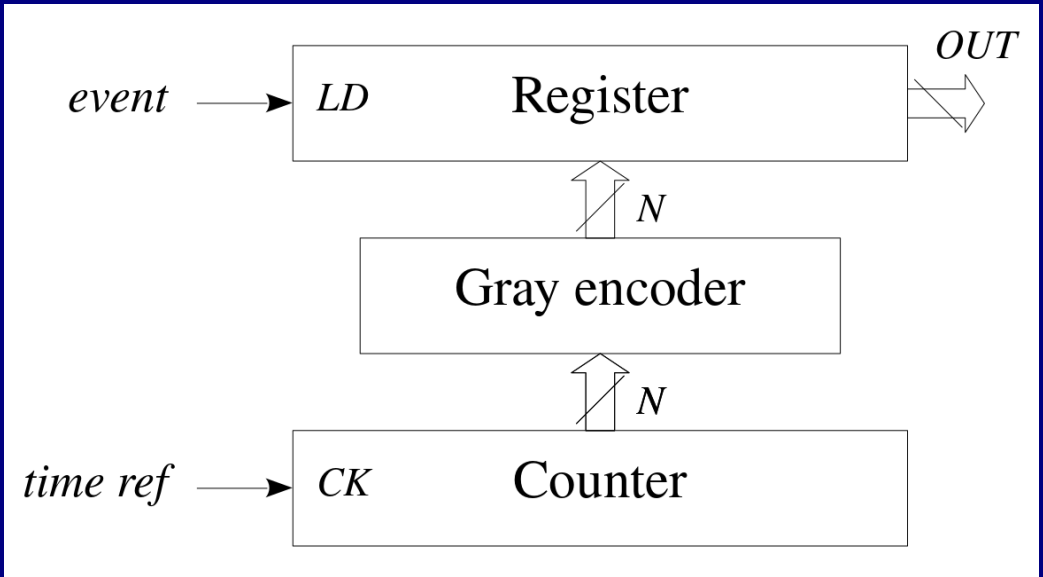


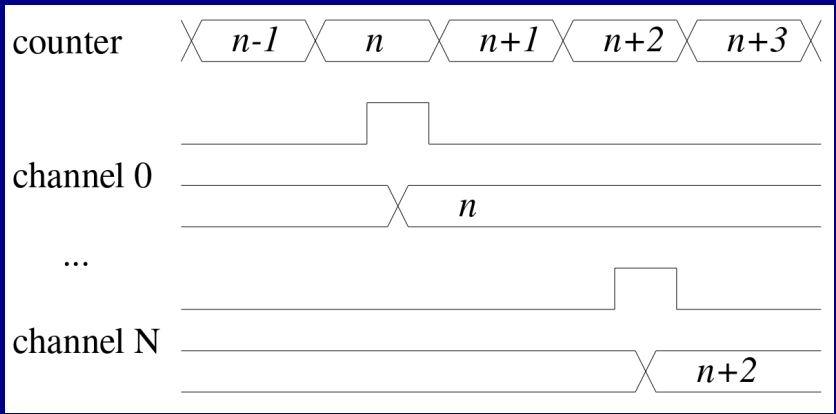
$$\Delta T = \tau_P ln\left(\frac{2k}{2k-1}\right)$$

$$k = \frac{V_P}{V_{Pmin}}$$

- Pulses of same shape and different amplitude crosses the threshold at different times
- Large variations if SNR is low
- Even worse if also the signal shape changes
- Time walk introduces an error in time measurement
- Correction techniques :
  - Amplitude correction
  - Zero crossing comparator
  - Constant fraction discriminator

Simplest TDC : digital counter





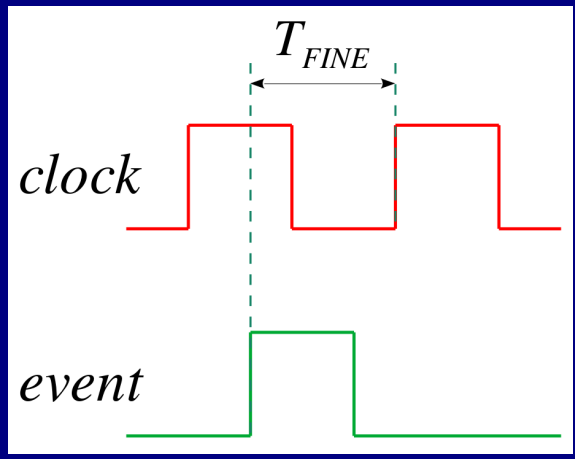
- Free running counter
- Upon hit arrival, the counter state is stored in a register
- Gray-coded counter if the hit is not synchronized with the clock
- Easy to extend to multiple channel - *caveat : power consumption*
- Time precision is limited by the clock period

$$\sigma_{TDC} = \frac{T_{CK}}{\sqrt{12}}$$

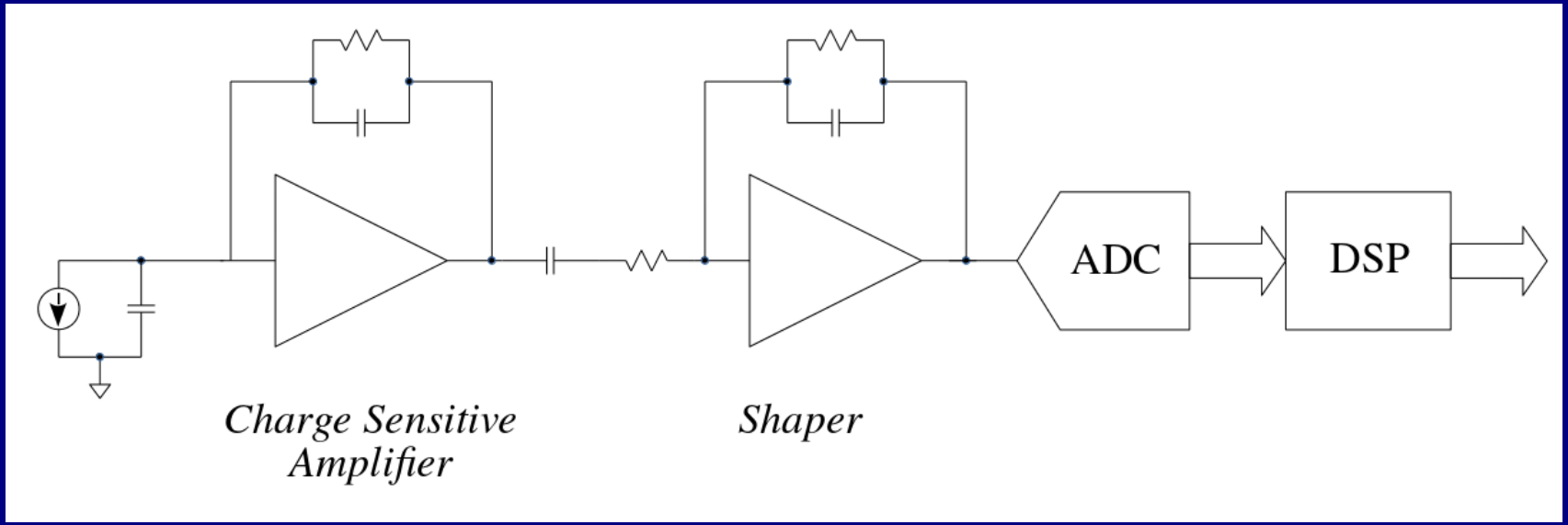
- *e.g. 1 ns resolution (i.e. 290 ps r.m.s.) requires a 1 GHz clock*

How to improve the resolution beyond the clock period

- Counter-based TDC ok for resolutions down to few ns, an additional circuit is required to measure the time elapsing between the event and the next clock transition
- Techniques to move into the ps resolution :
  - PLL, DLL
    - Closed loop system
    - Clock cleaning, clock multiplication (PLL)
    - Long delay chains (DLL)
    - Complex, high power
  - TAC
    - Simple, high time resolution
    - Dead time
  - Vernier line
    - High time resolution
    - Based on gate delays (PVT variations)
    - Long delay chains
  - Interpolation, RC delays



Timing systems: multiple samples

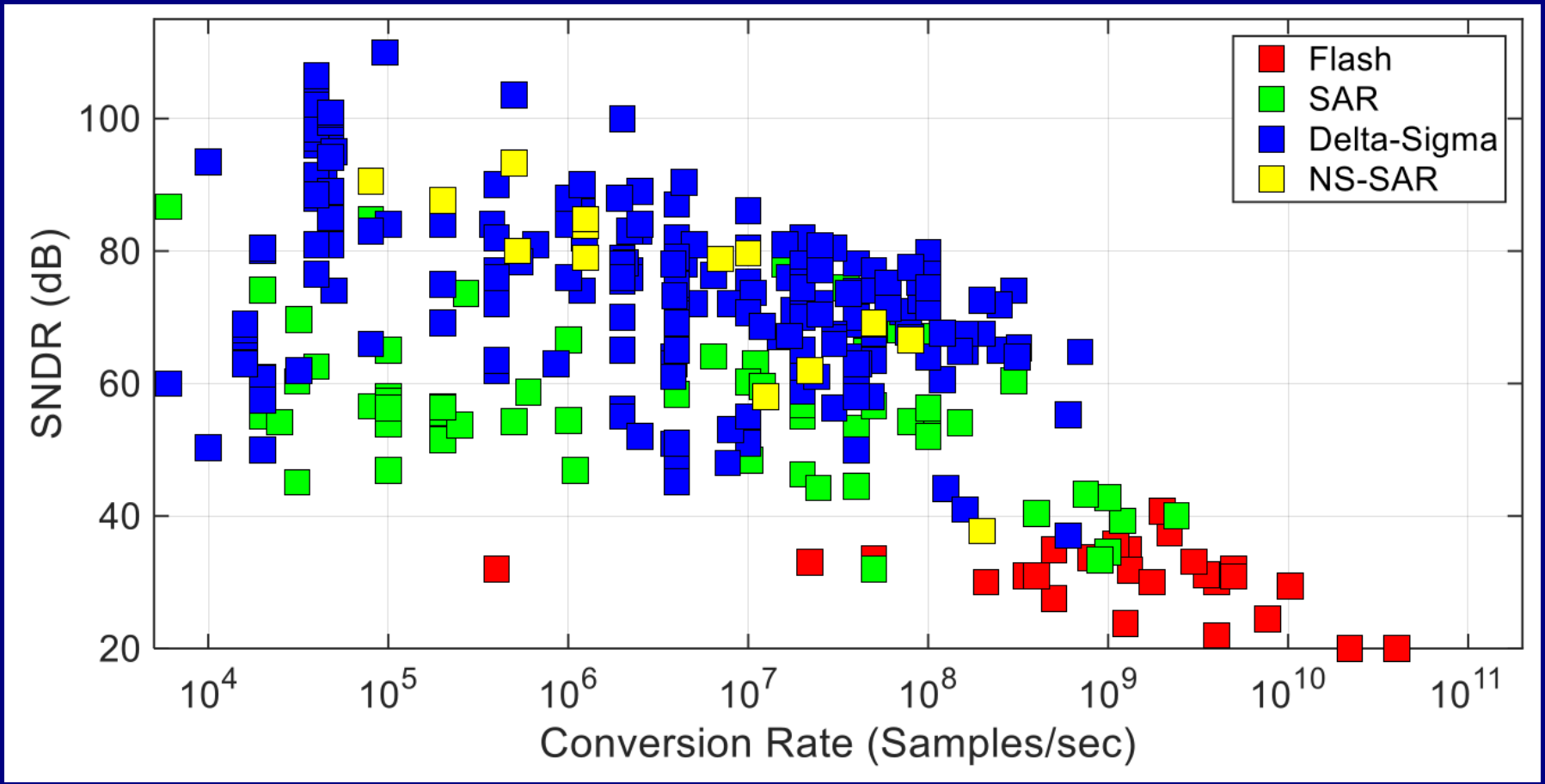


- The sensor signal is usually amplified and shaped
- The full waveform is sampled and digitized at high speed
- A high performance ADC is required
- In many systems, sampling and digitization are decoupled
- Timing is extracted with DSP algorithms from the digitized waveform samples
- Timing is derived from multiple samples

Choice of the sampling rate

- f_S : in principle the higher the better
  - *but increases cost, power consumption and data throughput*
- Shannon's theorem : $f_S > 2 \cdot f_{MAX}$
  - Mandatory for digital filtering
  - f_{MAX} is much higher than the -3 dB bandwidth
  - Not easy to calculate f_{MAX} from the pulse basic parameters (t_r,t_f,FWHM)
  - Anti aliasing filters
- Oscilloscope manufacturer rule of thumb : $f_S > 5 \cdot f_{MAX}$
- To emulate "analogue-like" timing algorithms, a minimum of 3 samples on the trailing edge are required. More samples allow the use of simpler algorithms
- If $f_S >> 2 \cdot f_{MAX}$, the extra samples can be used to decrease the quantization noise (oversampling)

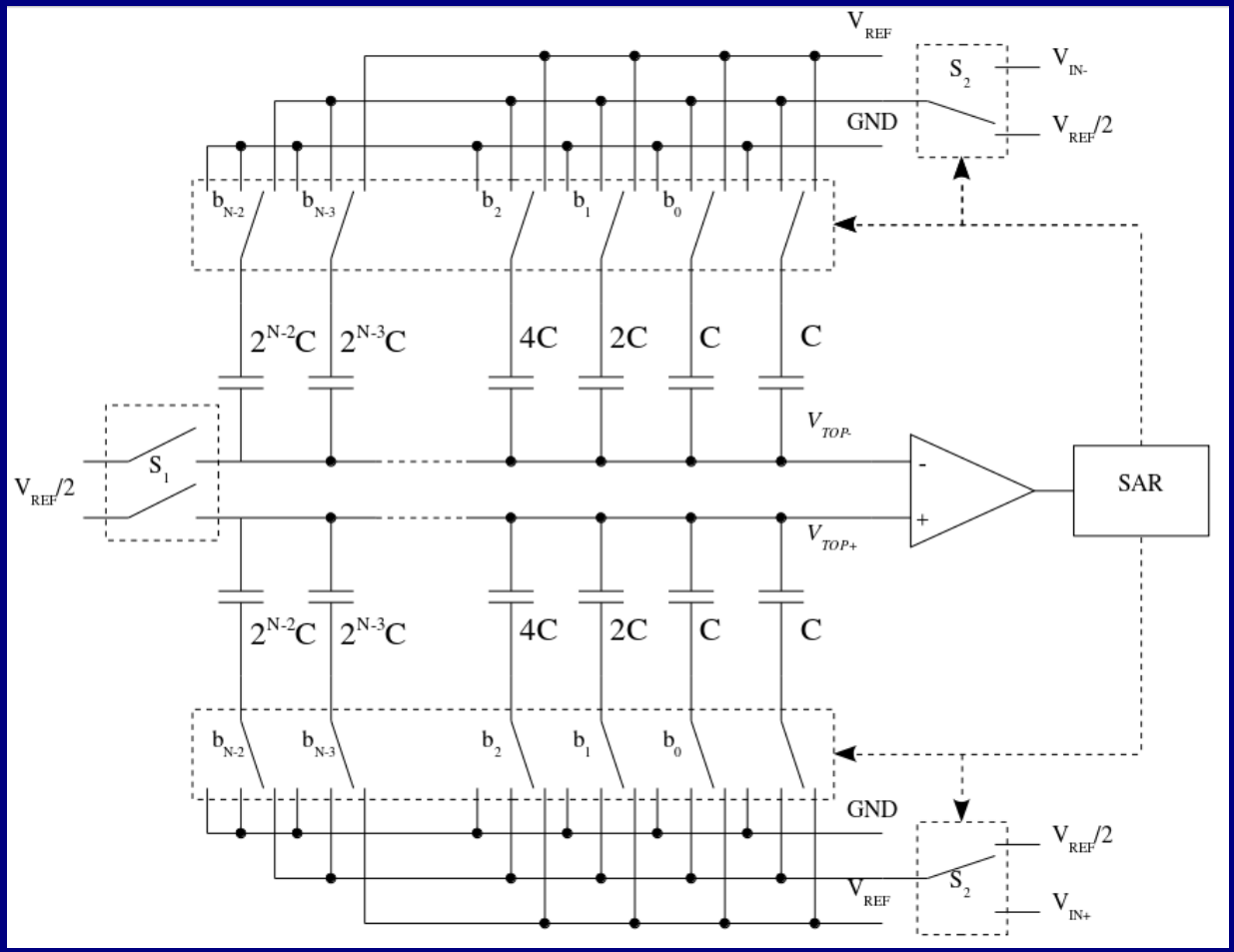
Comparison between ADC architectures



$$SNDR = 6.02 \times N + 1.78$$

B. Murmann, "ADC Performance Survey 1997-2023," [Available Online]

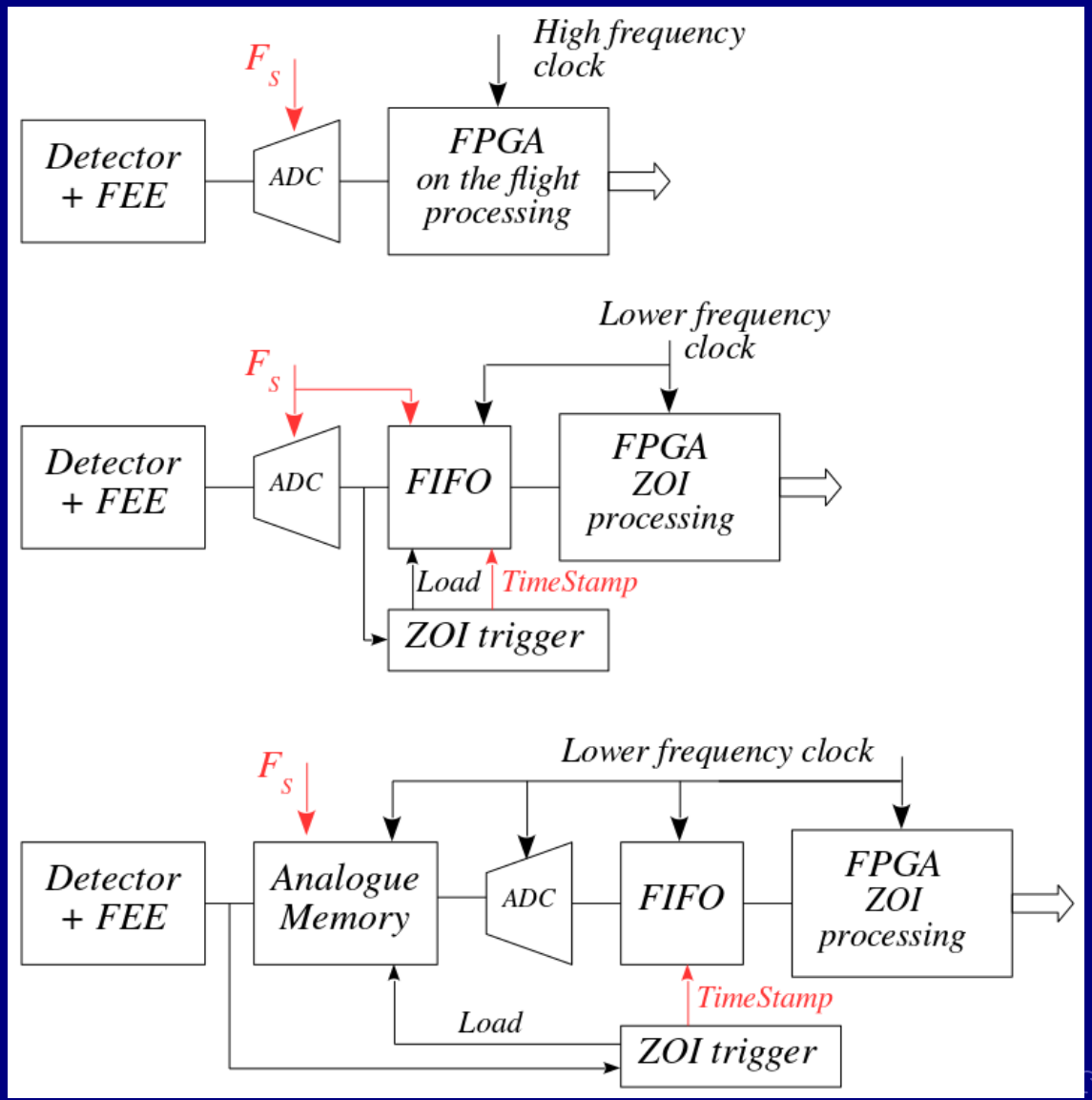
Successive approximation ADCs with capacitive DAC



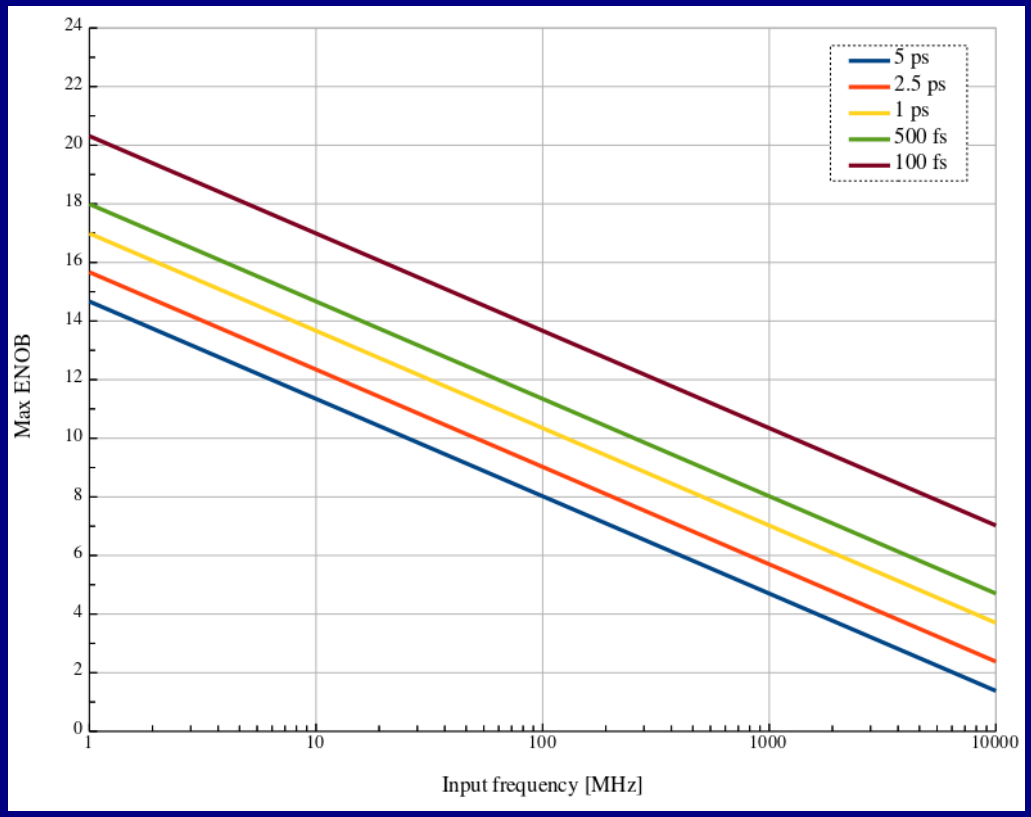
- Resolutions : 8-14 bits, sampling frequency : few hundreds MS/s
- Calibration required for N$>$10 bits
- Conversion in N-clock cycles (+sampling time). Often requires a PLL

Multiple sampling : possible architectures

- Continuous DAQ
  - All the data are acquired at the sampling rate
  - The result is obtained after a fixed latency
  - Require a continuously sampling ADC
  - 12 bits, 1 GS/s $\rightarrow$ 12 Gb/s per channel
- Zone of Interest DAQ
  - Require a trigger logic
  - Strong data rate reduction
  - No fixed latency
  - No full rate ADC if an analogue memory is used.



Maximum ENOB *vs* input frequency



$$SNR_{ideal} = 20log_{10}\left[\frac{1}{2\pi f_{sig} t_j}\right]$$

$$SNR_{bits} = [6.02N + 1.76]$$

f_{sig} : *signal maximum frequency*

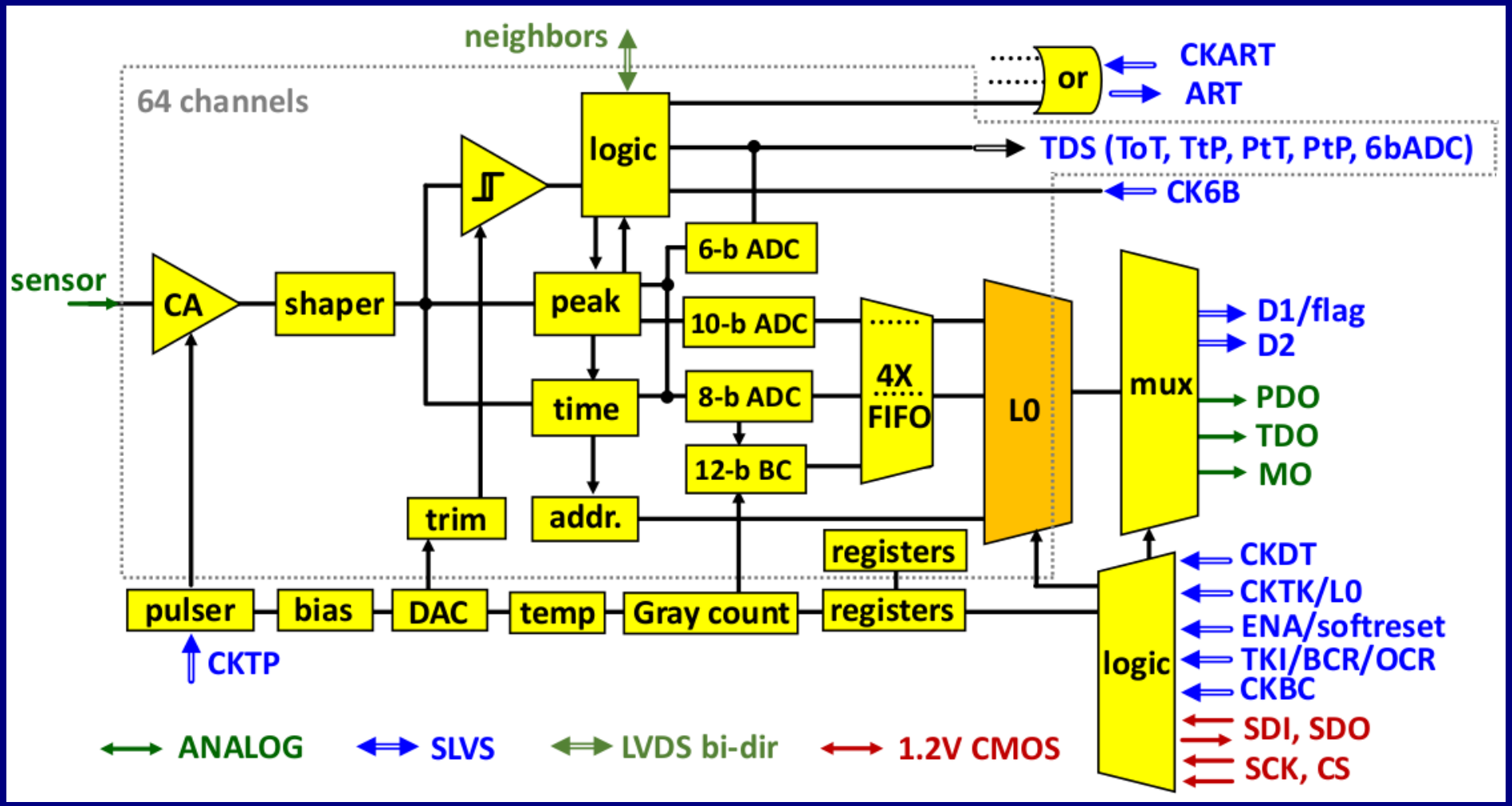
t_j : *r.m.s. jitter*

N : *number of bits*

Note :

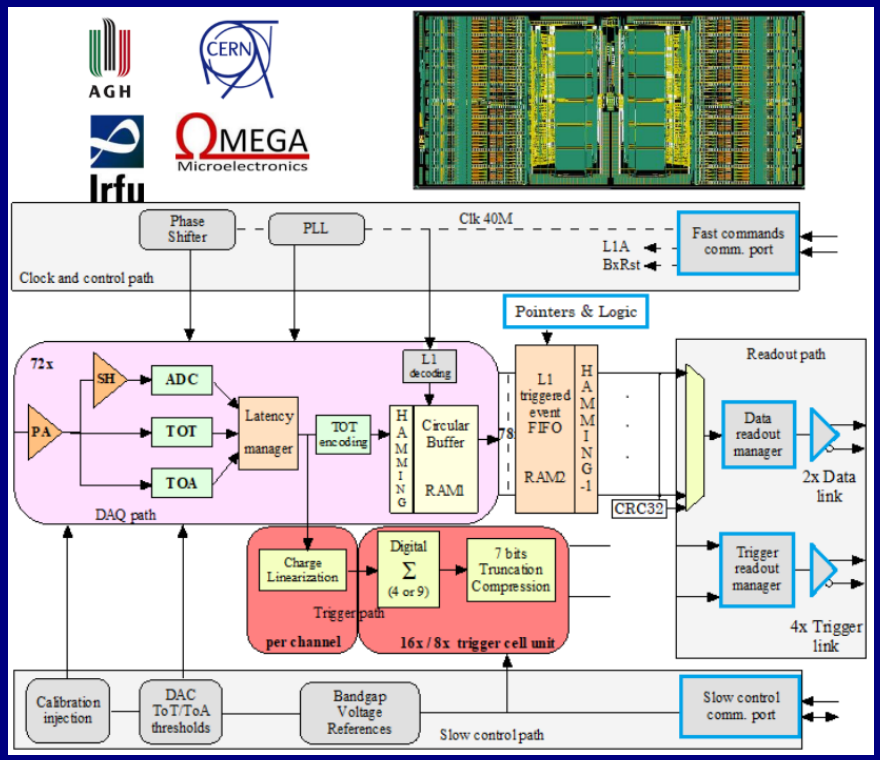
- f_{sig} is the **signal** (not the **sampling**) frequency
- ENOB always smaller than ADC resolution (includes errors and non-linearity)

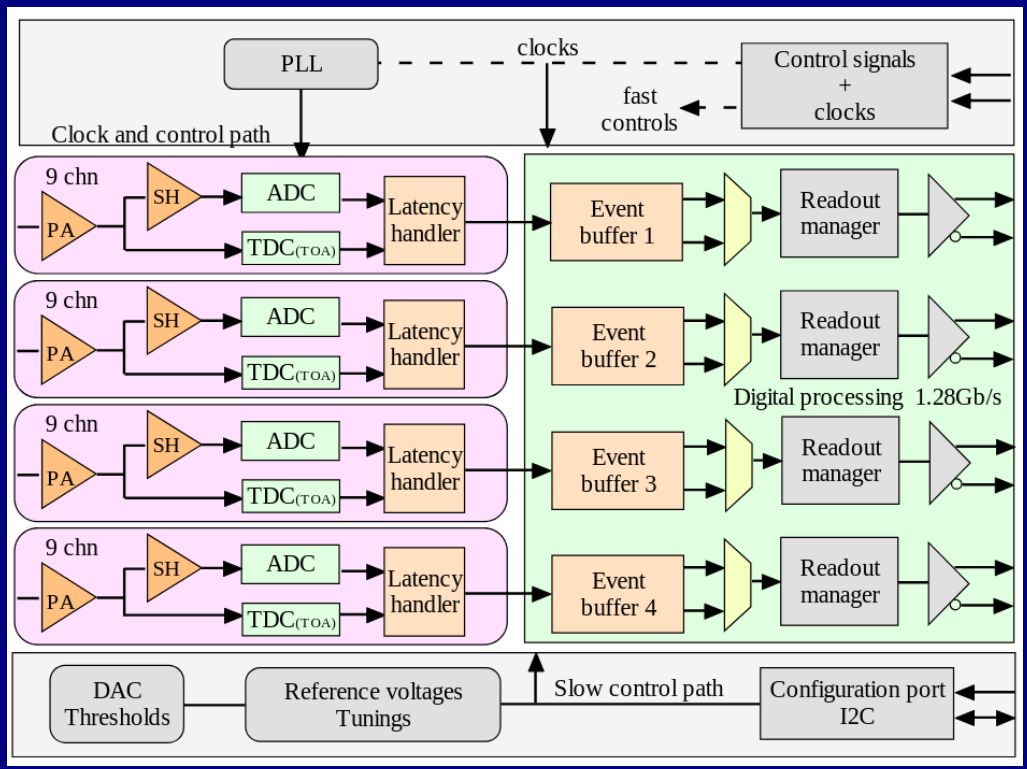
Design example : VMM3



G. De Geronimo, *Prospects for VMM4*, RD51 Collaboration Meeting, Dec. 4-8 2023

Design example : HGCROC/HKROC

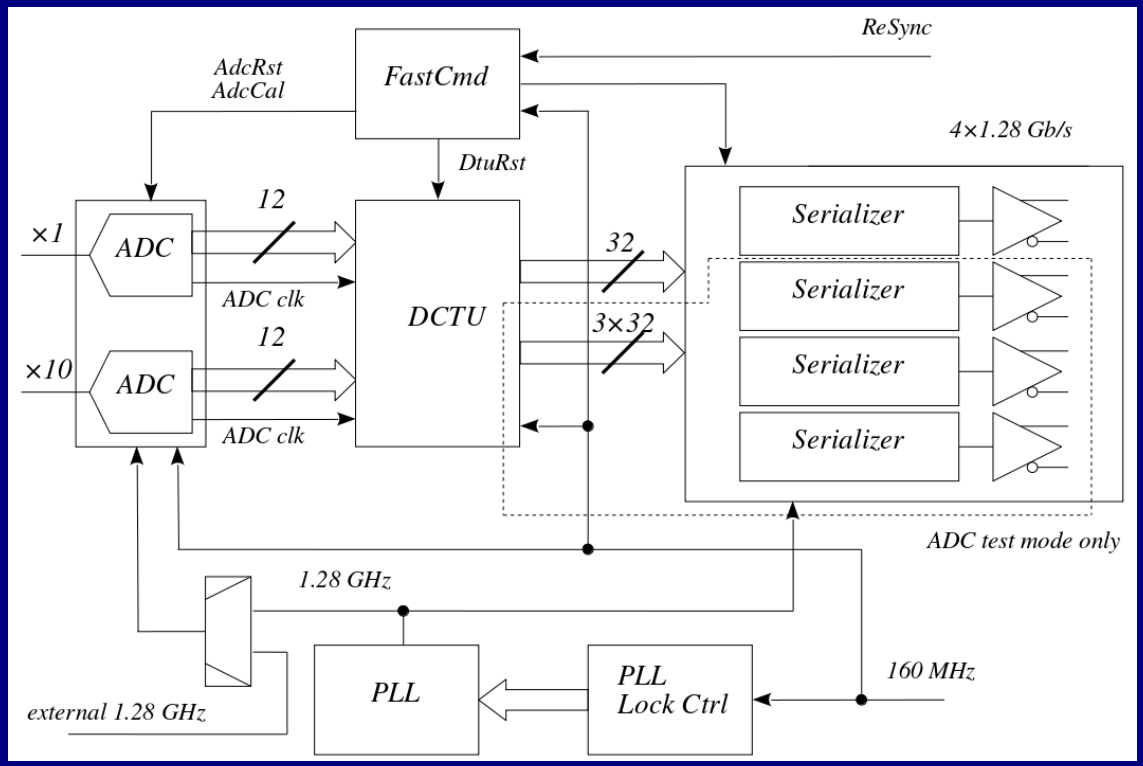




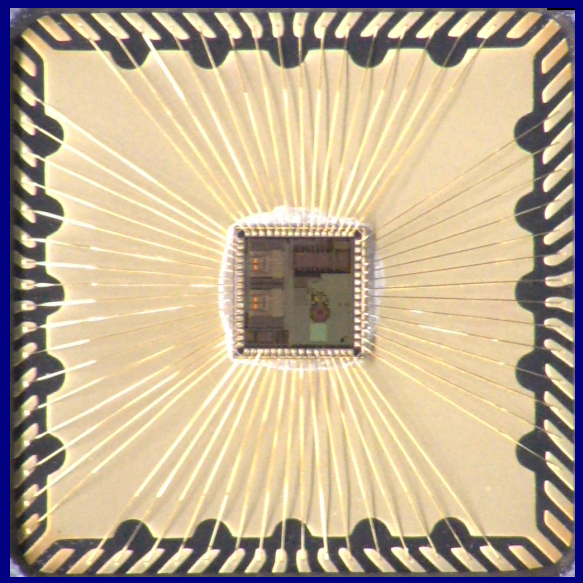
- ADC : 40 MS/s 10 bit (AGH Krakow), ToT to extend dynamic range
- Peak waveform sampling

C. De La Taille, *ASICs for 5D calorimetry at Ω*, 16^{th} Pisa meeting May 27-31 2024

Design example : LiTE-DTU



- Two 12 bits, 160 MS/s ADCs (designed by Renesas)
- Clock multiplication PLL (from LpGBT)
- Technology : CMOS 65 nm



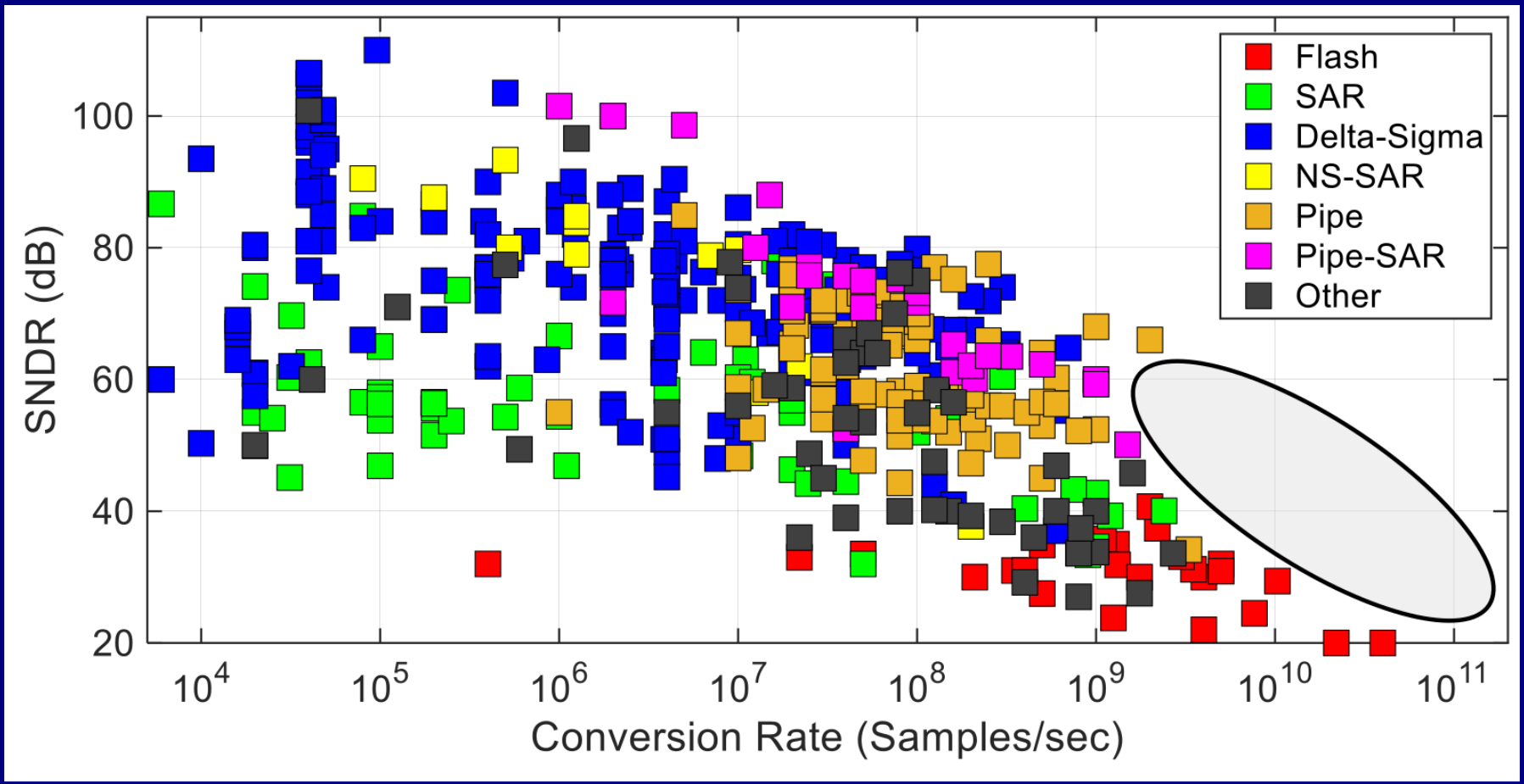
- Data Compression and Transmission Unit
- Fast command and lock control units
- 1.28 Gb/s serializers

Conclusions

- Time measurements : two main architectures
  - Single sample
  - Waveform sampler
- Single sample
  - Relative simple system
  - Time-walk correction required
  - Pile-up events can be difficult to detect
  - Key element : TDC
- Waveform sampler
  - Better signal reconstruction
  - Higher complexity and power requirements
  - High data rate
  - Key element : ADC
- Slow event rate allows for less demanding architectures

Backup slides

Extension with Time Interleaving



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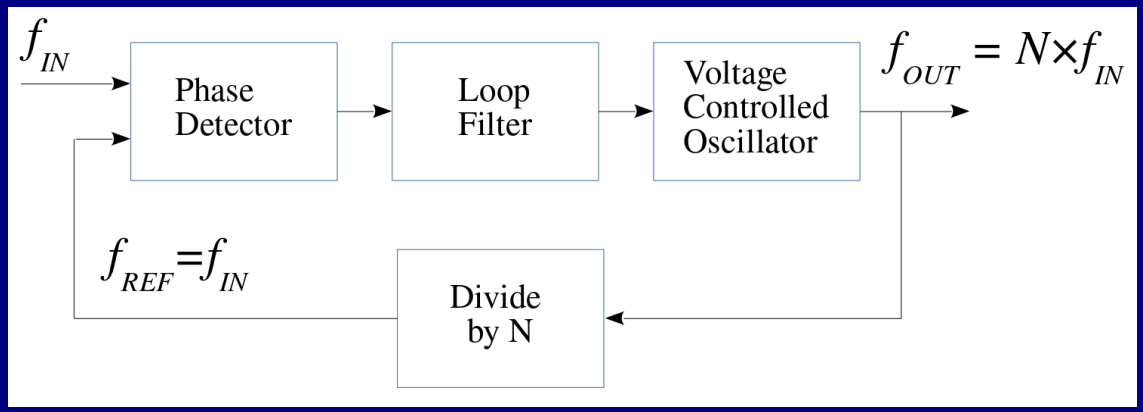
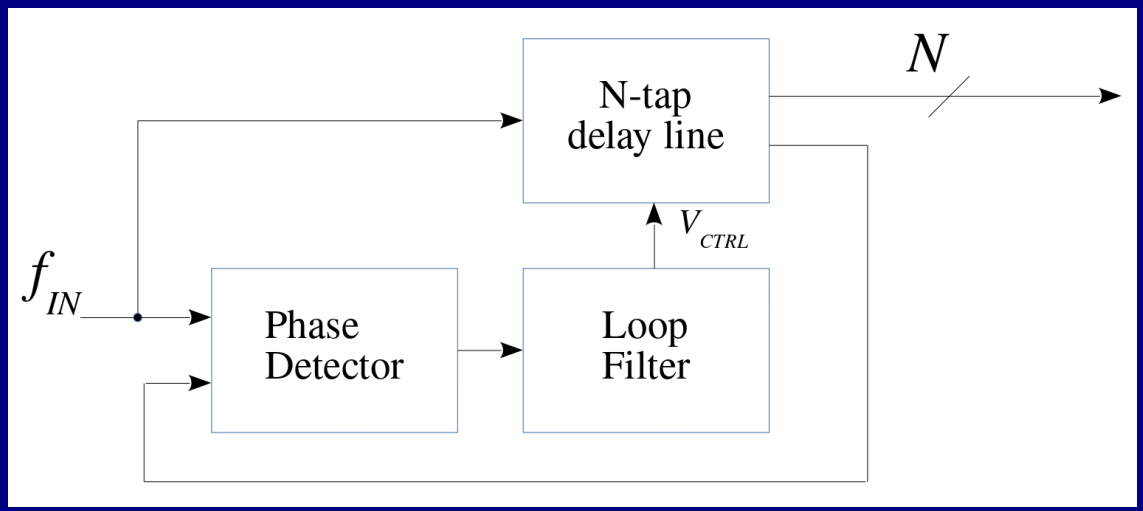
PLL and DLL

PLL



DLL



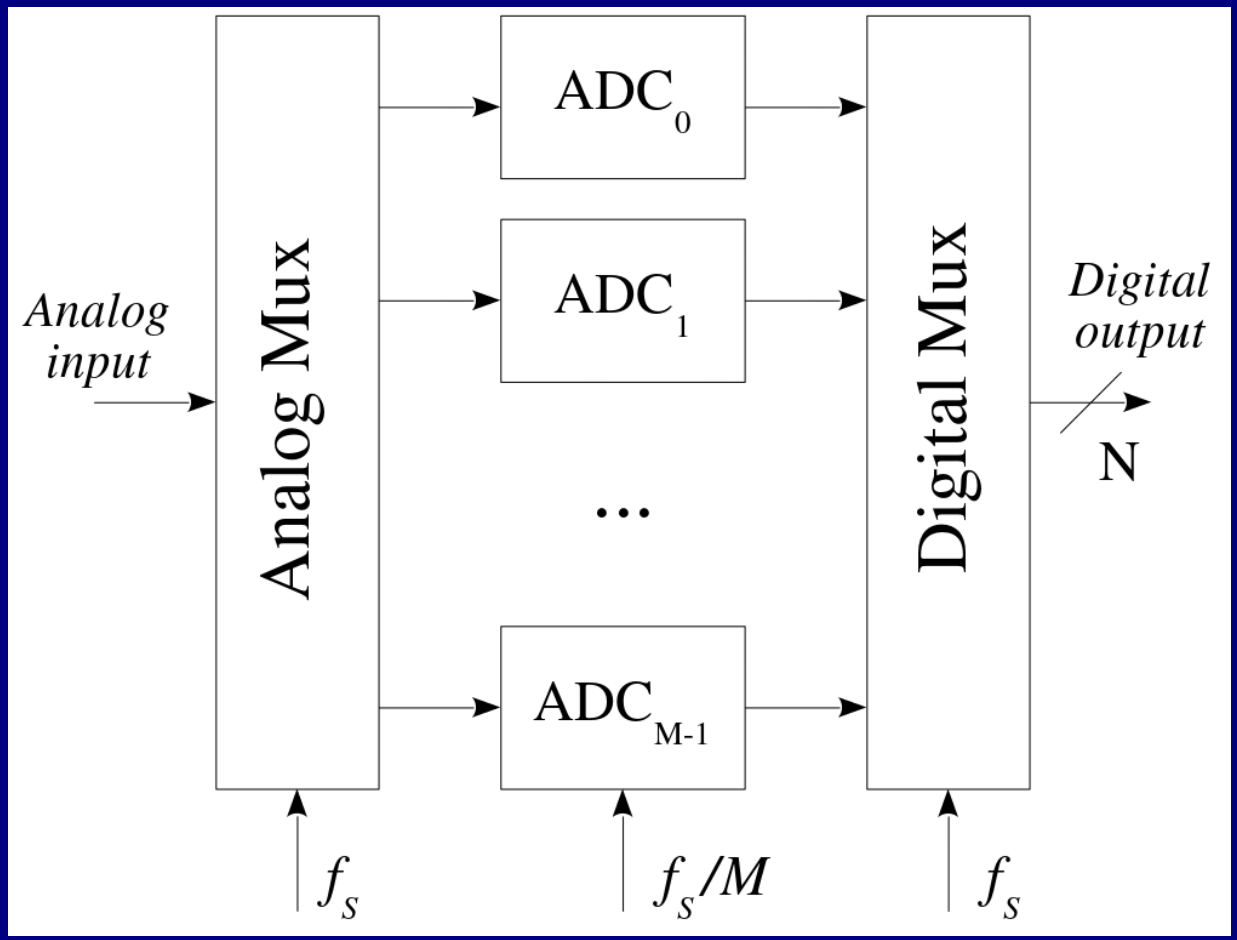
PLL

- Can improve clock jitter
- Key element is the VCO

DLL

- Does not improve clock jitter
- Long delay lines
- Simpler to design

Time interleaved converters



- Widely used in DSO
- Analog mux performances critical
- ADC intercalibration required