MPGD Electronics From R&D to ATLAS NSW

George Iakovidis

2nd DRD1 Collaboration Meeting & Topical Workshop on Electronics for Gaseous Detectors
June 19, 2024

Intro

- The VMM Frontend
- The NSW and evolution of VMM
- Architecture and issues along the way
- Implementation in SRS, applications
- Production
- Remarks

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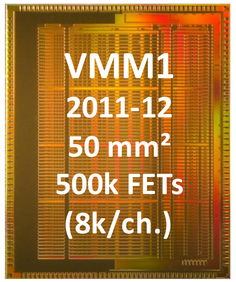
The VMM frontend!



- **Mixed-signal**
- 2-phase readout with external ADC
- **peak** and **timing** information
- neighboring readout
- sub-hysteresis **discrimination**
- few timing outputs

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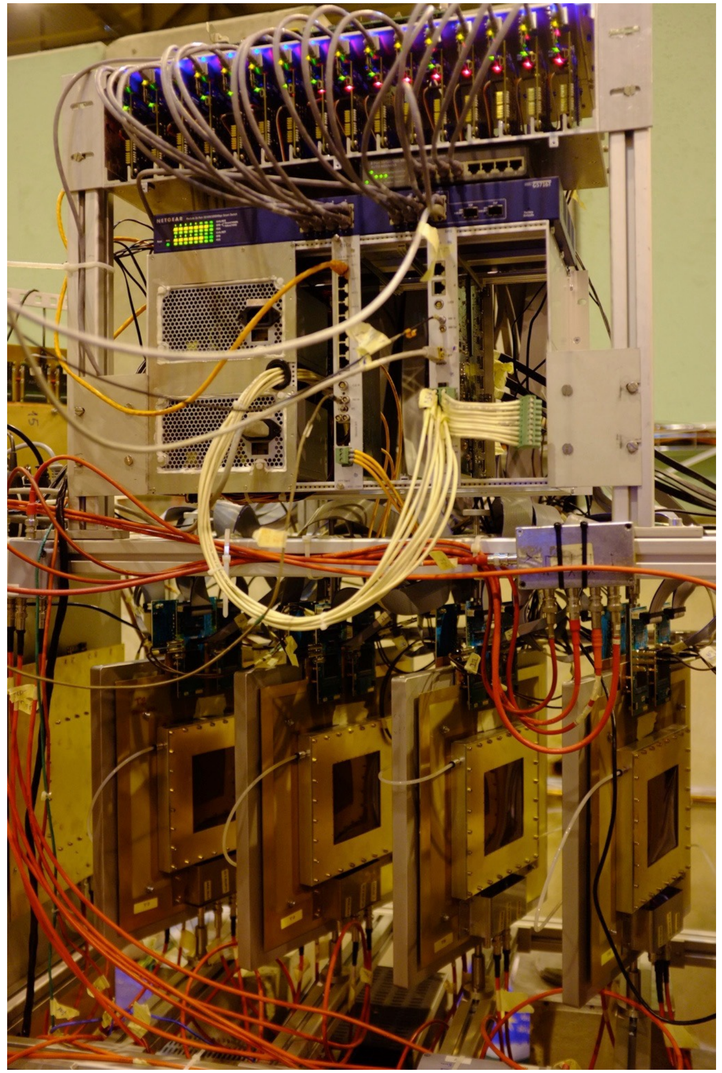
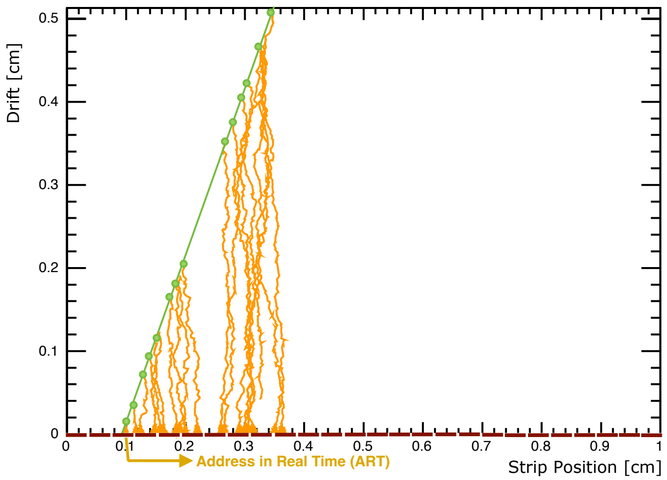
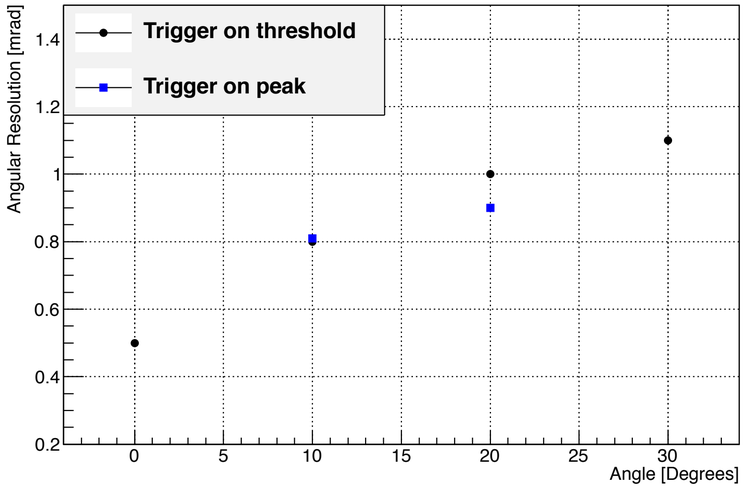
VMM1 implementation - The ART concept



- Custom readout system was developed to address the VMM1 performance and the possibility of Micromegas being in ATLAS Trigger (requirement)
- The Address in Real Time (ART) explored the possibility of getting the strip with the first in time signal as a primitive for trigger





- The performance of the architecture was demonstrated which gave a significant reduction in the # of channels used in trigger (2.1M→33k)
- **That among other studies allowed the biggest implementation of MPGDs in HEP experiments !**

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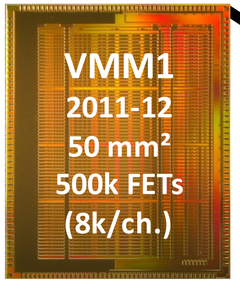
T. Alexopoulos et al. - Performance of the First Version of VMM Front-End ASIC with Resistive Micromegas Detectors, ATL-UPGRADE-PUB-2014-001, https://cds.cern.ch/record/1753328?ln=en

The VMM frontend evolution



- **Mixed-signal**
- 2-phase readout with external ADC
- **peak** and **timing** information
- neighboring readout
- sub-hysteresis **discrimination**
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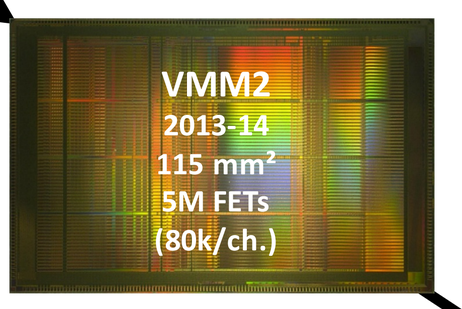
- Mixed-signal
- **Continuous** readout
- Current-output peak detector
- **Increased** range of **gains**
- **Three ADCs** per channel
- FIFOs, **serialised data with DDR**



- Serialised ART with DDR
- Additional timing modes
- **64 timing outputs**
- Additional functions and fixes

George Iakovidis 2020 J. Phys.: Conf. Ser. 1498 012051
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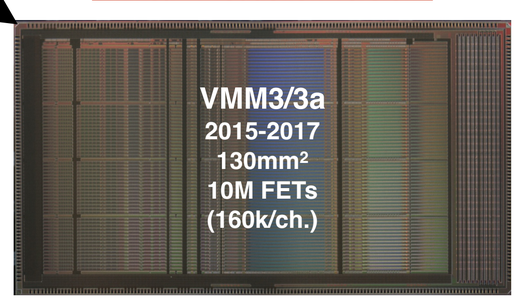
- **LVL0 pipeline** and buffering for ATLAS
- **SEU-tolerant logic**
- **Revised front-end** for high charge and capacitance (2nF, 50pC, fast recovery)
- SLVS signals
- Reset controls
- **Timing at threshold**
- Timing ramp optimisation
- Ion **tail suppressor** (fast recovery)
- Int. Pulser range extension
- ART synchronisation to BC clock
- **VMM3a fixed open bugs** from VMM3 and introduce some stability fixes on the ADCs and Front-end

- ***The VMM was designed at BNL in collaboration with IFIN-HH***
- ***It is fabricated in the 130nm Global Foundries 8RF-DM process (former IBM 8RF-DM)***

BGA 400, 1mm

VMM3a - Production Version !



~10mW/channel

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VMM Architecture

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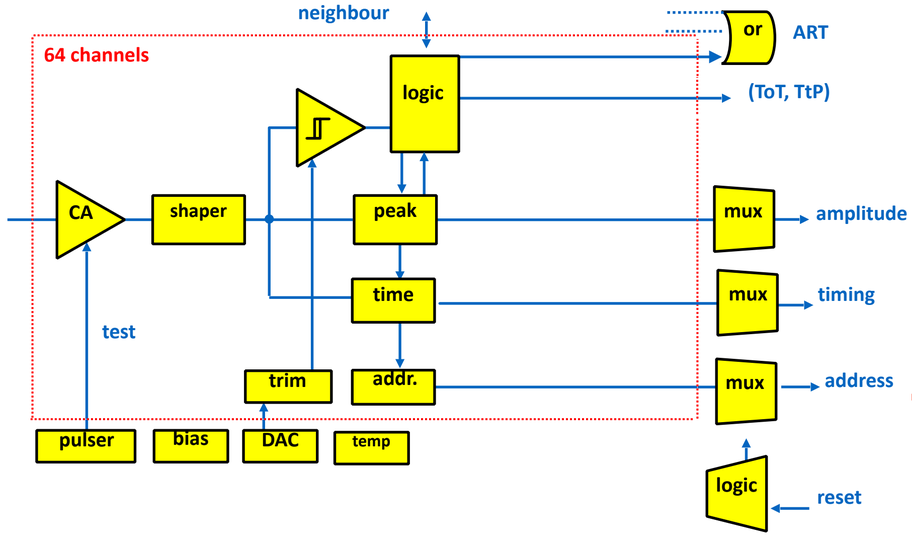
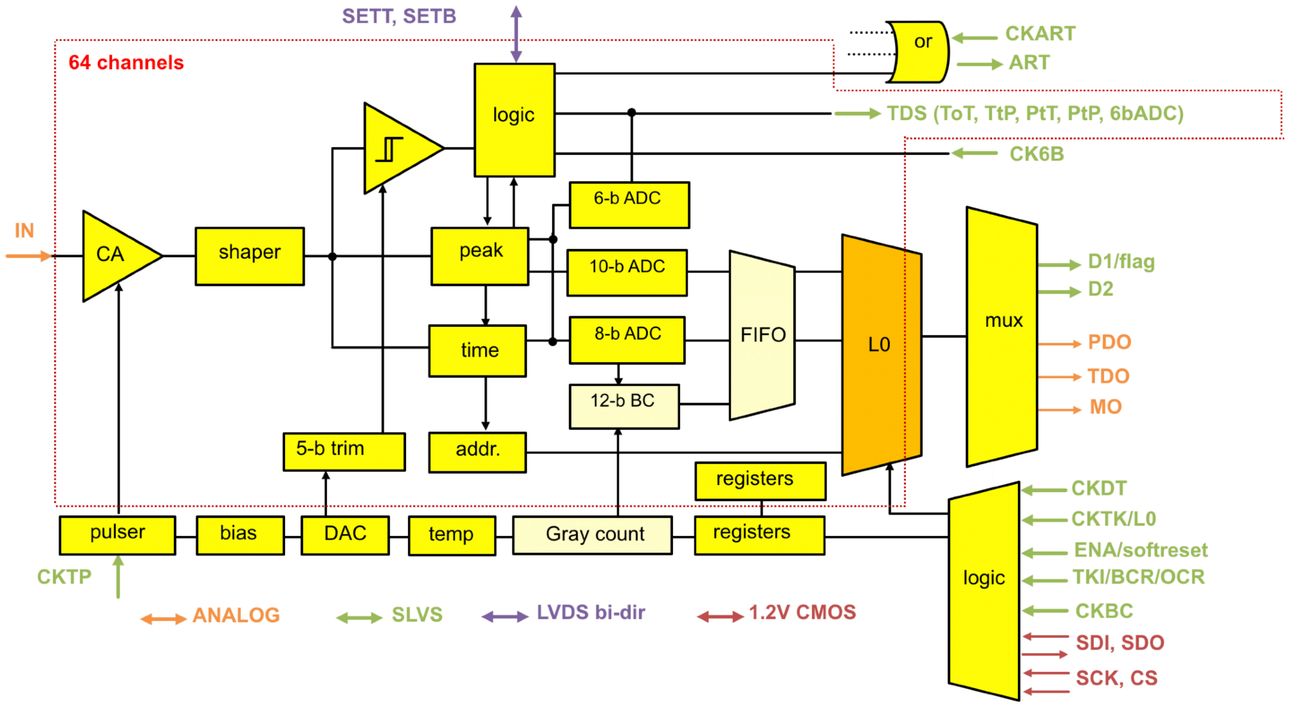


VMM1 to VMM3a

2011 to 2018



- The VMM1 FE was **mixed mode**: charge, time measurements with external ADCs, channel address in digital output
- VMM2 implemented the **continuous** digital readout logic through three ADCs/channel + **direct digital outputs** but **maintained** the analog readout mode
- VMM3/3a implemented **deep FIFOs (L0)** for **synchronous** operation needed in the LHC environment **maintaining** the analog, continuous and triggered readout modes
  - **Maintaining** all the readout abilities **made the VMM a very capable readout ASIC for many applications**

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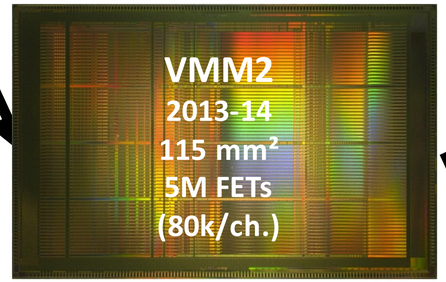
The VMM frontend - issues along the path

- Limited in gain
- Higher dynamic range
- Only analog implementation (limited in rate)
- Fast baseline recovery

x10

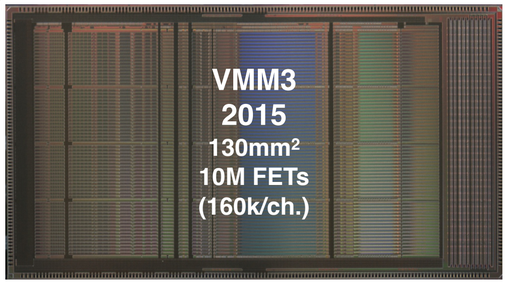
- Power distribution issues
- Major ADC accumulation, missing codes
- Major redesign of the frontend - no bipolar shape
- ADC reset needed
- Threshold bit error

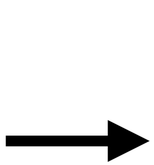


- Stuck token in continuous mode
- Locking in several direct outputs
- ASIC must handle ~10pC (sTGC)
- Stability with high input capacitance
- Peak detector issues
- BCID instabilities
- High dispersion of DACs
- Logic conflicts (direct outputs and high resolution ADCs)
- Test pulse slow and not wide enough
- High baselines
- Time logic
- SEU logic

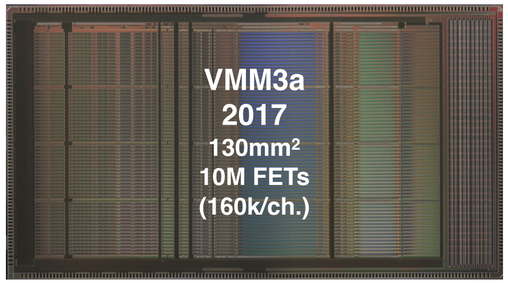
x2

- Residual accumulation in ADCs
- MO sensitive
- High baseline residual issue
- Trimming DAC non uniform
- Reset logic - startup reset
- Positive charge handling
- Timing logic
- 4x FIFO issue
- Locking issue at 25ns
- Locking at direct outputs
- Input currents not sufficient
- Need larger ESD diodes





VMM3a - Production Version !



- Residual linearity of ADCs - **good** for MPGDs
- BLH not stable - need bipolar shaping always on (**workaround**)
- 4x FIFO only 1x, **no issue**
- Higher ADC gain in central
- TAC at threshold logic

~10mW/channel

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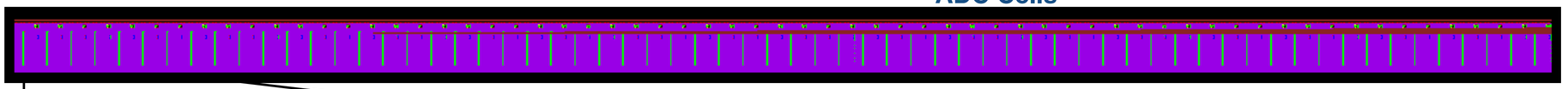
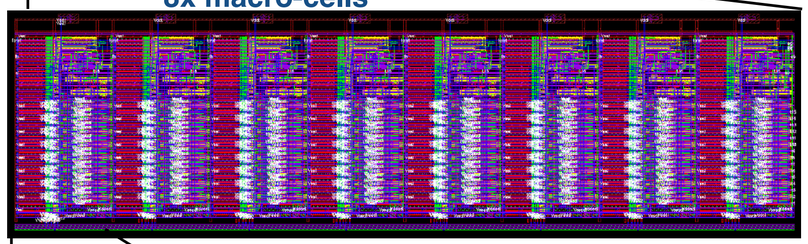
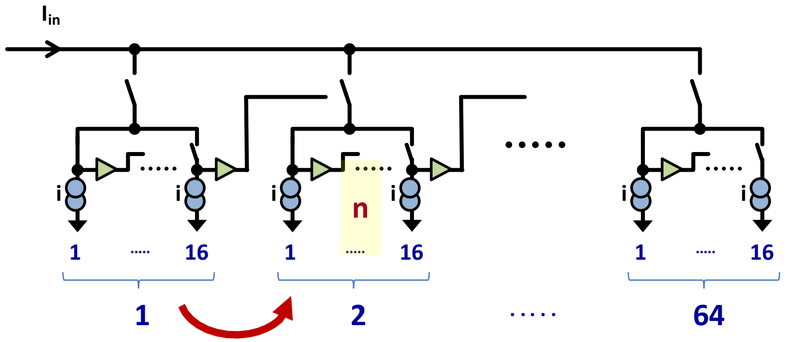
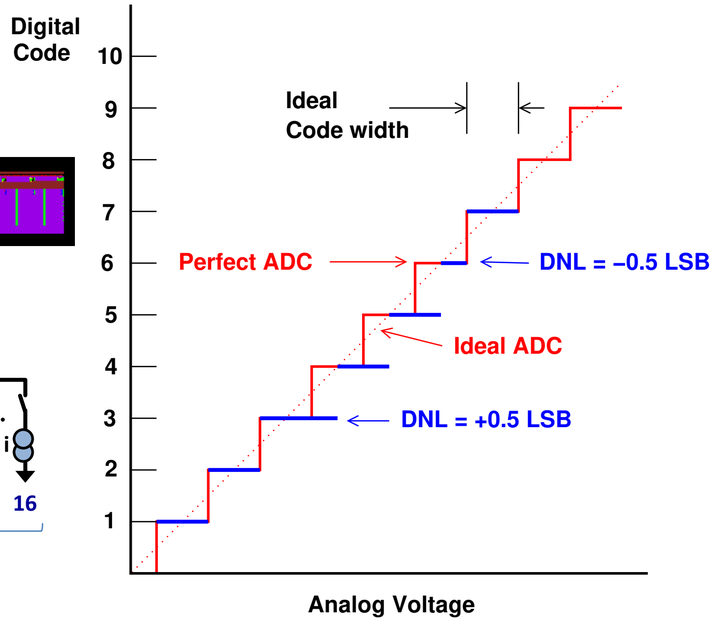
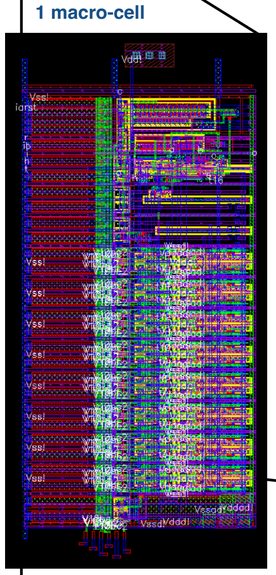
VMM ADC







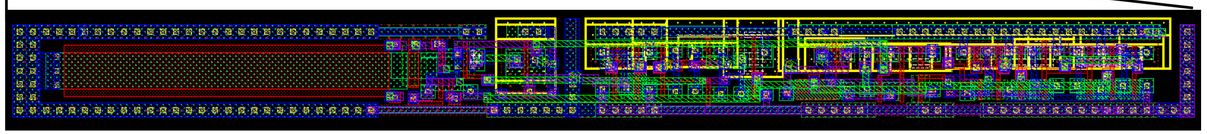


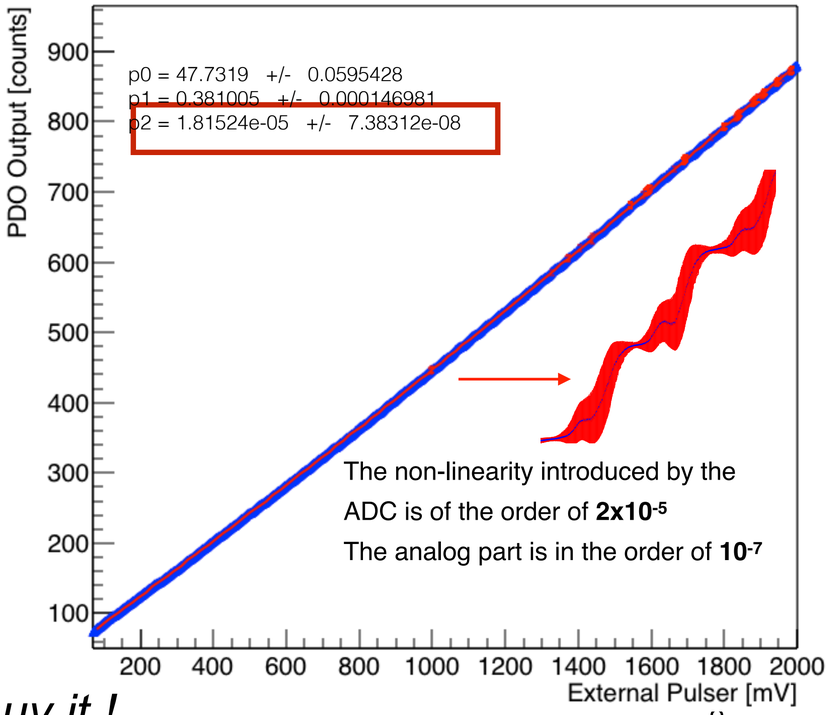


16x micro-cells

ADC Core (per channel)

- **1024 current sources** (similar to a digital thermometer) (**2 step mode**)
- **64 macro-shells** (6 upper bits xxxxxx0000), **16 micro-shells** (4 lower bits 000000xxxx)
- **8 bit ADC** is build in the similar way **(5+3)**
- 6 bit ADC is a single stage conversion similar to the 64 macro shells with fast digitisation (50ns)
  - Using **DNL** and **INL** calculated and used to estimate the ENOB Equivalent number of bits ~7.5 (noise free) for the 10-bit ADC
  - **Performance was considered enough for gaseous detectors (schedule constrains as well) - moved to production**





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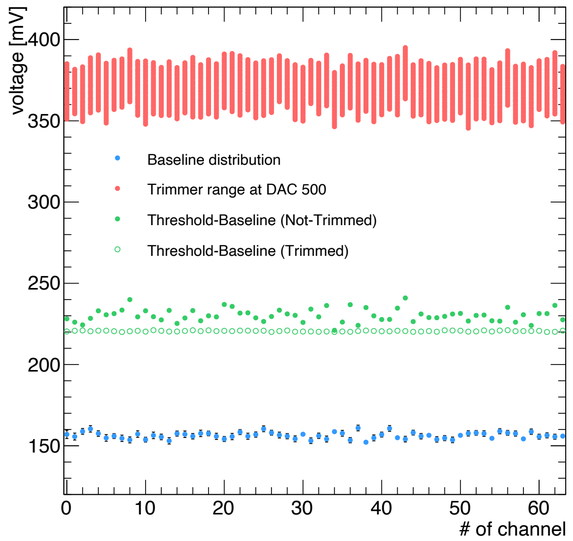
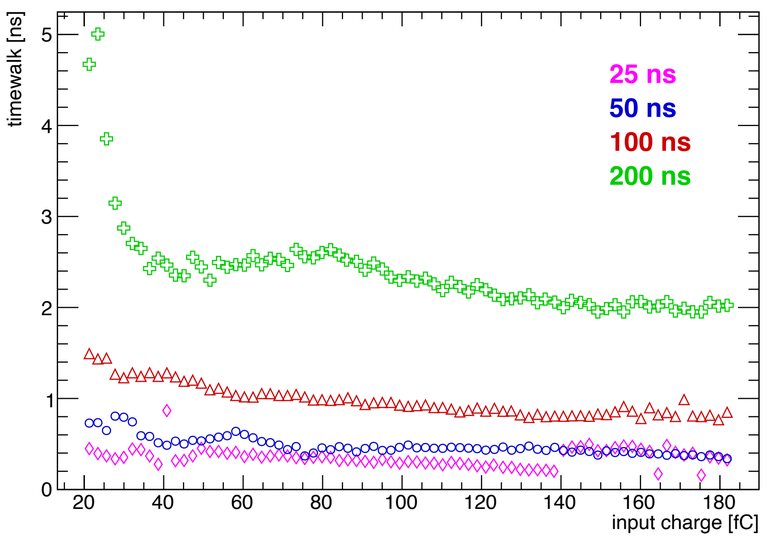
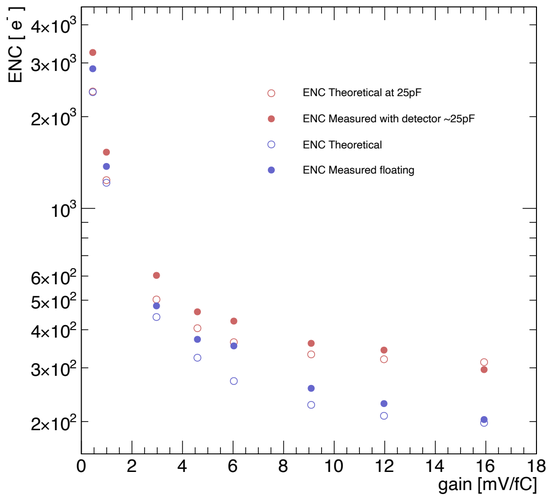
if you can find an ADC IP which has good performance…buy it !

Performance highlights







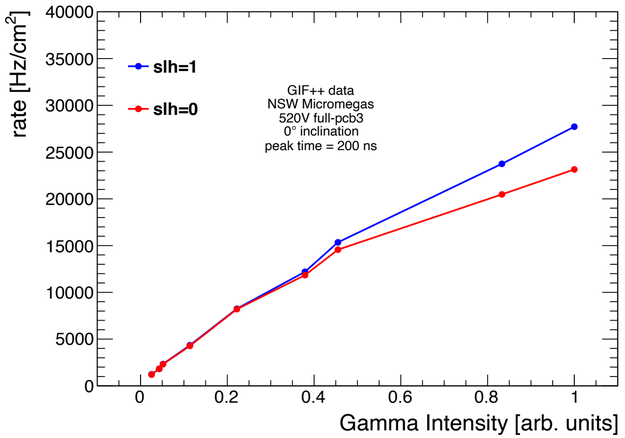
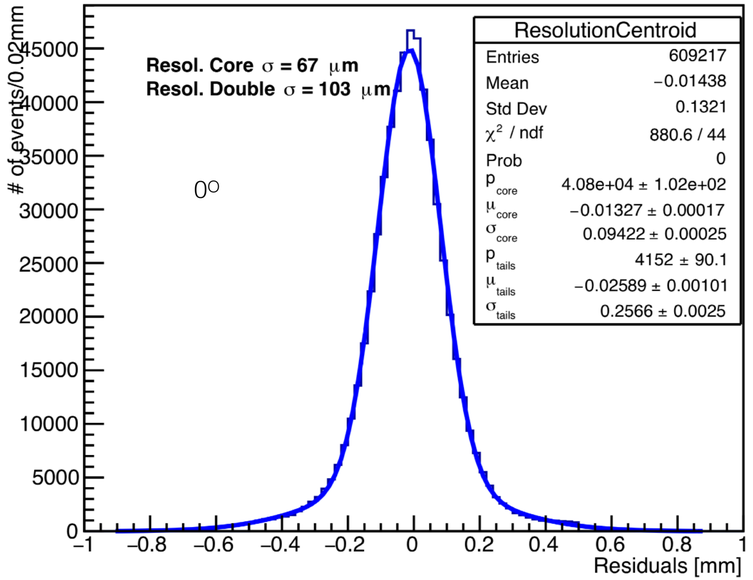
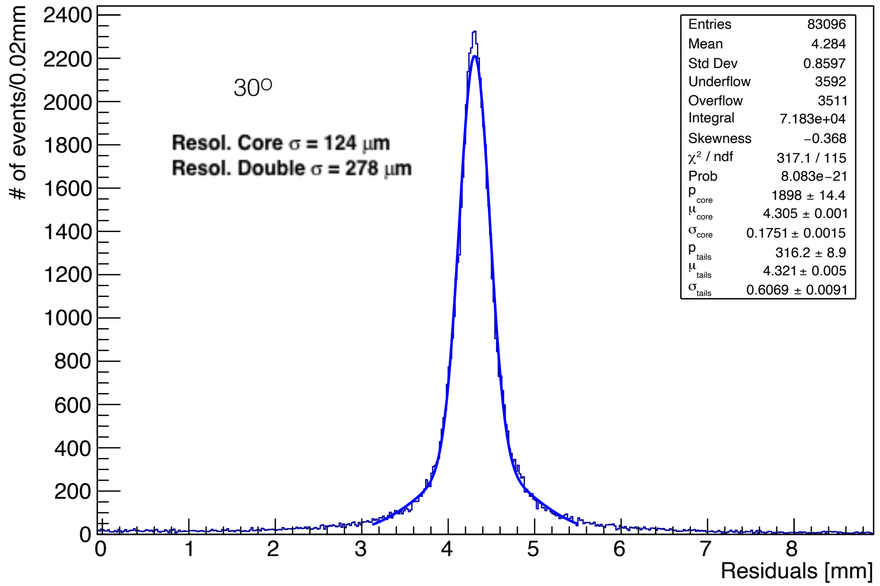


Figure 4: Cluster rate normalised to the active area of the benchmark PCB-3 as a function to the intensity of the GIF++ source, where Gamma Intensity 1 corresponds to no GIF++ source attenuation, when the source is not attenuated by any filter. The two lines show the different settings of the *slh* parameter [13] of the VMM electronics, corresponding to a higher ($slh = 1$) or lower ($slh = 0$) bias current at the input of the electronic channels.





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The game of shaper

Authors

Theo Alexopoulos, Gianluigi de Geronimo , George Iakovidis, Venetios Polychronakos

The VMM Shaper

The VMM "semi-Gaussian" shaper responds to an event with an analog pulse, the peak amplitude of which is proportional to the event charge. The time needed to return to baseline after the peak, depends on the the time constants and the configuration of poles. The VMM facilitates a 3rd order c-shaper with the combination of one real and two conjugate poles. The transfer function $T(s)$ for such shaper is given by the following expression:

$$T(s) = \frac{1}{(s+p_1)\prod_{i=2}^{(n+1)/2}\left[(s+r_i)^2+c_i^2\right]} = \frac{1}{(s+p_1)\left[(s+r_2)^2+c_2^2\right]}, \quad n=3$$

where n is the order of the shaper, and r_i, c_i are the real and imaging parts. The roots are:

$$(s+r_2)^2 + c_2^2 = 0 \Rightarrow s + r_2 = \pm jc_2 \Rightarrow s = -r_2 \pm jc_2$$

so the transfer function can be written with the simple fractions like :

$$T(s) = \frac{K_1}{(s+p_1)} + \frac{K_2}{(s+r_2-jc_2)} + \frac{K_3}{(s+r_2+jc_2)} \tag{1}$$

where one real pole, $\text{pole}_\emptyset = -p_1$ and the two complex poles, $\text{pole}_1 = -r_2 + jc_2$ and $\text{pole}_2 = -r_2 - jc_2 = p_1^*$, $\Re\text{pole}_1 = -r_2$, $\Im\text{pole}_1 = c_2$. The coefficients K_i are :

$$\begin{aligned}
K_1 &= \frac{1}{(s+r_2-jc_2)(s+r_2+jc_2)}\Big|_{s=-p_1} \\
&= \frac{1}{(-p_1+r_2-jc_2)(-p_1+r_2+jc_2)} = \frac{1}{(r_2-p_1)^2+c_2^2}, \quad \in \Re \\
K_2 &= \frac{1}{(s+p_1)(s+r_2+jc_2)}\Big|_{s=-r_2+jc_2} \\
&= \frac{1}{(-r_2-jc_2+p_1)(\cancel{-r_2}+jc_2+\cancel{r_2}+jc_2)} \\
&= \frac{1}{2jc_2(p_1-r_2+jc_2)} = |K_2|e^{j\phi}, \quad \phi = \angle K_2, \quad \in \mathbb{C} \\
K_3 &= \frac{1}{(s+p_1)(s+r_2-jc_2)}\Big|_{s=-r_2-jc_2} \\
&= \frac{1}{(-r_2-jc_2+p_1)(\cancel{-r_2}+jc_2+\cancel{r_2}-jc_2)} \\
&= \frac{1}{-2jc_2(p_1-r_2-jc_2)} = K_2^*, \quad \in \mathbb{C}
\end{aligned} \tag{2}$$

From Eq. (2) the Eq. (1) will be:

$$T(s) = \frac{K_1}{(s+p_1)} + \frac{K_2}{(s+r_2-jc_2)} + \frac{K_2^*}{(s+r_2+jc_2)} \tag{3}$$

The time-domain representations (apart from the amplitude factor) of the shapers in Eq. (3) can be calculated as the inverse Laplace transform $T(s) \overset{\mathcal{L}^{-1}}{\longleftrightarrow} f(t)$:

$$\begin{aligned}
f(t) &= K_1e^{-p_1t} + K_2e^{(-r_2+jc_2)t} + K_2^*e^{(-r_2-jc_2)t} \\
&= K_1e^{-p_1t} + e^{-r_2t}\left[K_2e^{jc_2t} + K_2^*e^{-jc_2t}\right] \\
&= K_1e^{-p_1t} + 2e^{-r_2t}2\Re\left(K_2e^{jc_2t}\right) = K_1e^{-p_1t} + e^{-r_2t}2\Re\left(|K_2|e^{j\phi}e^{jc_2t}\right) \\
&= K_1e^{-p_1t} + 2|K_2|e^{-r_2t}\cos\left(c_2t+\phi\right), \quad \text{where } \phi = \angle K_2 \\
&= K_1e^{\text{pole}_\emptyset t} + 2|K_2|e^{\Re\text{pole}_1 t}\cos\left(\Im\text{pole}_1 t + \angle K_2\right)
\end{aligned}$$

where

$$|K_2| = \frac{1}{2c_2\sqrt{(p_1-r_2)^2+c_2^2}} \overset{(2)}{\Longrightarrow} 4c_2^2|K_2|^2 = K_1$$

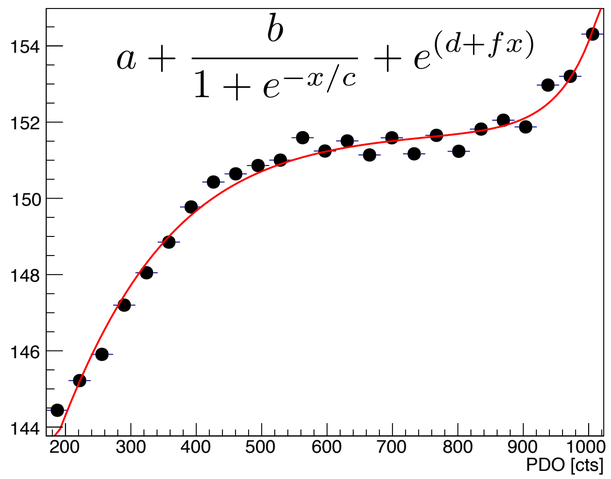
$$K_1 = \frac{1}{(\text{pole}_\emptyset - \Re\text{pole}_1)^2 + \Im\text{pole}_1^2}$$

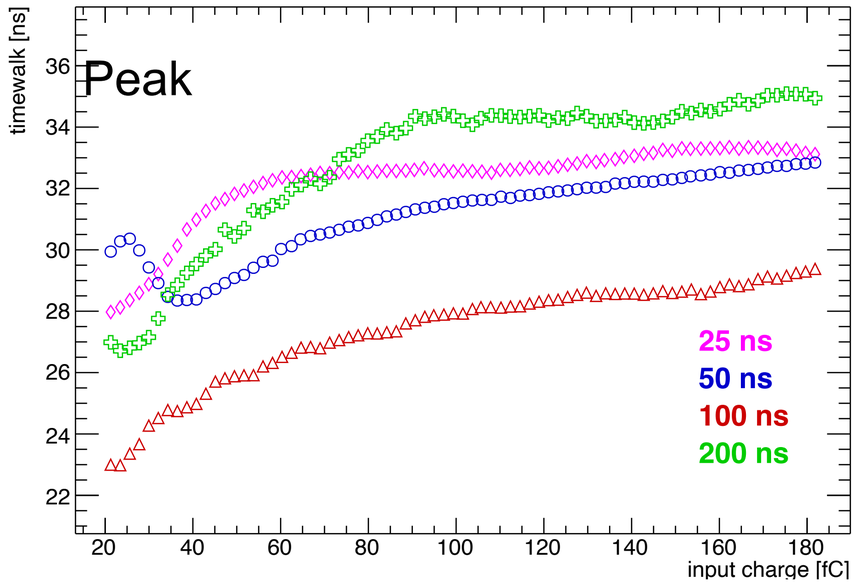
If someone defines the normalized: $\overline{H}(f) = H(f)/\tau$ which allows in our calculations, to take into account the proportionality of $H(f)$ to τ (so that the integral, a measure of the amplitude, is independent of τ). Through the normalization, the VMM shaper constants are :

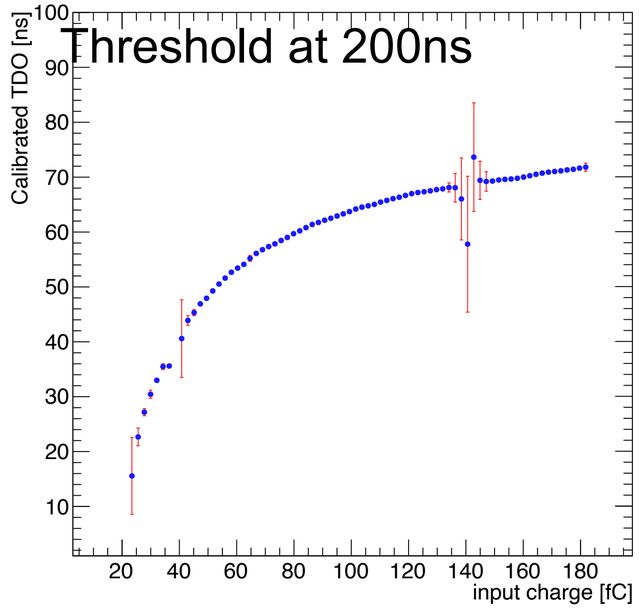
$$\begin{aligned}
\alpha &= 10^{-8} \\
\text{pole}_\emptyset &= \frac{1.263}{\alpha} \\
\text{pole}_1 &= (1.149 - j0.789)\frac{1}{\alpha} \\
K_1 &= 1.584 \\
K_2 &= -0.792 - 0.115j \\
t_{peak} &= 1.5\alpha
\end{aligned}$$

and the final function can be written in a computational form:

$$f(t) = \alpha^3|\text{pole}_\emptyset|\left(|\text{pole}_1|\right)^2\left[K_1e^{-t\text{pole}_\emptyset} + 2|K_2|e^{-t\Re\text{pole}_1}\cos\left(-t\Im\text{pole}_1 + \angle K_2\right)\right]$$







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NSW Electronics

ASIC	Quantity	Comment
VMM	40,192	
pTDS	768	
sTDS	2304	
ART	1024	2 / ADDC
ROC	5632	one / FEB
GBTx	3712	
SCA	7520	one / board
VTRx	1920	
VTTx	1056	
MTx	512	
FEAST IC	5760	

4 ASICs dedicated to NSW developments TDS (dual functionality)

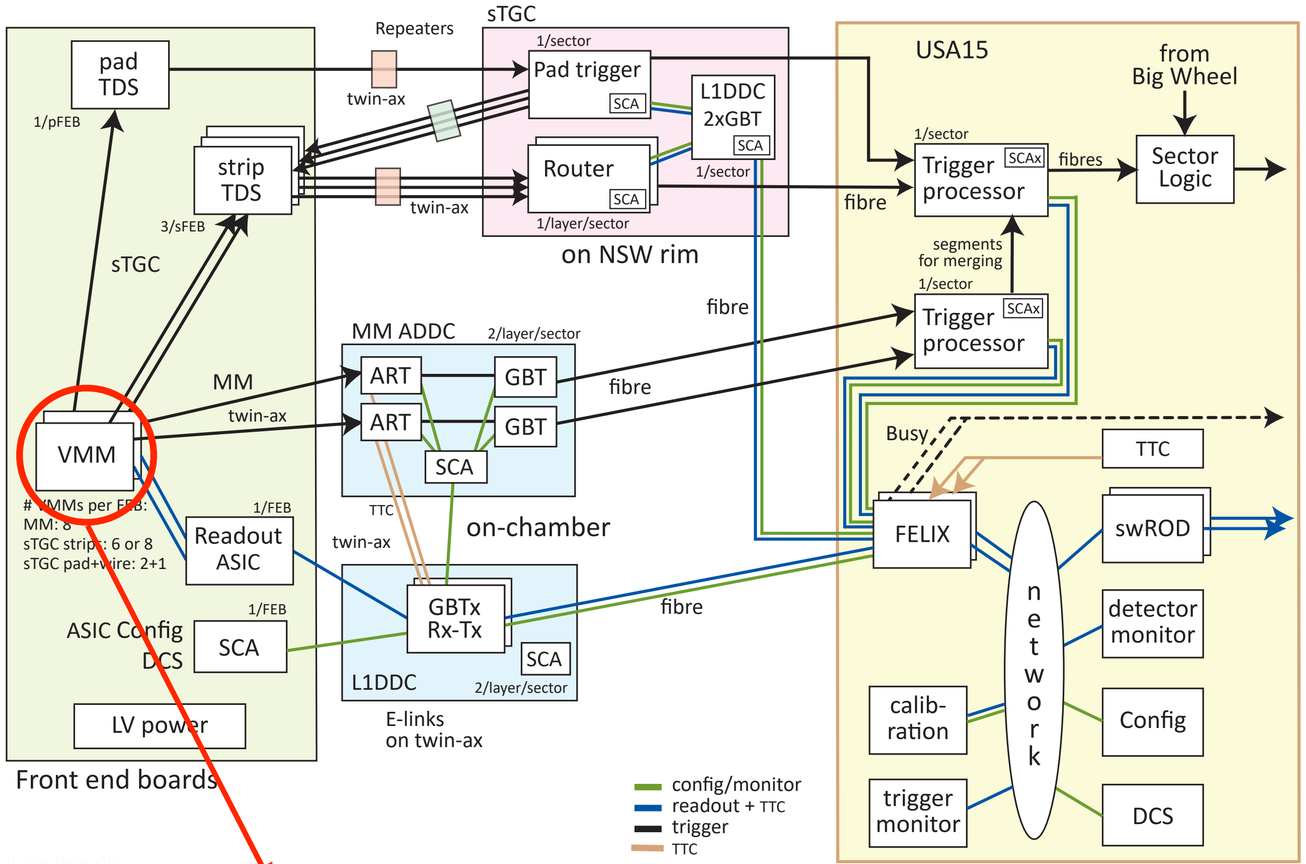
CERN Common electronics developments

1 Micromegas frontend
2 sTGC frontends)

Trigger electronics

Readout

Board	Quantity	Comment
MMFE8	4096	
pad-FEB	768	
strip-FEB	768	
ADDC	512	
MM L1DDC	512	
sTGC L1DDC	512	
Rim-L1DDC	32	
Pad Trigger	32	
Router	256	
Serial repeater	768	
LVDS repeater	128	
Direct clock	2	
FELIX FPGAs	60	
Trigger Processor	16	2 sectors each



Front-end Electronics Requirements

- Challenge of this Project - **More than 2.4 million** channels total (2.1M for Micromegas and 300k for sTGC) **(full MS of ATLAS ~1.6M channels)**
- Operate with **both charge polarities**
- Sensing element **capacitance** 50-200pF (sTGC Pad up to 3nF)
- Charge measurements up to **2pC @ < 1fC RMS**(6pC for sTGC pads)
- Time measurements ~ 200ns @ **< 1ns RMS**
- **Multiple Trigger** primitives, complex **logic**
- **Digitisation**, deep **FIFOs**, **Low power, programmable**
- **Space requirements on the detector**
- Radiation tolerant

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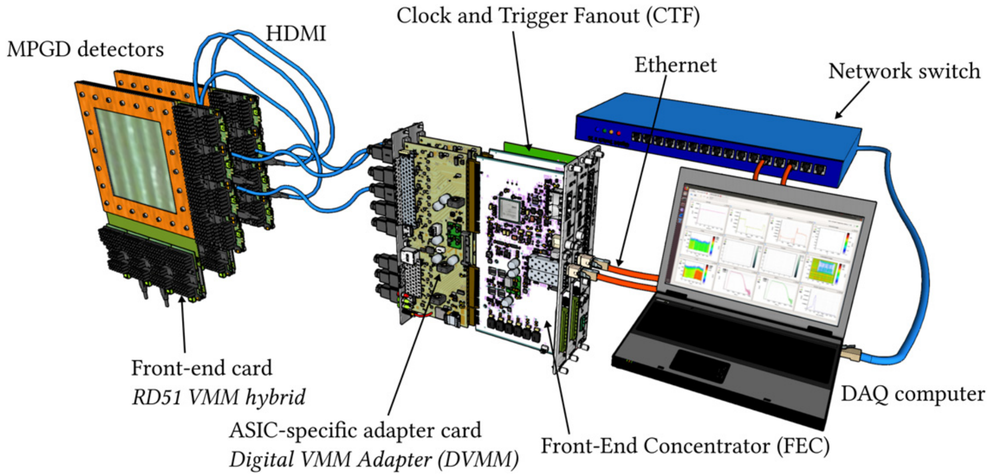
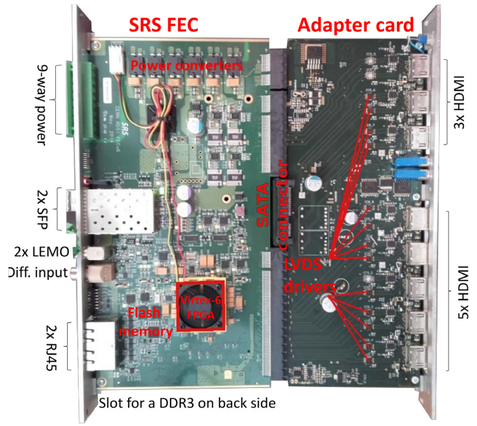
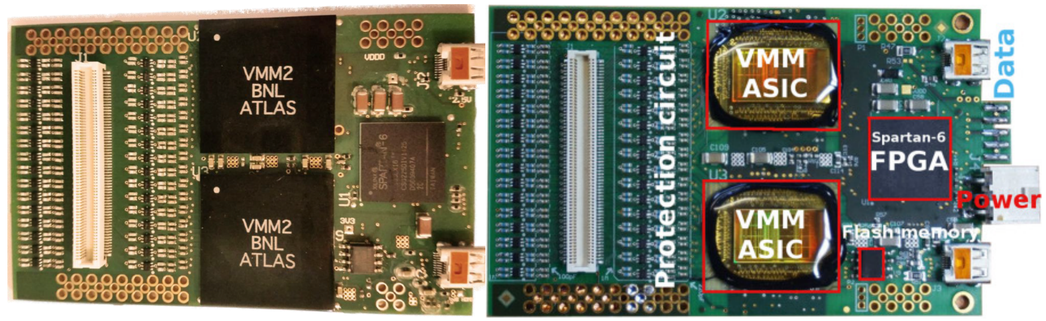
SRS implementation

- SRS developments towards a VMM FE implementation started 2014
  - VMM2 was the first version to be integrated
- Since VMM2 is an integrated FE ASIC it can provide digital output directly
  - Implied an FPGA on the FE for the readout and control of the VMM
  - Implied a digital adapter card as well
- A lot of progress was made since then implementing the VMM3/3a ASICs
- Power distribution changed as well, VMM is demanding on power and sensitive to noise !







VMM SRS Homepage

L. Scharenberg et al., JINST 17 (2022) C12014.
D. Pfeiffer et al., NIM A 1031 (2022) 166548
M. Lupberger et al., NIM A 903 (2018) 91-98.

Results from SRS developments

L. Scharenberg et al., JINST 17 (2022) C12014.
D. Pfeiffer et al., NIM A 1031 (2022) 166548
M. Lupberger et al., NIM A 903 (2018) 91-98.

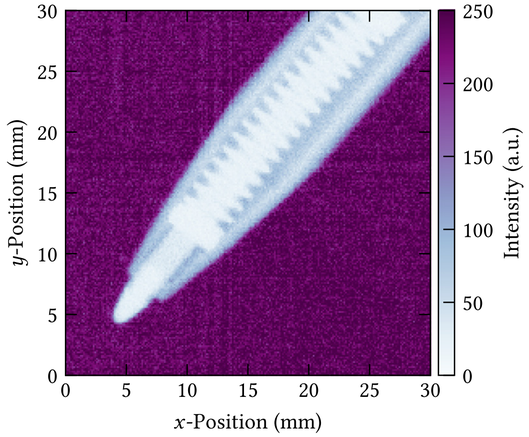


Fig. 16. Image of a pen containing 17×10^6 clusters. The full data set contains 50×10^6 clusters, that have been recorded in 30 seconds.

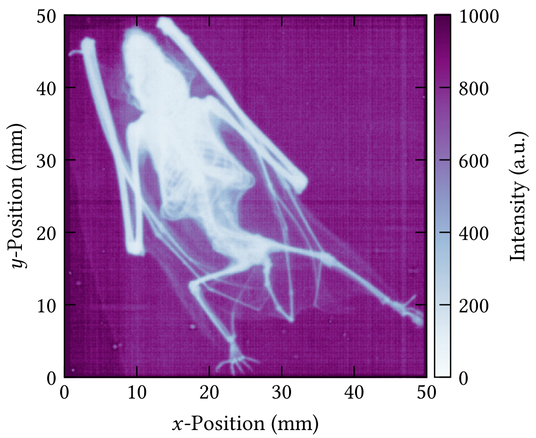
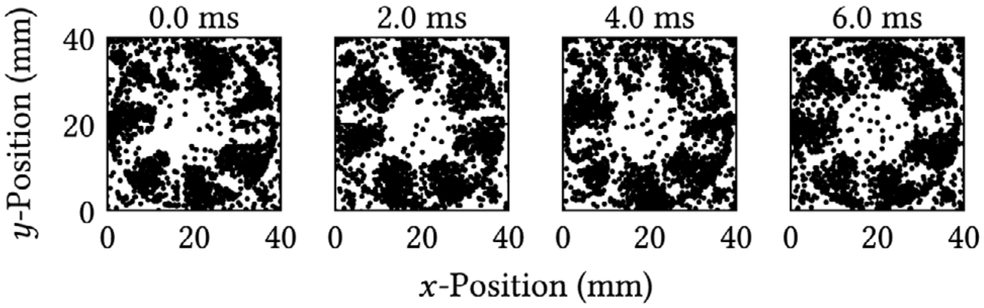


Fig. 17. Image of a dead mammal. The data set for this image contains 277×10^6 clusters, that have been recorded in 180 seconds.



(b) Frames of the rotating blades of a fan.

Fig. 18. Examples of the continuous data stream, which is sliced into frames, allowing to reconstruct dynamic processes.

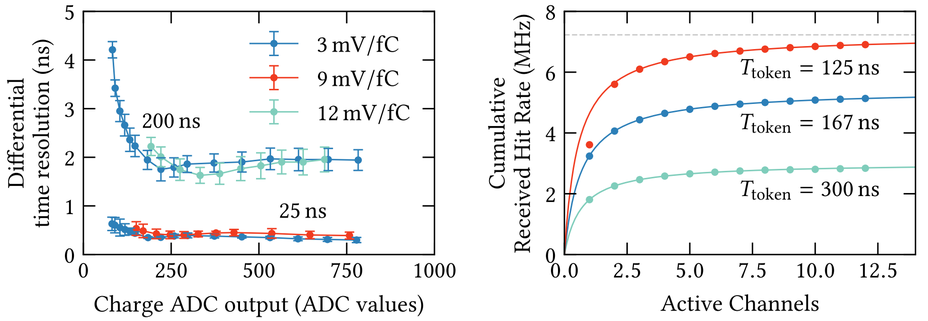


Figure 3. Measurement of the differential time resolution of the VMM3a (left). Illustration of the saturation of the maximum readout rate for different token clocks [4, 13] (right). The dashed line (right) indicates the theoretical maximum of the receivable hit rate.

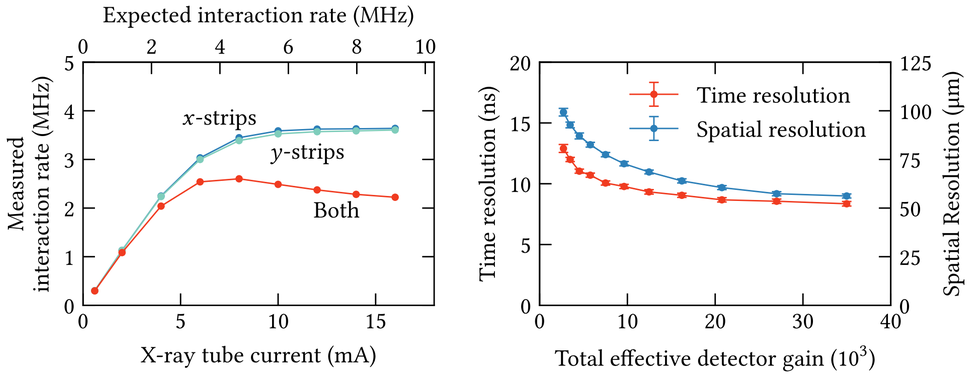


Figure 4. Measured X-ray interaction rate [4] (left). Time and spatial resolution (right) of a COMPASS-like triple-GEM detector (threshold of 1.5 fC per readout channel). This measurement was performed with the RD51 VMM3a/SRS beam telescope at the CERN SPS using 80 GeV/c muons.

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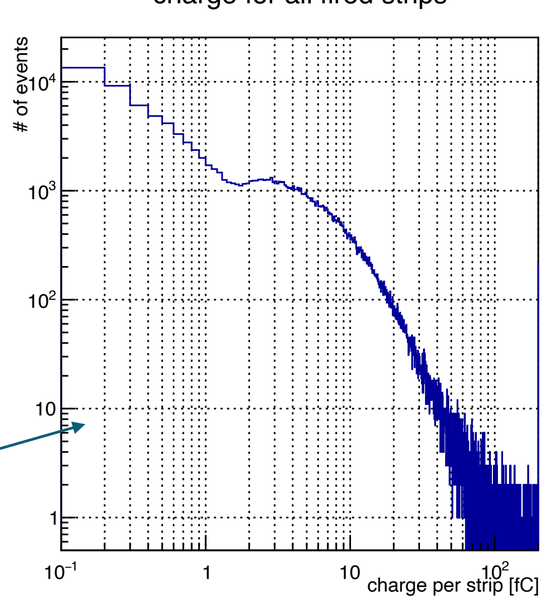
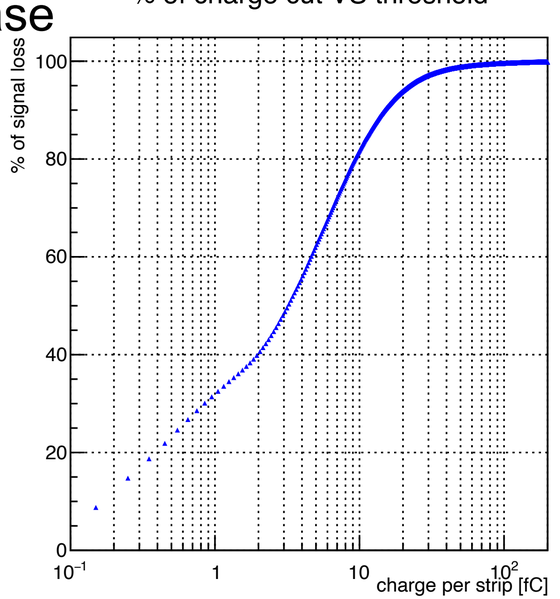
In the TB of last weeks with NSW MMs, one run of 300k events was completed in 4 sec

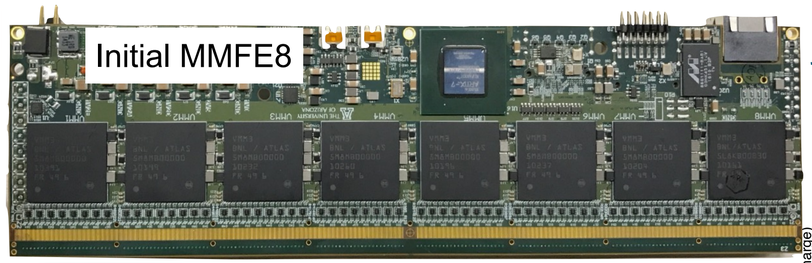
Front end developments Importance of Noise !

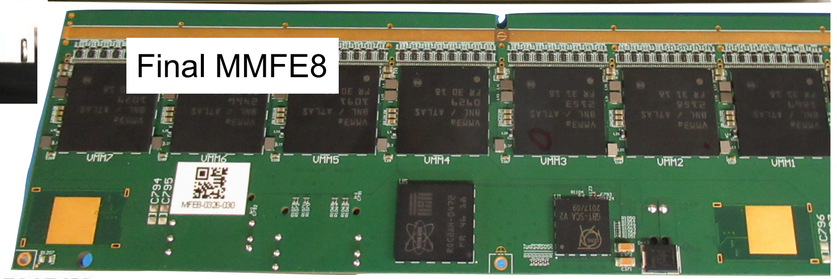
- Frontend board design is crucial for the performance of the ASICs
- Monte Carlo based on Garfield parametrization was developed long time ago showing the signal loss as a function of threshold !
- Struggled a lot during the developments but key element was the implementation of DCDC
- Final MMFE8 board 1k-2.5k ENC (100-250pF MM)

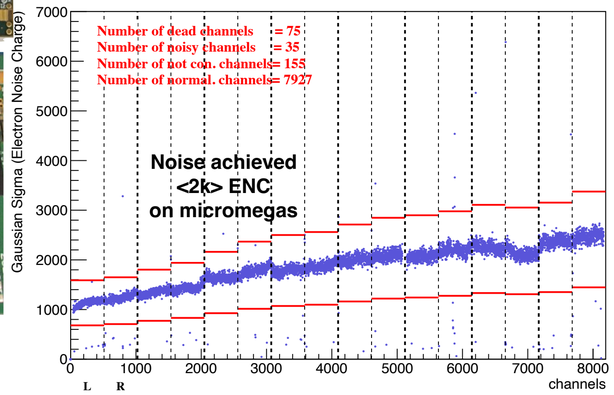
Micromegas Case

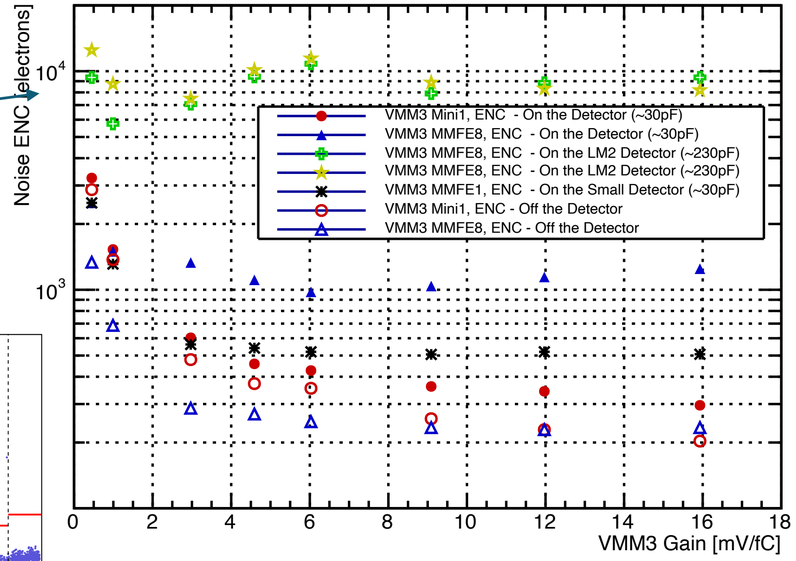












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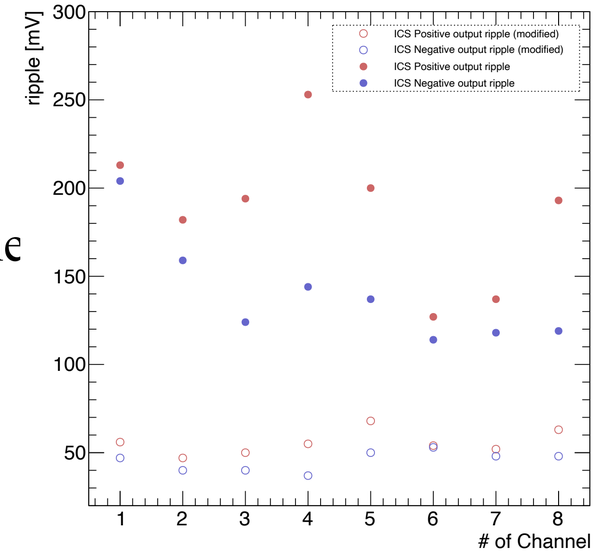
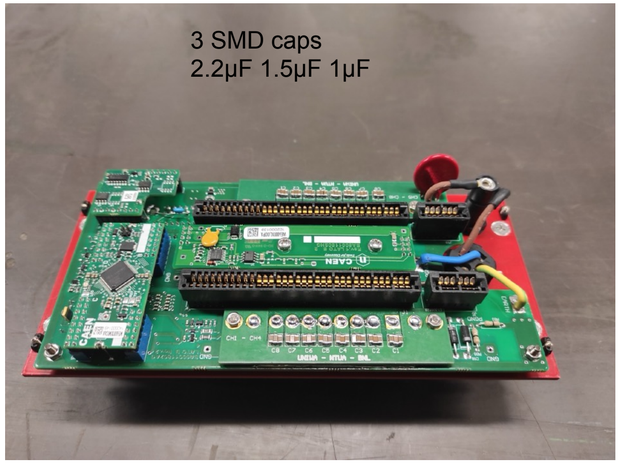
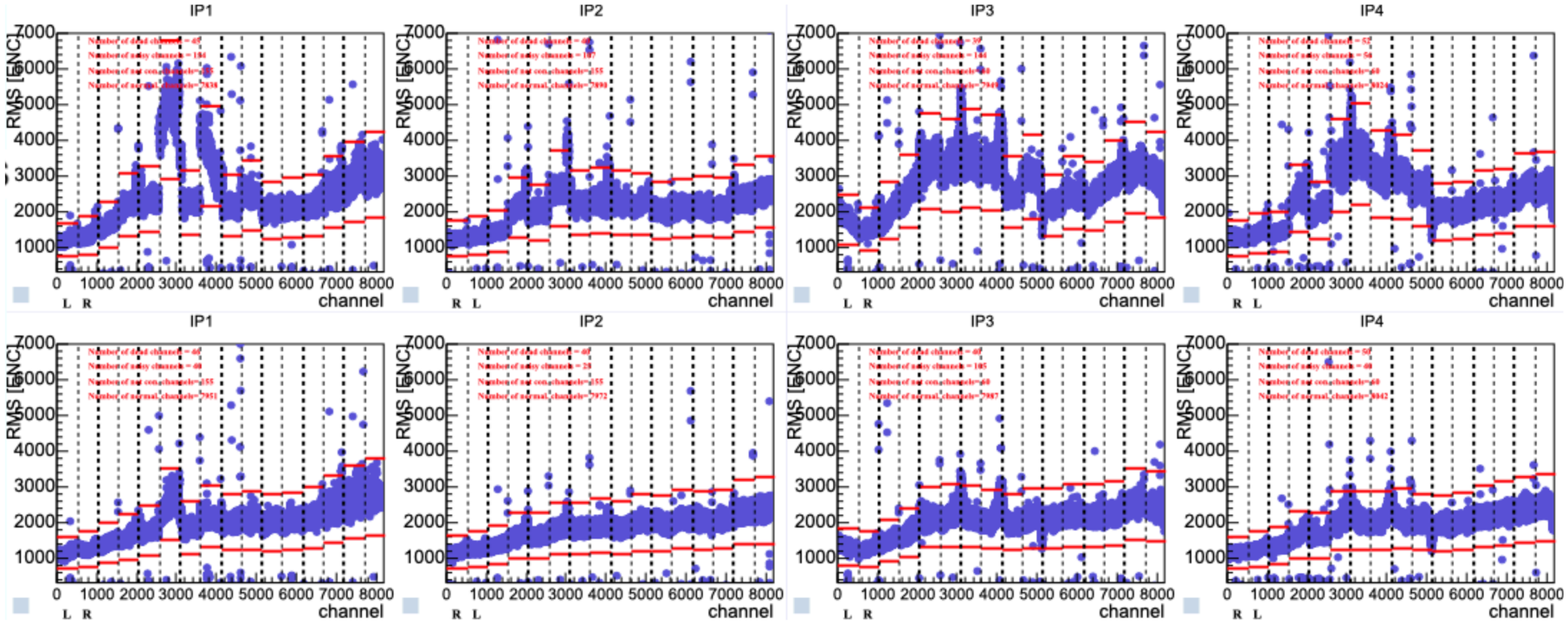
NSW Integration
The importance of Power supplies

- During integration a major noise issue was observed in the NSW electronics
- After almost 1.5y the issue was attributed to high noise (ripple) and non symmetric power lines on the power supply
- Increased filtering and grounding mitigated the issue
  - The issue though was not solved but patched !

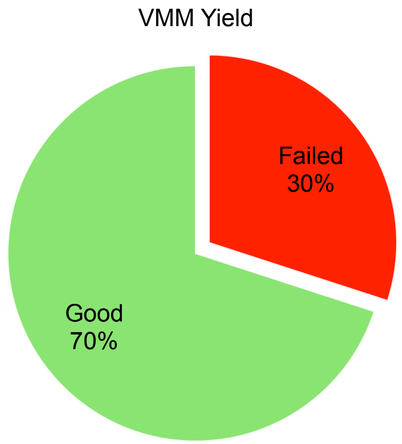




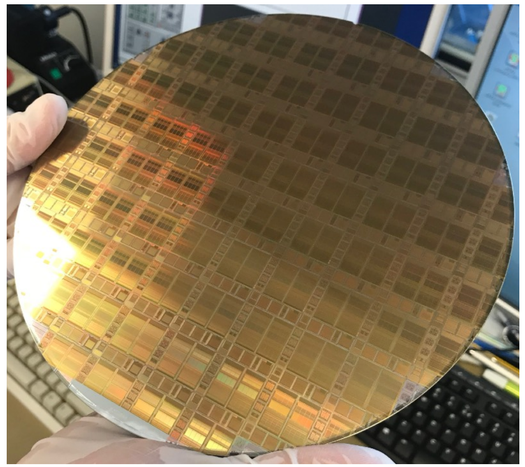
Adding filtering



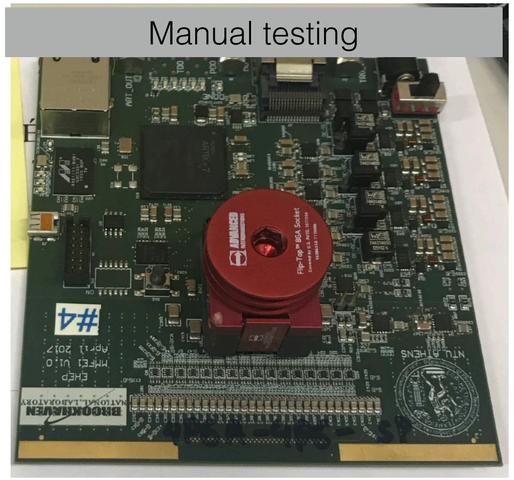
Production



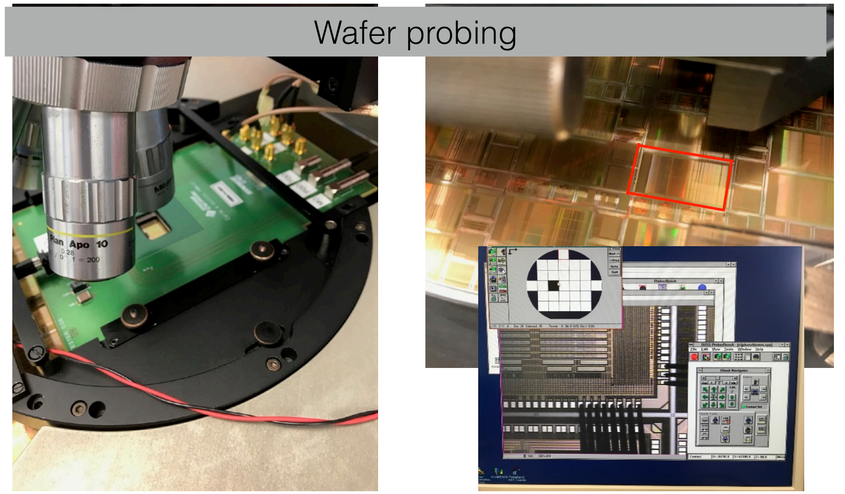
- The **VMM** is **produced** in a 8” **wafer** with 2 copies of the chip in a reticle, **total 113 chips / wafer**
  - During the production we faced several issues due to GF processing affecting the yield
  - Many iterations with experts from Global Foundries to improve the yield and understand the issue
  - Investigation concluded (HPT process maintained throughout the production for high density metal layers)
- ATLAS has already produced and packaged **73k** VMMs (incl. prototyping)
- Many testing protocols have been produced for testing the devices
- Direct wafer probing was developed to allow initial screening of the production batch
- Half of the production was tested by manual operators (lengthy process)
- Due to constrains in time, we developed automated testing (30sec/device) which accelerated dramatically the process
- Throughout the process, 70% yield was achieved, 30% mainly due to ESD damage on input transistor or baseline stabilizing circuit



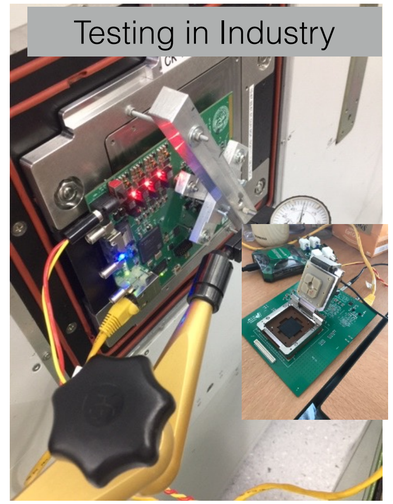
Manual testing



Wafer probing



Testing in Industry



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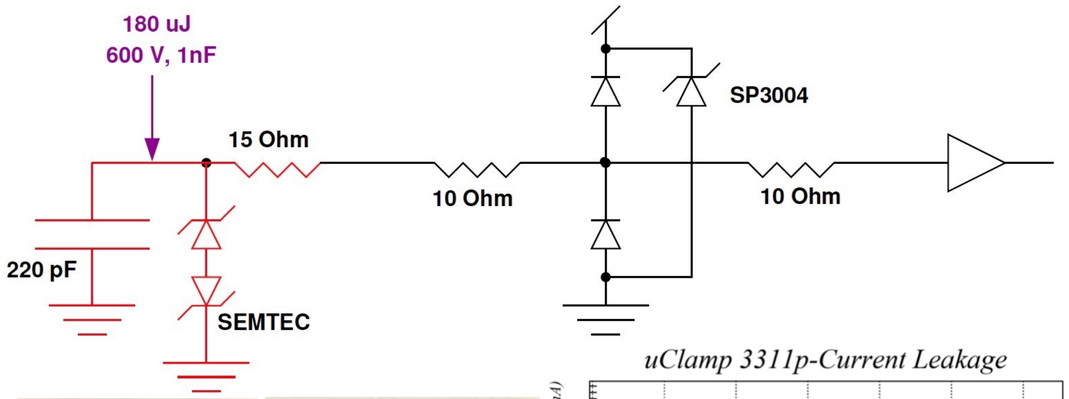
Remarks

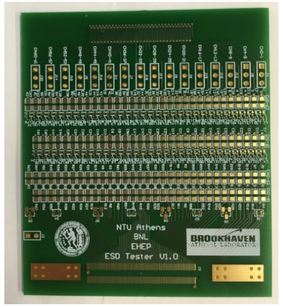
- The **VMM frontend took almost 8y of developments**, was a **difficult and expensive path** with many issues along the line
  - But **successful**! **NSW operates in ATLAS for the last 3 years**
  - **Many other applications** followed after NSW
- The **SRS implementation** allowed an even high number of applications
  - **VMM is fully flexible** and capable of high rates, can match many many requirements due to its highly configurable parameters
  - **R&Ds should follow the big experiments**, any integrated ASIC development is expensive !
  - Foundry plays a big role in the production and even prototyping, field is evolving !
  - **Community** lacks software and firmware developers as well as electronics engineers with analog design skills
    - Implementation of **highly complex electronics becomes more and more difficult**
- **Technology is evolving → Power distribution is a key element** for low noise electronics, it costed NSW almost 2y and continues to cost due to failures !

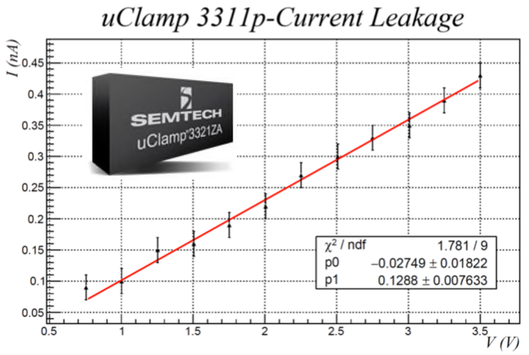
backup

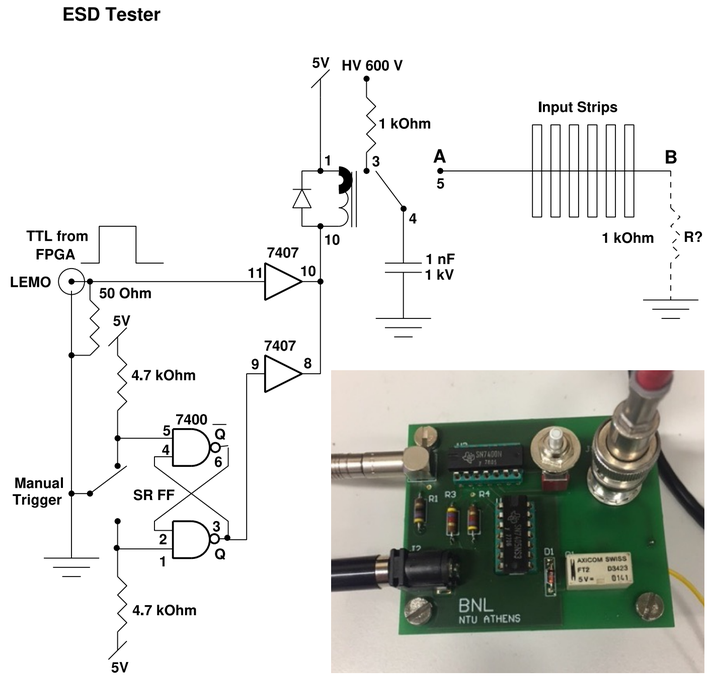
Input protection

- Since the VMM2, we have experience major channel (initial NUP4114 issue). Moving to 130nm technology made the requirements on input protection higher. Current protection scheme based on the SP3004 seems inadequate to protect the VMM front ends
- A dedicated ESD testing procedure was lunched allowing a systematic test of the VMM input.
- A VMM board (MMFE1) with Panasonic connector and a VMM socket was developed to perform systematic tests. On top a Panasonic based connector daughter-board was built to test different protection schemes and different footprints.
- 220 pF capacitor emulates typical MM strip capacitance, a channel like this survived repeated discharges while without protection is dead after a single discharge. Then survived zapping overnight (>30,000 discharges)









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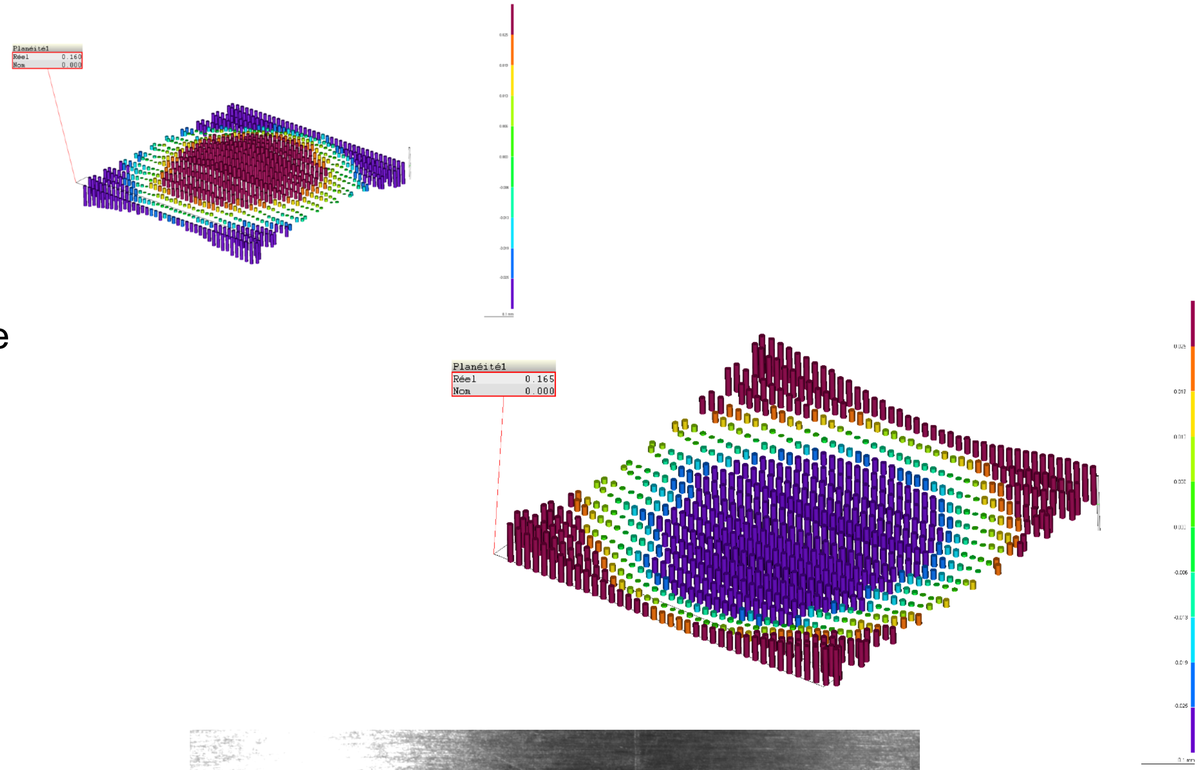
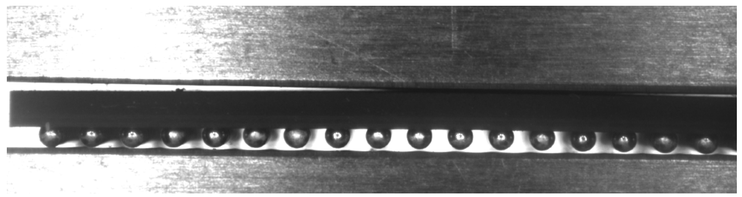
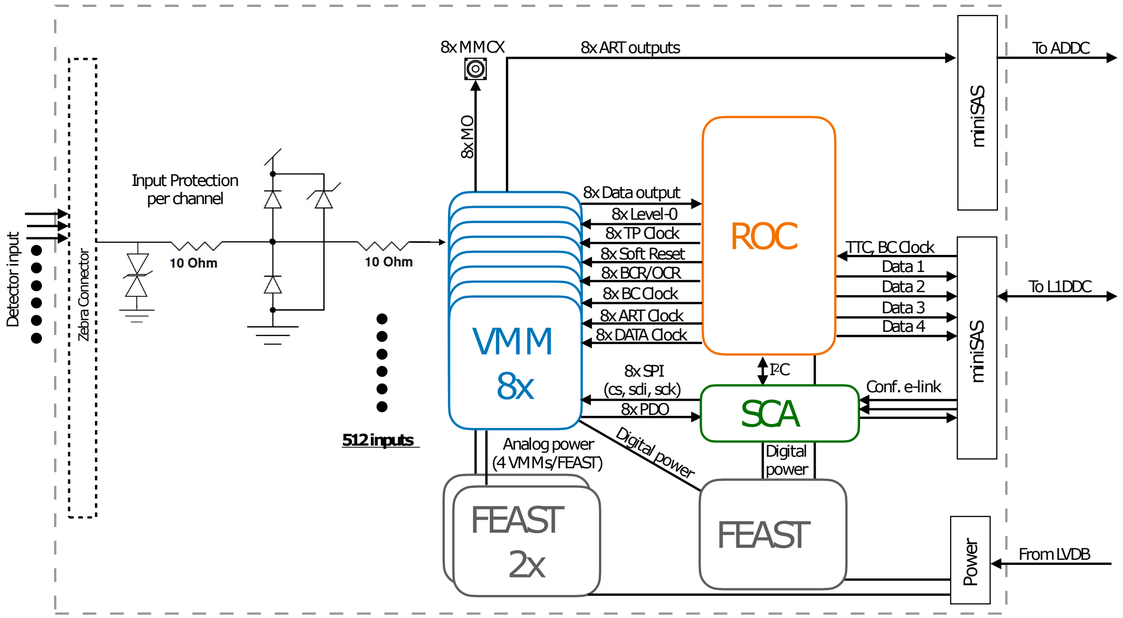
Packaging issue

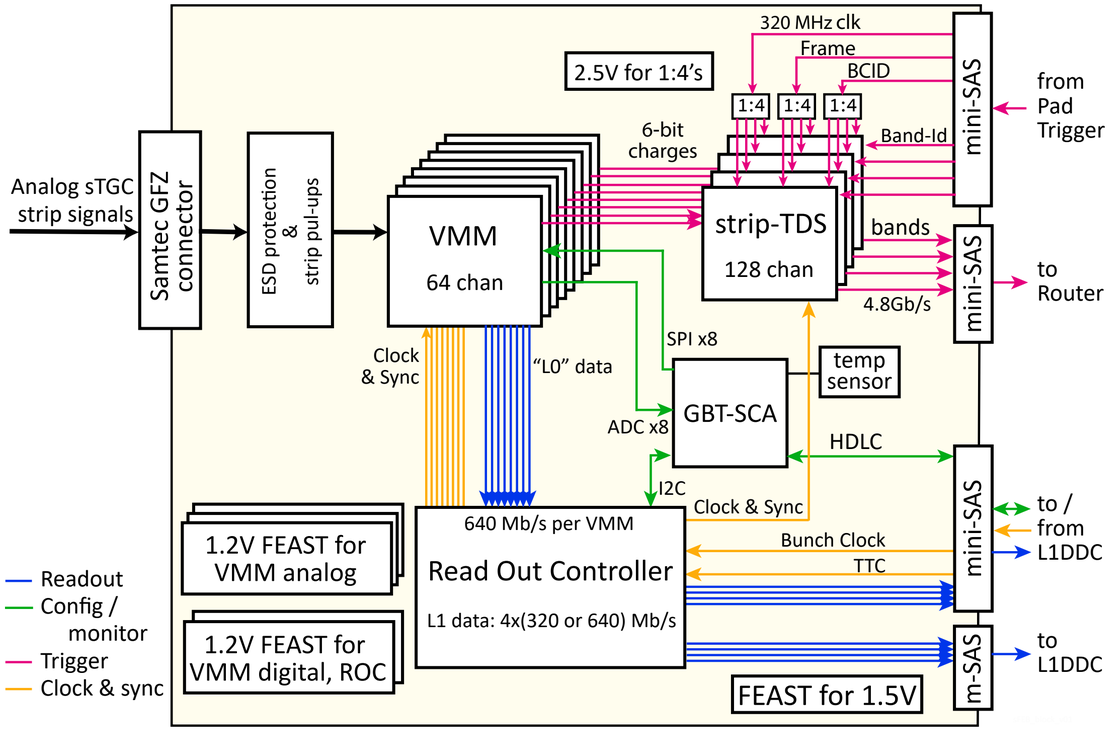
- Why ?: The package bend when CTE (Coefficient of Temperature Expansion) of the substrate is larger compared to the silicon or the mold compound.
- At the die attach cure temperature the substrate is then flat and stress free connected to the silicon die.
- The warpage is then worse at the temperature farthest away from the attach cure temperature i.e. room temperature.
- The reflow temperature will be higher than the die attach cure and post mold cure temperature, so the warpage I expect to be significantly smaller (and in the opposite direction) compared to room temperature.
- **<u>IMEC/ASE though acknowledged the issue and proposed to increase the mold thickness to 0.65 from 0.53</u>**





Board developments





VMM implementation in NSW