Readout of Straw Tube Tracker for Neutrino Physics

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for the WP3 Project D

DRD1 collaboration meeting
Topical workshop on electronics for gaseous detectors
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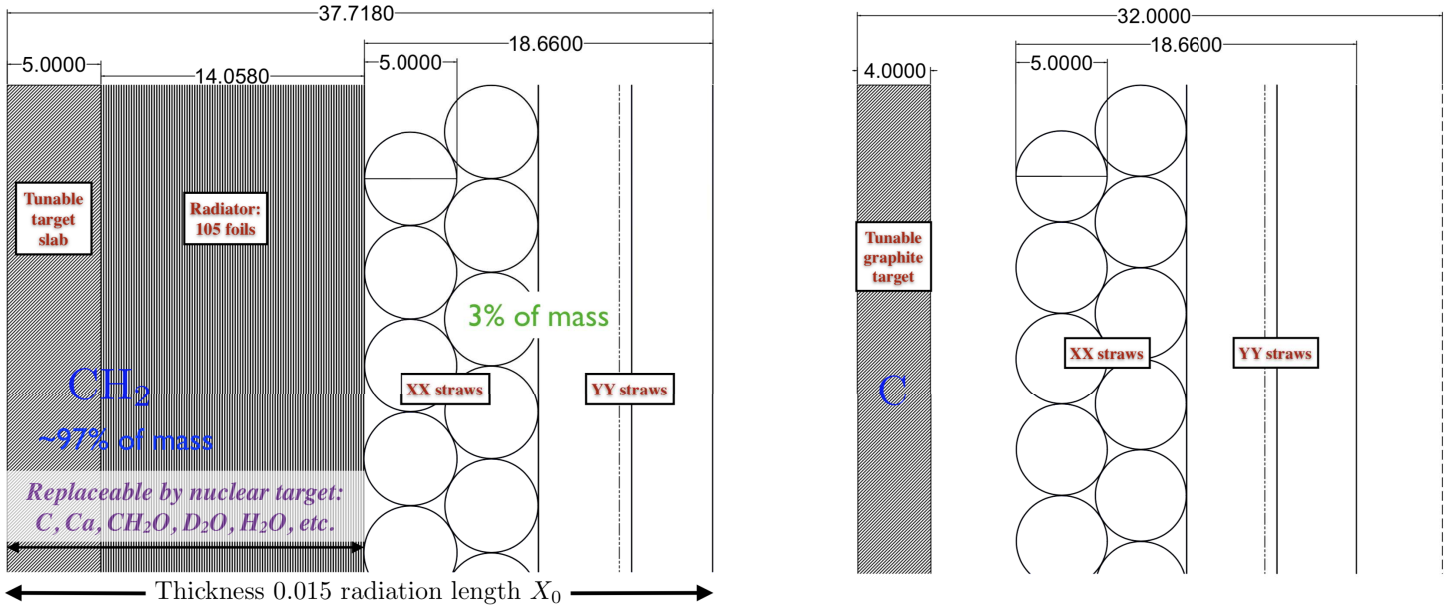
STRAW TUBE TRACKER FOR NEUTRINO PHYSICS



- *Many (∼80-100) thin (∼1.5% X_0) passive targets separated from active detector (straw layers);*
- *Targets of high chemical purity* (∼ 97% *of mass) keeping average density* $\rho \leq 0.17\ g/cm^3$
- *High track sampling: 0.15 (0.36)%*X_0 $\perp$ ($\parallel$) *with total detector dimensions* $\sim 1X_0$;
- *"Solid" hydrogen target from a subtraction of* CH_2 & C *targets;*
- *Common tracking modules with 4 XXYY straw layers across entire detector.*

$\Longrightarrow$ *Individual targets can be replaced with planar targets of desired material of varying thickness*

REQUIRED PERFORMANCE

- *STT designed to offer a control of ν-target(s) similar to $e^{\pm}$ fixed-target experiments*
  $\Longrightarrow$ *Detector fully tunable/configurable during data taking*

- *Low-density design & target mass allow accurate in-situ calibrations:*
  - $\boxed{\Delta p < 0.2\%}$ *momentum scale uncertainty from $K_0 \to \pi^+\pi^-$ in STT volume ($\sim$ 300k);*
  - *p reconstruction and identification, vertex, etc. from $\Lambda \to p\pi^-$ in STT volume ($\sim$ 500k);*
  - *$e^{\pm}$ reconstruction and identification from $\gamma \to e^+e^-$ in STT volume ($\sim 10^7$).*

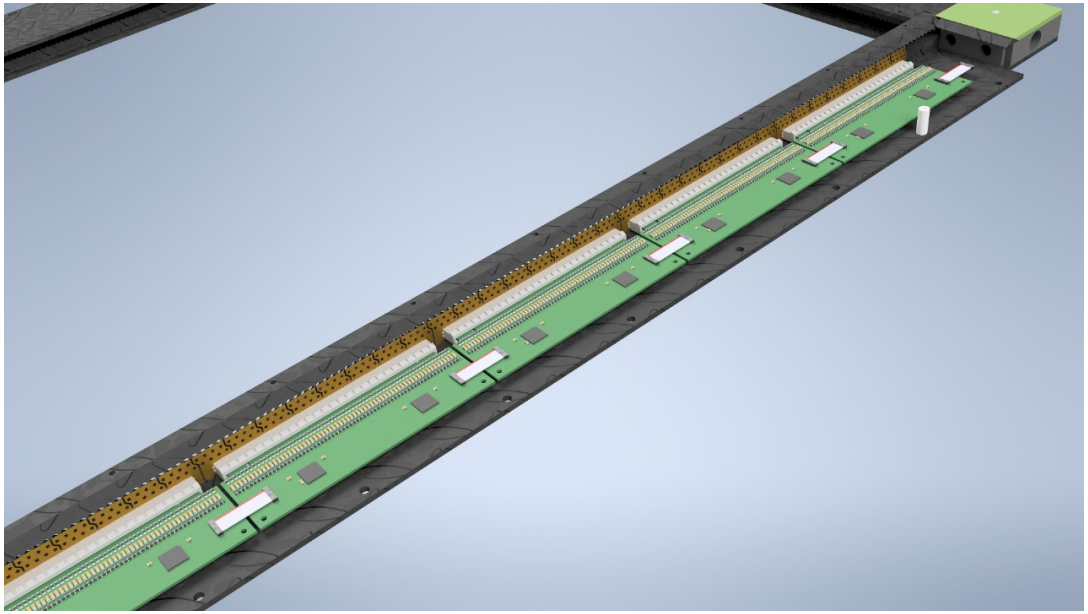
- *Combined particle ID & tracking over the entire STT volume:*
  - *Electron ID with Transition Radiation (TR) and dE/dx* $\Longrightarrow$ $\boxed{\pi/e \sim 10^{-3}}$;
  - *4π detection of π^0 from γ conversions ($\sim 49\%$) within the STT volume;*
  - *$p/\pi/K$ ID with dE/dx, range, and time-of-flight with surrounding calorimeter.*

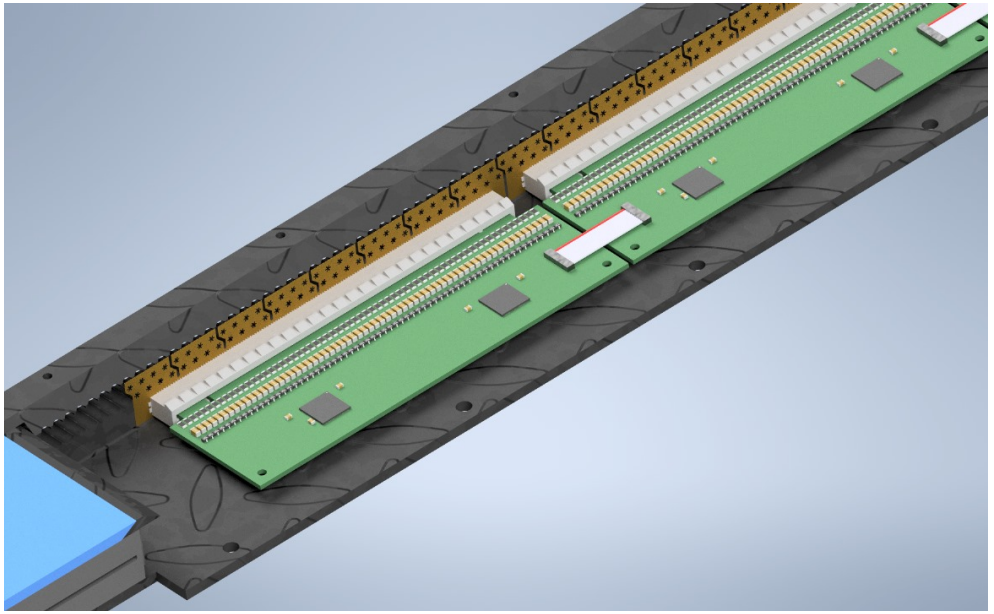
  $\Longrightarrow$ *Readout of both drift time and charge with 10^3 dynamic range for $\mathcal{O}(100k)$ straws*

- *Accurate reconstruction of transverse plane kinematics from particle 4-momenta:*
  - *"Transparent" target/tracker system with dimensions* $\boxed{\sim 1X_0}$ *and* $\boxed{4\pi}$ *acceptance;*
  - *Momentum resolution $\delta p/p \sim 3\%$, angular resolution $\sim$ 1-2 mrad.*

INTEGRATED STT READOUT BOARDS

V. Bautin





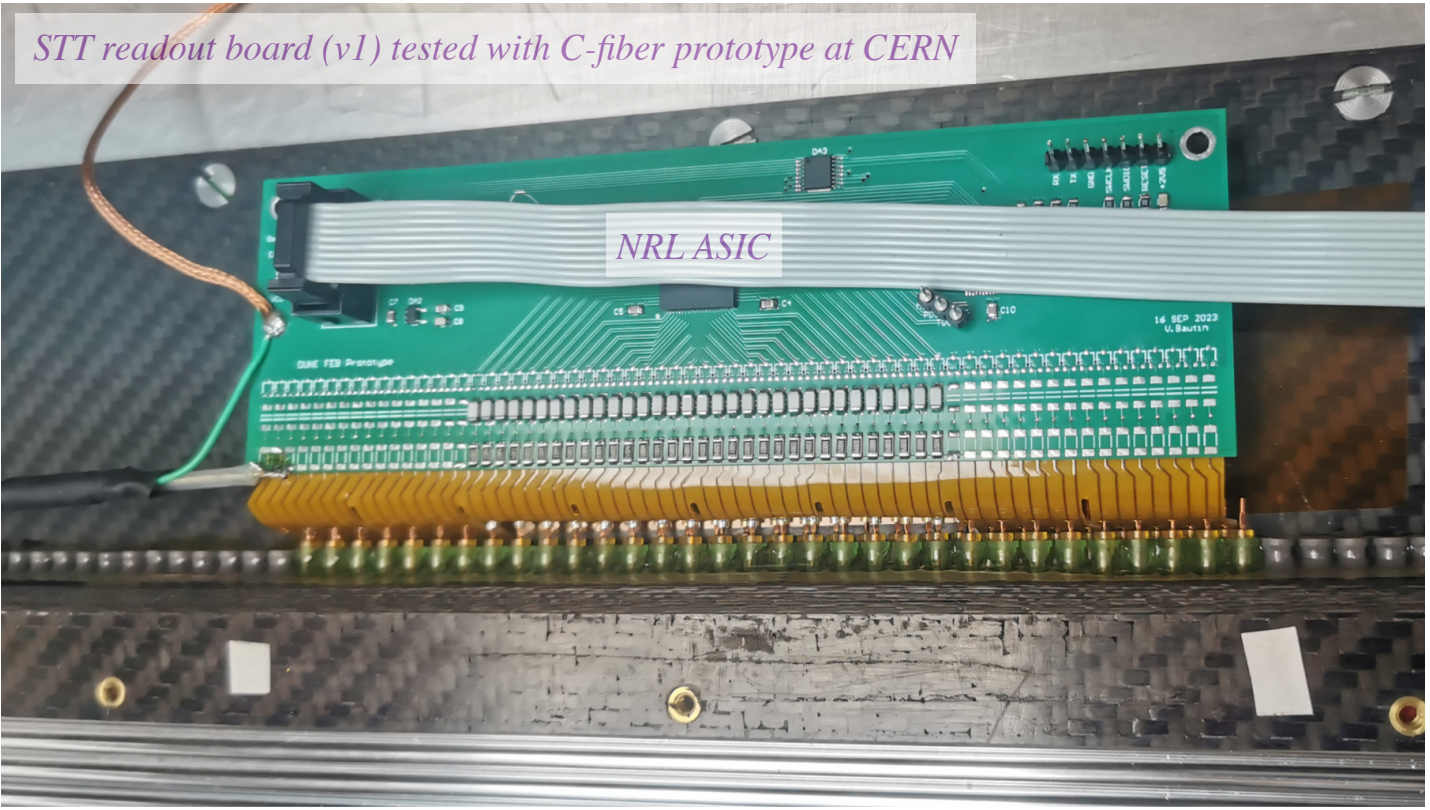
✦ *Integrated boards reading up to 64 straws each with ASIC + micro-controller (MCU):*

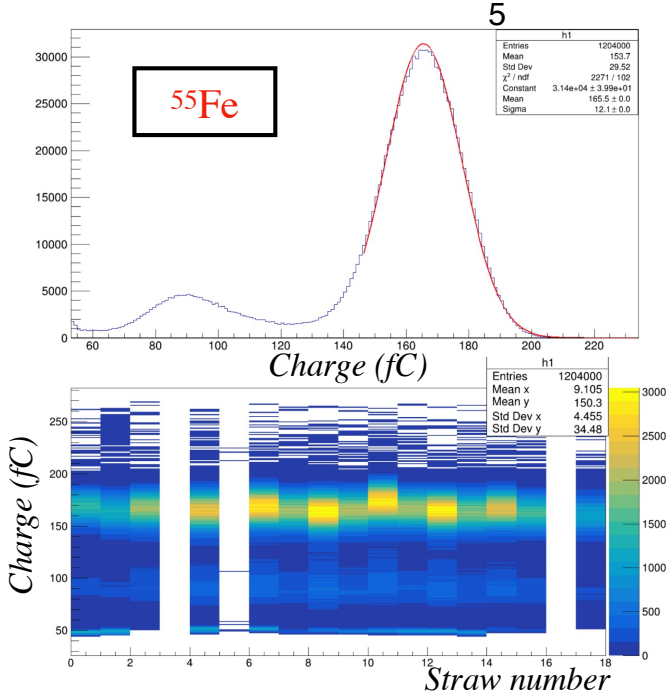
- *Connection with straw pins via flexible kapton PCBs with PCIe connector for easy upgradability/replacement;*
- *Design variants with different ASICs: NRL analog (G. De Geronimo), VMM3a, custom ASIC;*
- *Surge protections, LV fuses, and Solid State Relay (SSR) for HV connect/disconnect.*

✦ *Low-power boards (~0.65 W for 64 channels with NRL ASIC) minimizing signal path*

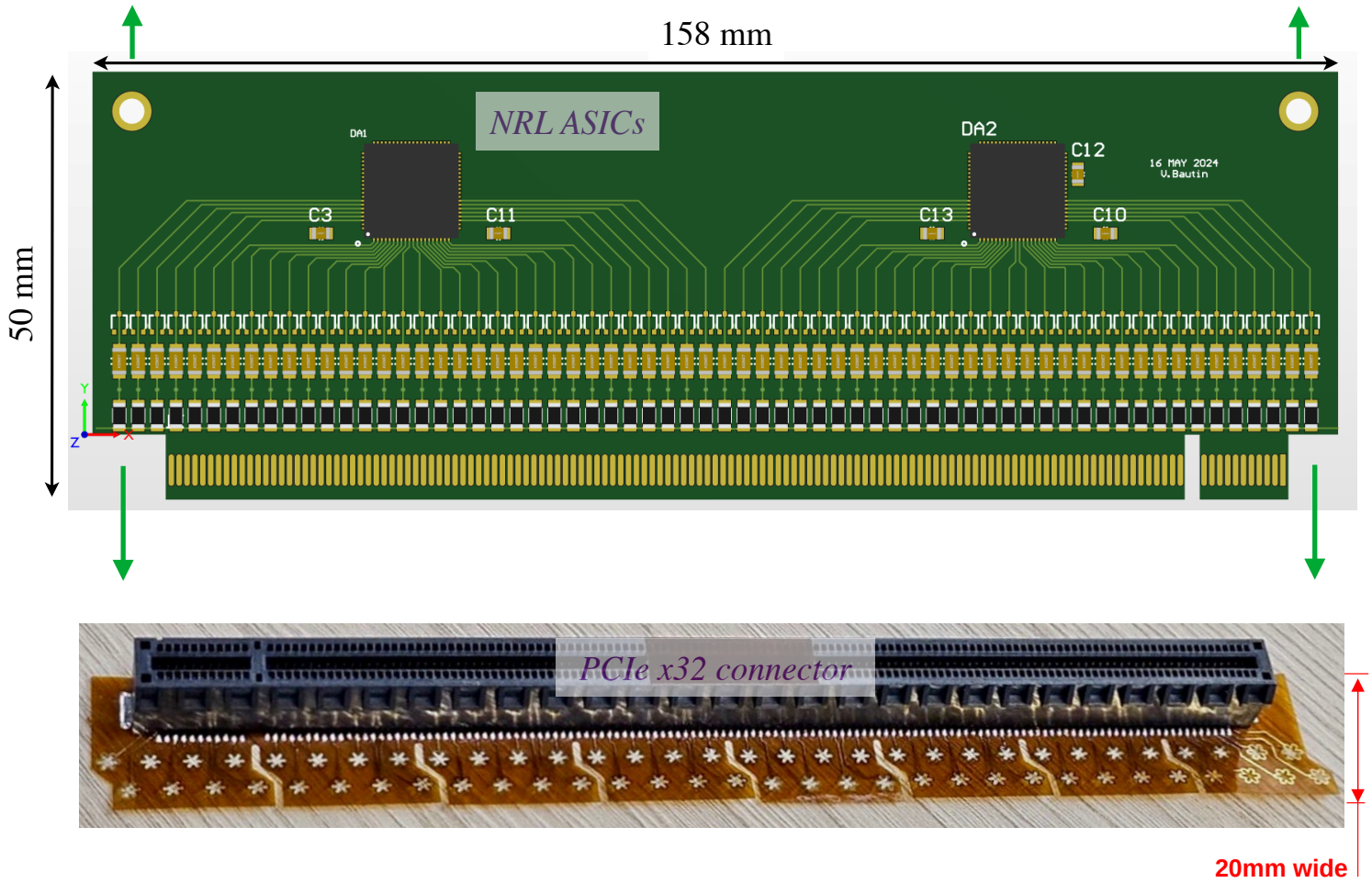
$\Longrightarrow$ *First version (v1) successfully tested, prototypes of revised version (v2) in preparation*

STT readout board (v1) tested with C-fiber prototype at CERN

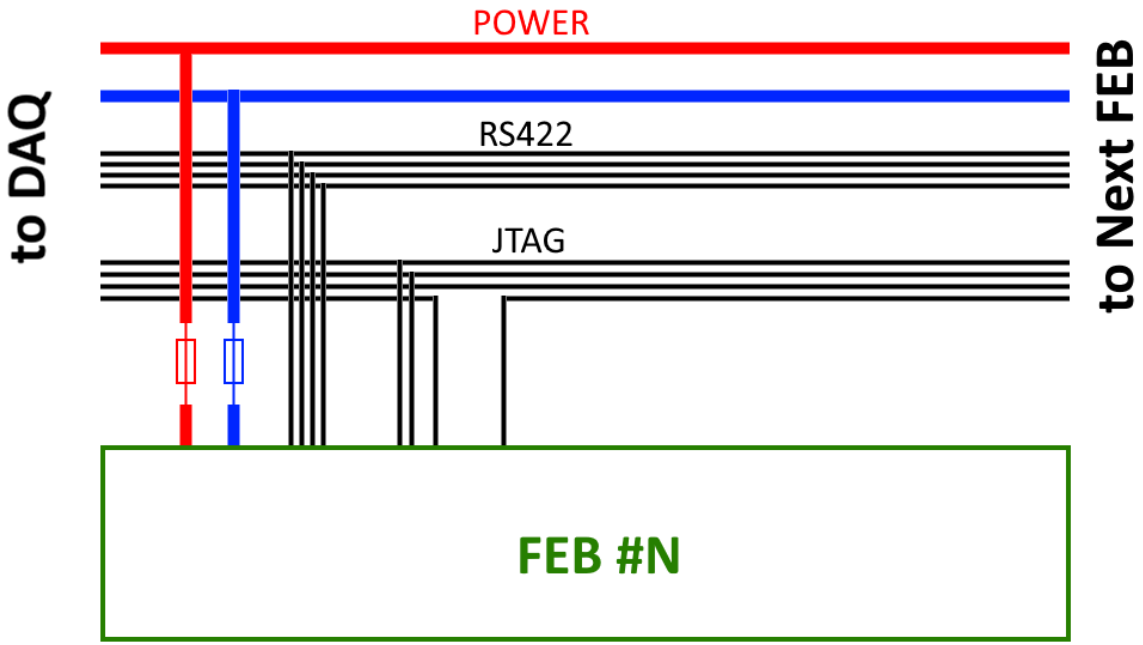




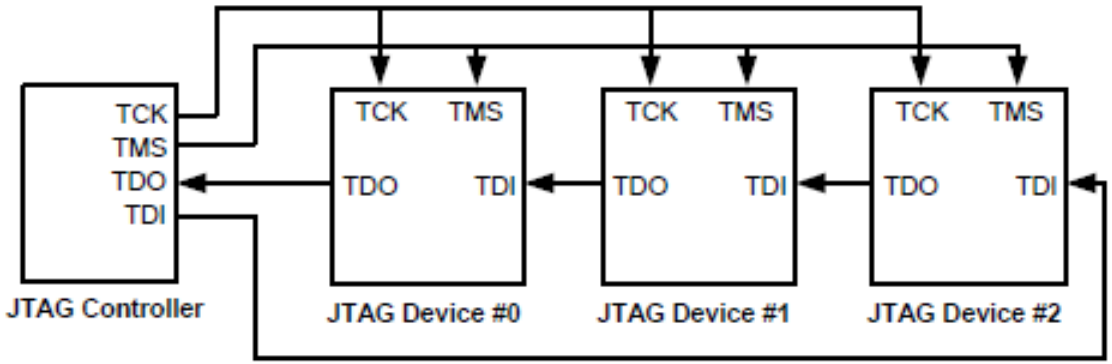
STT prototype 1.2 m × 0.8 m (~700 straws in 4 XXYY layers)
28 mm thick overall with C-fiber frame built at CERN



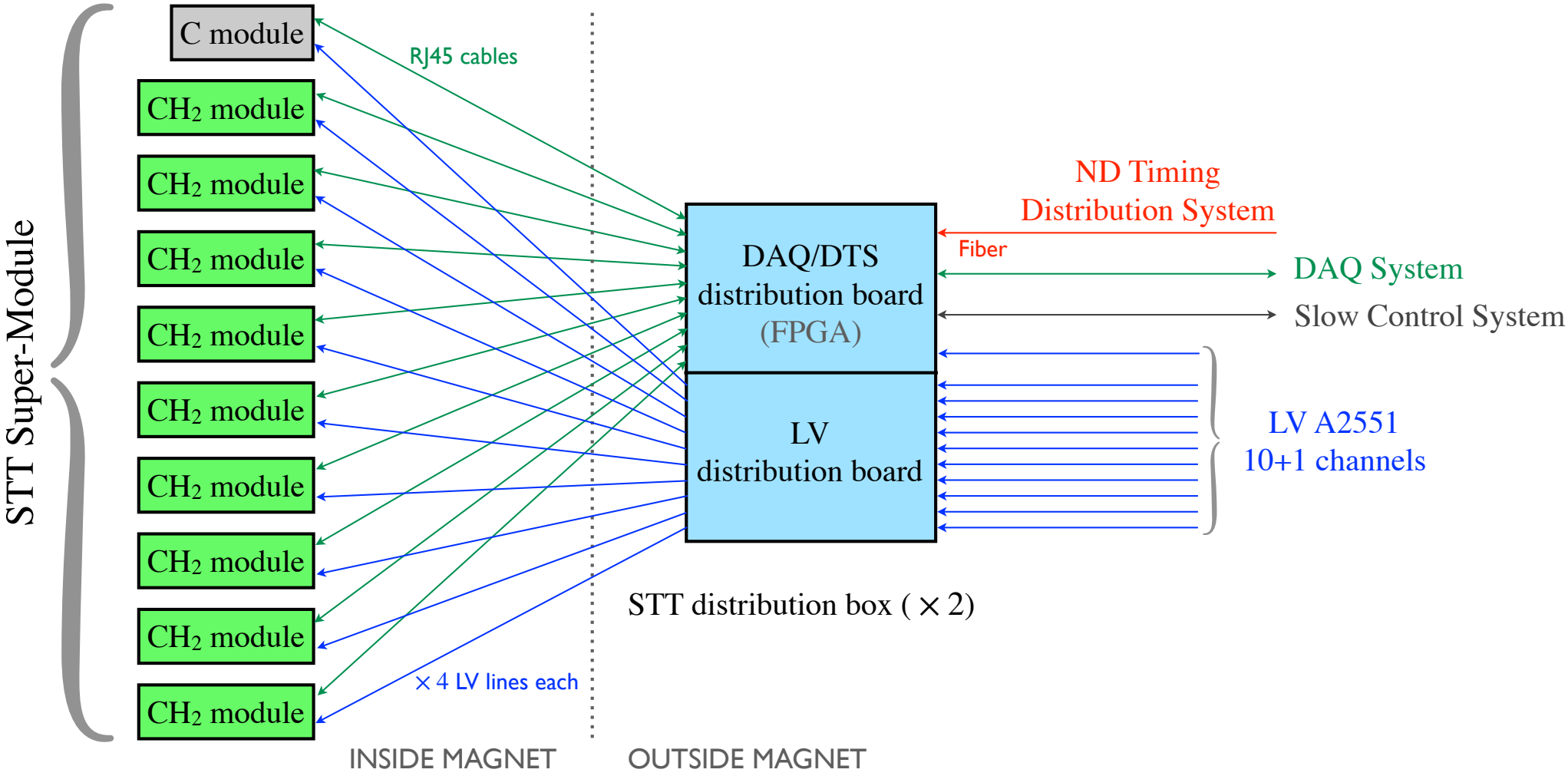
Revised design (v2) of the readout board and of the connecting flexible kapton board



BUS interface connecting in parallel all readout boards (failure of a FEB does not affect others)

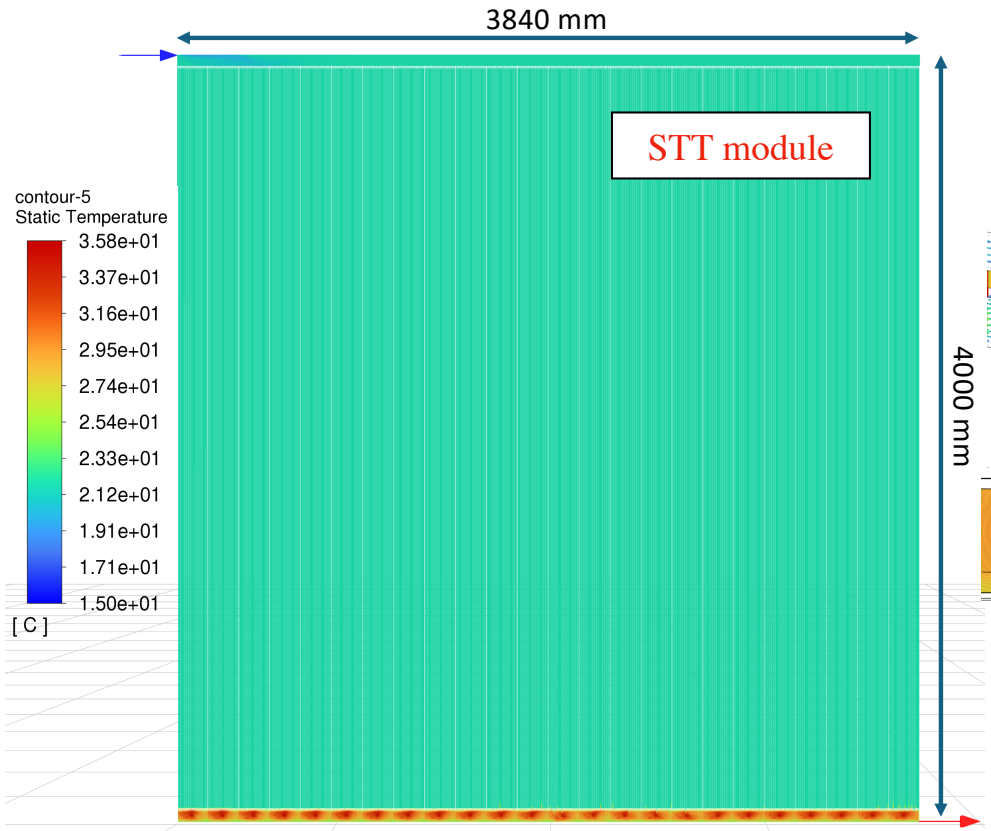


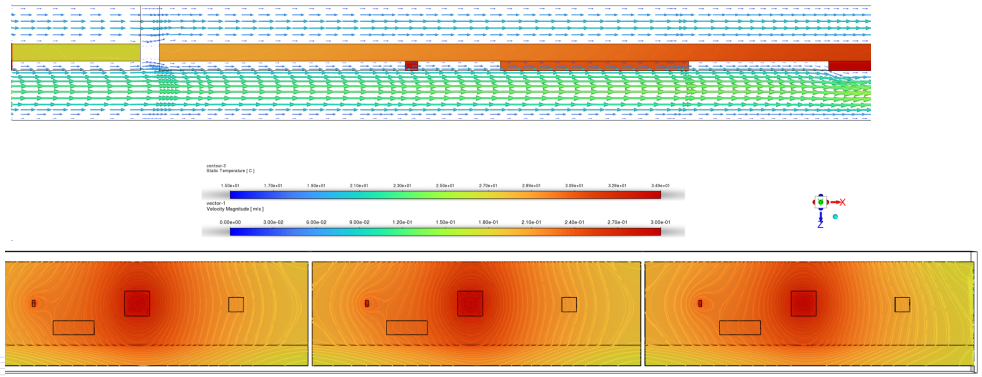
JTAG chain to update firmware across all readout boards



Schematic diagram of the DAQ/DTS and LV connections for one STT Super-Module

THERMAL ANALYSIS

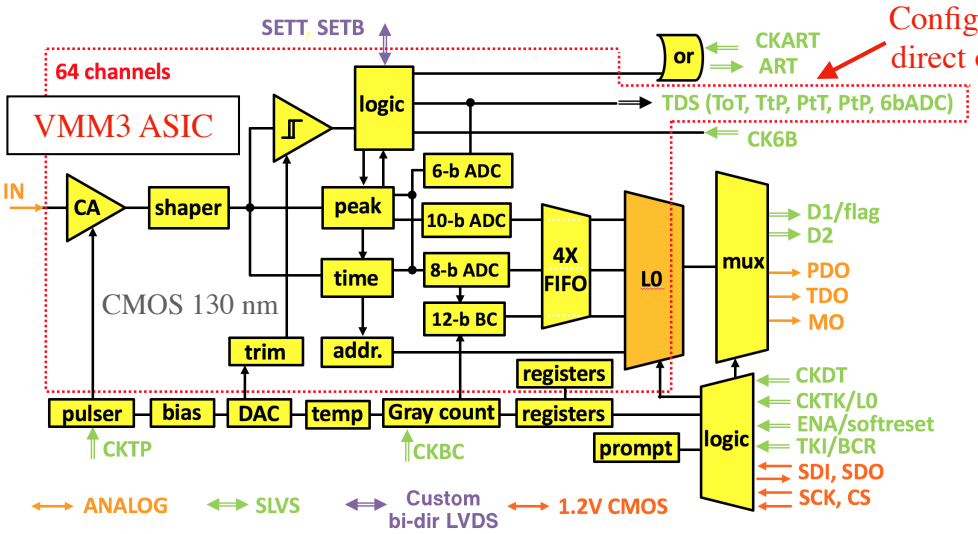


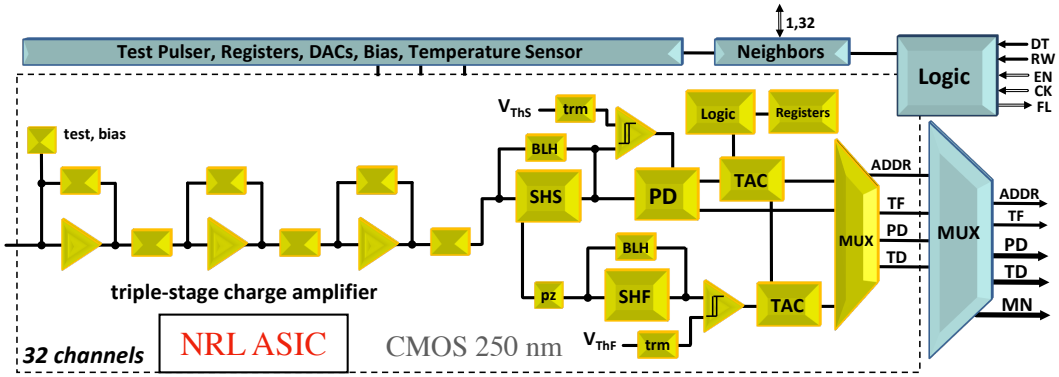


- *Thermal analysis of full scale STT module with 24 integrated readout boards;*
- *Self-cooling design with expected total power dissipation about 0.65 W per board (mostly ASIC)*

$\Longrightarrow$ *Maximal temperatures obtained below 40^0 C allow extended board lifetime*

VMM3A ASIC AND NRL ASIC



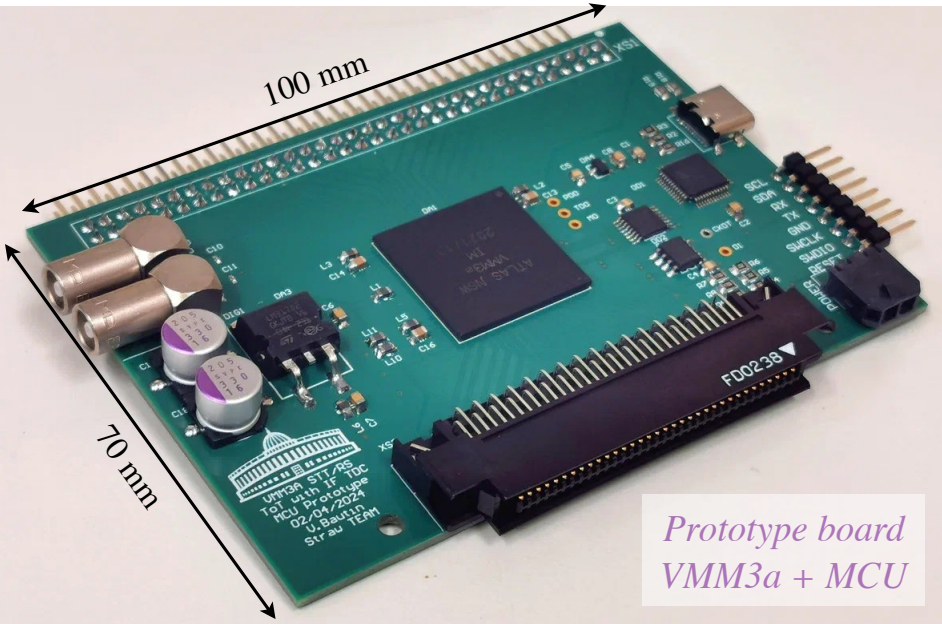


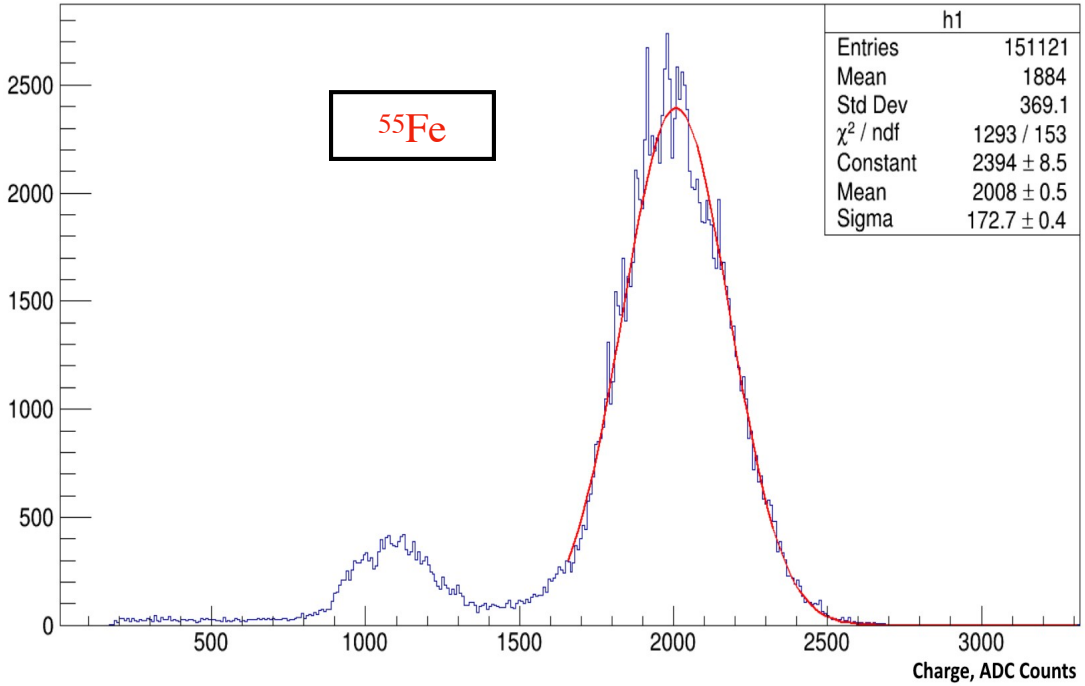
✦ *Design variant of STT readout board with existing VMM3a as backup solution:*

- *Use VMM3a direct output in "external" ADC mode with the MCU (bypassing internal ADCs);*
- *Readout variant readily available which could be used during construction and initial data taking;*
- *Default STT readout minimizing project risks while developing custom ASIC.*

✦ *Design variant with existing NRL ASIC to test base architecture for custom ASIC*

$\Longrightarrow$ *Flexible design allows easy exchange/upgrade of individual STT readout boards*



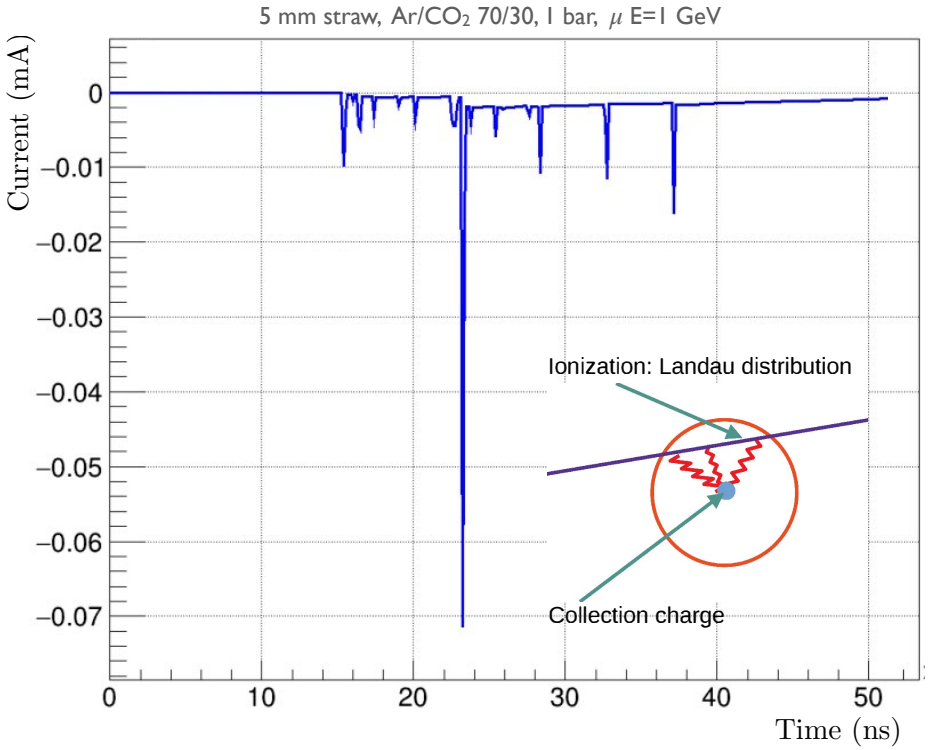


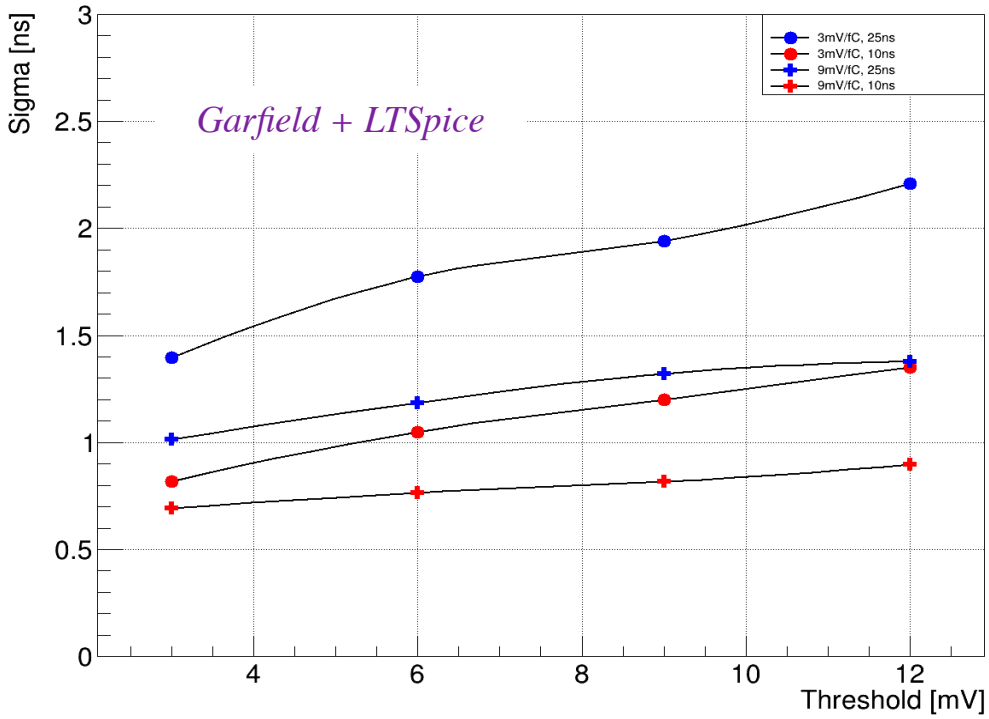
- *Prototype board with VMM3a in "external" ADC mode and 12-bit 4MSPS ADC in MCU;*
- *Successful test of charge readout from a straw tracker prototype with ^{55}Fe source;*
- *External ADC mode fixes known bad ADC/TDC performance in VMM3a continuous mode.*

$\Longrightarrow$ *Prototype with the form factor and connections of STT readout boards in preparation*

PRELIMINARY ASIC REQUIREMENTS

- *Modularity*: *64 channels*
- *Input capacitance*: *10-40 pF (optimize for 40 pF)*
- *Flat cable*: *~1 cm traces + PCIe connector (capacitance <1 pF)*
- *Architecture*: *dual sub-channel with independent gain and shaper*
  (i) fast shaper & high gain for time measurement
  (ii) slow shaper & low gain for energy measurement
- *Minimum charge*: *4 fC (time measurement), 20 fC (energy measurement)*
- *Maximal charge*: *10 pC (energy measurement)*
- *Dynamic range*: *1,000 (energy measurement)*
- *Timing resolution*: *< 1ns*
- *Gain settings*: *(i) 6, 9, 12 mV/fC for time measurement*
  (ii) ≤0.5 mV/fC for energy measurement
- *Peaking times*: *(i) 10, 25 ns fast shaper*
  (ii) 50, 100 ns slow shaper
- *Power consumption*: *<10 mW/channel*
- *Expected rates*: *≪1 kHz*

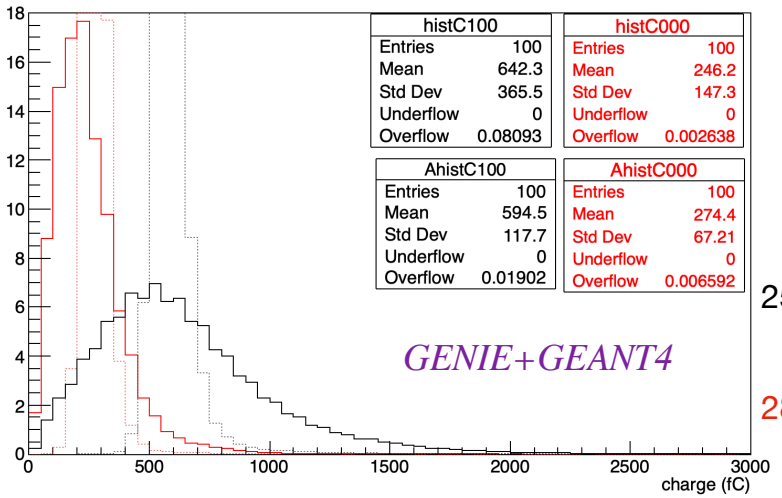




Timing resolution depends on the peaking time and gain used in the FE readout: study impact of time-walk corrections and noise

$\Longrightarrow$ *Peaking time ~10 ns with high gain can give resolutions around 1 ns*

muon

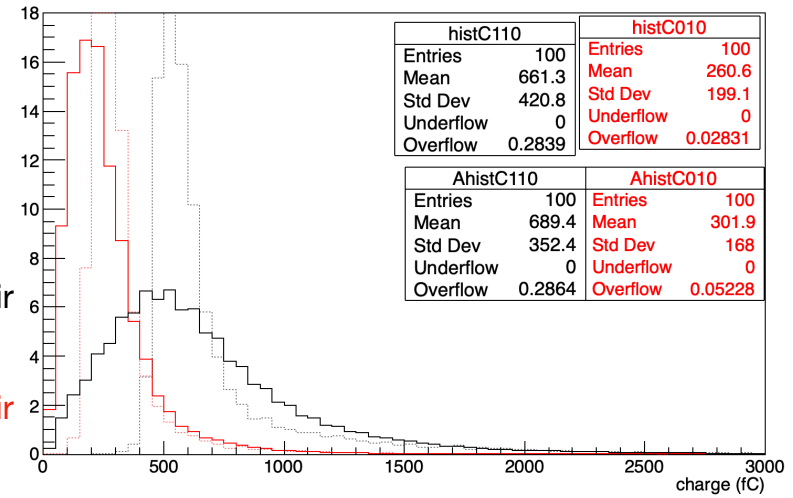


Gas gain
25,000

Xe/CO2
25.6 eV/pair

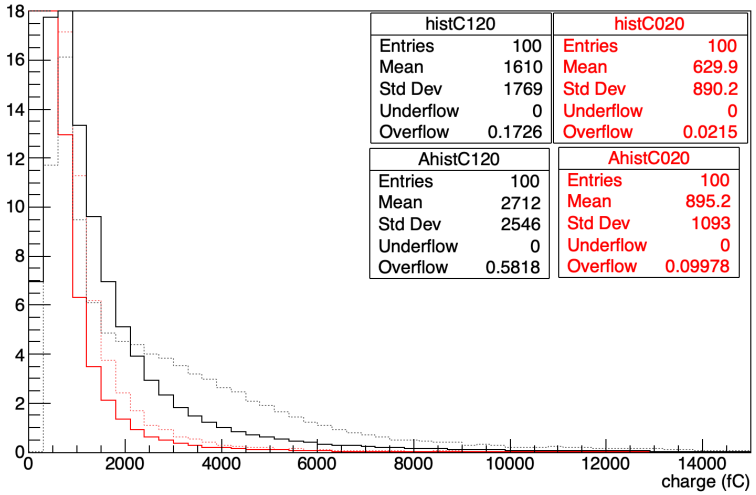
Ar/CO2
28.4 eV/pair

pion

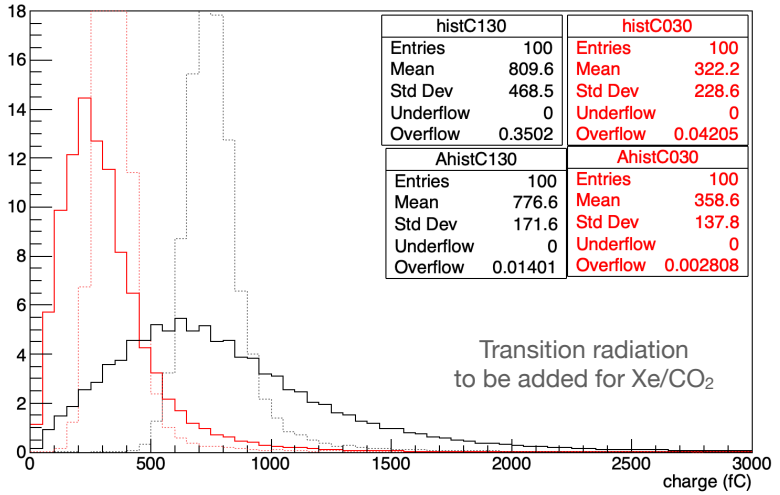


Dashed - averaged for the track
Solid - individual straws

proton



e+-



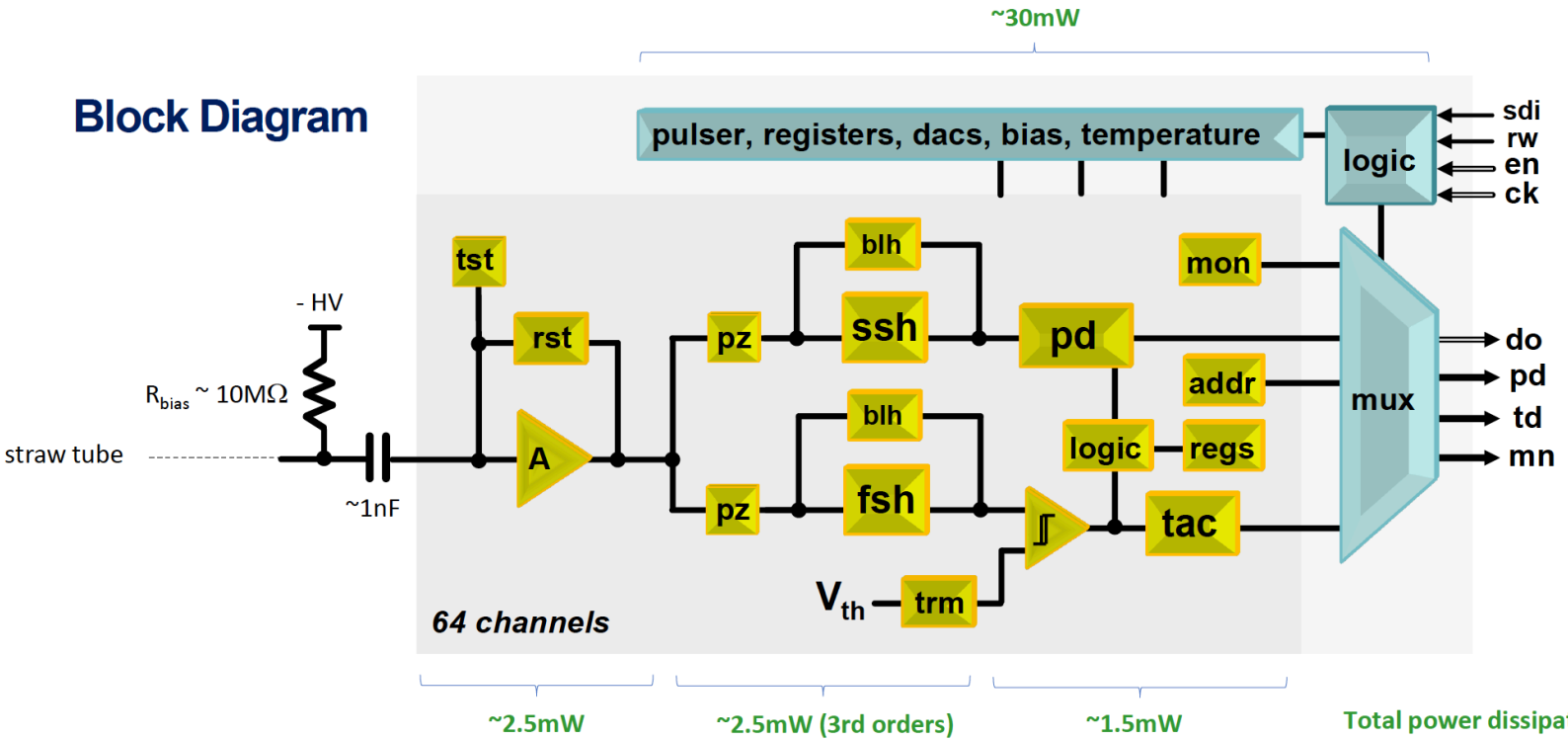
$\Longrightarrow$ *Dynamic range ~1,000 with charge <10 pC and peaking times ~50 ns*

CUSTOM ASIC FOR STT

G. De Geronimo

- programmable test pulse generator
- programmable event threshold
- temperature sensor
- 1.8V analog supply/ground with self-biasing circuits
- 1.8V digital supply/ground

Block Diagram



CMOS/LVDS interface for configuration & control with programmable termination

mixed-signal event output:
- data-flag with serialized address
- peak amplitude
- TAC amplitude
- analog monitor

Total power dissipation: 7.5mW x 64 +30mW = 510mW @ 1.8V

- optimized for 50pF
- charge amplifier linear to 10pC
- dedicated front-end supply
- programmable gain
- programmable test capacitor
- continuous adaptive reset

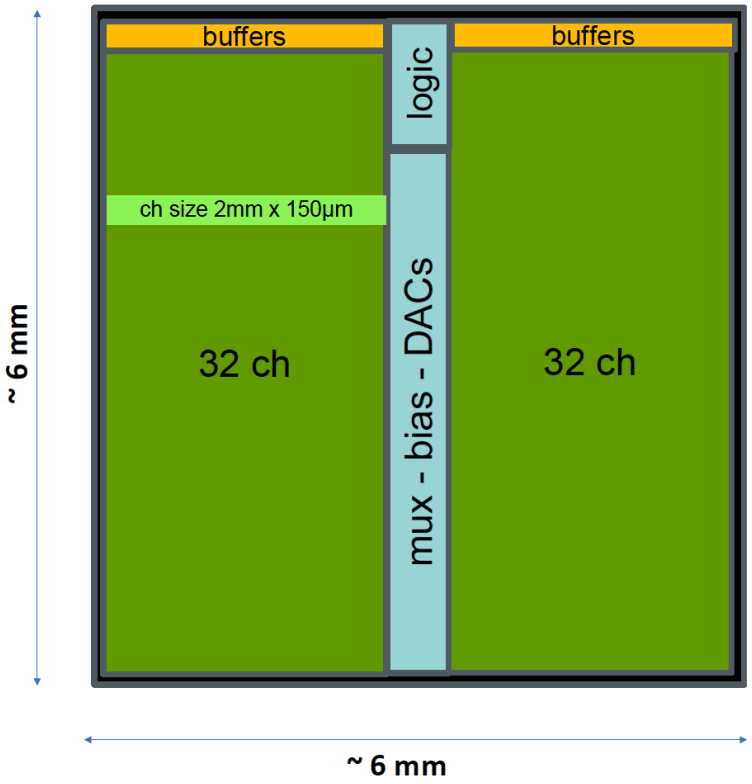
- programmable fast shaper for timing measurement
- programmable slow shaper for charge measurement to 10pC
- high-speed low-hysteresis discriminator with trimmer
- leading-edge timing detection on fast shaper
- timing resolution < 1ns at 4fC
- programmable low-noise time-to-amplitude converter (TAC)
- peak detection on slow shaper

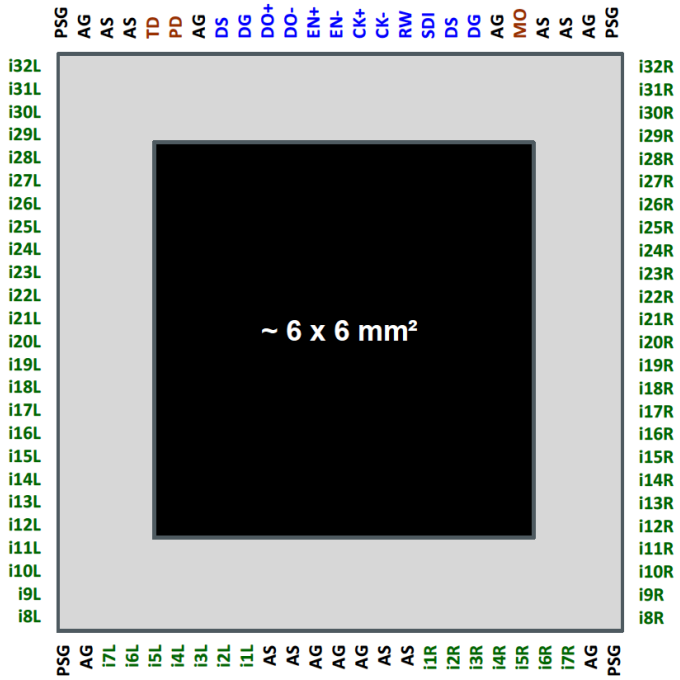
- event flag with programmable delay
- sparse readout with event multiplexing
- programmable analog monitoring
- local registers
- channel power-down

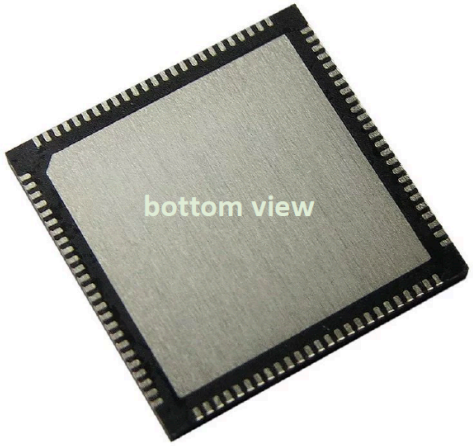
sub-circuits and functions largely inherited from well established NRL and VMM

Floorplan, Pinout, Packaging

Technology: 180nm, 1.8V (~1.5V linear swing)







Fabrication MPW for prototypes

Packaging QFN100 12×12 mm²

Estimated yield ~ 90%

SUMMARY

- *Straw Tube Tracker for neutrino physics applications characterized by compact tracking modules with 4 XXYY straw layers and high level of detector integration*

- *Developed integrated boards reading 64 straws with ASIC + micro-controller:*
  - *Design variants with different ASICs: NRL analog, VMM3a, custom ASIC;*
  - *Low-power boards (0.65 W for 64 channels with NRL ASIC) minimizing signal path.*

  $\Longrightarrow$ *Flexible design allows easy upgrade/exchange of individual readout boards*

- *Prototypes of STT readout boards equipped with NRL and VMM3a ASICs tested with straw tracker prototypes*

- *Preliminary studies for the development of custom ASIC for STT*

  $\Longrightarrow$ *ASIC requirements and overall architecture based on VMM3a and NRL*

Backup slides