

uRoc Concentrator for VMM Front End's.

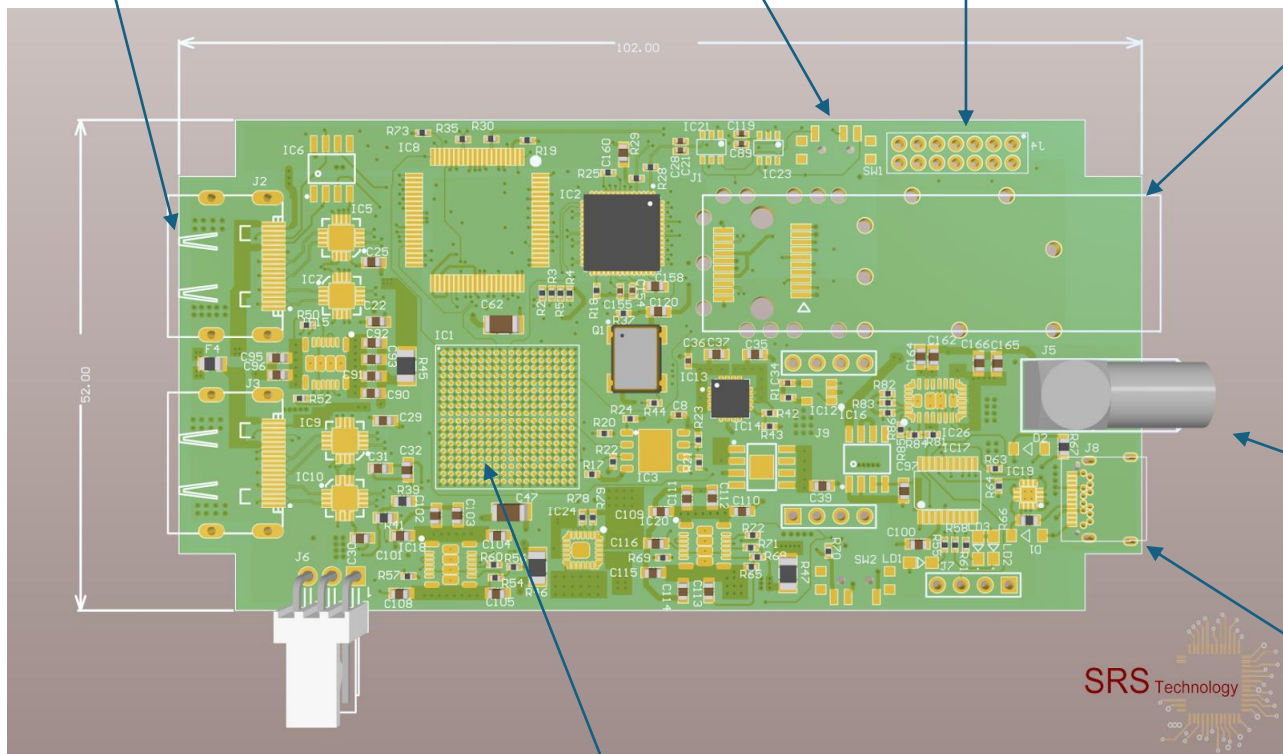
μRoc V1 design

2 Hybrids inputs plus power trough cable

Switch for Ethernet or SERDES protocol

Jtag

SFP for 1GBE fiber or copper



Output for the bias voltage

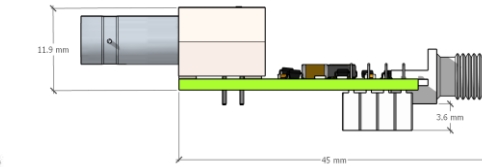
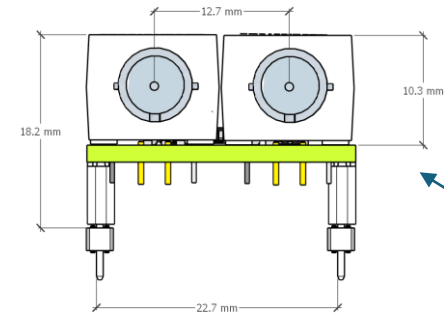
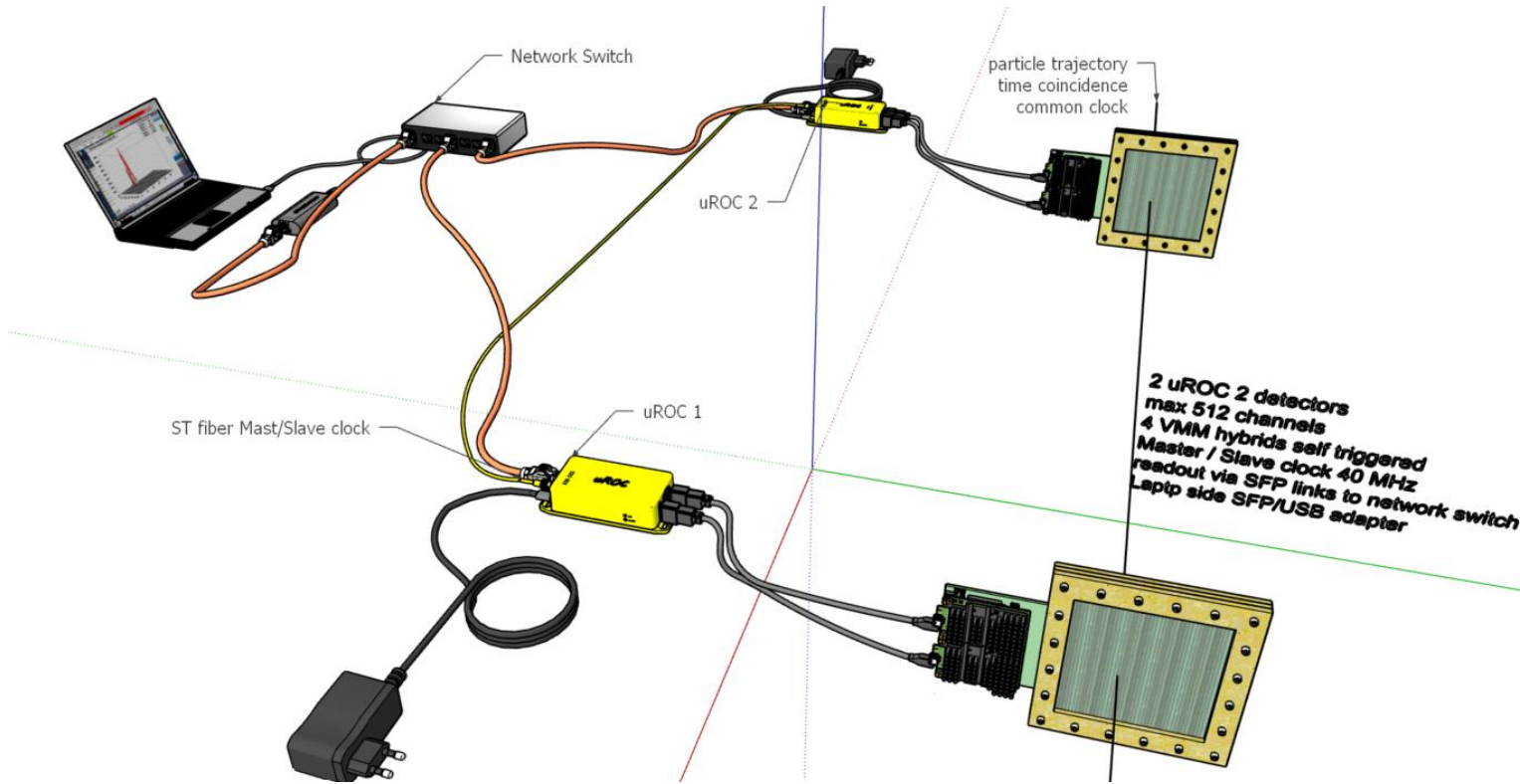
Artix 7 FPGA

USB C Power

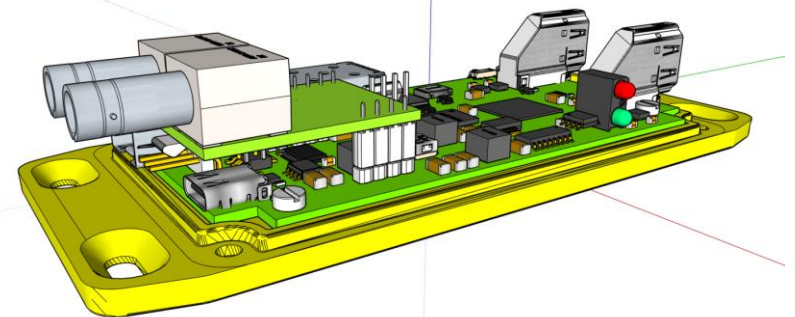
- μRoc is a mini concentrator for the VMM hybrids very small 102x52 mm almost the size of the hybrids that can fit in the VTC box.
- Initially it was designed for SiPM applications however it works also for gas detectors.
- The μRoc is be capable to read 2 VMM hybrids with the same HDMI connectivity and also provide LV power and Bias Voltage for the SiPM's.
- The output of the μRoc is done with Fiber SFP or Ethernet SFP at 1GBE.
- For several μRoc's one board will become the master and will distribute optically to the others the clock.
- Possibility to switch On/Off μRoc's and VMM's via Lemo connector by inserting a 50 ohm termination or via command in the slow control (needs to be implemented in the firmware)
- The power consumption for the uRoc and 2 hybrids is around 15W.

μROC common clock distribution

- The circuit was defined and design is ongoing
- It does require firmware

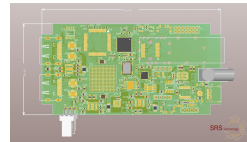
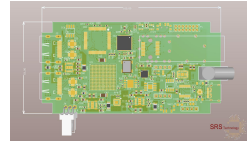
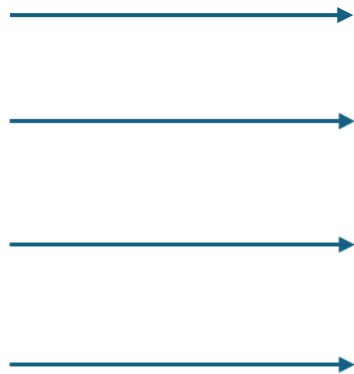


Roc Ck Mezzanine



Thanks to Hans for the 3D representation

Alternative clock distribution



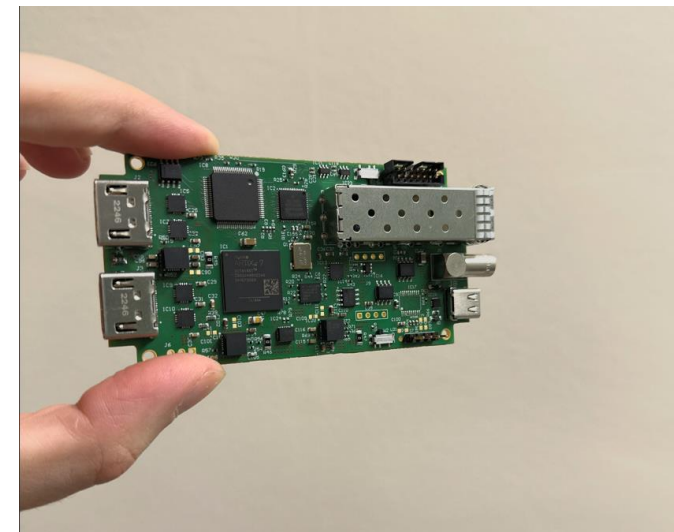
- Similar to the CTF one can make a clock fanout board
- Ideally the board should fit in the same box as the uRoc.
- The advantage is that there is no firmware required
- In the 2nd revision of the uROC an RJ45 connector will be added, and we will remove the SERDES chip (for space reasons) that is currently unused.

Status for μ Roc V1

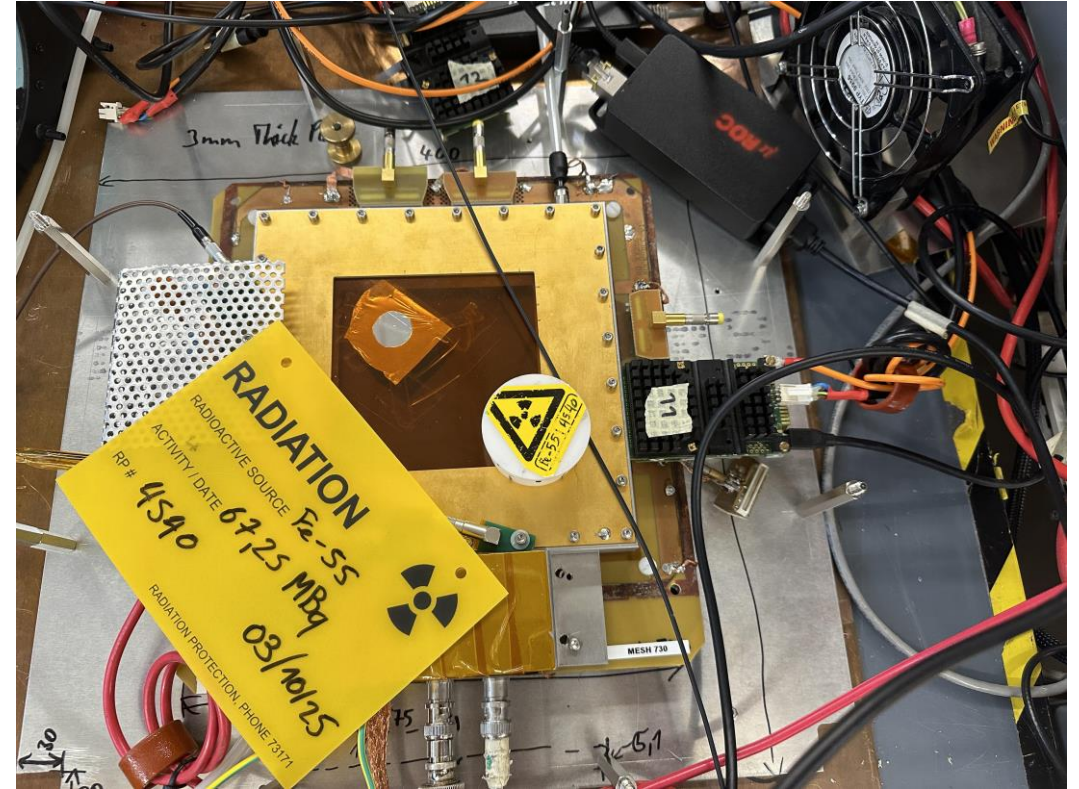
- First 2 prototypes have been built
- The firmware for the board is completed
- A second revision of the board is mandatory.
- The revision is ongoing and explorations are done for a production of larger batch.



Size comparison between
VMM Hybrid and μ Roc

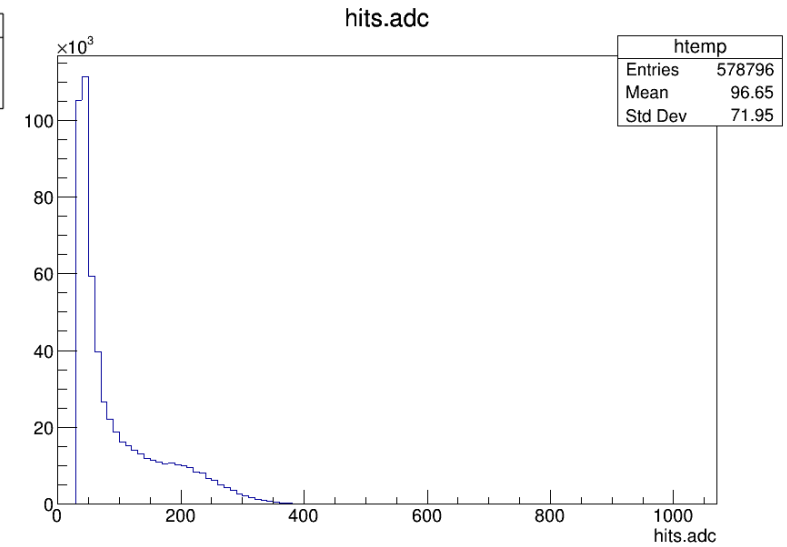
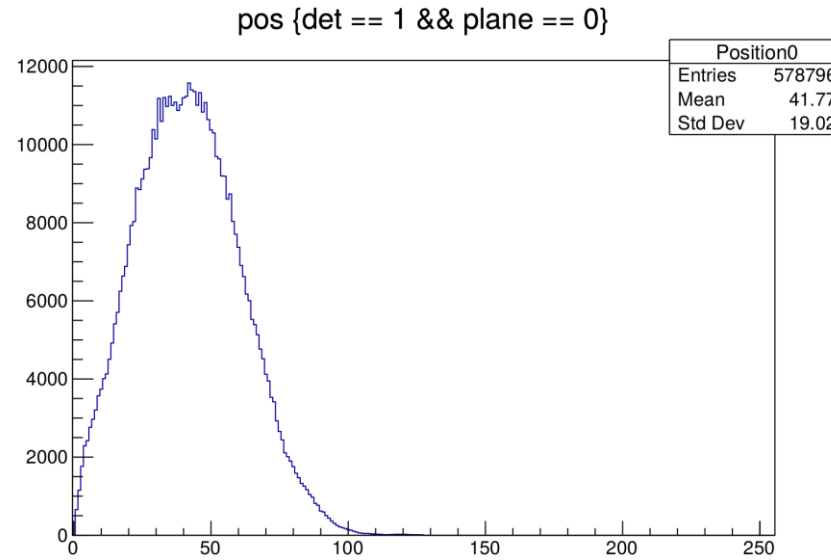
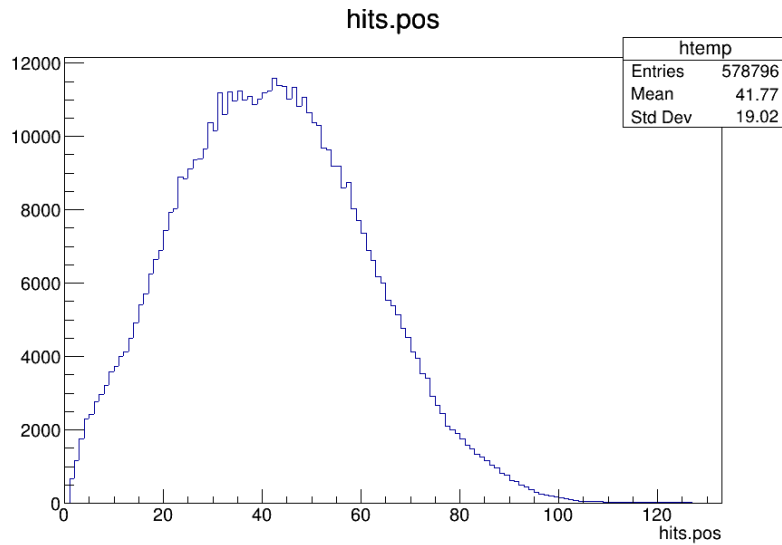


Testing set-up in the GDD lab



For better maneuverability, the uRoc was inserted in the same box as the PBX.

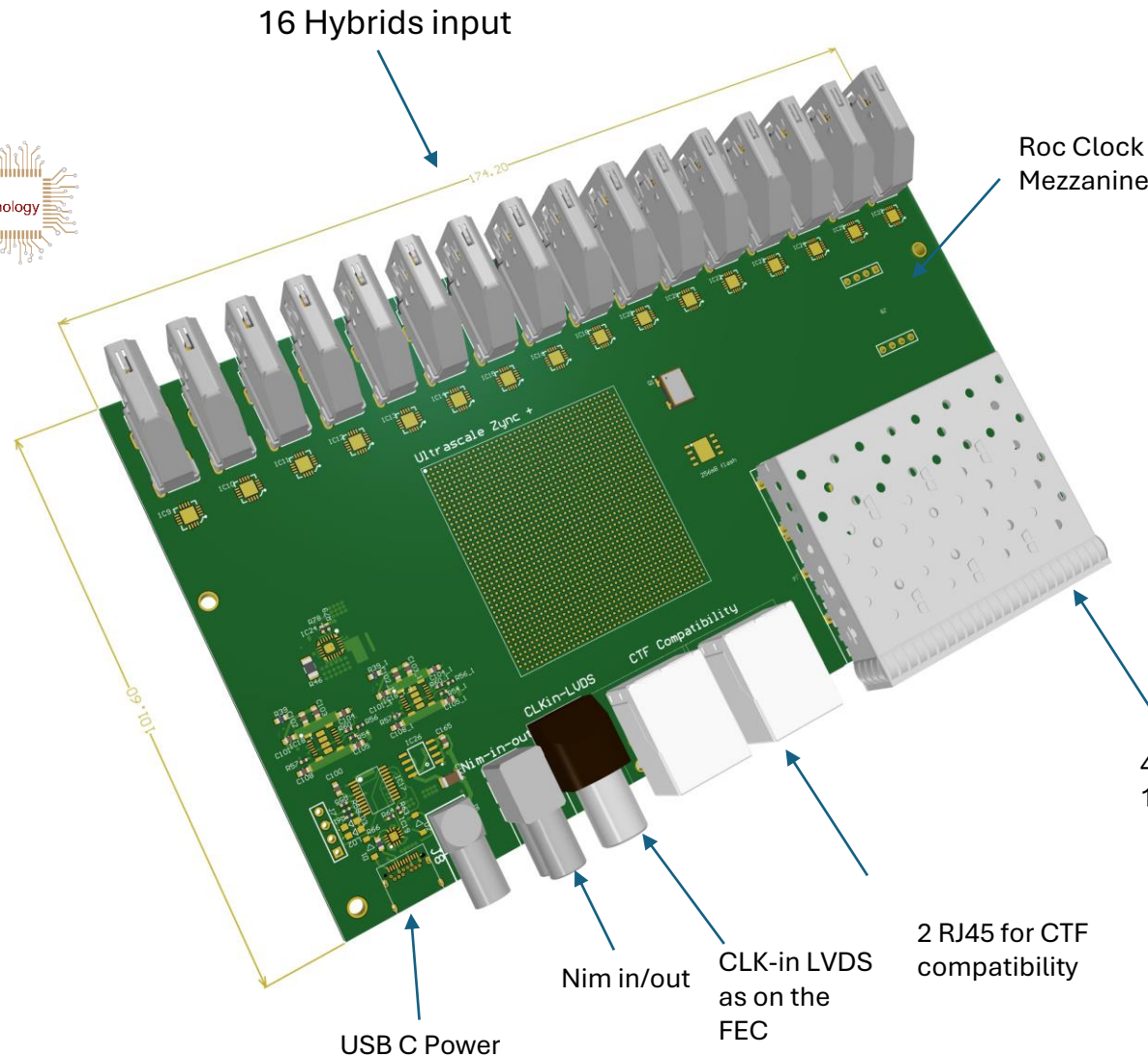
Data taken with μ Roc



Due to some bugs in the 1st μ Roc prototype we could not use the 2nd HDMI port and we took data with only 1 hybrid.

Backup Slides

maxiRoc V1



- Similar to the uRoc the maxiRoc is a compact concentrator with higher number of channels.
- The maxiRoc features the powerful Ultrascale + ZU17EG that has 32 Transceivers of 16.3 Gb/s and 16 of 32.75 Gb/s much faster than the current FEC with Virtex 6 130T at 6.6Gb/s.
- For reading 16 Hybrids at 10 GBE it requires around 70k Slices (thanks to Doro Simulation) and the Ultrascale + has 423000 LUTs (1 slice à 8 LUTs)
- 926k Logic cells and 796 Block Rams.
- The board will be in smaller size 174x101 mm and it can be fitted in a box.
- The power comes from the USB-C.
- The maxiRoc will not power the 16 Hybrids. Power should be used from the PBX or external.
- The Roc Mezzanine can be plugged in for common clock.
- The CTF can be used for common clock.
- The design has started.
- 4GB DDR4 Memory implemented

4 SFP ports where 2 are 10GB fiber and 2 TBD

2 RJ45 for CTF compatibility