Contribution to SRSe design – the eFEC module

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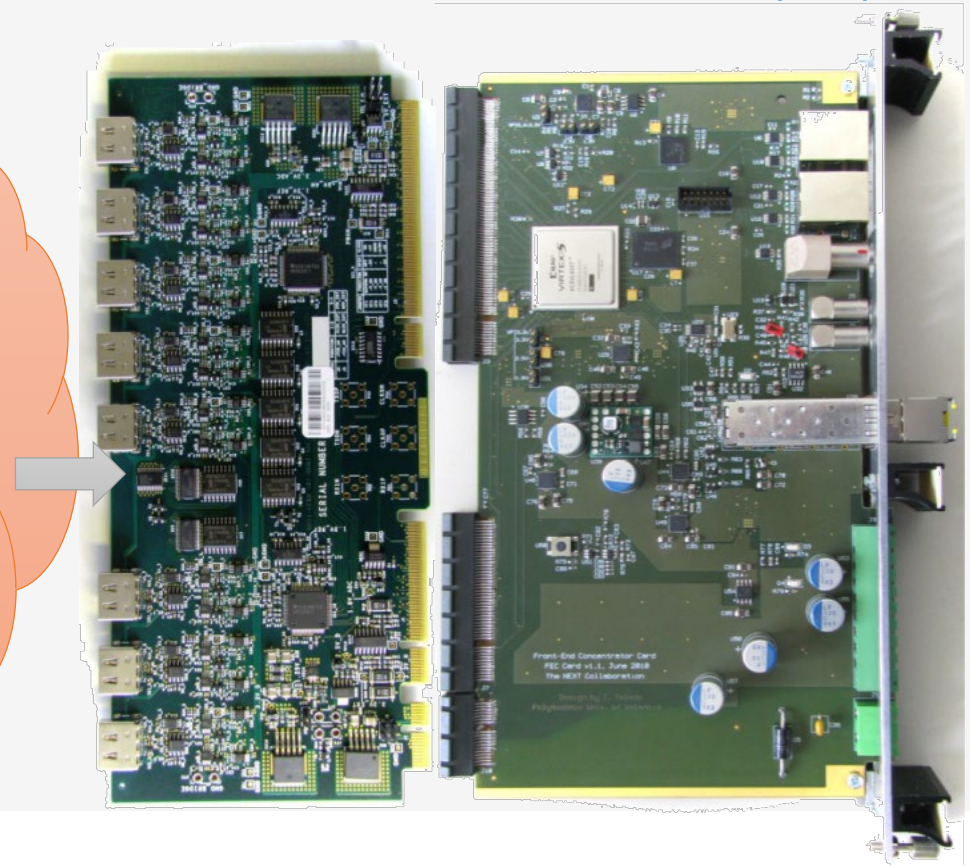
UPV group – recent activities

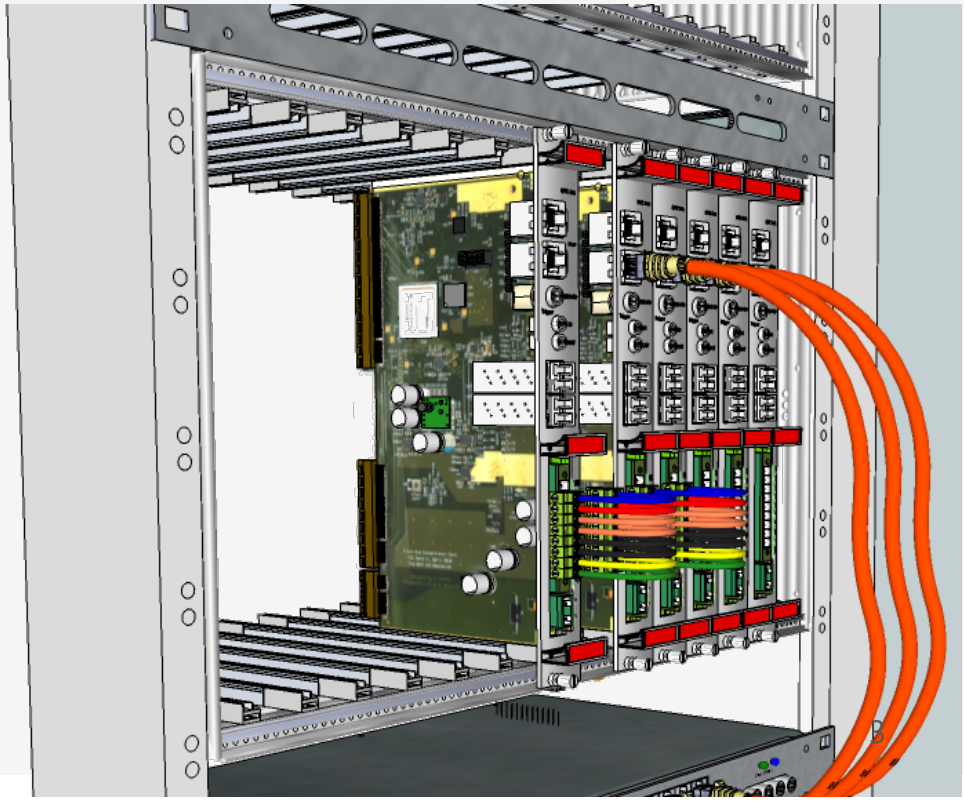
UPV group activities

- 25+ years designing FE, readout and DAQ for HEP, nuclear and medical physics
- Former RD51 members: co-designed SRS classic (FEC module) with CERN and IFIN-HH
- Currently designing electronics for the NEXT Collabration and Hyper-Kamiokande

CERN RD-51 SCALABLE READOUT SYSTEM (SRS) IN THE NEXT-DEMO DETECTOR

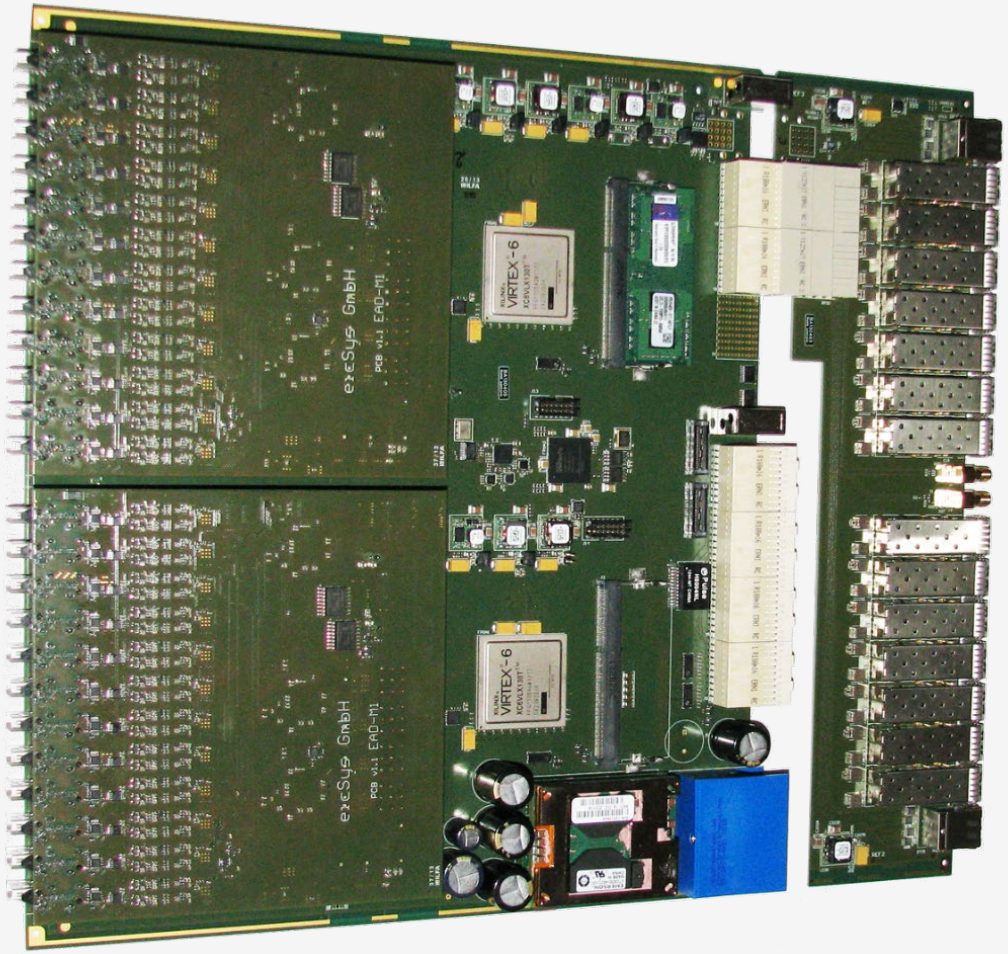
ASICs or discrete, analog, binary or digital readout front-ends

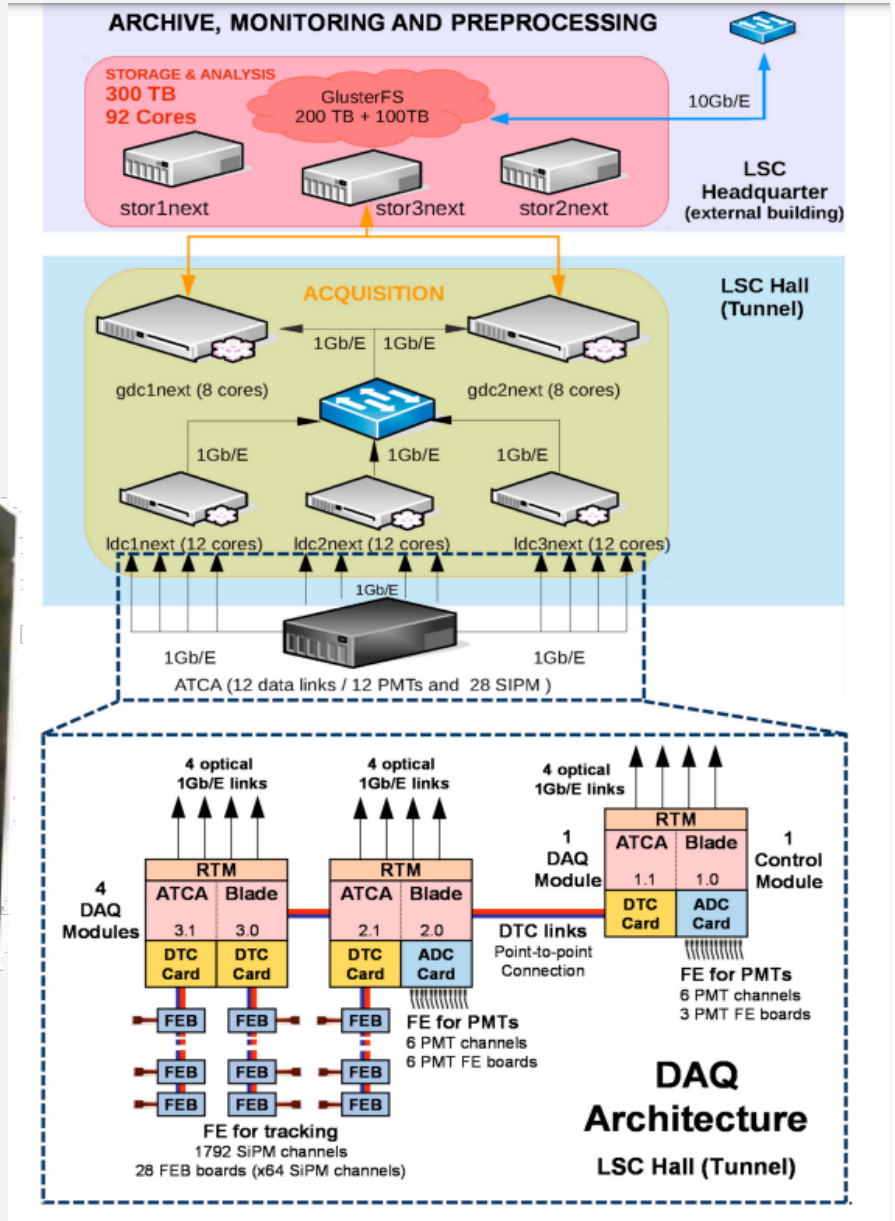




UPV group activities

- Adopted SRS ATCA for former NEXT-WHITE and current NEXT-100 detectors

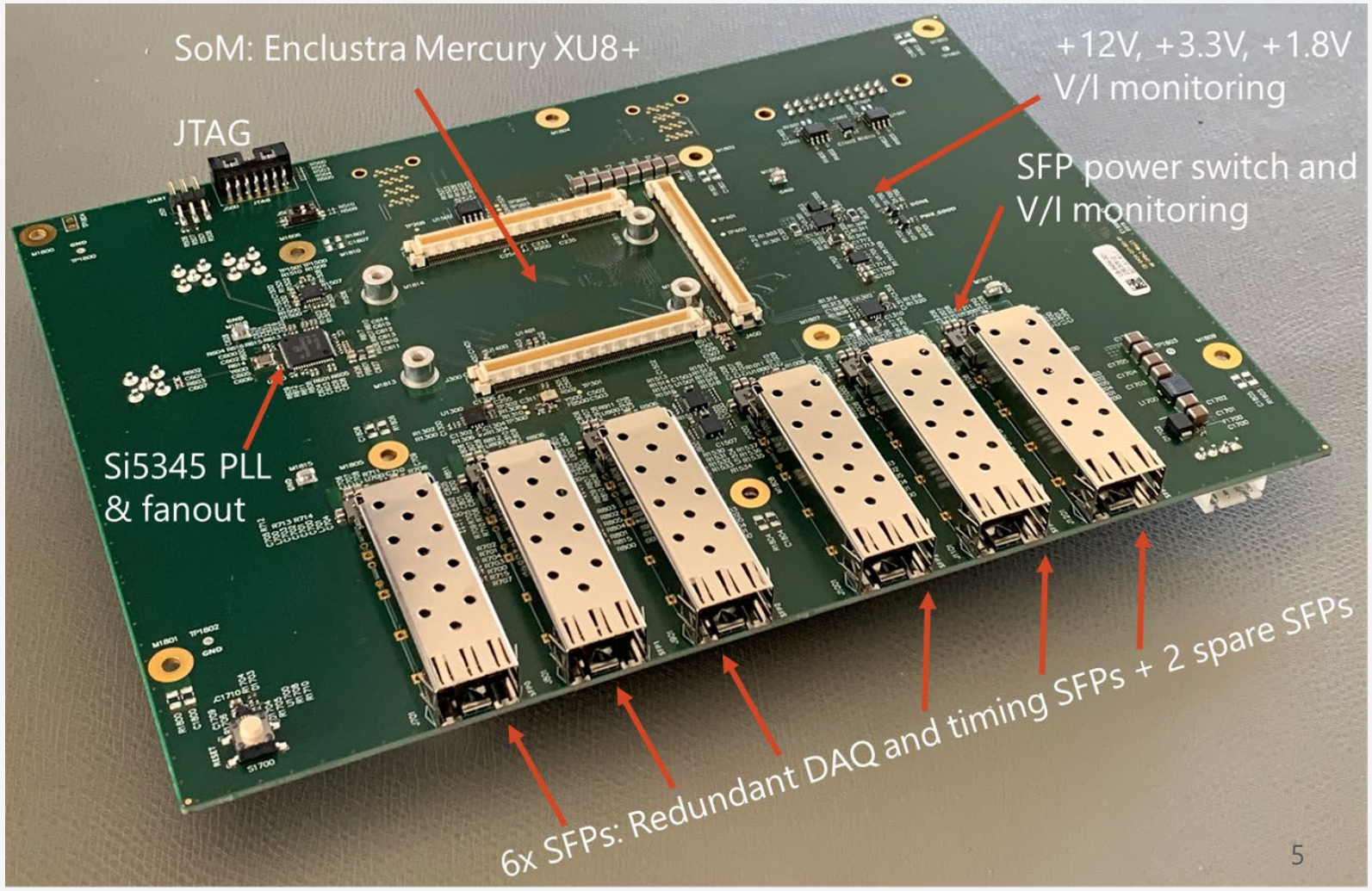




UPV group activities

- Hyper-Kamiokande: currently developing the DPB module in the FE box, inner detector.

- Based on SoM
- Zynq Ultascale+ SoC
- Petalinux
- DDR4 buffer (data flow)
- Several GbE I/O
- Redunancy&High reliability



UPV plans for the coming 1–2 years

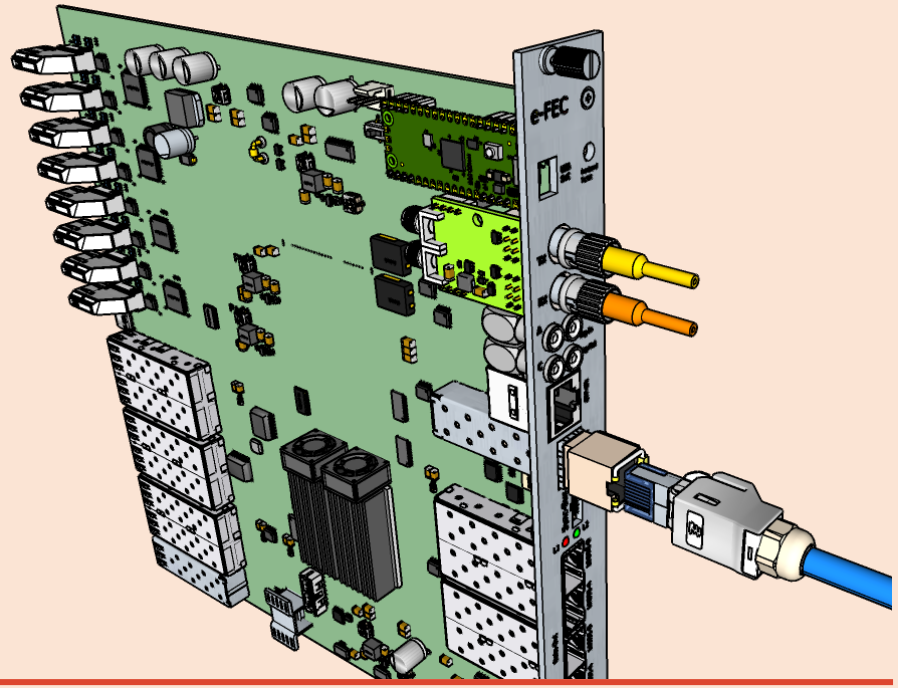
UPV group plans

- Currently looking for a new readout&DAQ electronics and SW for coming NEXT-HD/BOLD
  - O(10^5) channels, developing a readout ASIC
  - In-detector low-background readout and channel reduction
  - External DAQ
  - Need to find a suitable DAQ SW!!!

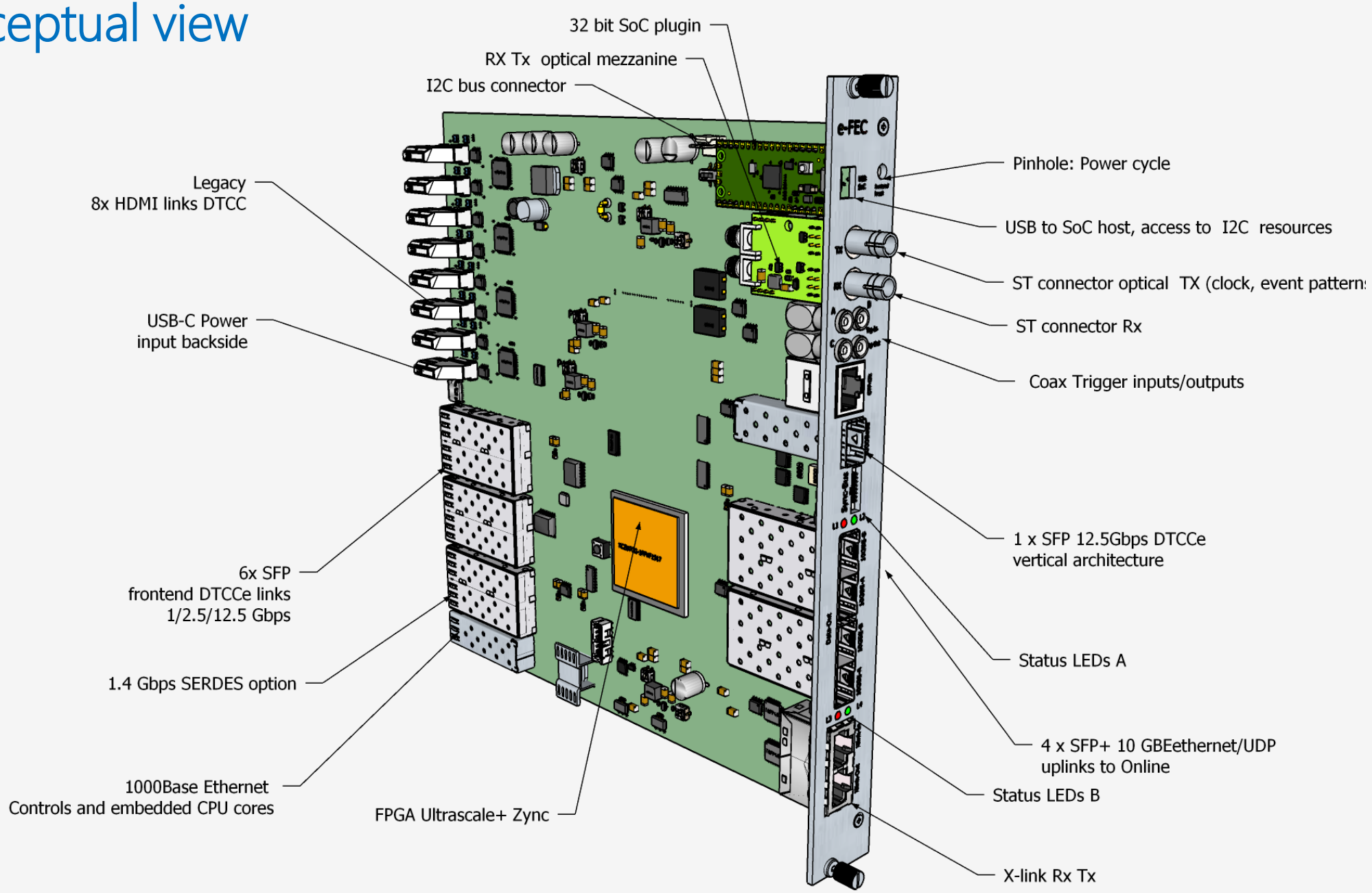
- Currently interested in DRD1 for co-developing eFEC module, using our expertise in SoM

- Continue Hyper-Kamiokande support (development, production, installation)

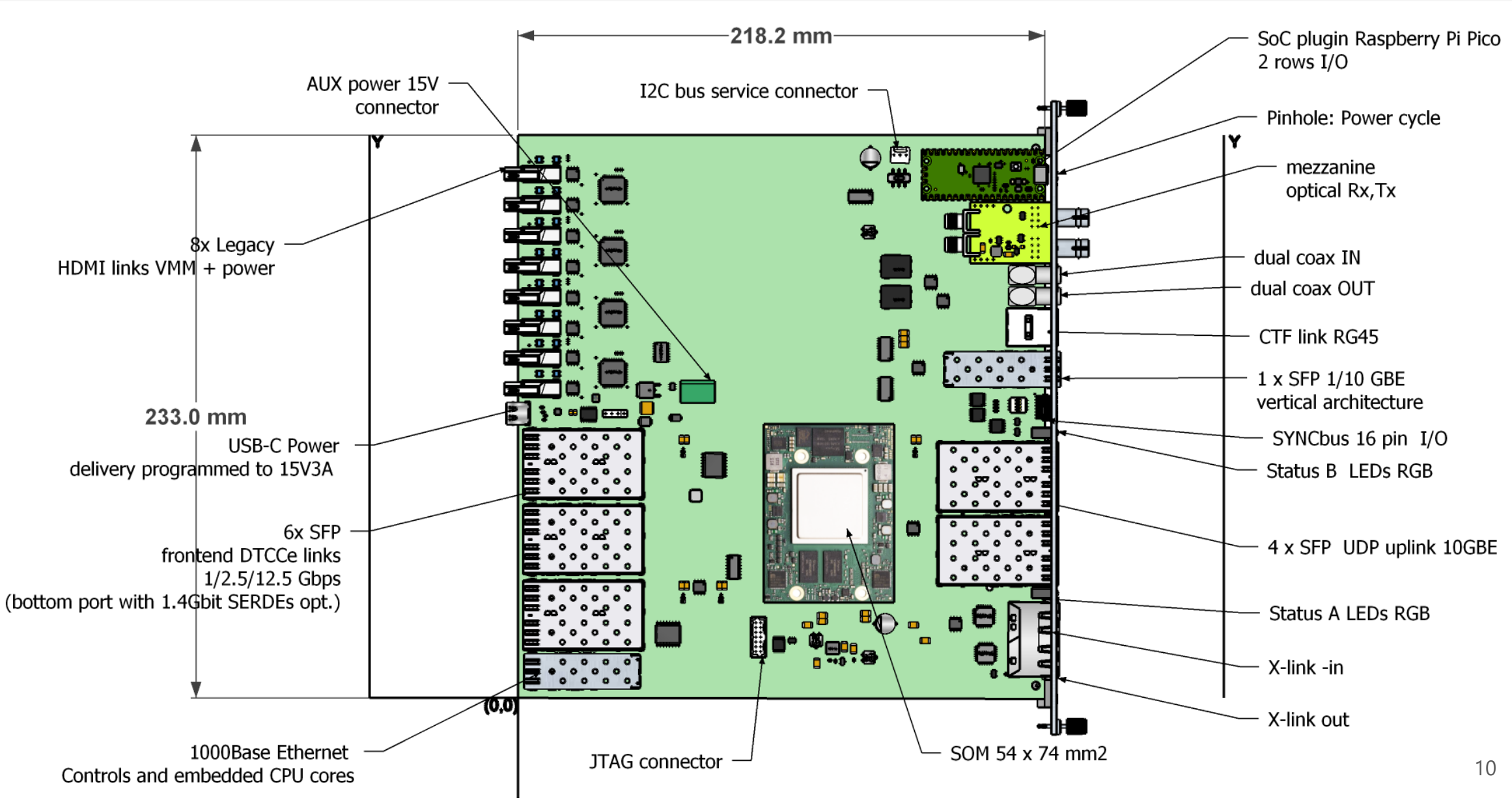
eFEC prototyping



eFEC conceptual view

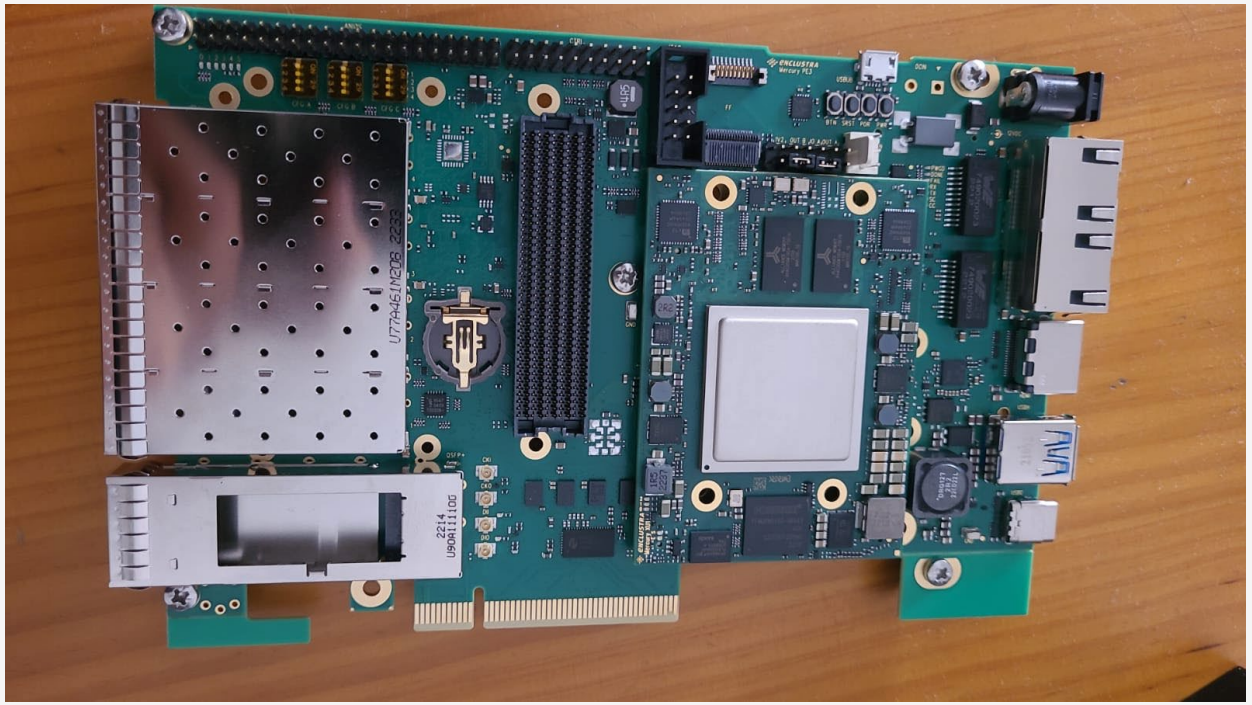


eFEC conceptual view

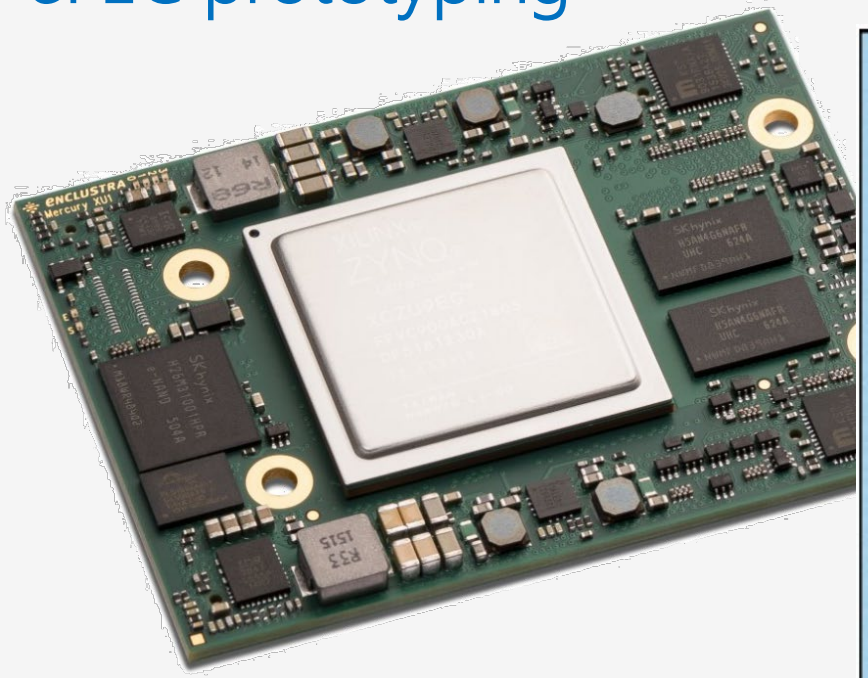


eFEC prototyping

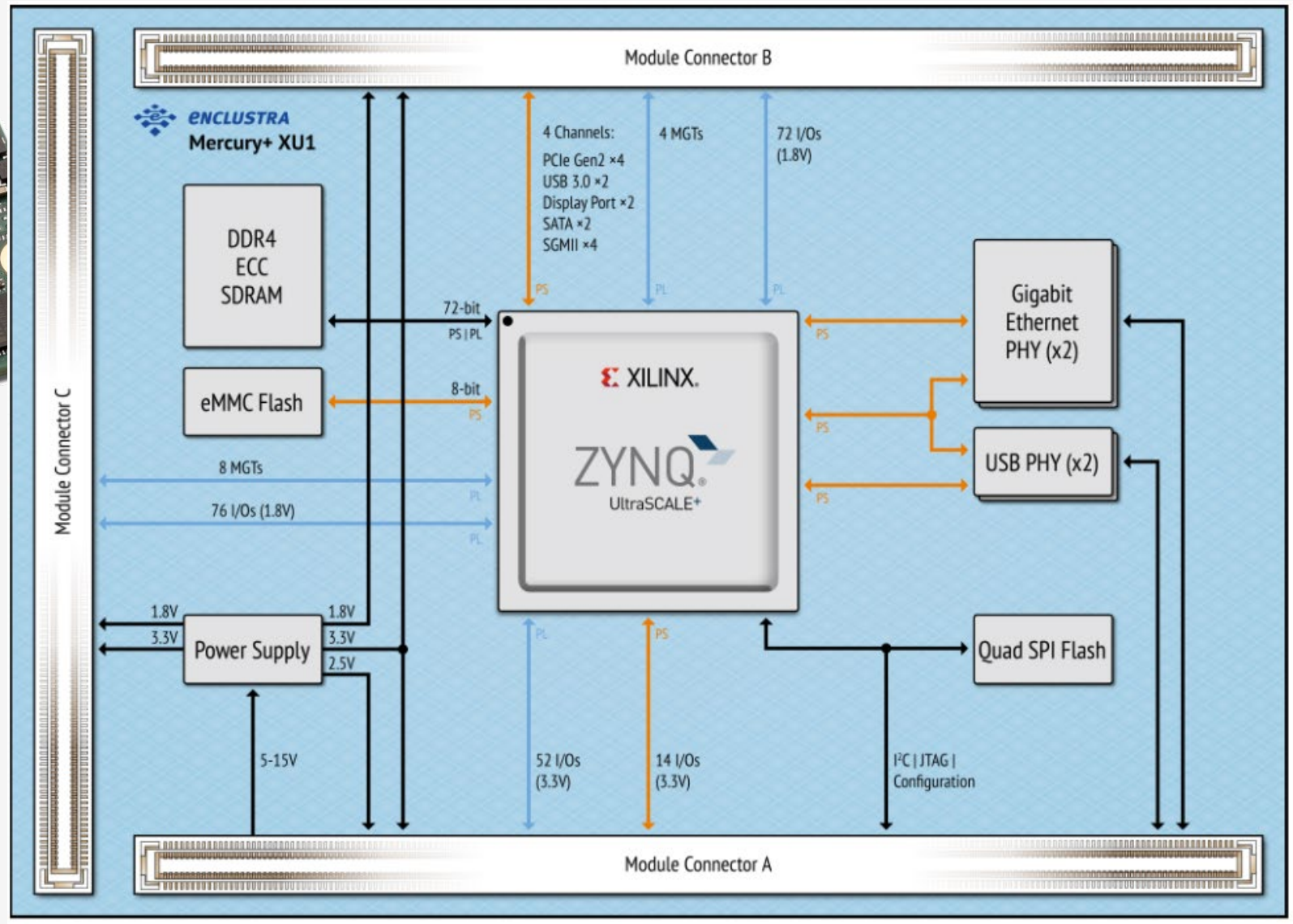
- Already started prototyping eFEC: purchased 2x PE3 board + SoM with -9EG SoC
  - SOM: Enclustra ME-XU1-9EG-1E-D11E-G1 (10% reduction in the price list for SRSe project)
  - Base board: Enclustra Mercury+ PE3 board
  - 1 kit in Valencia + 1 kit available for CERN



eFEC prototyping



Enclustra ME-XU1-9EG-1E-D11E-G1-R4.2



12x MGTs PL side

2x GbE PHY PS side

4x additional PS MGTs (SGMII)

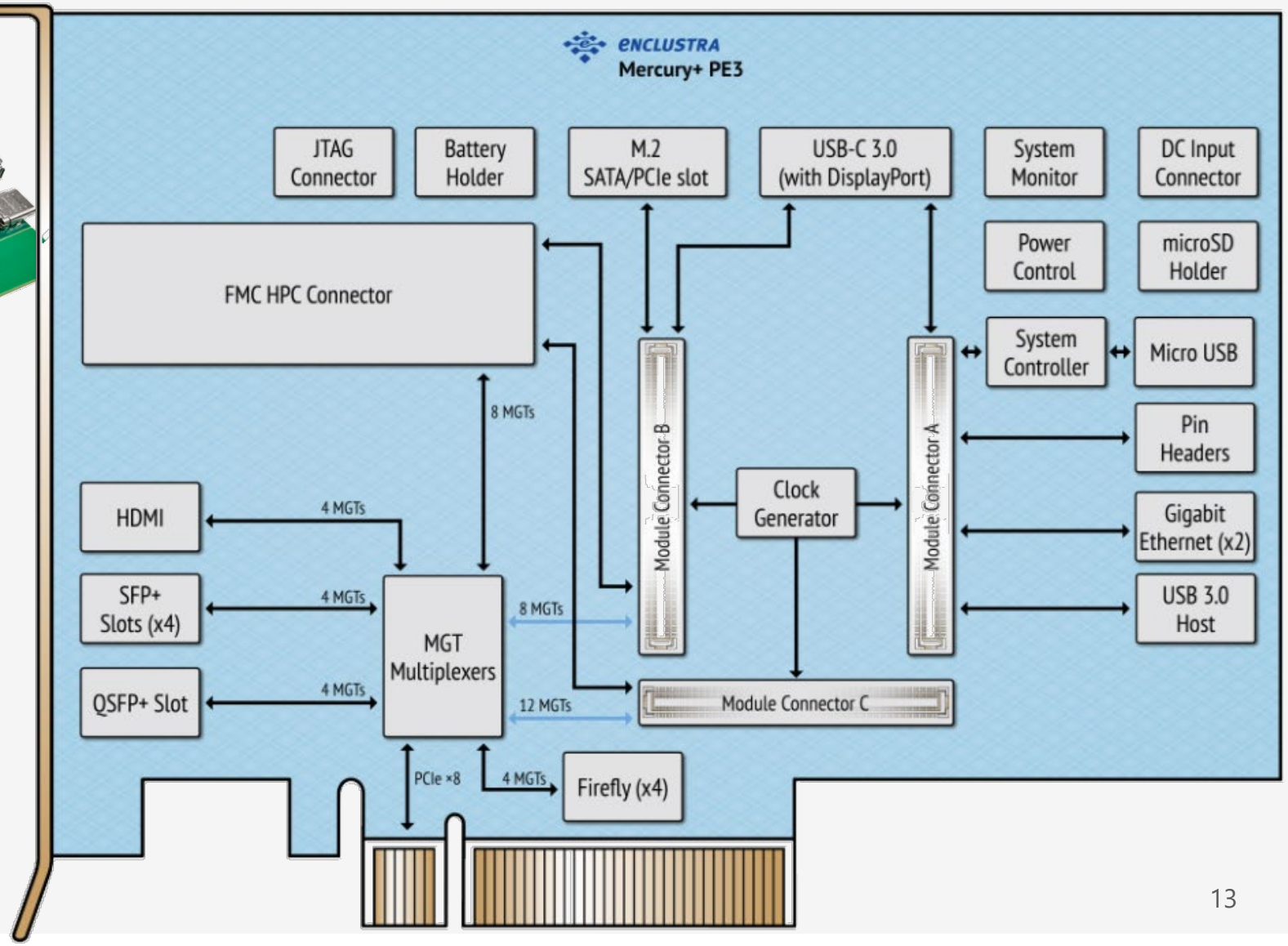
2x USB 3.0

2GB DDR4 (up to 8 GB)

eMMC + QSPI boot memory

eFEC prototyping

Enclustra Mercury+ PE3



eFEC prototyping – this month's activities

- Already preparing a first boot and network exercise
- Need to find ASAP throughput limitations in both PS and PL
- Speedgrade -1 SoC reaches ca. 6 Gb/s

Resources in Valencia

- 2x development kits
- 1-year engineer contract (could be extended)
- 1x MSc.Eng. thesis student
- Expertise in development with SoM (HW&SW)

eFEC prototyping – Who does what?

UPV Valencia Group

- Prototyping on Enclustra baseboard: 1x Engineer
- Contribution to co-develop schematics: 1x Student
- Contribution to board layout: need additional help/funding from DRD1 groups

Other groups are required to

- Co-develop on the Enclustra baseboard
- Contribute to board layout effort/funding
- SW&FW development for final application
- Those interested, please reach H. Müller

Thanks for your attention!