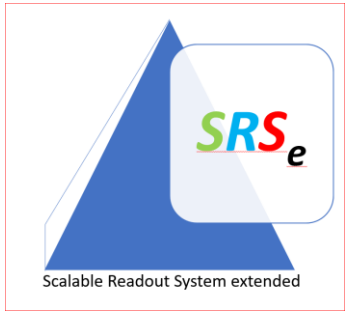
SRSe



Update on SRSe

eFEC and dFEC are system modules of the new SRSe concept

Hans.Muller@cern.ch

SRSe Readout Systems

-common scalable readout for gas detectors, self triggered or ext. triggered

-new and old ASIC carriers (hybrids) with standard HRS connectors

-upgrade from very small to very large systems

-new, portable dFEC boxes for up 2k ch each

-frontend power option via PBX power fanout (USB-C)

-new, small (backend-less) systems: Ethernet direct to the frontend

-new, eFEC backend for high BW aggregation & embedded triggers

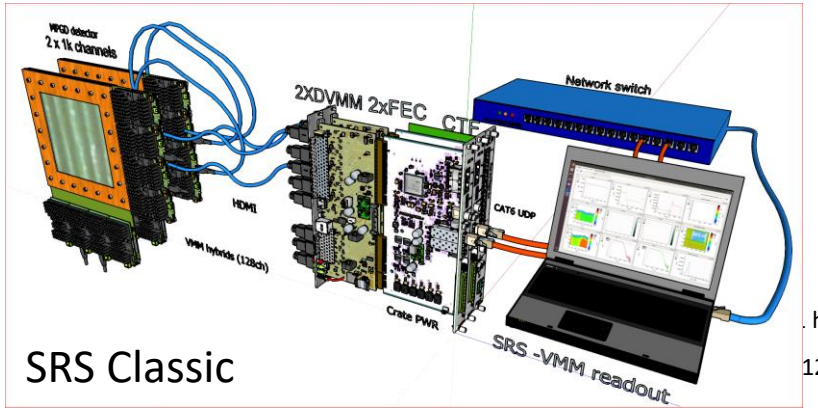
-new, ertical & horizontal backend architectures

-new, packet-based backend link over fibers: DTCCe (Data, Trigger, Clock, Controls)

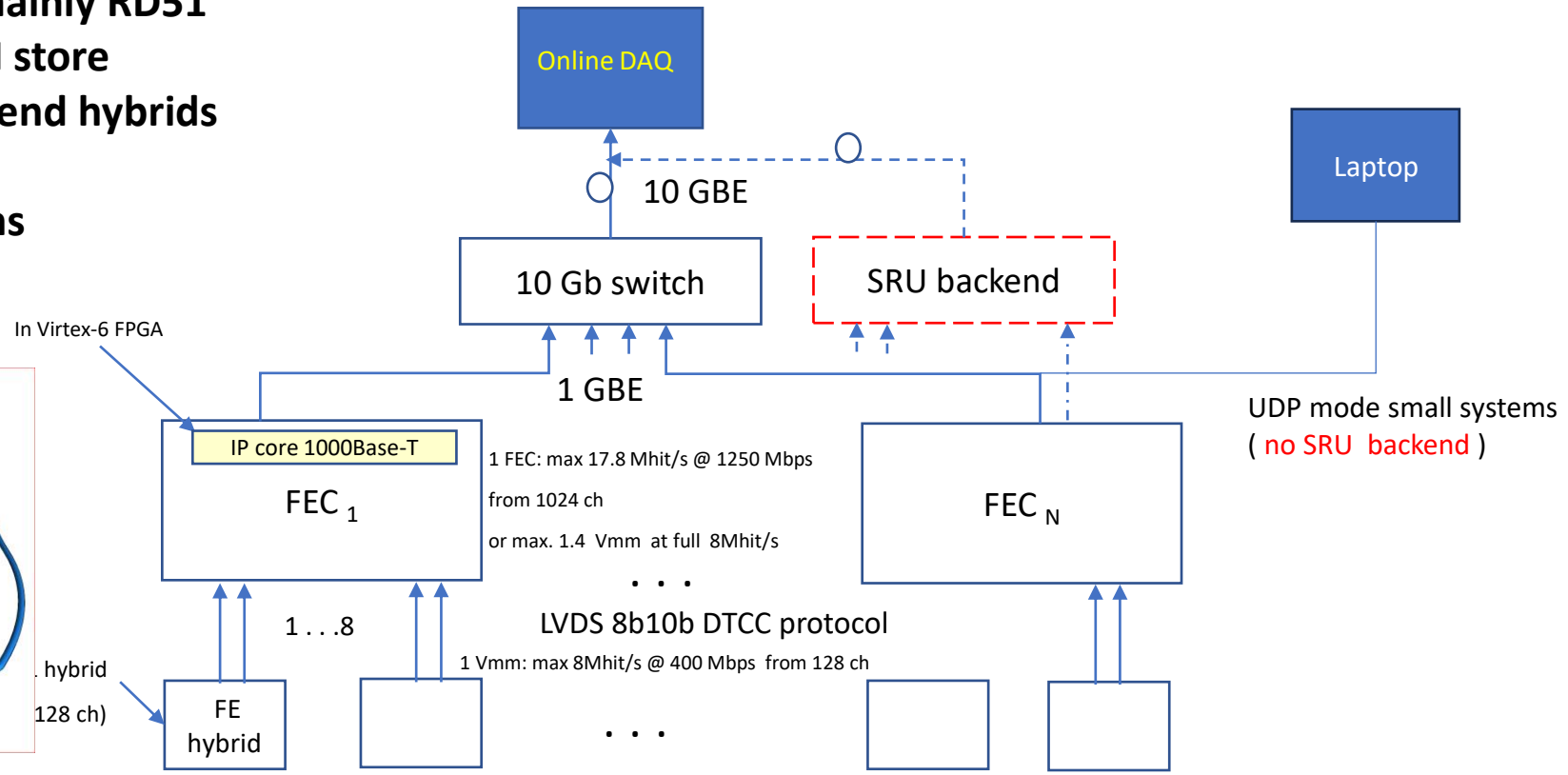
Hans.Muller@cern.ch

Old SRS Scalable RO architecture

- **hundreds of systems and users , mainly RD51**
- **SRS material distribution via CERN store**
- **thousands of APV and VMM frontend hybrids**
- **Mini- and Eurocrates**
- **many testbeam-proven RO systems**



SRS Classic



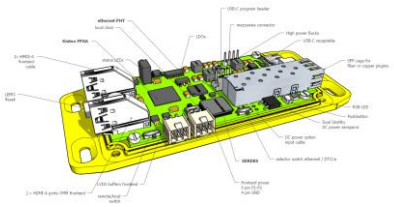
Hans.Muller@cern.ch

What is new for SRSe

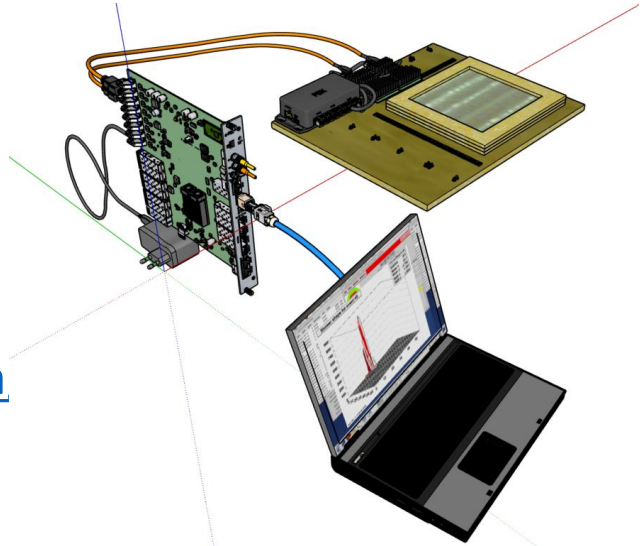
- crateless dFECs: up 2kch/box with direct Etherent RO
- scaling to both smaller and larger systems
- distributed detector readout
- optical clock-links
- FE power via PBX (USB-C)
- 10G readout links via SFP

\+ -------- workplan ----------

- eFEC backend with FPGA-SOM
- DTCCe backend and trigger link
- SiPM FE adapter VMM w. high dyn ran
- New ASIC carriers tbd
- New Auxiliaries (PBX, QNI, CTFe, …)



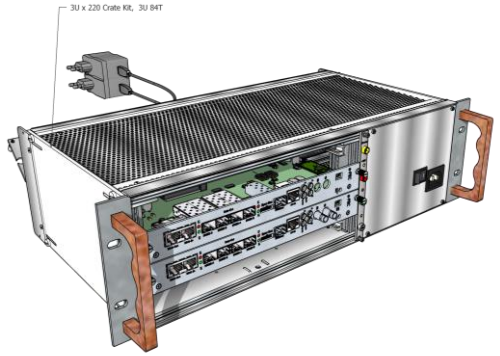
New, stand-alone dFEC
for ethernet RO of 2 hybrids



eFEC legacy mode: table-top
small detector via HDMI

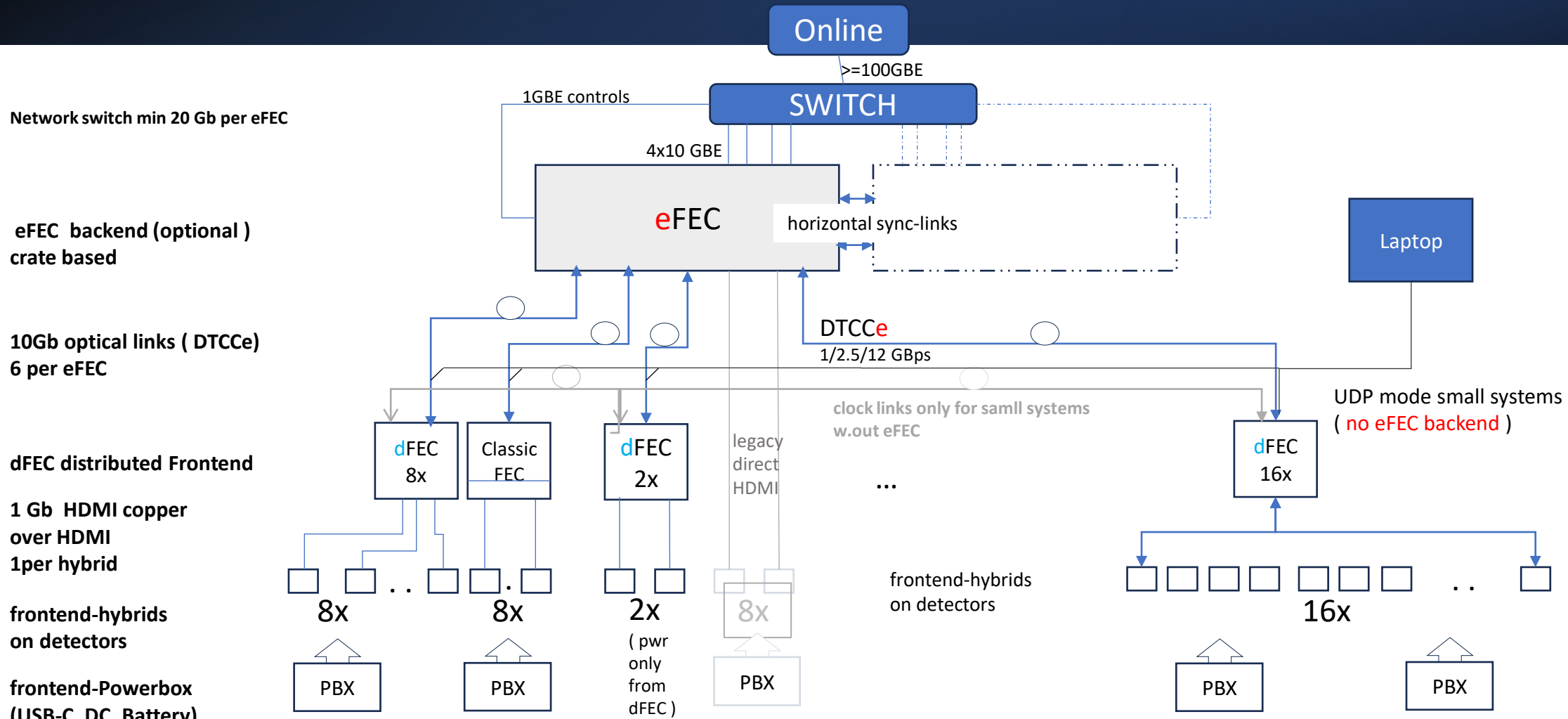
What is maintained

- FE hybrid links : HDMI A-D
- VMM3a hybrids
- FEC V6 and DVMM cards
- Crates to include eFECs
- DAQ and slow controls



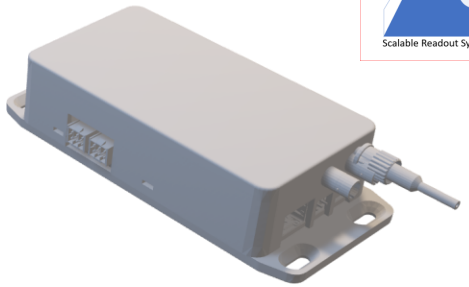
2x eFECs in simplified
SRS Minicrate: USB-C powered

SRSe Scalable RO architecture



crate-less dFECs

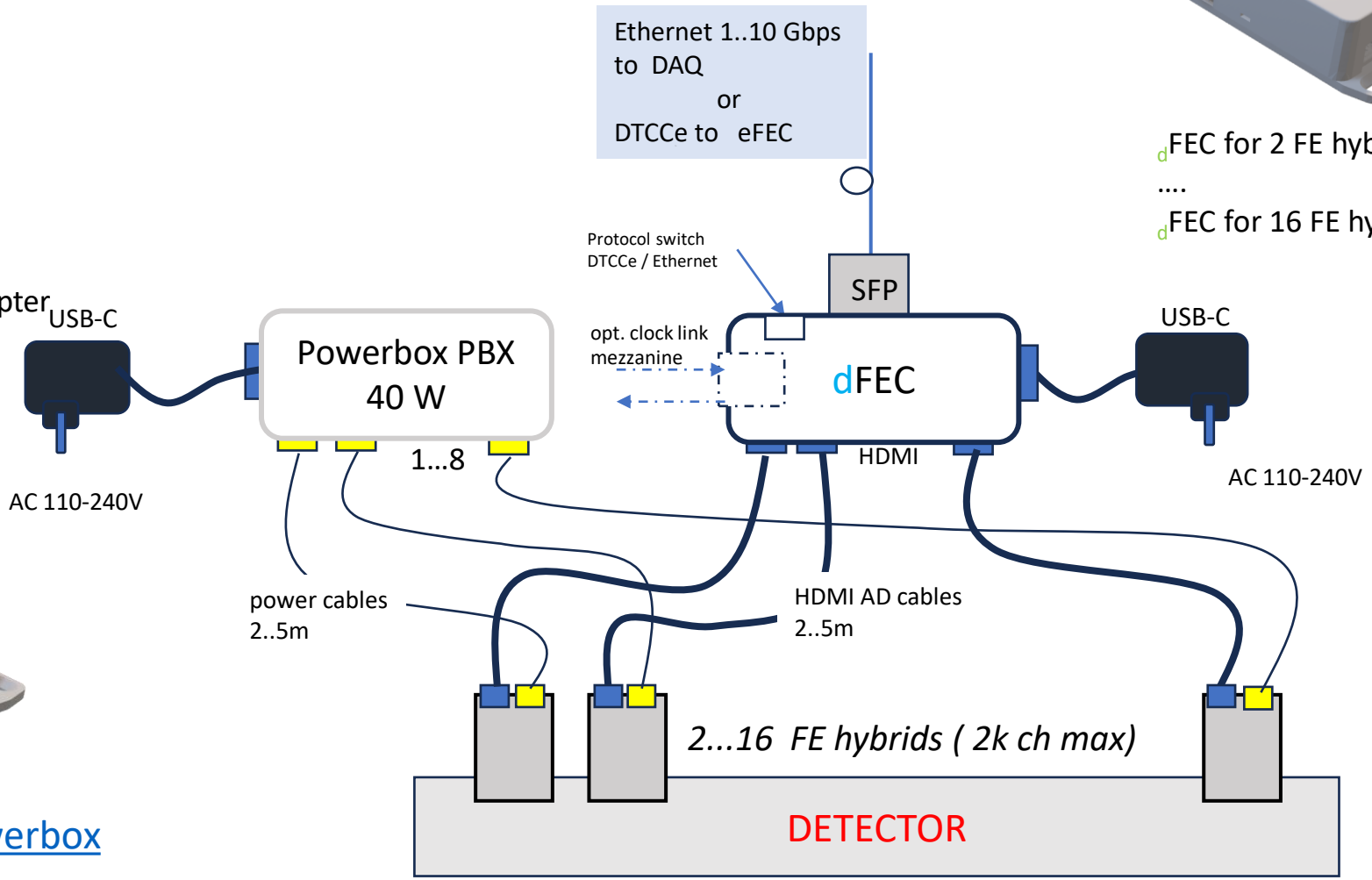
DAQ Ethernet to FE or DTCCe to backend

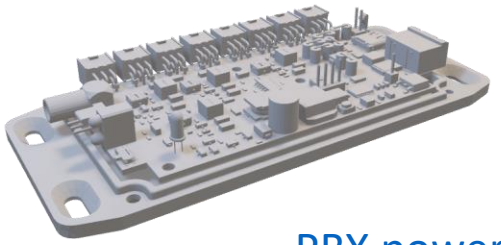


dFEC for 2 FE hybrids: **uROC**
....
dFEC for 16 FE hybrids: **maxiROC**

dFEC's

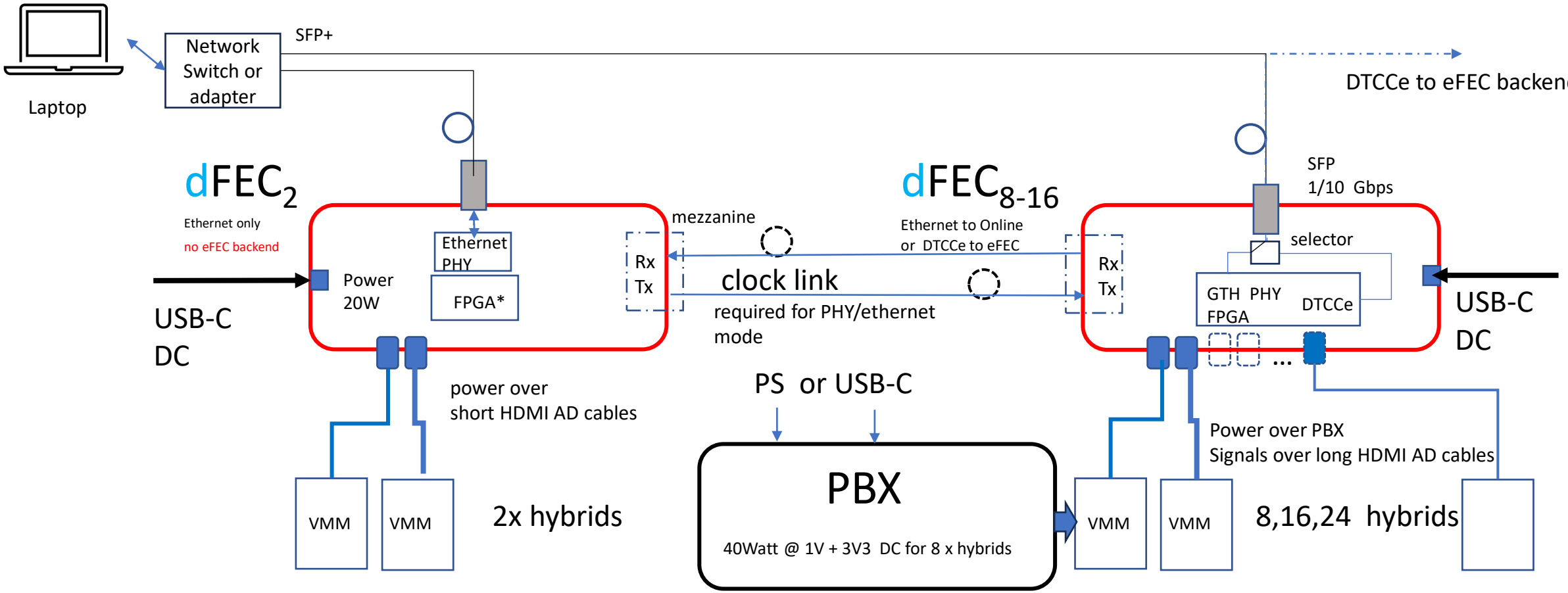
- portable / handheld boxes
- state-of-art FPGA logic
- 2 ..16 HDMI powered frontend ports
- max. 2k channels/ dFEC
- USB-C powered via PBX
- RO links copper or fiber with SFP adapter
- Ethernet to direct Online systems
- DTCCe to eFEC backend
- ST optical clock link (plugin option)





PBX powerbox

Ethernet readout mode: small or low-rate without eFEC backend



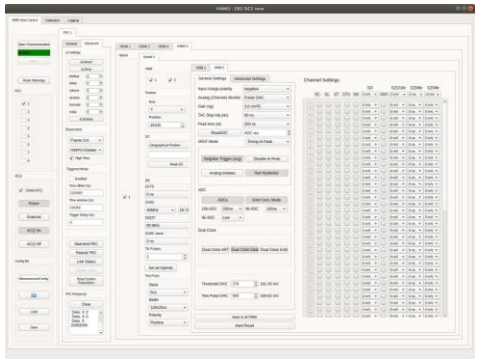
* low-cost FPGA, I/O w. Io 2x16 bit @ 80 MHz , 800Mbps

** high-end FPGA with 12.5Gbit GTH transceivers

Hans.Muller@cern.ch

Small systems: ethernet to frontend, no backend

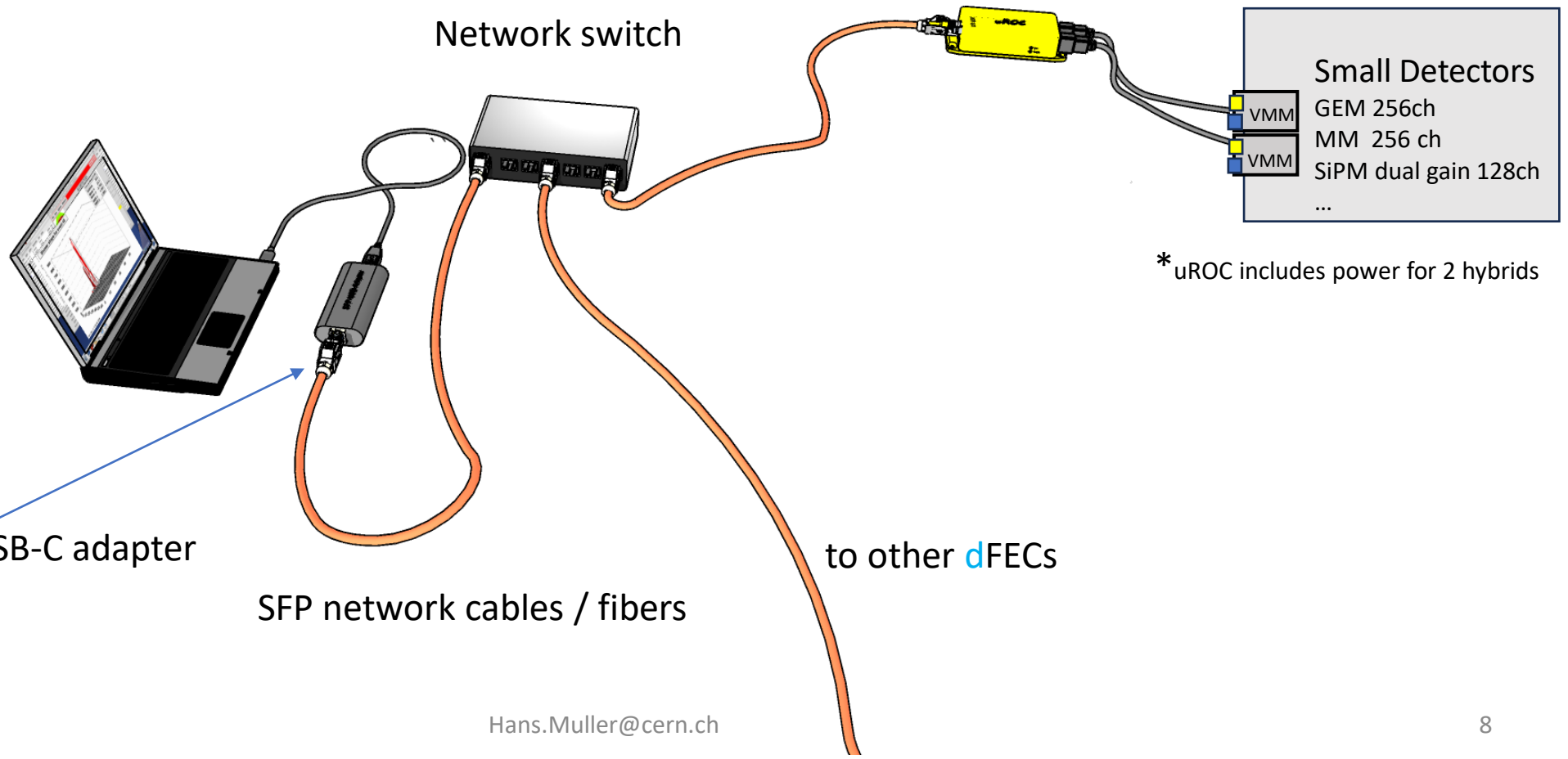
ESS DAQ and Controls on Laptop



see talk A.Rusu

$_{d}FEC_2$ => uROC*

Network switch

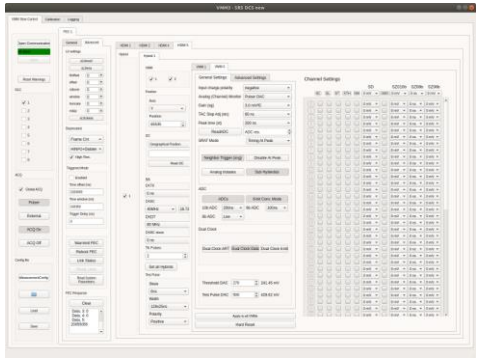


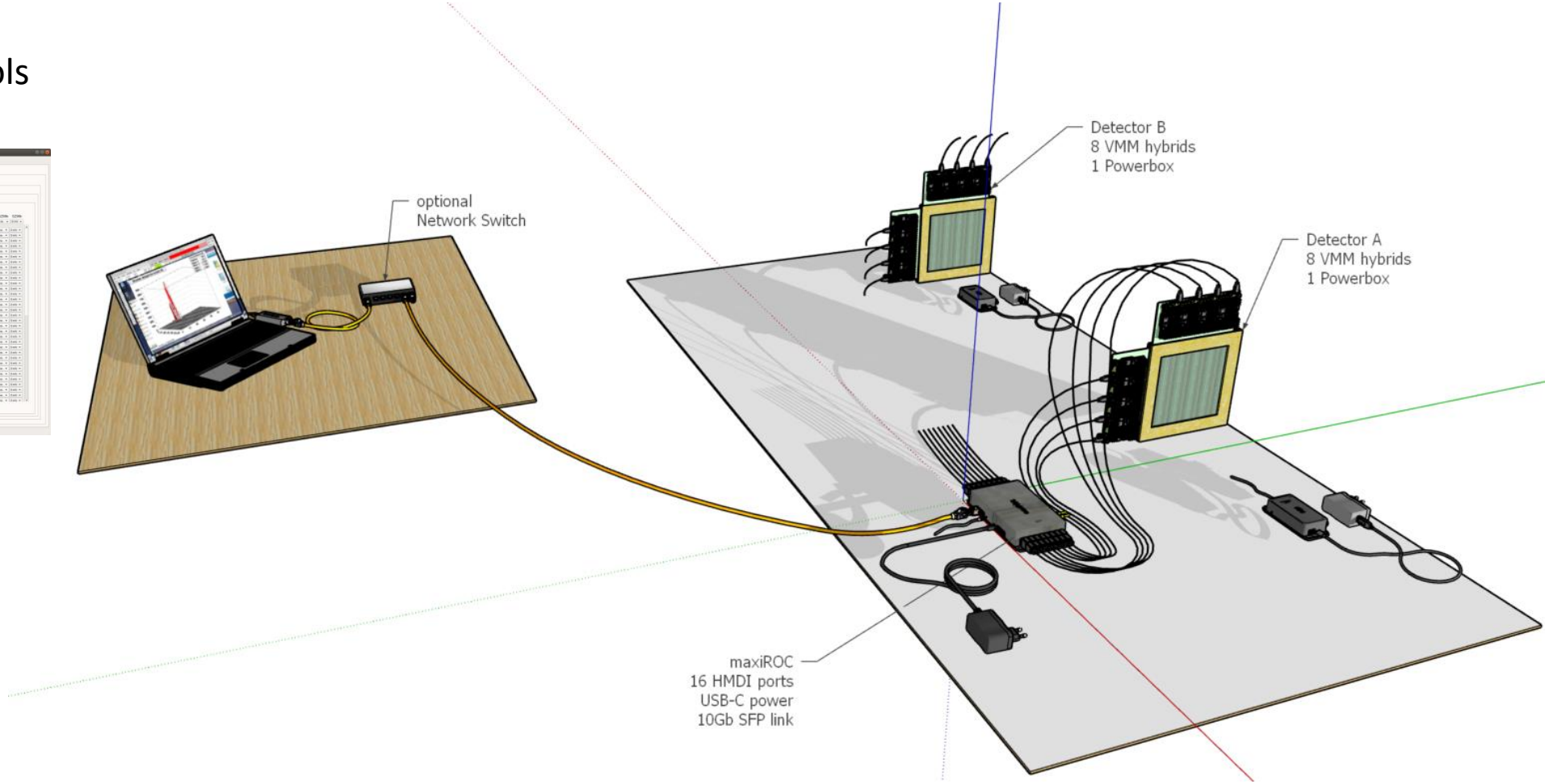
*uROC includes power for 2 hybrids

Medium-sized & low-rate up 2k: ethernet to frontend no backend

Readout & DAQ of 2k detector channels via $_{d}FEC_{16}$ => MaxiROC

ESS DAQ and Controls on Laptop





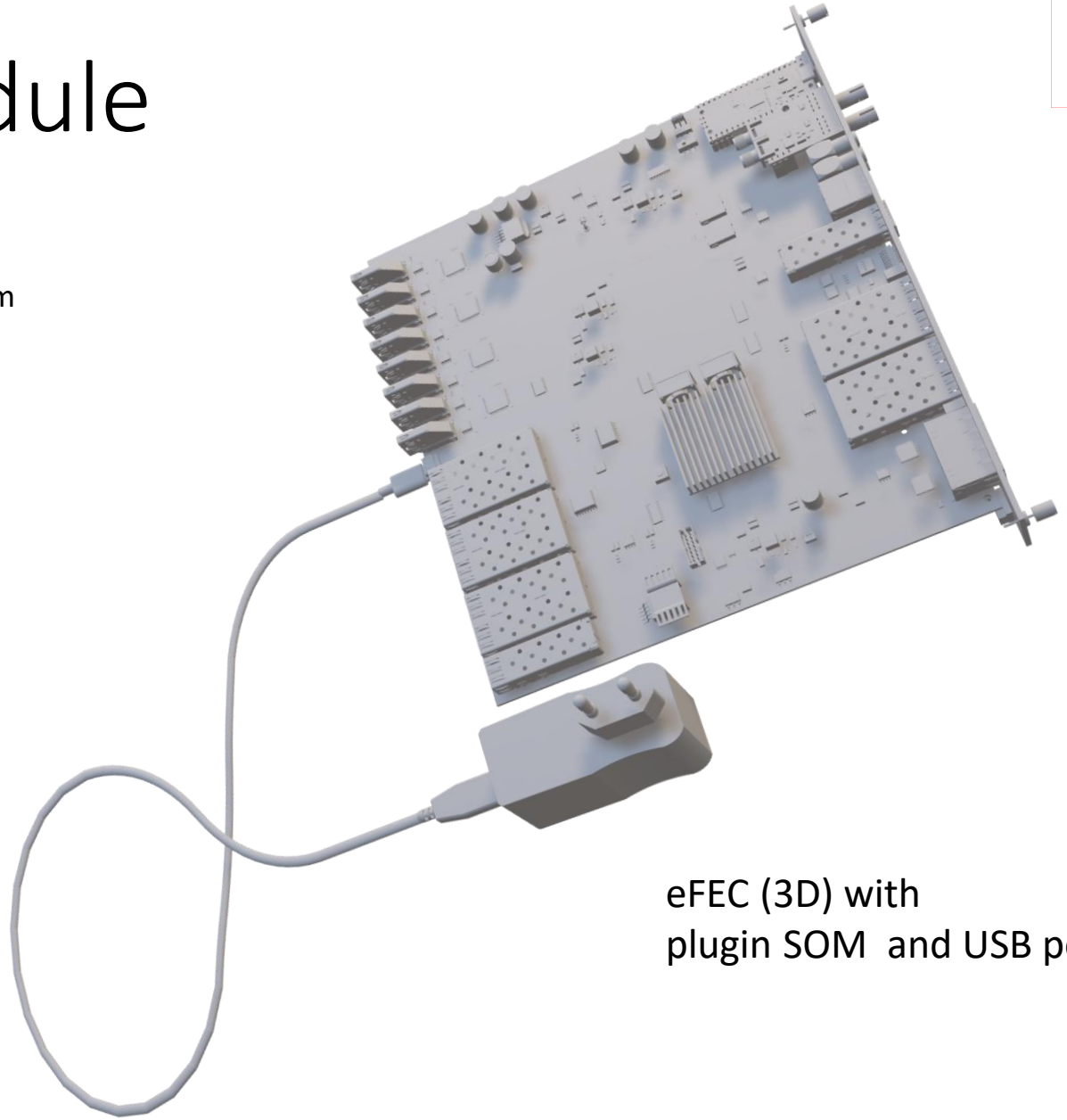
eFEC backend module

General
- same physical outlines as FEC + DVMM together 6U x 220mm
- housed and powered (USB-C) in classic SRS crates
- Ultrascale + Zync 9 FPGA **on SOM plugin** with DDR4

Connectors rear
- 8 x legacy, powered HDMI link ports to VMM frontend
- 6x frontend DTCCe link port SFP+ 1 /2.5/ 12.5 Gbps
- 1x 100Base Ethernet for Controls link
- USB-C power connector , alternative 2 pin DC power supply

Connectors front
- 4 x uplinks SFP+ to Online 10 GBE/UDP
- 1 x uplink SFP+ vertical architecture summary link
- 2 coax Trigger Inputs and 2 coax trigger outputs (NIM)
- 1 CTF+ clock and trigger links (RG45)
- 1 x horizontal Xlink Rx Tx horizontal serial link (RG45)
- 1 x horixontal SYNCbus mixed analogue / digital

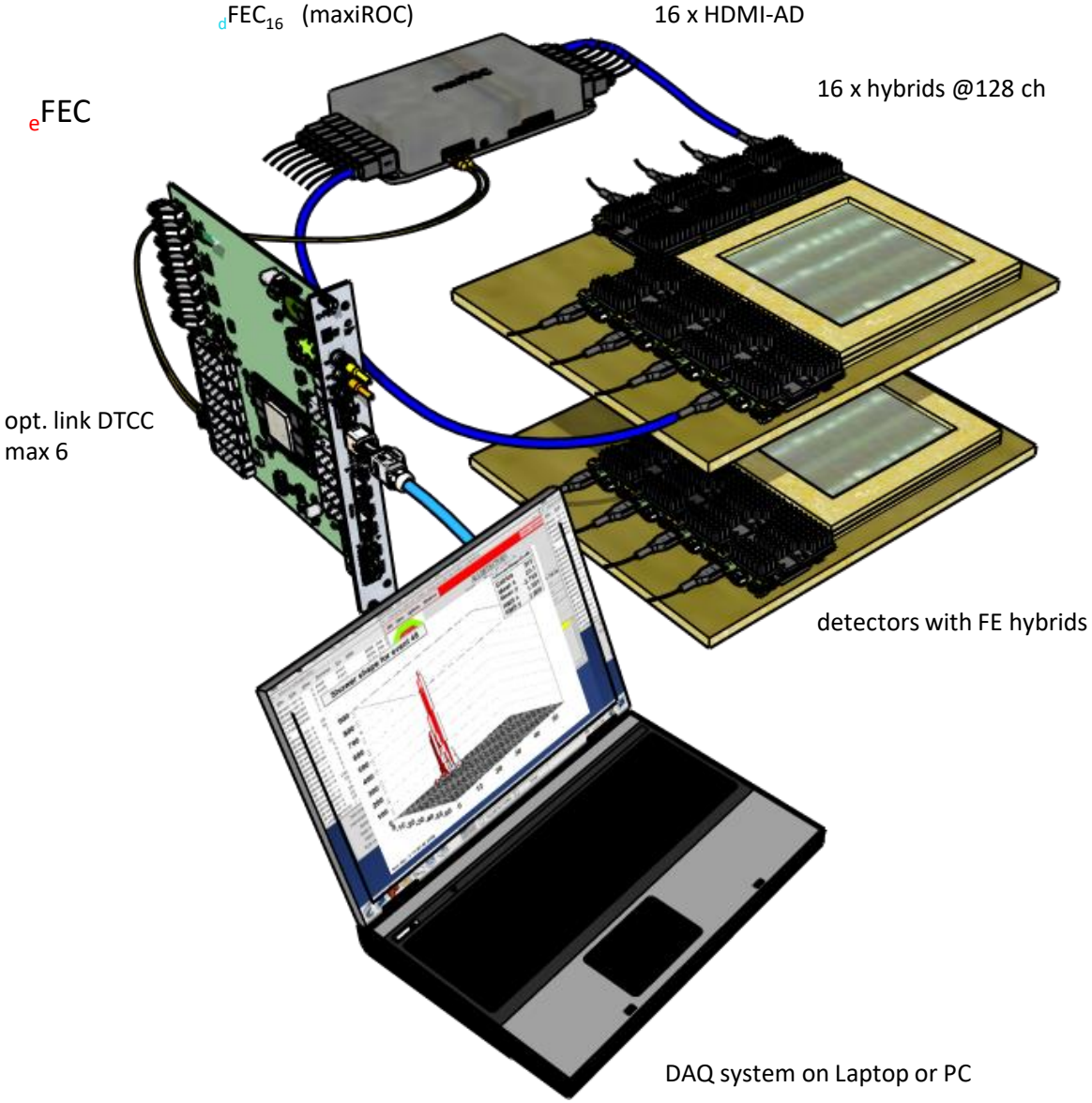
Plugin options
- 1 optical ST RX / TX link mezzanine
- 32 bit SoC with USB debug port (Raspberry Pi pico)



eFEC (3D) with
plugin SOM and USB power

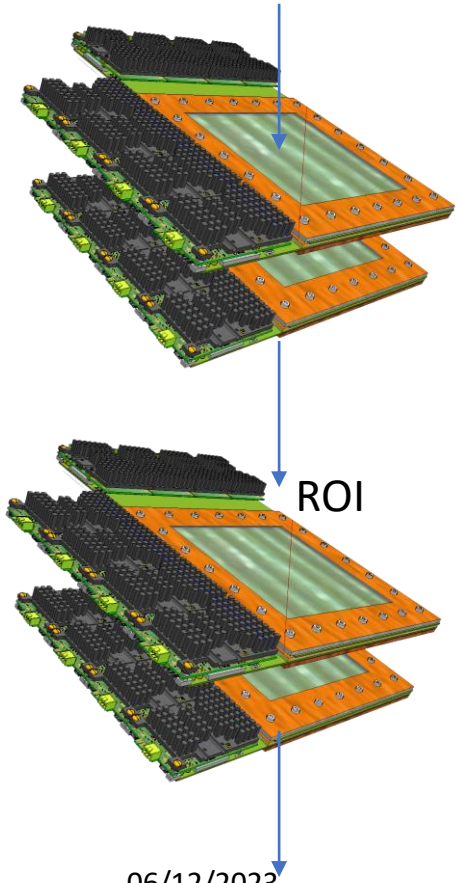
Hans.Muller@cern.ch

high-rate & triggered systems with eFEC backend



Simplified view: single maxiROC 2kch
2x PBX not shown

New: online triggers in backend FPGA

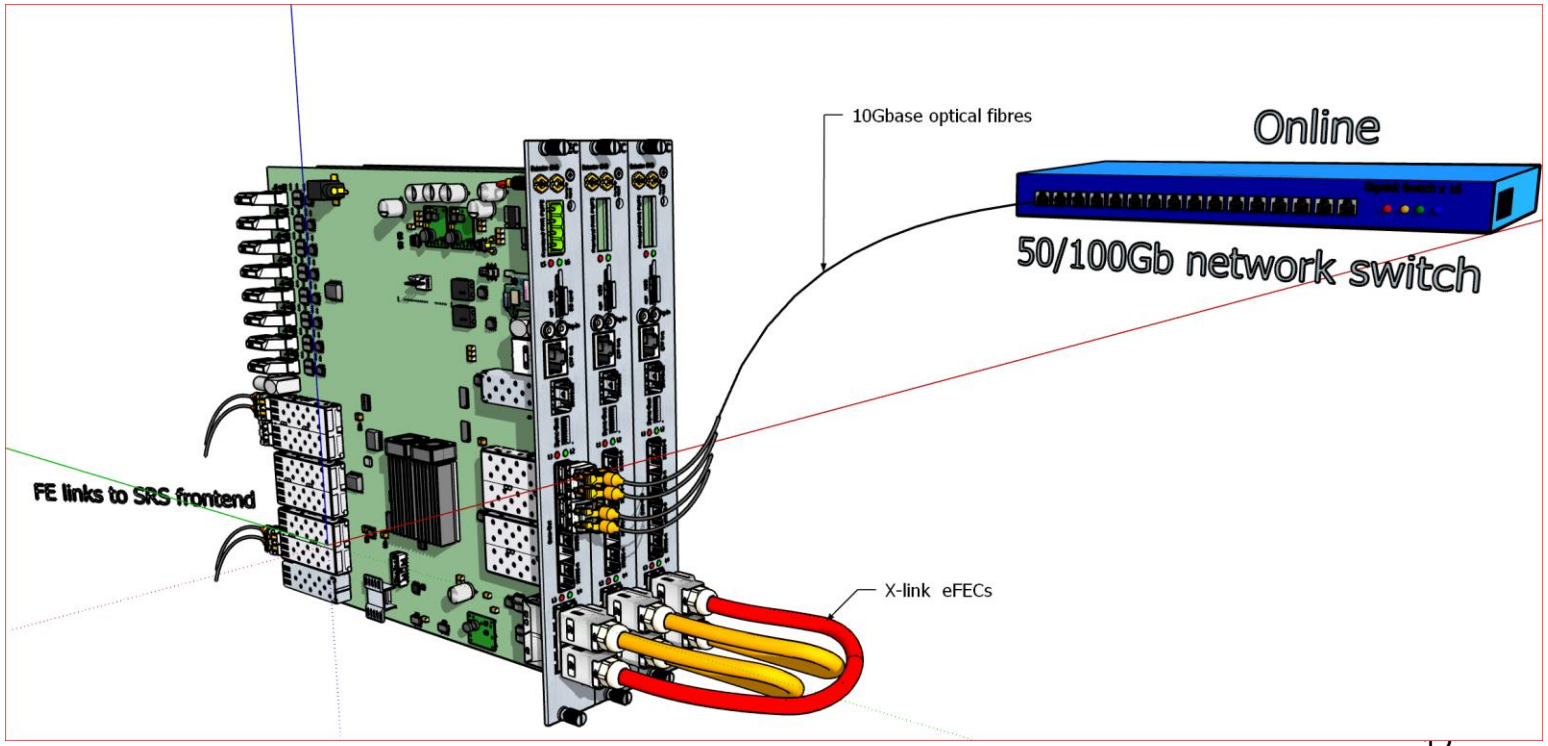


High-rate regional HW triggers

DTCCe protocols geographically map up to 912 FE ASICs to BRAM address blocks in FPGA: Fast ROI trigger algorithms

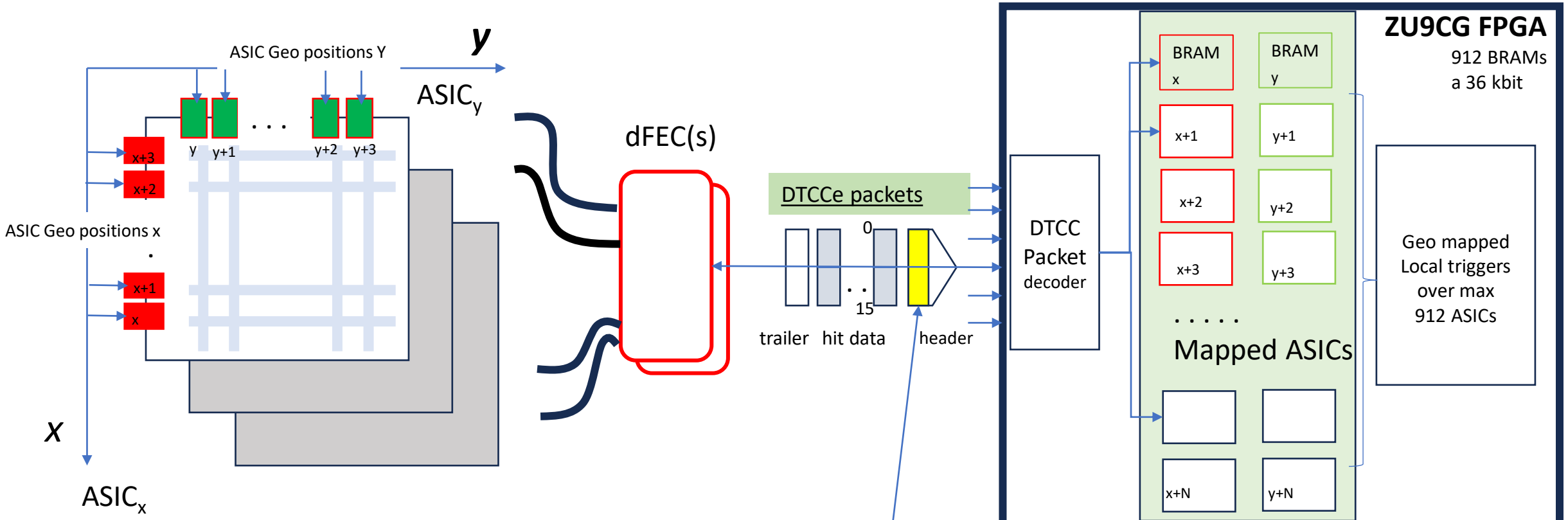
Low-rate, detector-scale SW triggers

SW algorithms over full detector data in DDR4 RAM also across eFEC boundaries via Xlink between eFECs



Fast triggers: ASIC geo mapping to BRAMs

Detector(s) => dFEC(s)=> DTCCe link(s)=> eFEC FPGA=> HW trigger



ASIC Geo position read out via HRS connector coding on detector	dFEC injects Geo code in DTCCe header	Hit header contains ASIC GEO index	Store hit data to Geo-assigned BRAM	Local geo trigger max 912 ASICs

Hans.Muller@cern.ch

New DTCCe protocol*

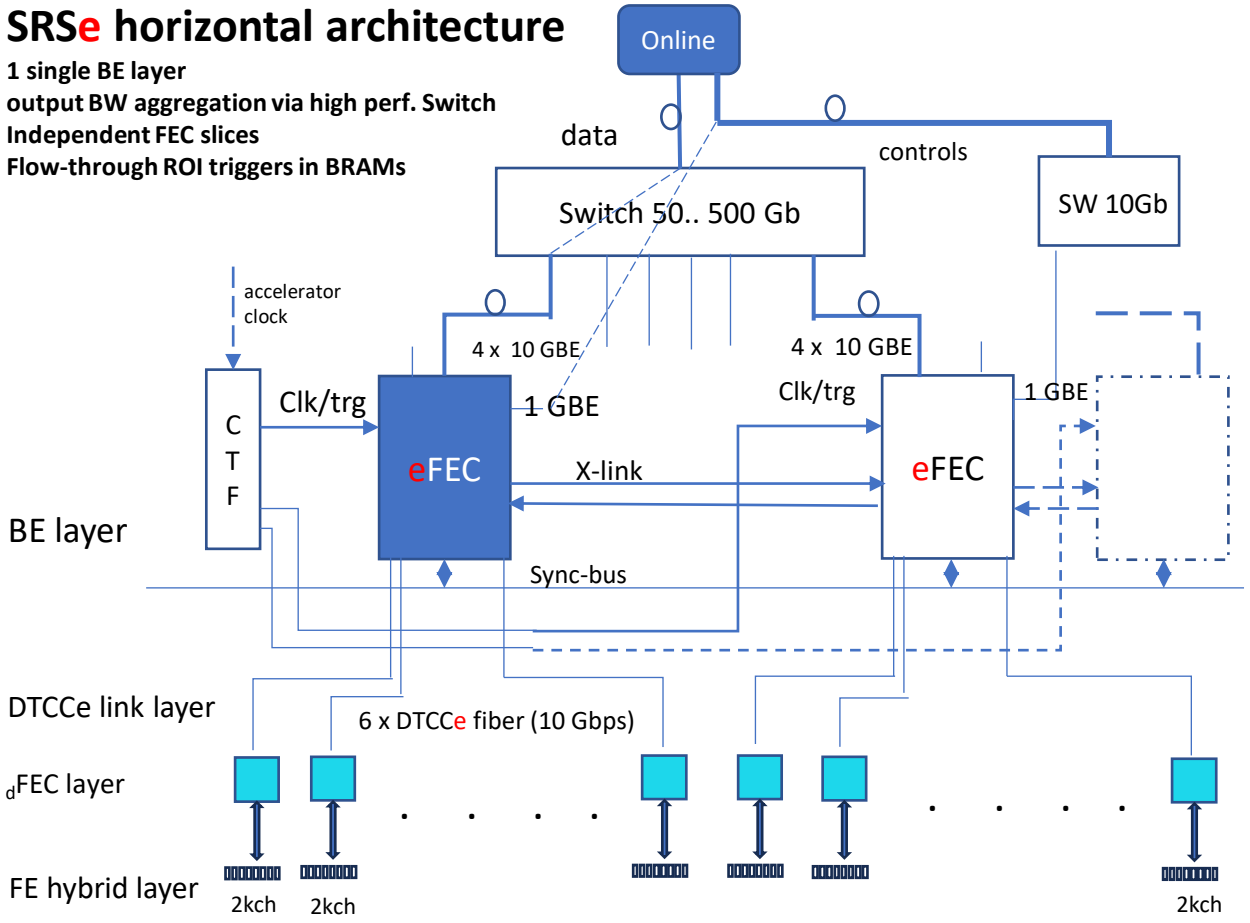
- packet-based protocol **eFEC <-> dFEC** over optical links
- native serial GTH links w. built-in 16/1 SERDES at 12.5 Gbps
- SFP+ up 12.5 Gbps and up 20km optical
- self-triggered or triggered hits to eFEC
- Geo. index of ASICs included in packet headers
- Optional safe-mode with roundtrip packet Ack and Retry
- Common eFEC clock to all dFECs
- Bi-dir command messages include error codes
- Remote I2C write/read to I2C resources in FE

*DTCCe draft spec on request for developers

Lage and high-rate systems: backend

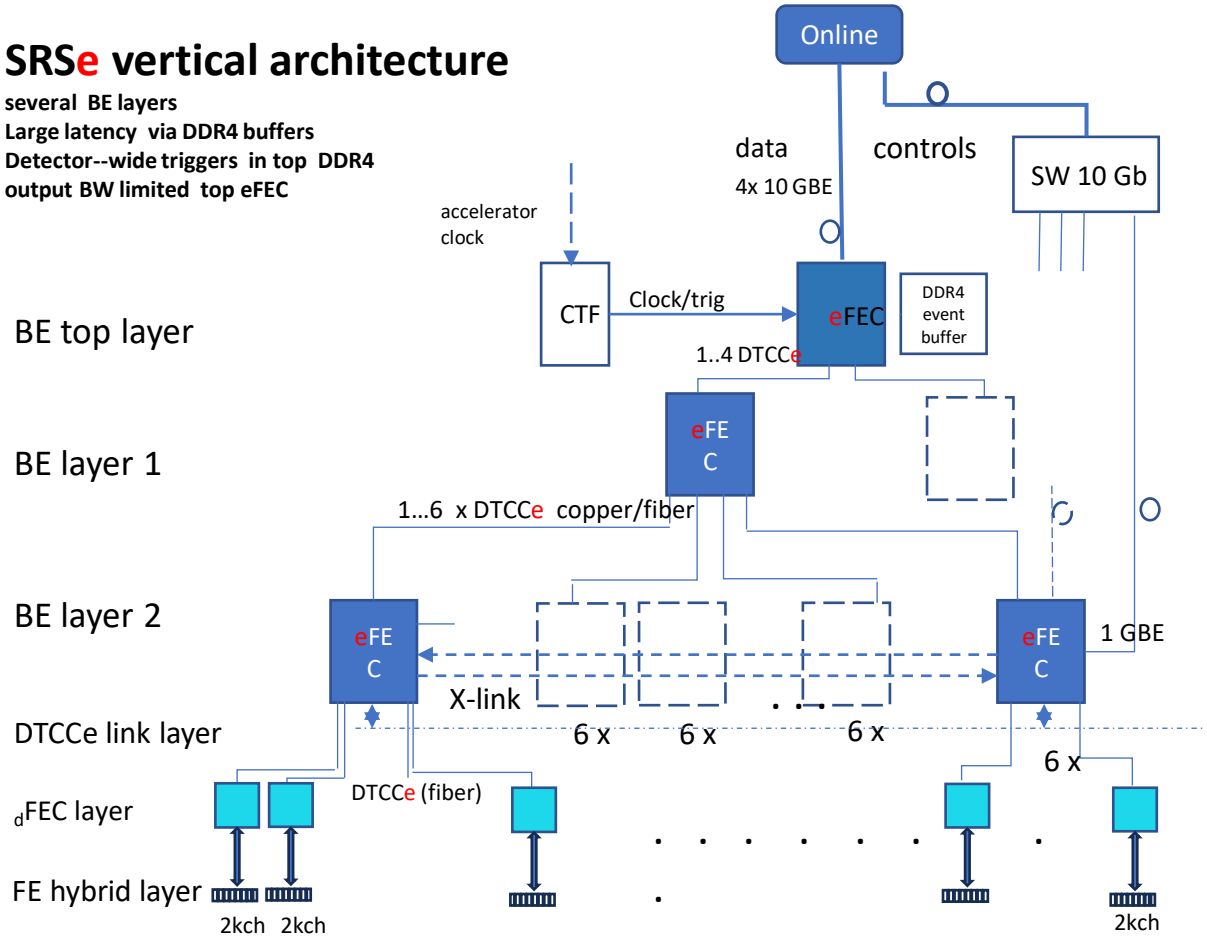
SRSe horizontal architecture

1 single BE layer
output BW aggregation via high perf. Switch
Independent FEC slices
Flow-through ROI triggers in BRAMs



SRSe vertical architecture

several BE layers
Large latency via DDR4 buffers
Detector--wide triggers in top DDR4
output BW limited top eFEC



SRSe project draft, call for DRD1 teams

FE -HW

-VMM3a 128 ch (standard)

-SAMPA 128 ch (proto)

-HGCRoc study case

….

dFEC-HW

uROC 256 ch -> see talk A.Rusu

MaxiROC 2k ch under design

PBX power box (in production)

Clock link mezzanine (under design)

eFEC-HW

New SOM concept-> see talk J.Toledo

Co-design CERN/UPV

FW / Scripts

-VMM3a Spartan7 (standard)

-SAMPA see talk G. A. de Souza IF-USP

dFEC -FW

uROC 256 ch -> see talk A.Rusu

MaxiROC 2k ch -> see talk D.Pfeiffer

PBX

V-Monitor via RP (uPython)

dFEC Clock synchronizer (tbd)

eFEC FW

DTCCe coder- decoder (tbd)

10GB Ethernet cores **ZU9CG**

Template triggers (tbd)

DAQ & Slow Controls SW

-VMM3a self triggered (standard)

-VMM3a triggered mode->
Jin-Hee Chang / FRIB

dFEC DAQ Ethernet

uROC 256ch -> see talk A.Rusu

MaxiROC 2k -> see talk D.Pfeiffer

Clock-Trigger-EvNr distribution

TLU ? under investigation

eFEC

Linux for **ZU9CG ARM core <->** DDR4
UPV Valencia

DAQ choice & integration (tbd)

get on the SRS$_e$ boat

wanted competences (min 1):

- Ultrascale+ Zync Firmware developer AMD Vivado
- Ultrascale+ Zync PS : MPSOC* /DDR4 (4GB) Linux (->UPV)
- Custom DTCCe link protocol via GTH 16/1 SERDES 12.5 Gbps
- Geo-mapped BRAM trigger Algo template
- Data output via 10G IP core + Jumbo subsystem
- uPython – GUI developer I2C &SPI resources on eFEC
- eFEC to DAQ system integration

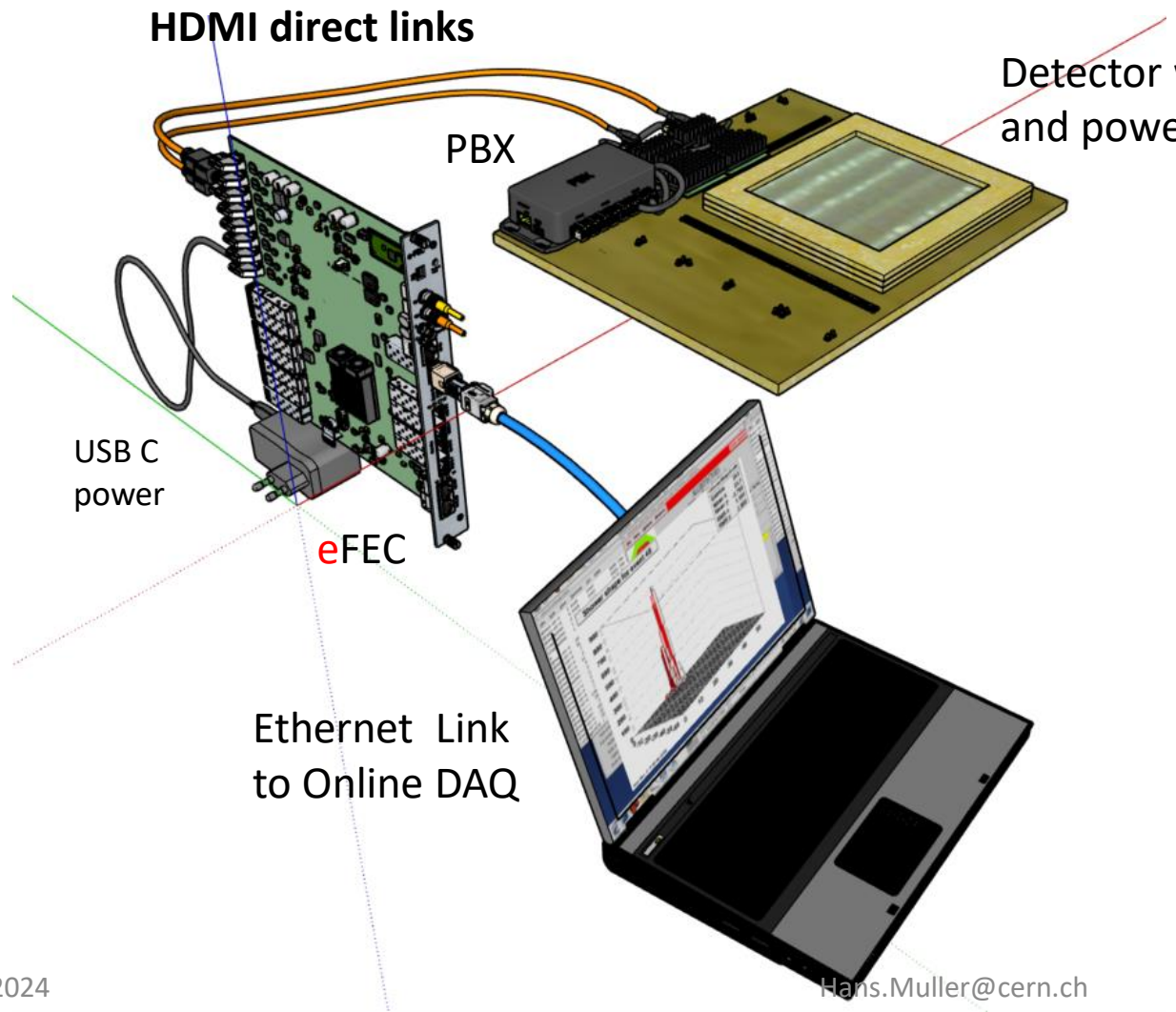
NB: for development on Ultrascale Zync FPGA on eFEC
*we start start with Enclustra SOM **
ME-XU1-9EG-1E-D11E-G1-R4.2
plugged on their carrier card
ME-PE3-4S-C-R1.1

see talk J. Toledo

- initial EG version with 4GB DDR4, 1 APU unit: quad core ARM Cortex A53 , 1 RT unit:
- realtime dual core ARM Cortex R5F. If required later SOM upgrade can be considered

Backup material

legacy HMDI ports on eFEC



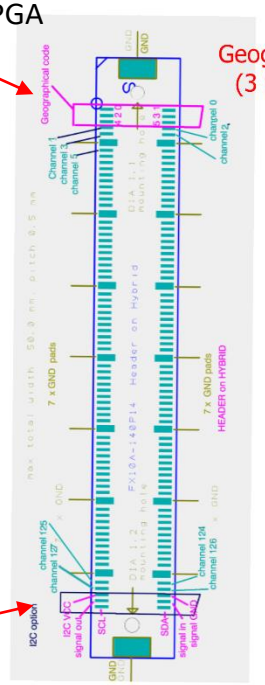
Example of a small, crate-less
SRS readout system with eFEC module

eFECs can be powered via USB-C
and include frontend power over 8 short
HDMI AD cables with GND copper braid
for the GND return.
Alternatively, for longer distances up 25m
the frontend can be powered
via PBX.

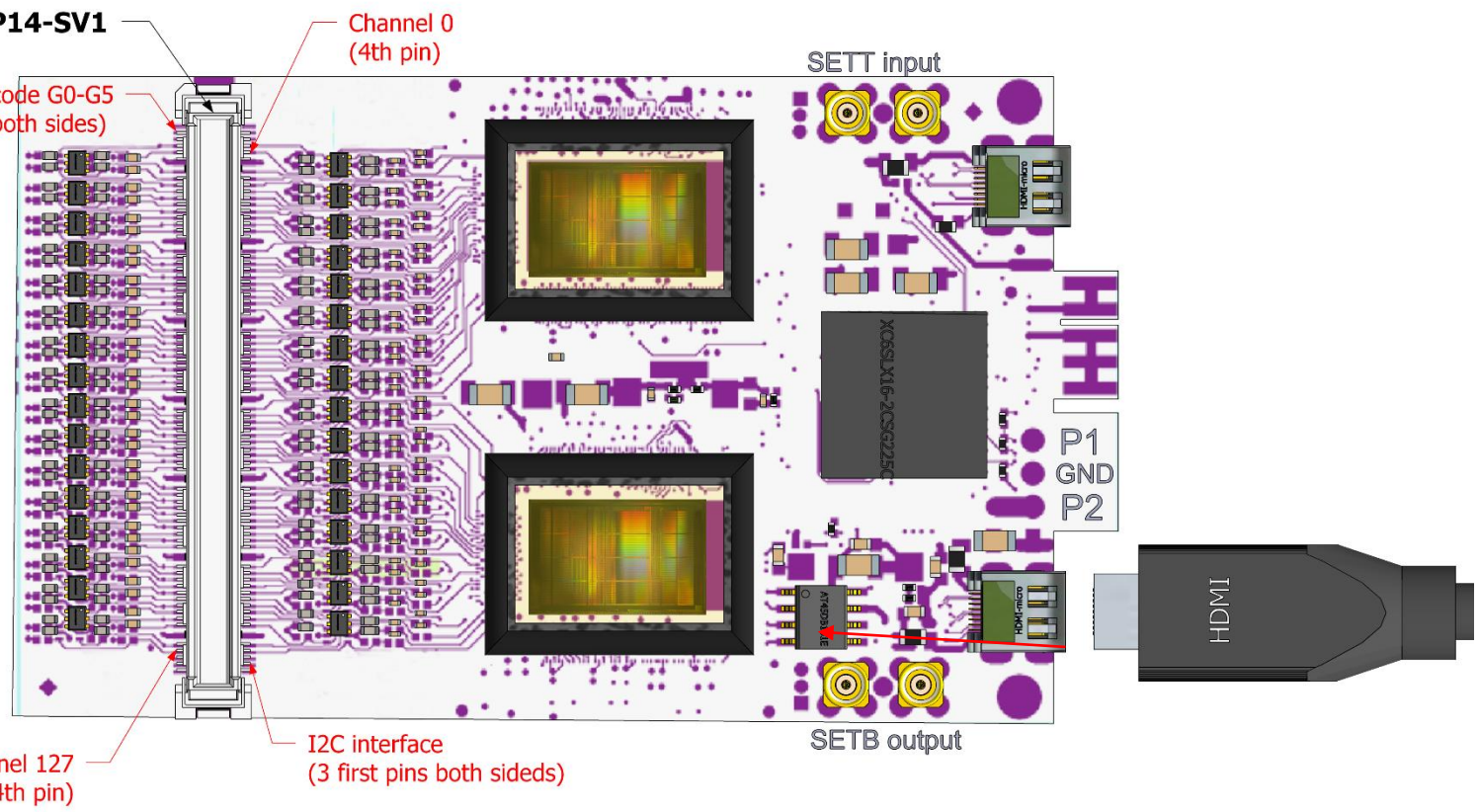
geo. position code on 140 pin HRS connector

Geographic address on detector
As from VMM hybrid V5 (Spartan7)
6 geographical code pins go
to 10k pullup I/O on FPGA

6 bit position
coding
on detector
frames
1= floating
0= GND



I2C option
OPTION: Connect
SCL, SDA to FPGA IO pins
and I2C VCC to UAUX =2.5V

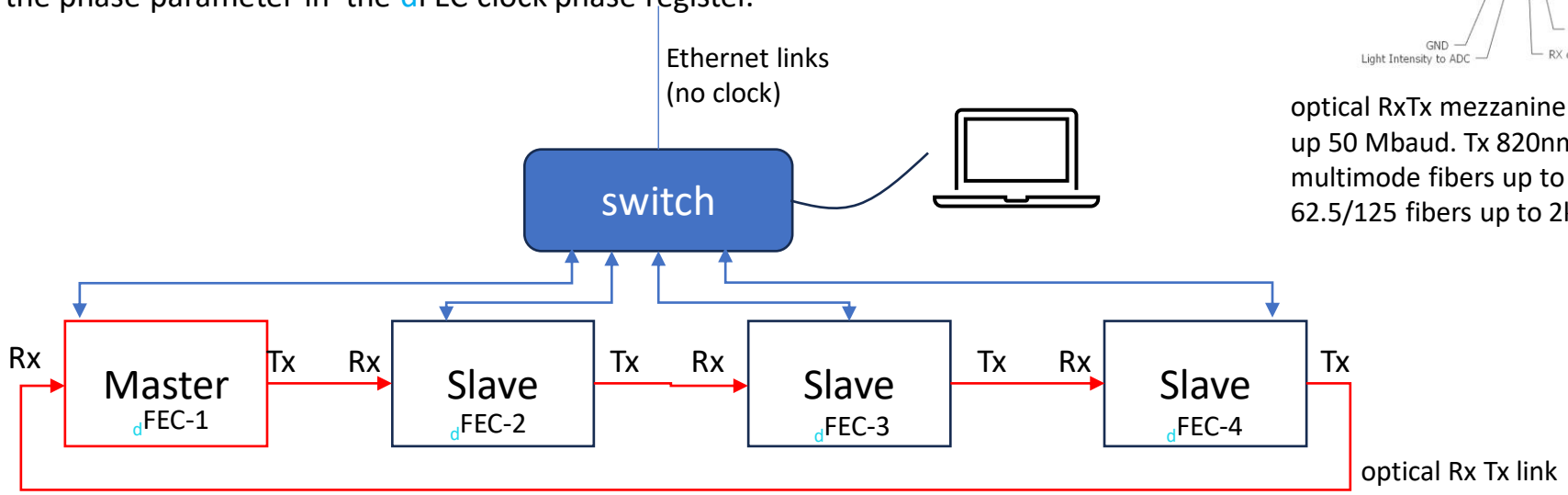


Hans.Muller@cern.ch

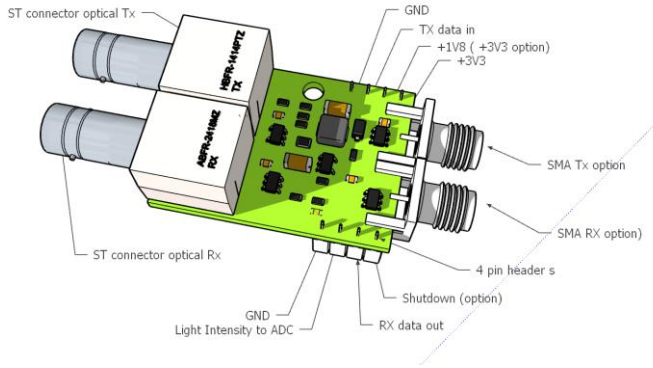
FE clock (dFECs without backend)

dFECs with direct ethernet RO don’t receive a common clock via ethernet, they use their own master clock connected via a fiber optics clock link, each dFEC using the clock of the previous in line.

phase delay between the Tx output of the dFEC master and Rx input can be measured and, divided by the number of dFECs connected in a complete Rx Tx ring.
A training run stores the phase parameter in the dFEC clock phase register.



Common clock small systems

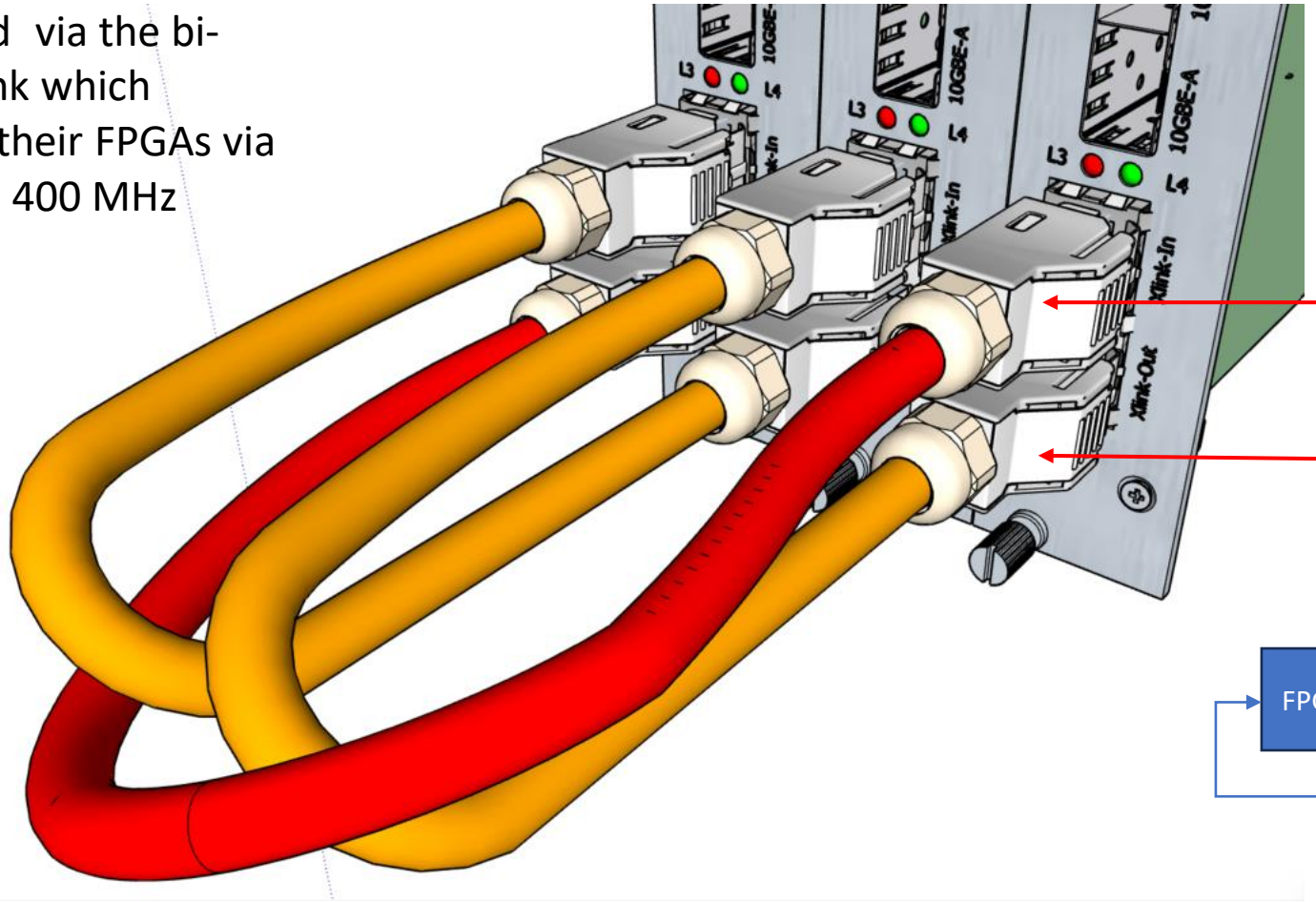


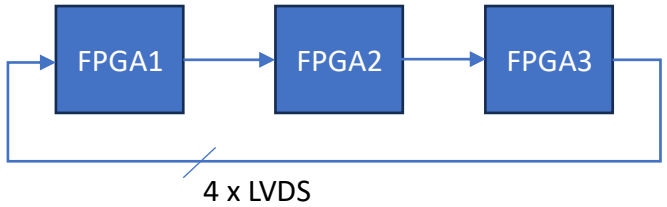
optical RxTx mezzanine for clock link up 50 Mbaud. Tx 820nm 50/125 multimode fibers up to 900m and 62.5/125 fibers up to 2km.

Hans.Muller@cern.ch

Xlink

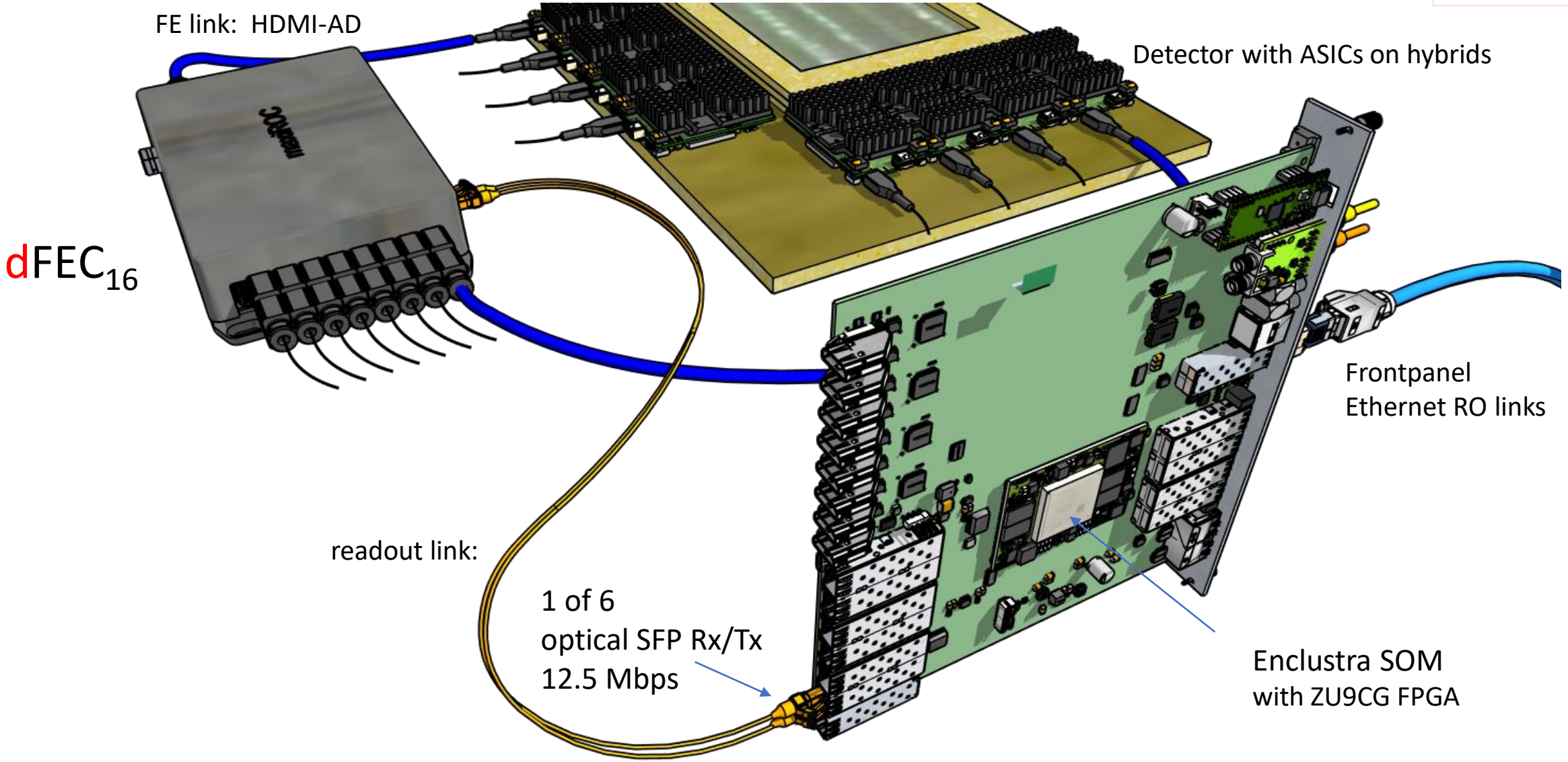
Multiple eFECs can be interconnected via the bi-directional Xlink which interconnects their FPGAs via 4 LVDS links @ 400 MHz





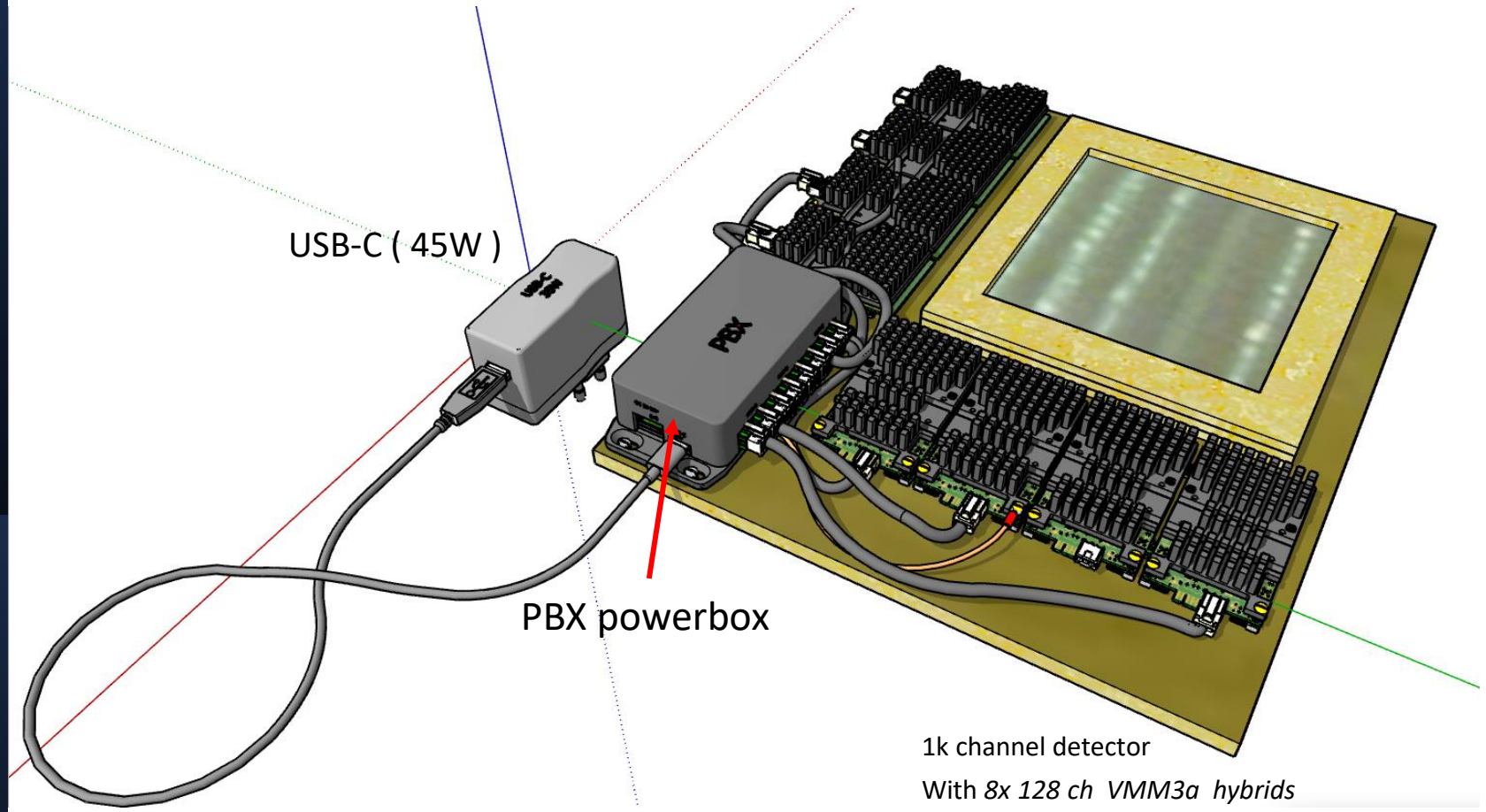
Hans.Muller@cern.ch

DTCCe link over fiber optics on one of 6 rear-side SFP ports



PBX frontend power

PBX user manual



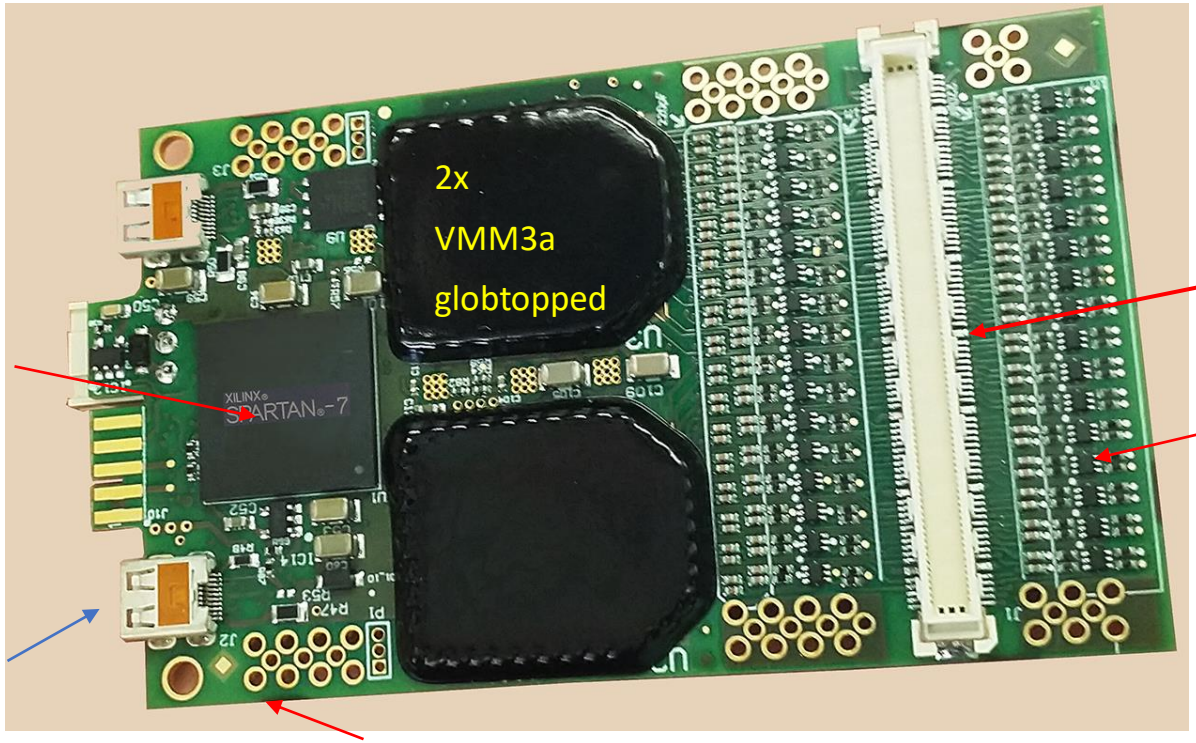
1k channel detector

With *8x 128 ch VMM3a hybrids*

Hans.Muller@cern.ch

128 ch. frontend hybrid: VMM3a

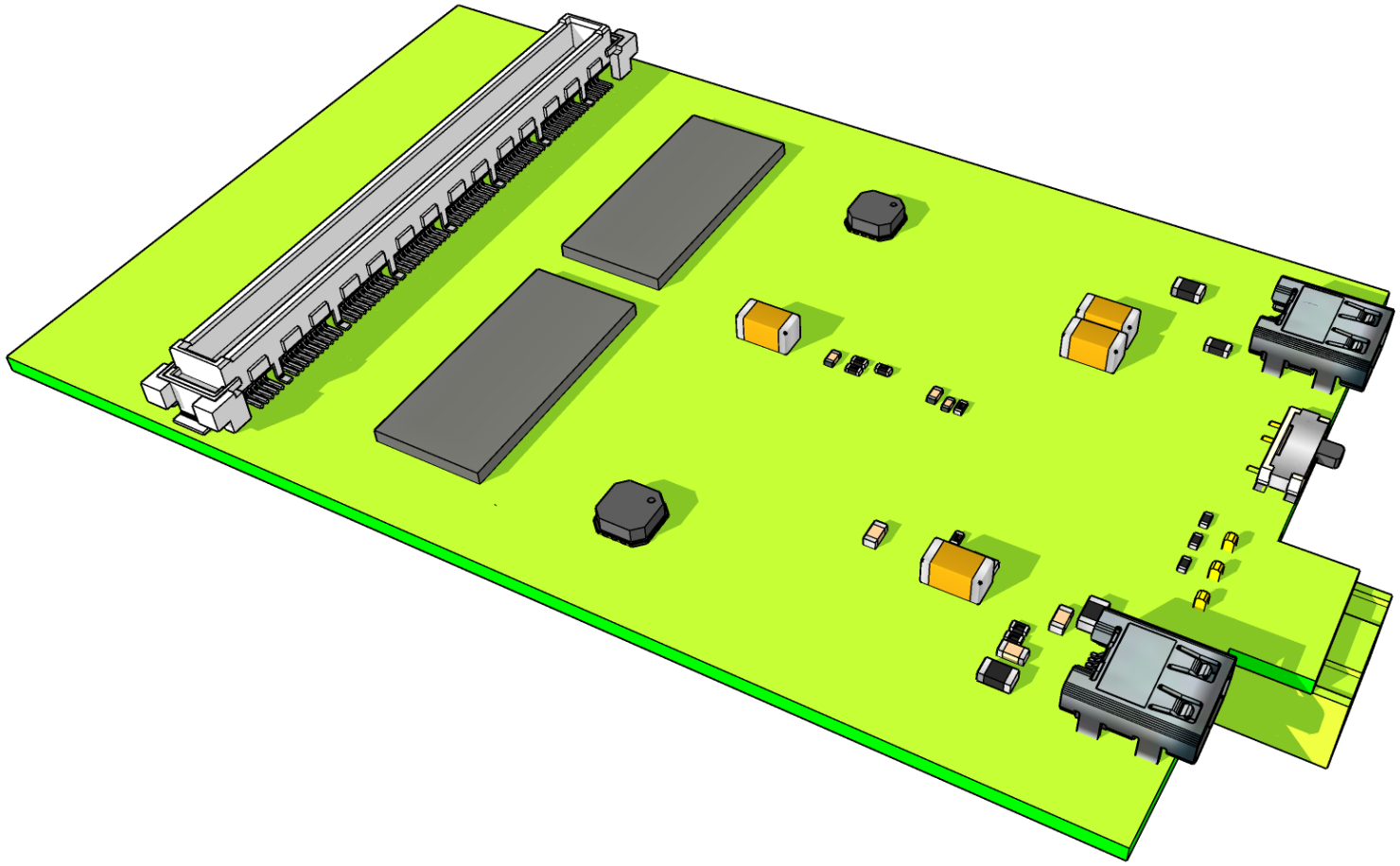
VMM hybrid user manual



Successor to the
2010-2019 APV frontend hybrid

Photo VMM hybrid V5 (2022+) bottom side (cooler plate removed)

Draft: HGCROC hybrid



No FPGA
HRS FE connector
Plugin for MPGD detectors
128 channels (2x HGCROC ASICs)
SLVS to LVDS conversion
One HMDI per ASIC
Charge & Trigger decoding in dFEC
Clock and config from dFEC