Versatile Link+ / lpGBT overview

2nd DRD1 Collaboration Meeting

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Versatile Link+ Project

High-speed, radiation-tolerant optical links for (HL)-LHC experiments

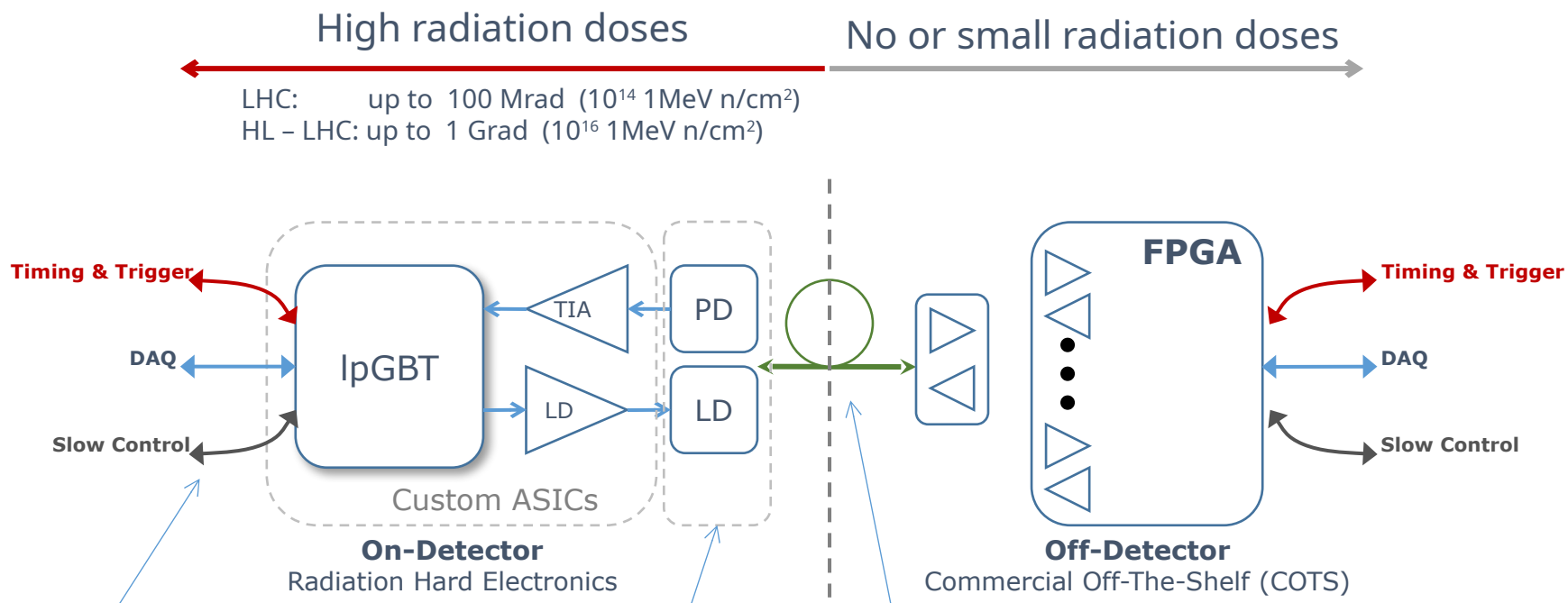
- Recurring challenge, similar needs in many detectors & experiments

VL+ project: common development of ‘standardized’ link components

- Successor to Versatile Link project (GBTX, VTRx, …)
- One link for TT&C (Timing, Trigger & Control)
- Covering rad-hard ASICs, front-end modules, passives, back-end support

Today: Introduction to VL+ links & lpGBT ASIC

Versatile Link+ Architecture



lpGBT – Main Feature Set

High-speed links (back-end ↔ lpGBT)

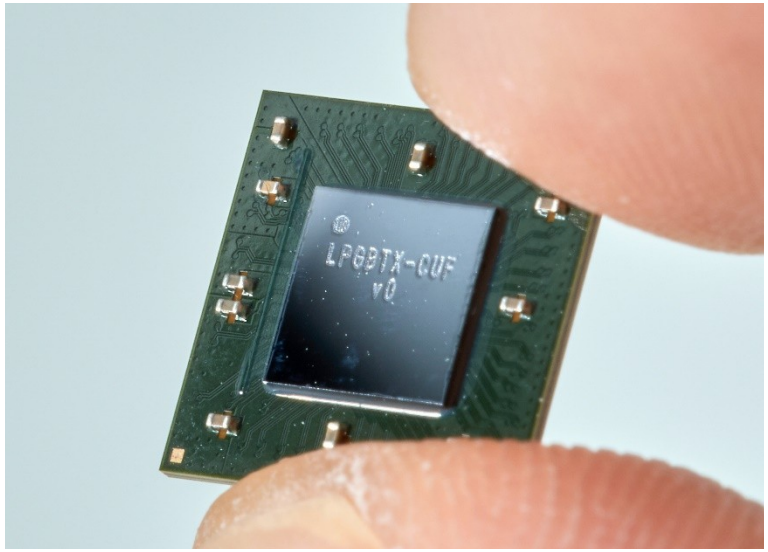
- Uplink: 5.12 or 10.24 Gb/s
- Downlink: 2.56 Gb/s

Electrical links (lpGBT ↔ front-end)

- Up to 28 (up) + 16 (down)links, 80 Mb/s - 1.28 Gb/s per link
- Low-voltage differential I/O links (CLPS = CERN Low Power Signalling)
    - Pre-emphasis & equalization provided to manage signal integrity
- Phase-aligner for data from front ends (automatic or manual)

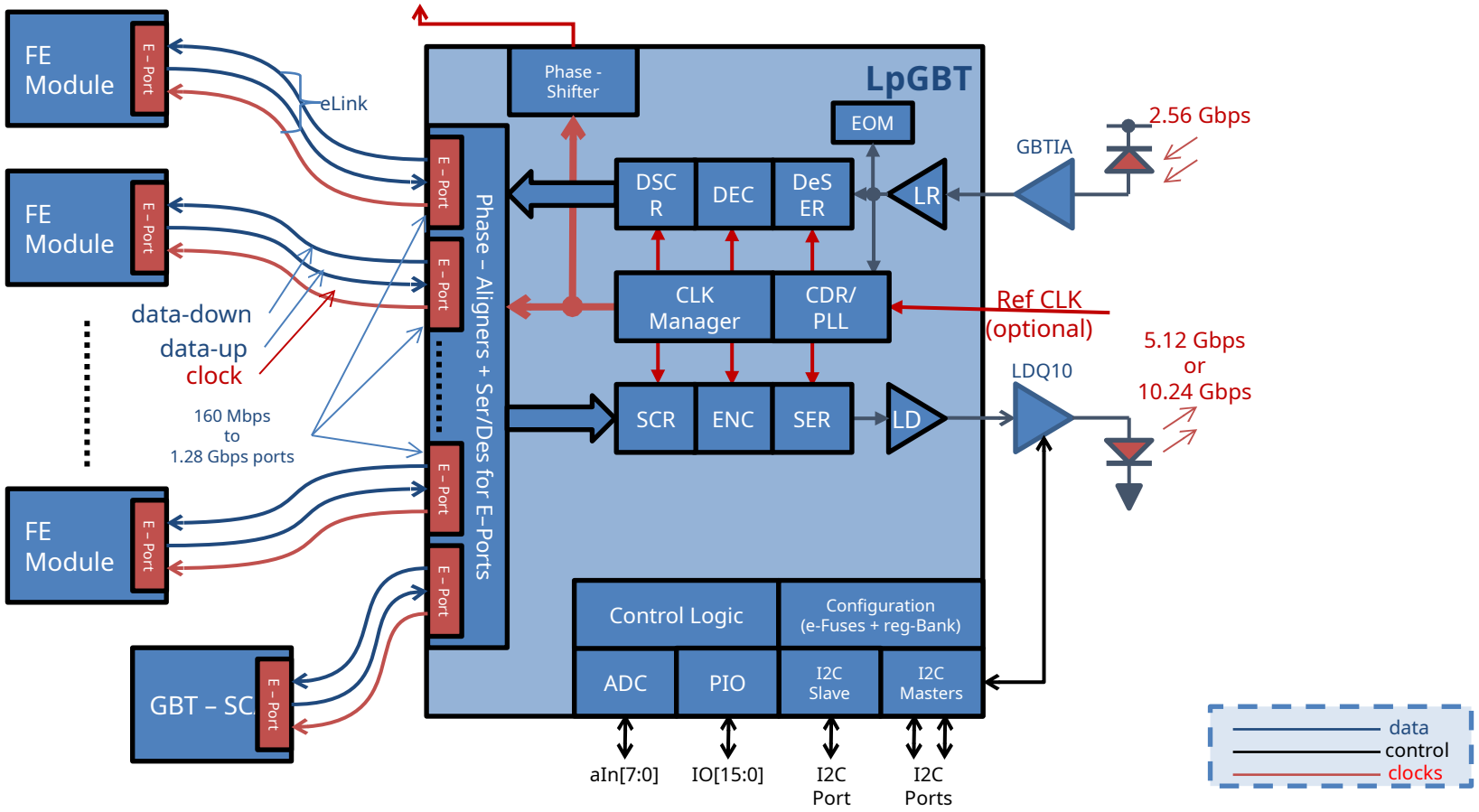
Timing functionality

- Deterministic & fixed latency (for clocks & data, both directions)
- Frequency-programmable clock outputs (40 MHz – 1.28 GHz)
- Phase- and frequency-programmable clock outputs (50 ps step size)
- Low jitter (<5 ps rms)



Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

lpGBT – Block Diagram Overview



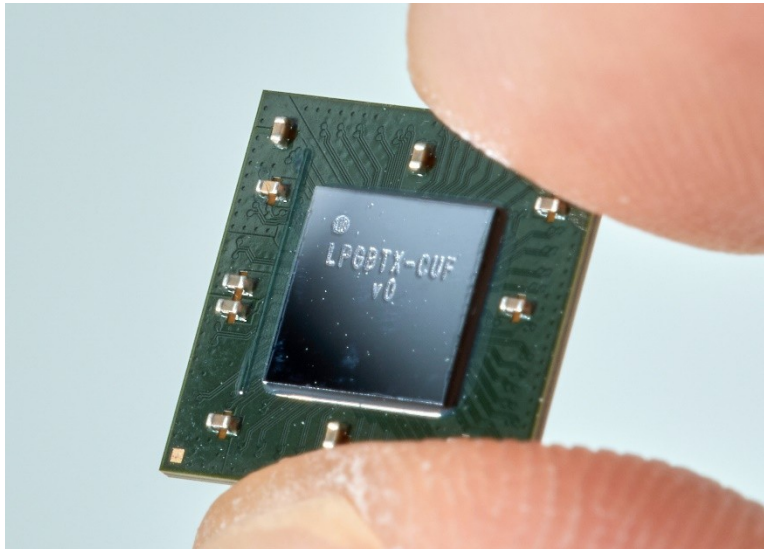
lpGBT – Main Feature Set

Experiment Monitoring & Control

- 3x I2C masters, 16 CMOS GPIOs
- Factory-calibrated analog subsystem
  - 8-channel, 10 bit ADC
  - 8 bit current DACs (e.g. for PT-1000)
  - 12 bit voltage DAC
  - Reference voltage generator
- Extensible using external slow control ASIC (GBT-SCA)

Configuration

- Power-Up State Machine, Automated ROM start-up, Watchdog, BOR, …
- User configuration via optical link, I^2C or serial control channel
- READY & RESET signal generation for downstream ASICs



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lpGBT – Radiation Tolerance

lpGBT ASIC manufactured in 65 nm CMOS

- Technology resistant to TID-effects, widely adopted for HL-LHC

Protected against single-event effects (SEU, SET) by design

- Configuration, control logic, clock generation covered by TMR or RHBD methods
- Data links protected using forward error correction (FEC) – two modes available (tradeoff bandwidth/data protection)

SEE and TID response fully characterized (e.g. expected error rates, etc)

- TID response is being screened for all production lots, spec: 2 MGy (200 Mrad)

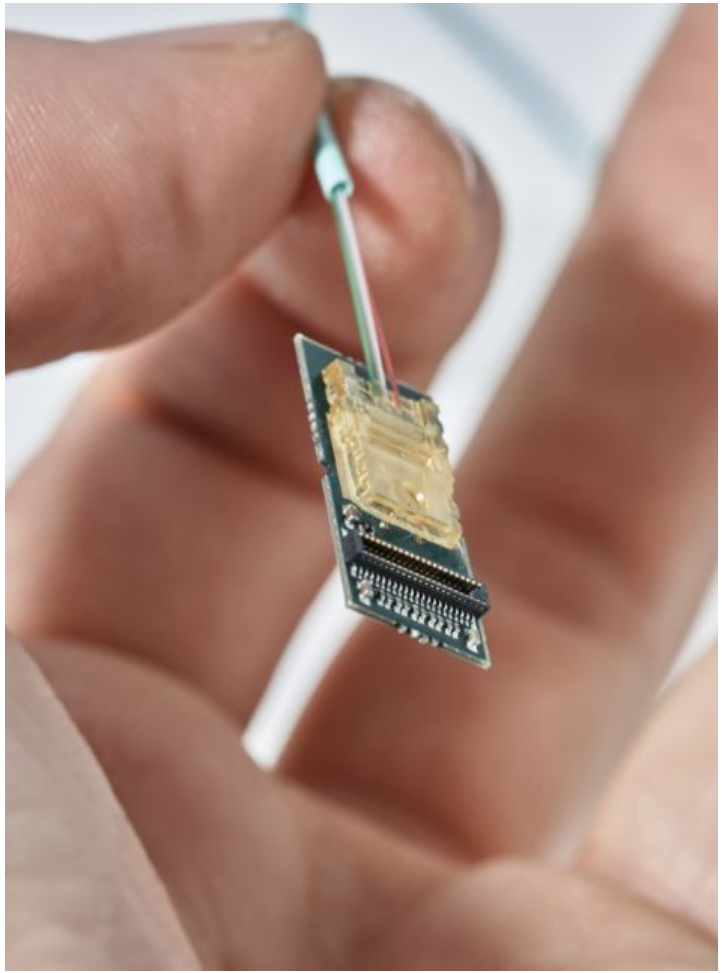
VTRx+ Optical Link Module

Off-the shelf optical modules not compatible with on-detector applications

- Form factor, radiation tolerance, …

VTRX+: Custom Module - Key Specifications

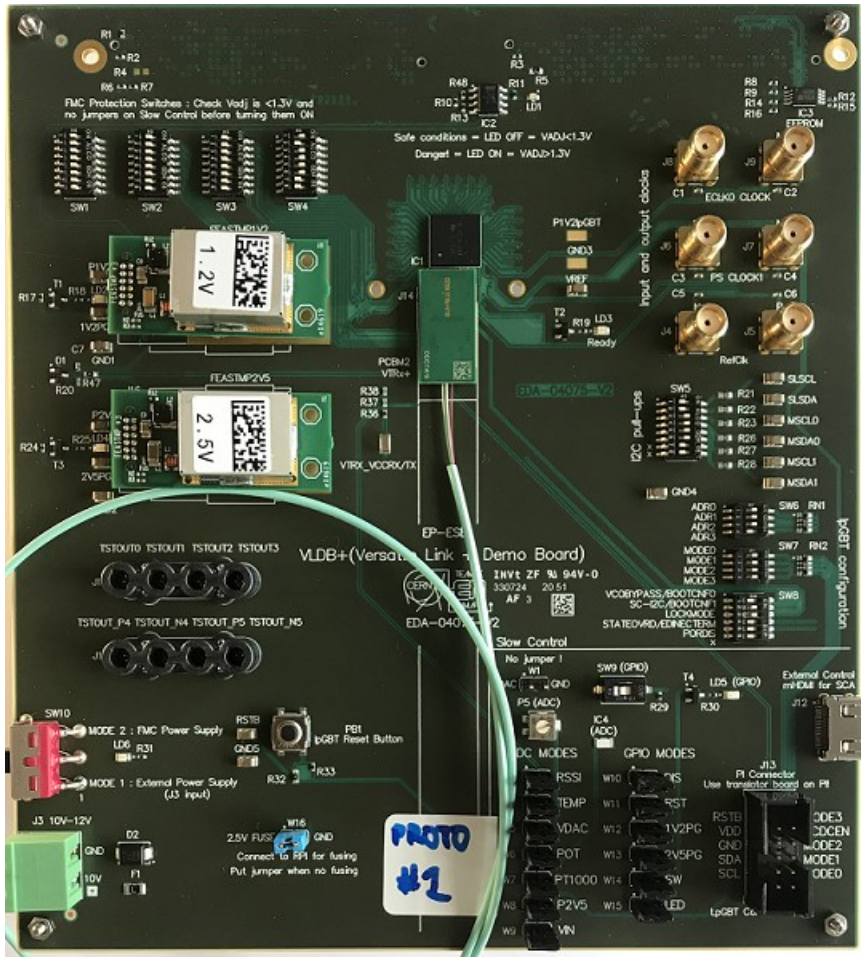
- 850 nm multi-mode fiber, 4 (uplink) + 1 (downlink) channels, data rate compatible with lpGBT
- Miniaturized: 20x10x4 mm
- Pluggable: board-to-board connector (electrical), fiber pigtail (optical, made to order)
- Temperature range: -30 – 60°C
- TID: 1 MGy (100 Mrad), 10^{15} n/cm^2



VLDB+

Demonstrator board for VL+

- ‘Batteries-included’ demonstrator board for full system
- On-board: lpGBT, VTRX+, DC/DC regulators
  - Access to clock & data in/outputs, analog and digital I/O
  - Dual HPC FMC connectors – allows prototyping with FEB or FPGA development kits
- Raspberry Pi-based control toolkit
- More information: https://vldbplus.web.cern.ch/



System Integration Support

lpGBT is a custom, complex device – requires support ecosystem

- lpGBT-FPGA: Open source FPGA IP core
  - Implements data encoding/decoding, configuration links, etc
  - Can be included in FPGA back-end systems, compatible with various FPGA families
  - Provides transparent user data bridge, configuration access, etc
- lpGBT control library: Python-based driver library
  - Reference implementation, to be integrated or adapted by users
- Support forum/mailing list for users, place for discussion: https://lpgbt-support.web.cern.ch
  - User base ~ 500 people, dedicated support team for following up issues

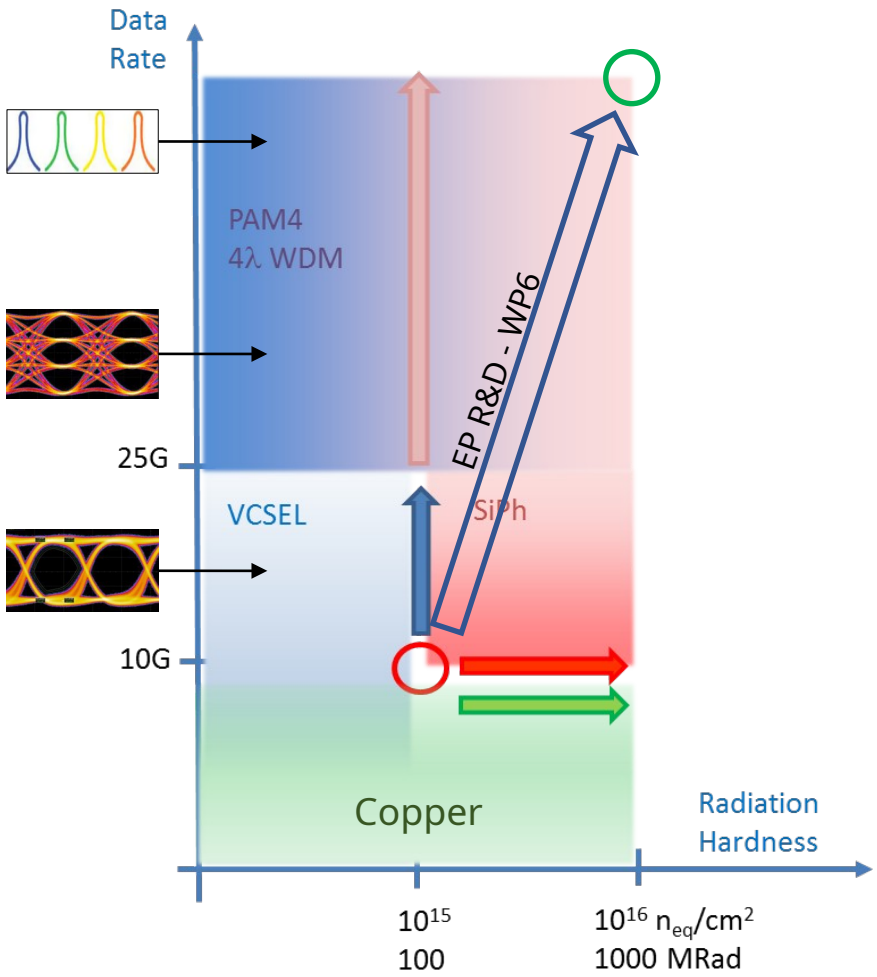
The Future

VL+ components designed for the HL-LHC upgrade

- Manufactured in quantities demanded by experiments (~50-300k units)

R&D in progress to develop new HEP links (e.g. EP R&D WP6, DRD7)

- Higher luminosities, detector resolutions, addition of timing → increase of data rate & radiation dose
- Current ambitions: 10 Gb/s → 100 Gb/s per fiber (WDM, 4 x 25 Gb/s), 1 MGy → 10 MGy
    - New technologies: Silicon photonics, 28 nm CMOS



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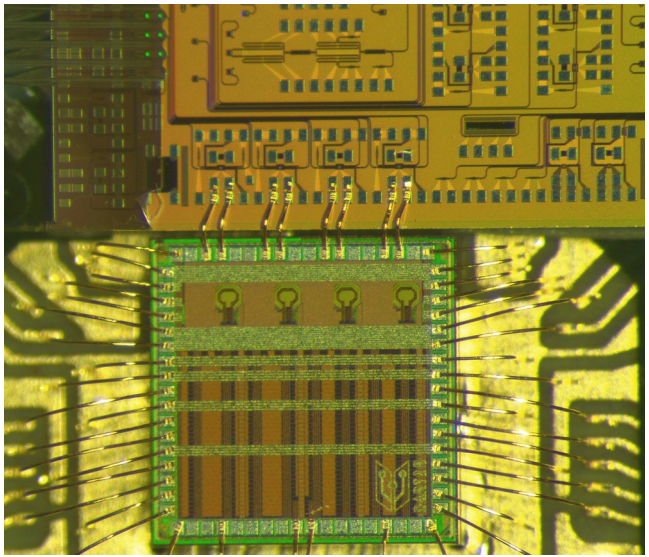

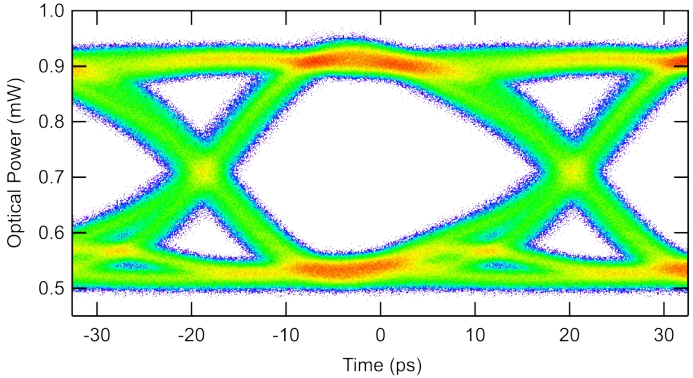

Resources

lpGBT manual: https://lpgbt.web.cern.ch or https://cds.cern.ch/record/2809058/

lpGBT-FPGA documentation: https://lpgbt-fpga.web.cern.ch

lpGBT / VL+ ordering information: https://ep-ese.web.cern.ch/project/lpgbt-and-versatile-link

VLDB+ documentation, ordering information: https://vldbplus.web.cern.ch

Versatile Link+ project: https://cern.sharepoint.com/sites/project-Versatile-Link-Plus/

Communications ASICs overview: https://gbtproject.web.cern.ch/gbtproject/

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