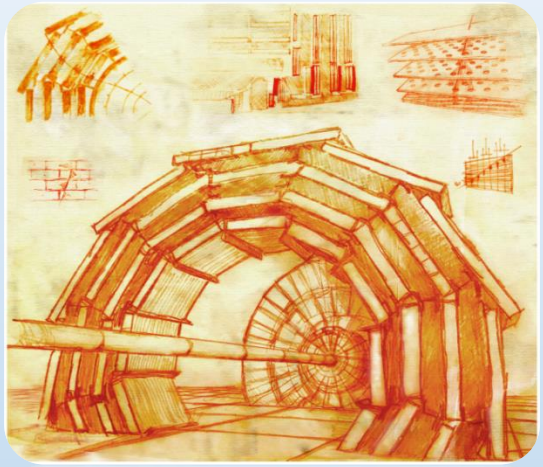
CMS RPC Link System

(2nd DRD1 Collaboration Meeting & Topical Workshop on Electronics for Gaseous Detectors)



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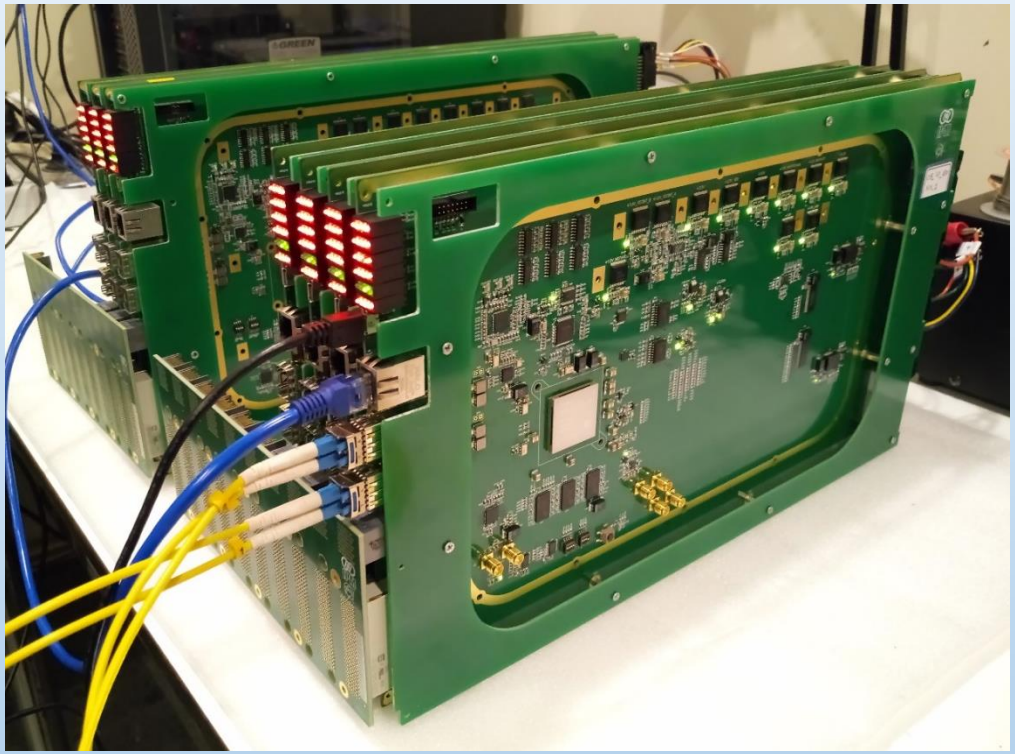
19 June 2024

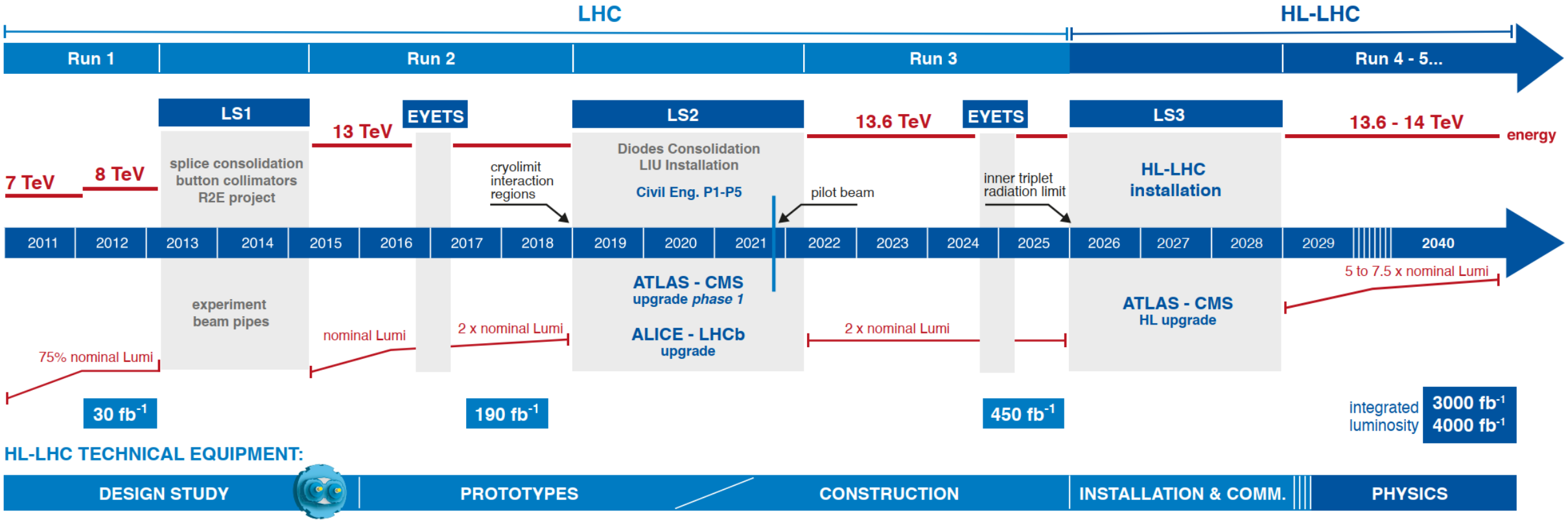
Outlook

- ❑ *Present CMS RPC Link System – Upgrade Motivation*
- ❑ *CMS RPC Phase-2 Upgrade Projects*
- ❑ *Review on new RPC Link System Project*
- ❑ *Irradiation Test Results and Validation at P5*
- ❑ *Summary*



Back-up: *96-Channel TDC , HL-LHC Background Rate, Project Schedule, Radiation level at the CMS Tower Racks, CHARM location G0, CHARM TID and Fluences distribution, CHARM Irradiation Results*

LHC / HL-LHC Plan



HL-LHC TECHNICAL EQUIPMENT:

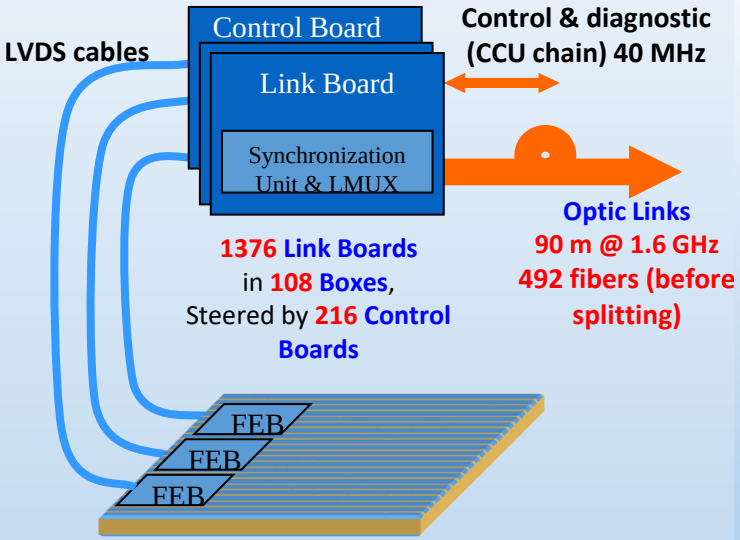
DESIGN STUDY	PROTOTYPES	CONSTRUCTION	INSTALLATION & COMM.	PHYSICS

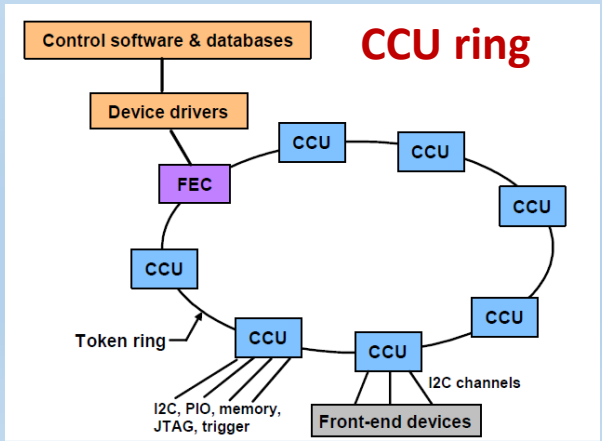
HL-LHC CIVIL ENGINEERING:

DEFINITION	EXCAVATION	BUILDINGS

Present RPC Link System - Upgrade Motivation

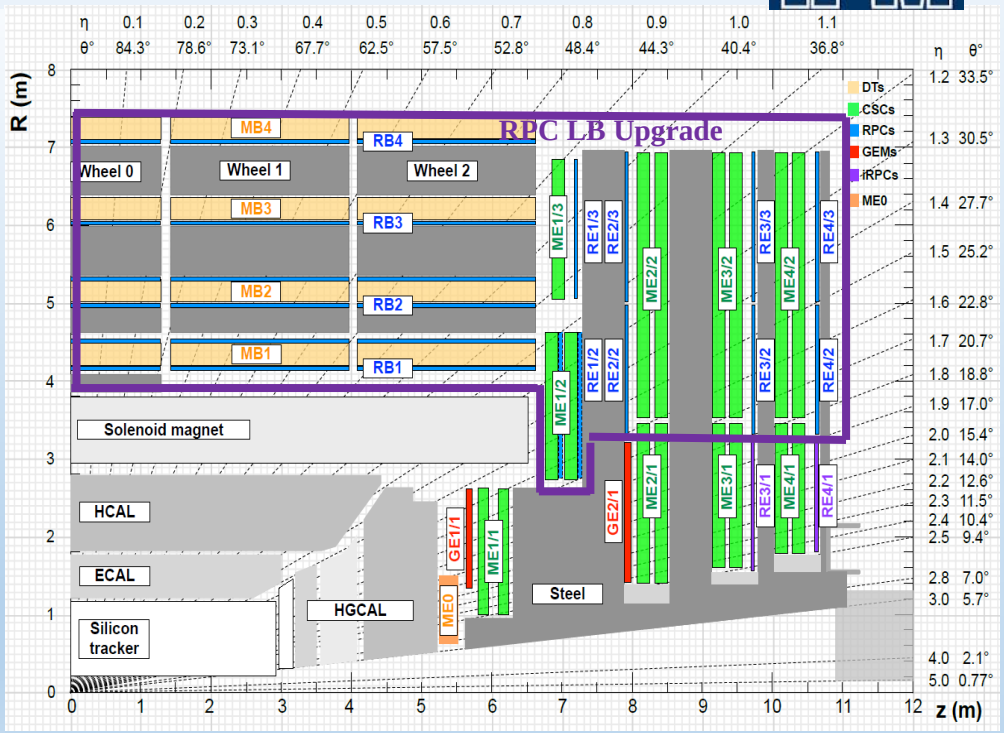
Present RPC Link System





Upgrade Motivation

- RPC signals synchronization, timing resolution is 25ns
- Data transmission speed is about 1.6 Gbps
- Control, diagnostic and monitoring of the Link system has been designed based on CCU ring (combination of copper cable and fiber optic), very susceptible to electromagnetic interference



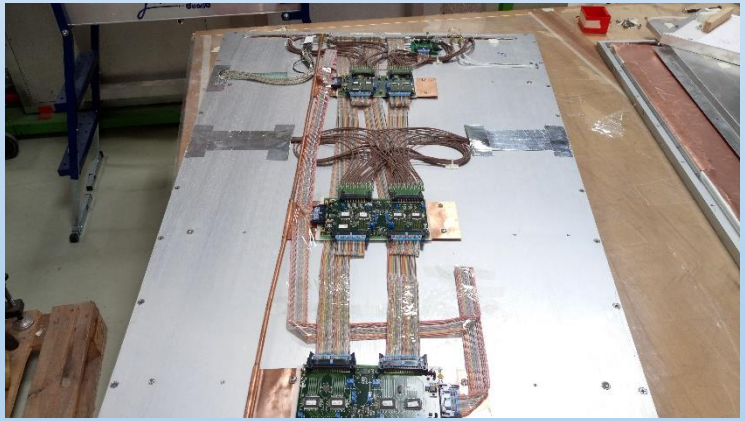
- CCU ring is not very fast, the bandwidth (40 MHz) share between 12 control boards
- Most radiation hard electronic components are obsoleted
- Electronic aging, presently the Link system at the end of LS3 is already 17 years old

Present RPC System Ingredients

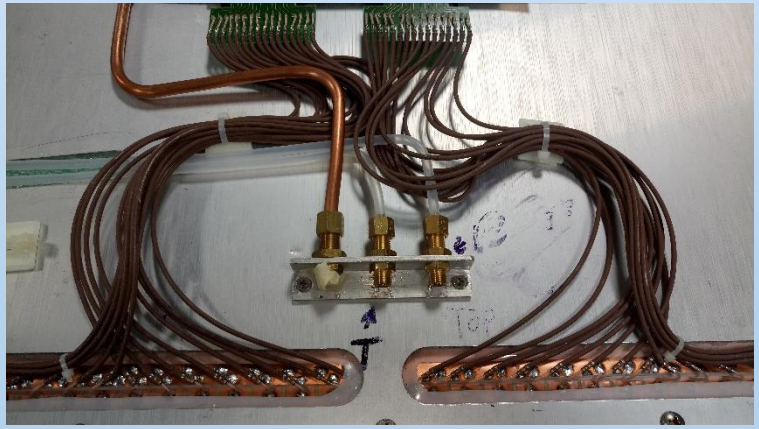
RPC Endcap Chamber

Front-end Board

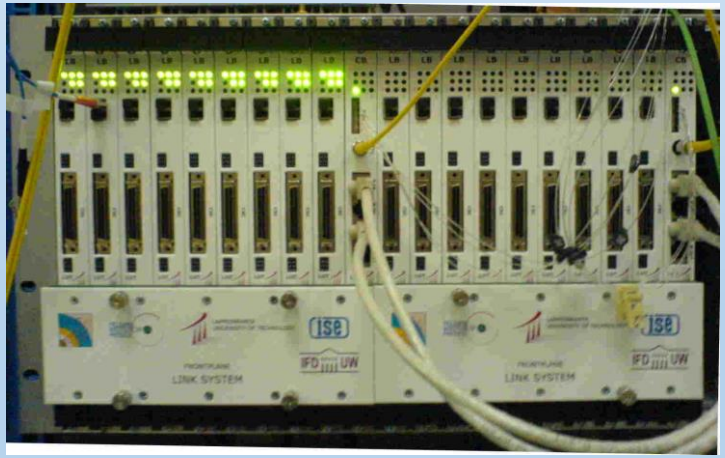
Present Link Board



On-detector Electronics

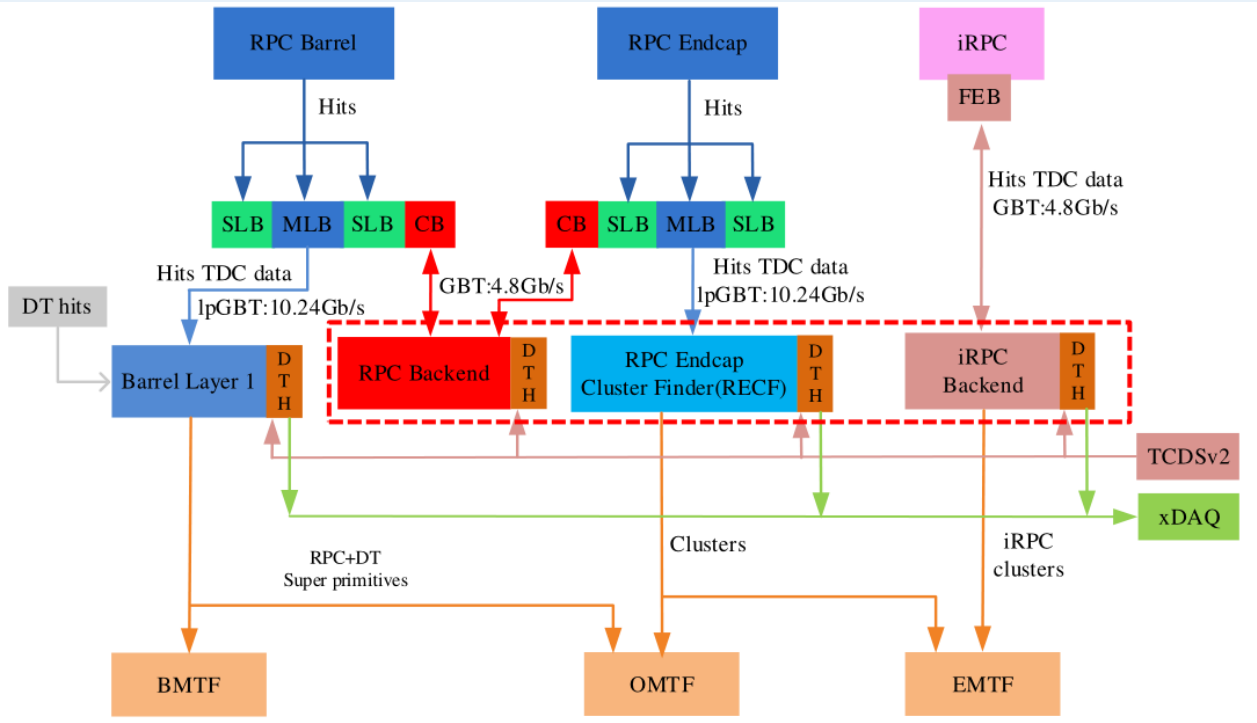


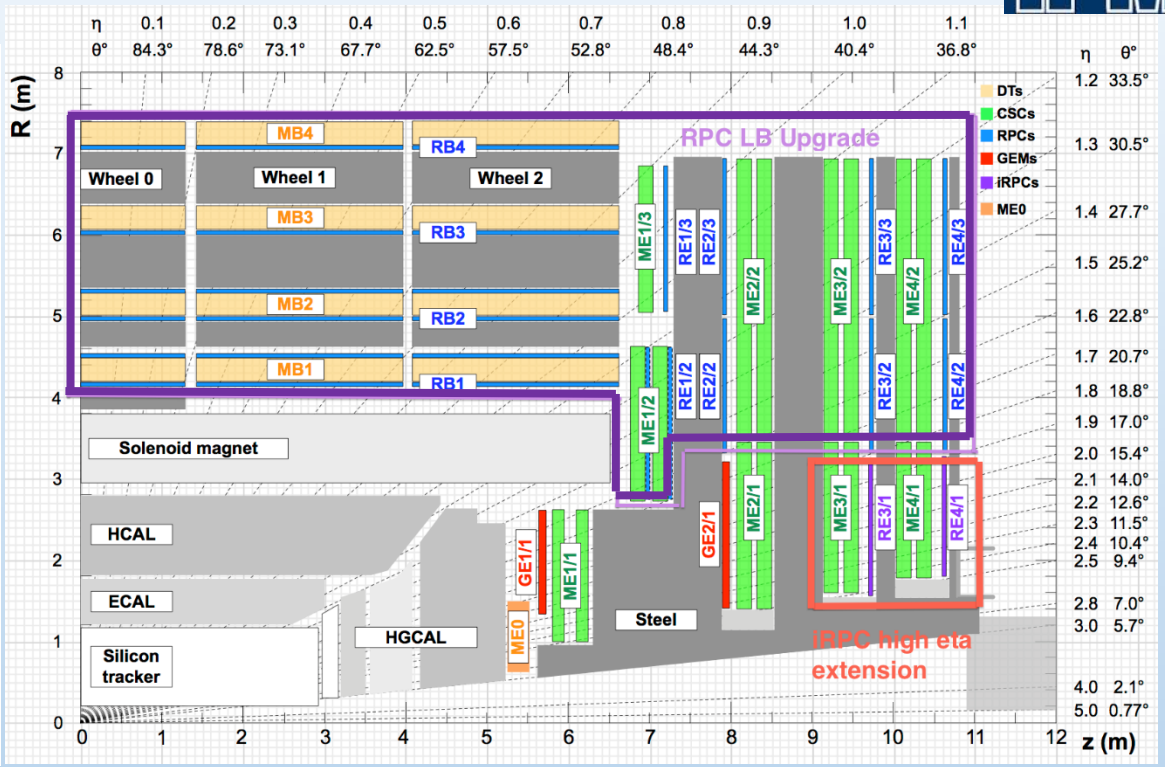
RPC Strips, Coaxial cables, Cooling and Gas Pipe



Link System (LBB)

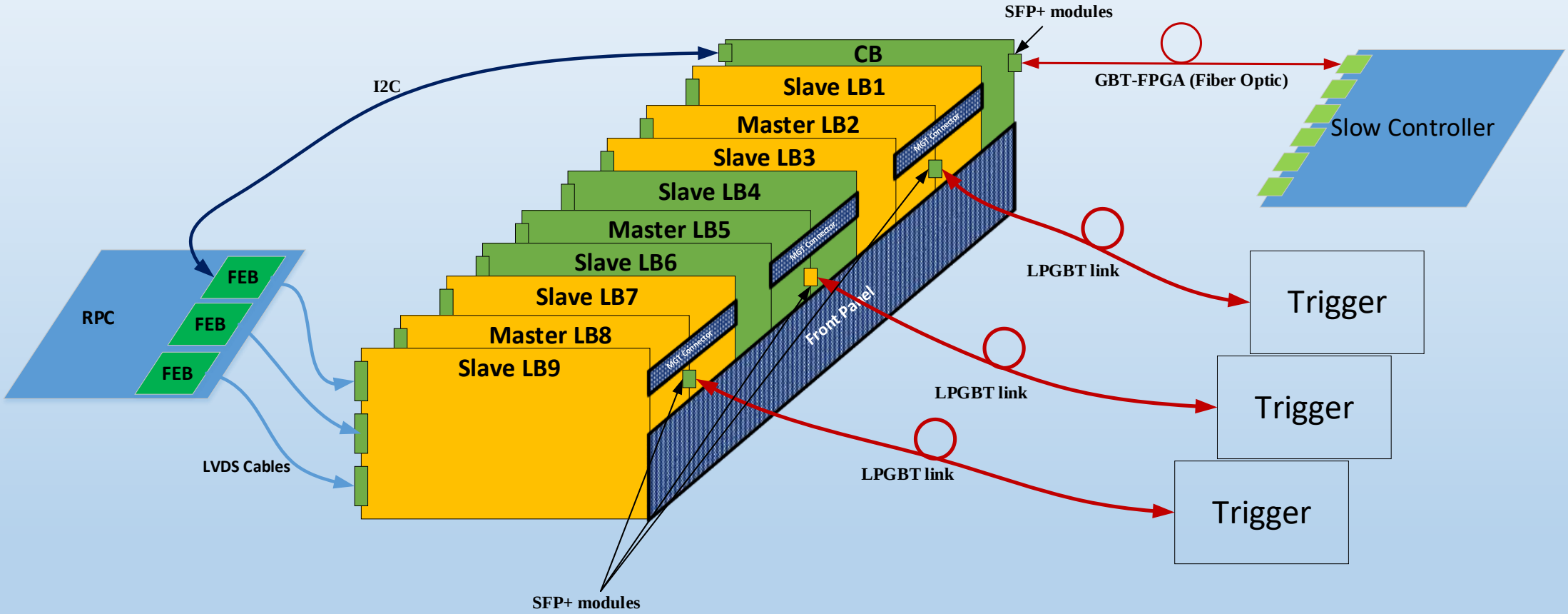
RPC Phase-2 Upgrade Architecture and Layer1





SLB: Slave Link Board
MLB: Master Link Board
CB: Control Board
B/O/E MTF: Barrel/ Overlap/ Endcap Muon Track Finder

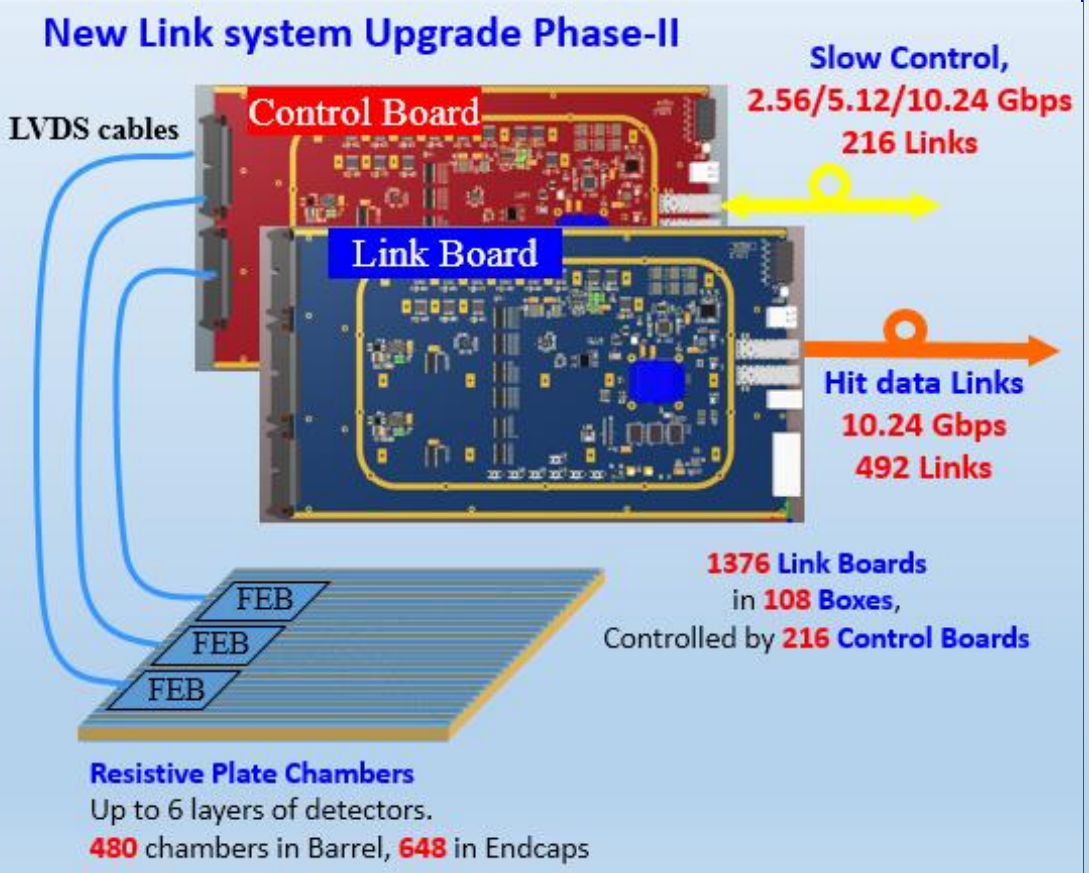
New RPC System for Phase-2 Upgrade



Overview of the Electronics

New Link system Features :

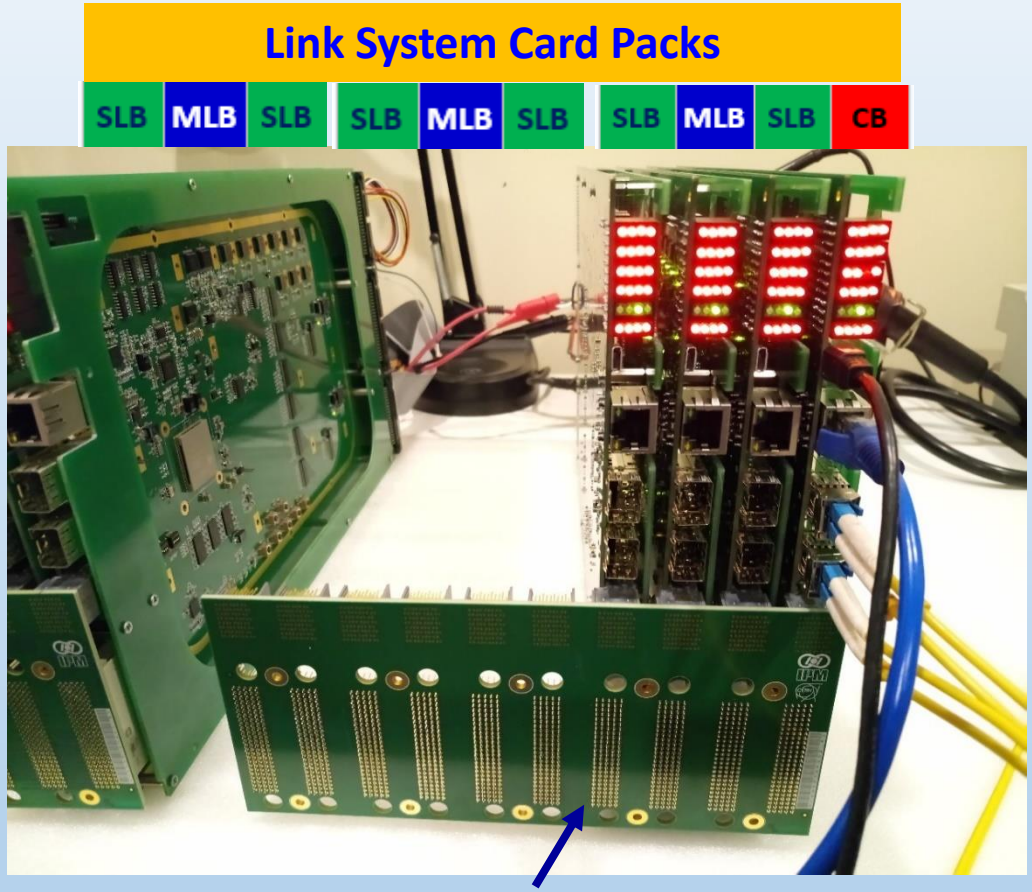
1. 14 Layer PCB , 40 × 28 cm^2
2. FPGAs are KINTEX-7, XC7K160T – Industrial Version
3. Muon hit time, TDC timing Resolution : 1.56 ns
4. Master Link board output data rate : 10.24 Gbps
5. Control Board communication with RPC Backend electronics: 4.8 Gbps
6. Input Voltage: 4.0 V (3.8V – 5.1 V)
7. Current: 3 A -> 2 A
8. Power Consumption: 12 W -> 8 W
5. Embedded internal buffer (DDR3) : 4 Gbyte
6. Optical Transceiver: SFP-10G-SR
7. Radiation Mitigation: TMR + Internal Scrubbing
   - Scrub Rate of entire FPGA (Real time SEU detection and Correction) : 13ms (31,770 times faster than the rate of SEU at the tower racks)
   - SEU at the tower racks : Every 413000 ms
8. Safety Systems:
   - Over & Under Voltage Protection, FPGA Over temperature Protection, Transient Voltage Suppressor
   - ESD Protection (15 kV)



System Requirements

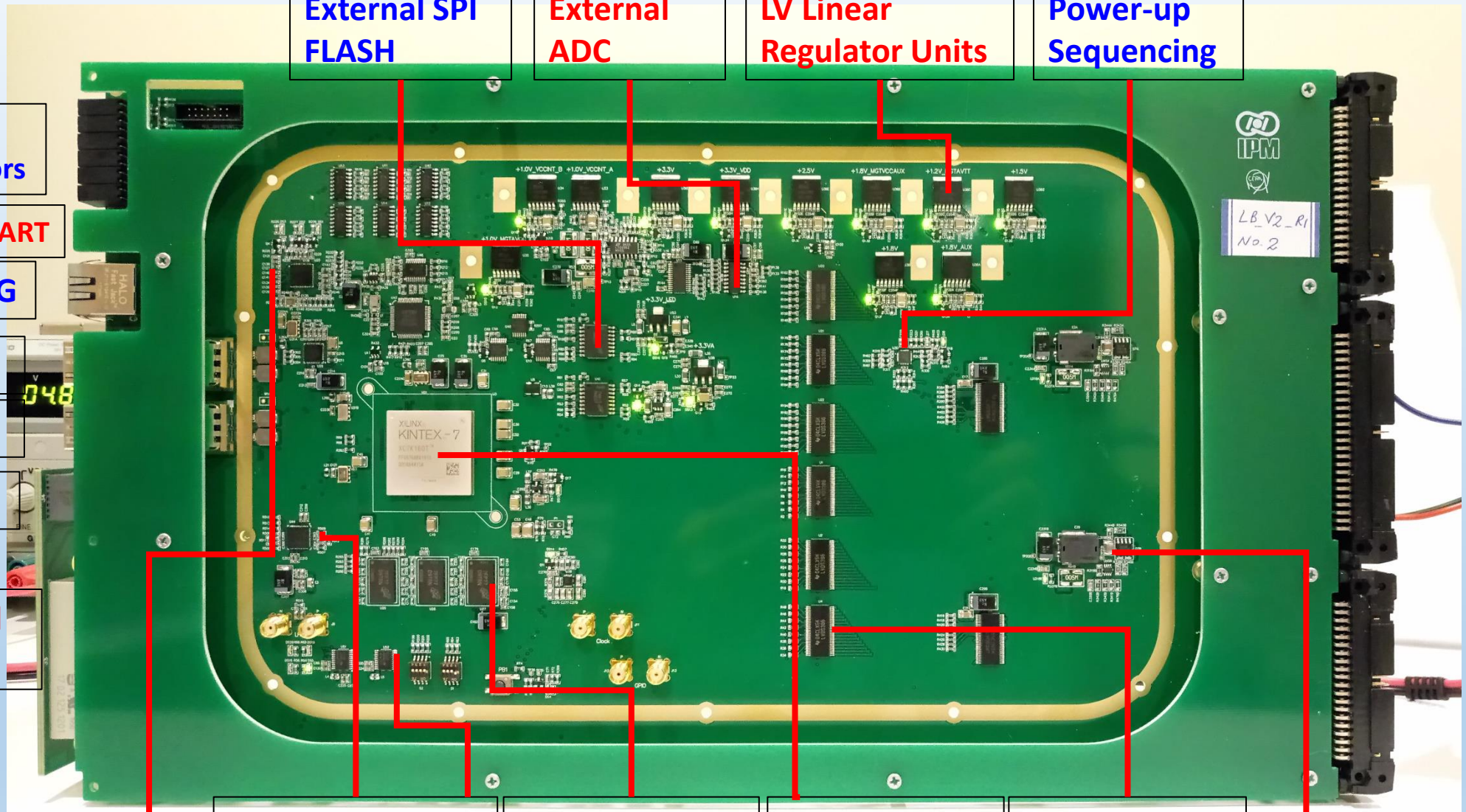
1. **Signal Conditioning:** Single LVDS signal (pair of wires/pins) for each RPC channel (strip). RPC hit is a pulse of 100ns.
   - Each LB receives 96 RPC channels i.e. full Endcap RPC (3 eta rolls),
   - or one roll of barrel RPC.
2. **Impedance Matching:** According to the LVDS standard, the line should be terminated on the receiver side by ~100 Ω resistance inside the LVDS line receiver chips.
3. **Time-Stamping:** The signals are asynchronous, and the rising pulse edge brings information about the RPC hits timing (the signals are not synchronous to any clock). Time-Stamping unit, implemented in the FPGA, measures the arrival time of the rising edge of the pulses to the corresponding bunch crossing.
4. **Latency Compensation:** The RPC signal and received TTC clock has been delayed concerning the main bunch crossing and should be fixed first. RPC signal delay and TTC clock phase shift compensator.
5. **Data collection and transmitter:** Data of 42 fired strips at each bunch crossing are selected and buffered by the data collector inside the Link Board FPGA. Crossing data of 6 hits from one Link Board will be sent to the Master Link Board. In the Master Link board, its data and the data of two adjacent Link boards are collected and merged. At Final, data of 18 hits of current bunch crossing will send to the next layer of the trigger.

- **Master/ Slave Link Board:** The system is built with Slave Link Boards and Master Link Boards, the PCB is the same, but the firmware is different.



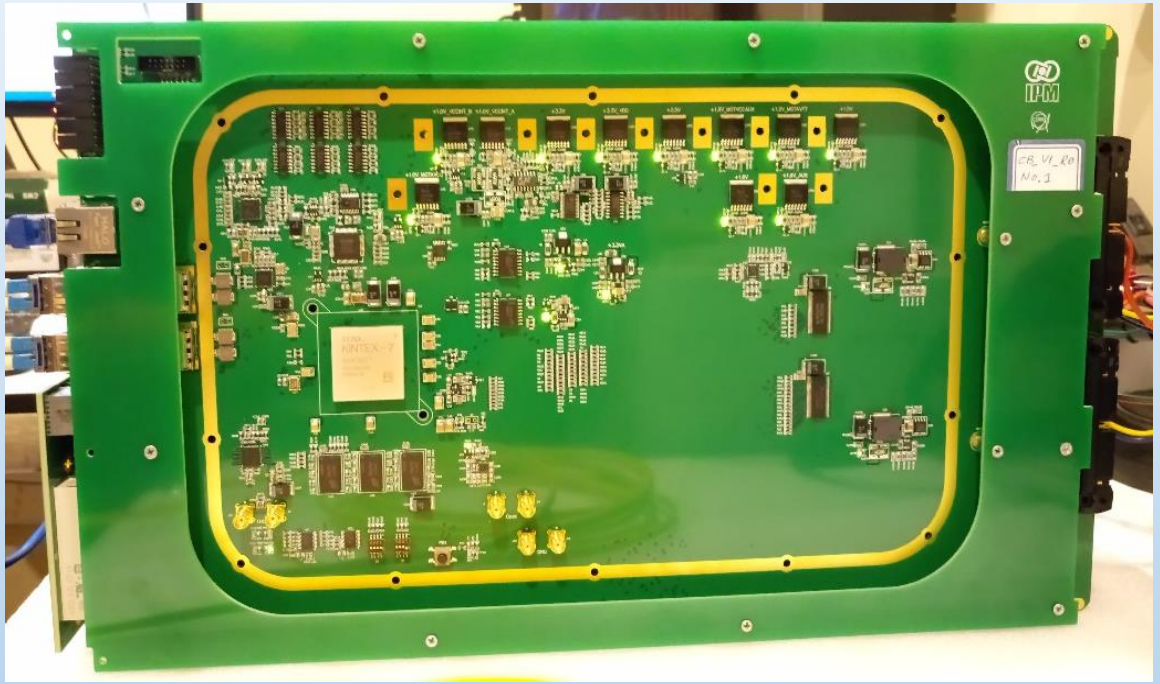
- Link System Front Panel
- 16 Layer PCB
- Board will be cover by an insulator layer

Hardware Prototype of New Link Board (V2.R1)



Control Board

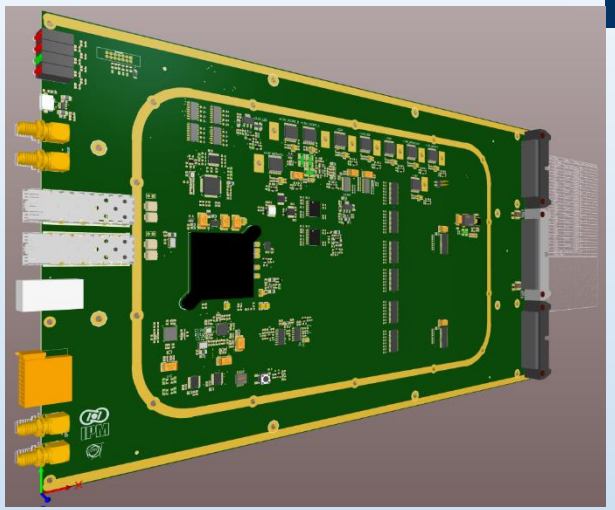
1. 14 Layers PCB – FR4
2. The only bridge between RPC backend electronics and Link Boards
3. Optical Links to receive TTC, Fast, and Slow commands. GBT-FPGA link driver.
4. TTC clock and Fast BGo commands, BC0
5. TTC Clock Phase shift adjustment
6. FEB Parameter Configuration and Verification.
7. Control and monitor the Link Boards Histograms, Data Logs, and Diagnostics through the front panel bus.

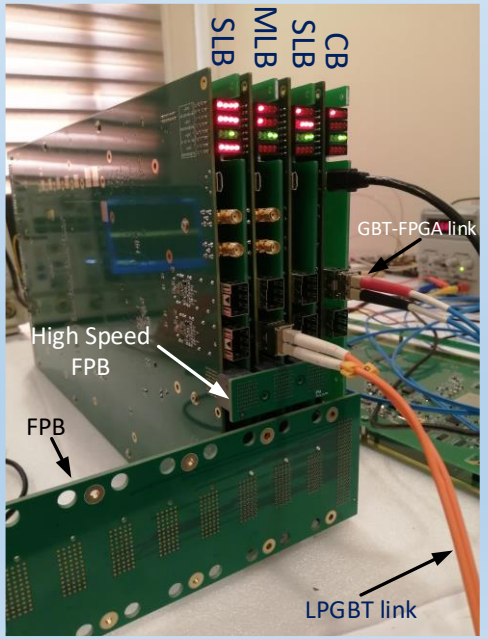


Hardware Prototype of New Link Board (V2.R2)

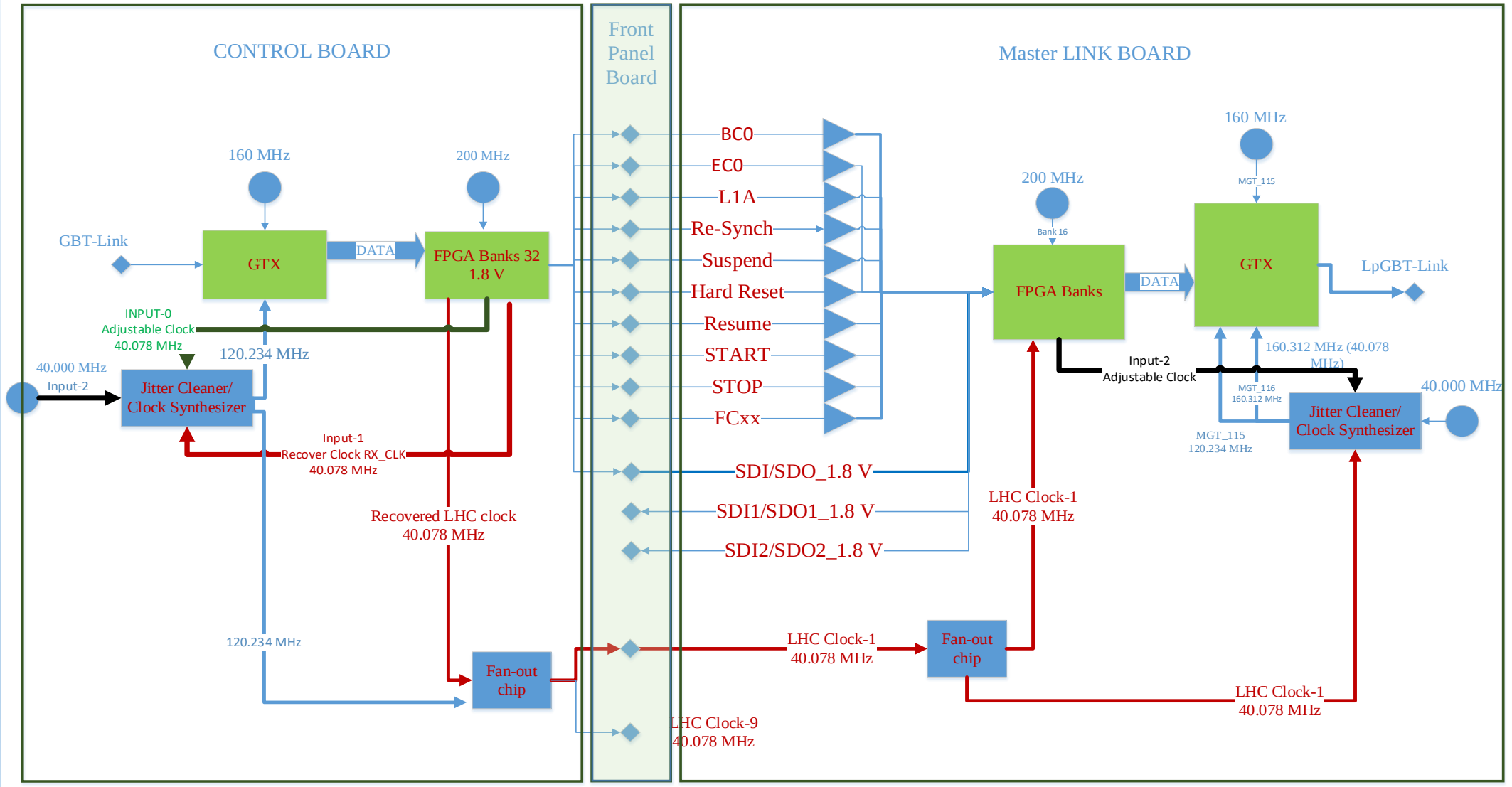
Link system final Version:

- Based on the ESR/PRR recommendations (Nov. 2022) and our experience especially from irradiation test at CHARM, a few modifications applied to the electronics:
  1. PCB Material changed to Halogen-free.
  2. To optimise power consumption from 12 W to 8 W, some unnecessary components were removed
     1. Ethernet interface
     2. DDR3 Memories
     3. Optimized Voltage regulators
     4. Two of six front-panel diagnostic LEDs
  3. The Link system clock chain was modified for more flexibility in measuring the TTC and BC0 latency.
  4. An Analogue Watchdog Supervisor (AWS) is added to recover electronics from the link loss failure.
  5. A large front panel connector (125-pin) was replaced with a smaller one (55-pin). It helps to shrink the size of the front panel board and prevent any damage during the system assembly by the technicians at P5.





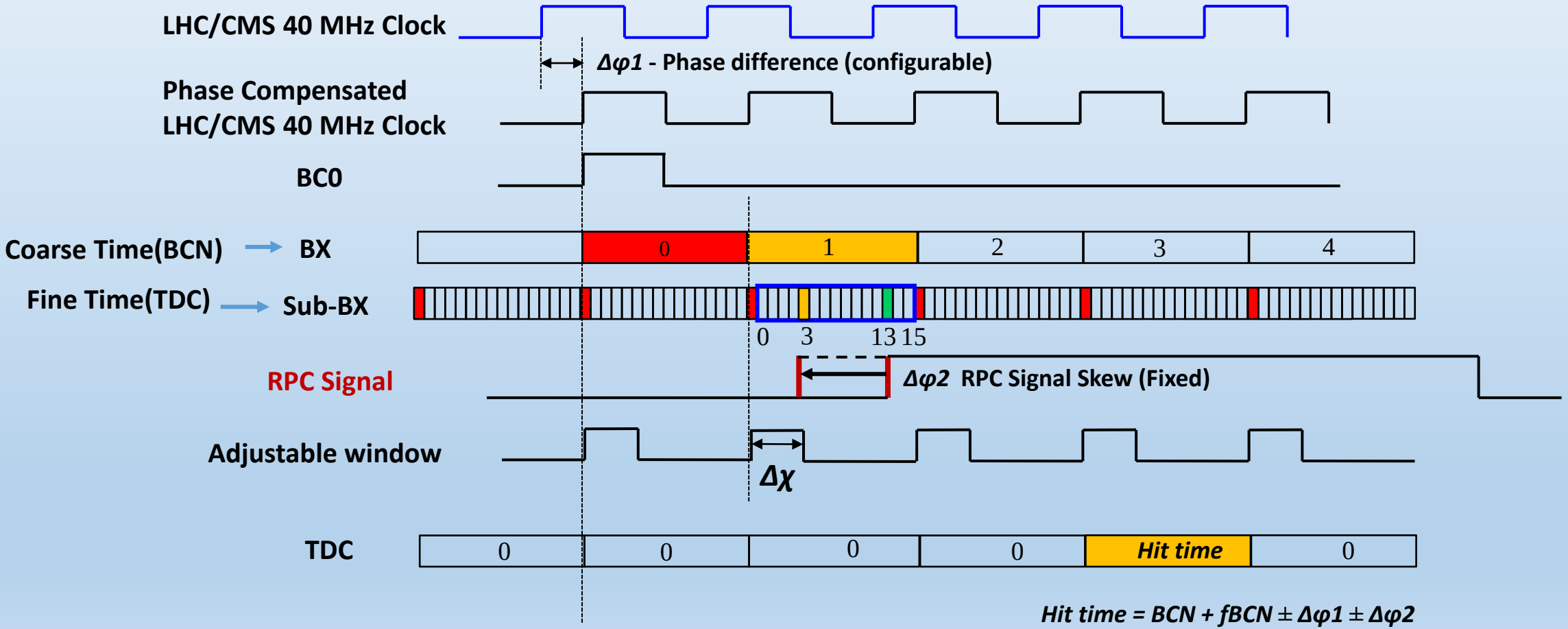
Link System Clock distribution Scheme (modified)



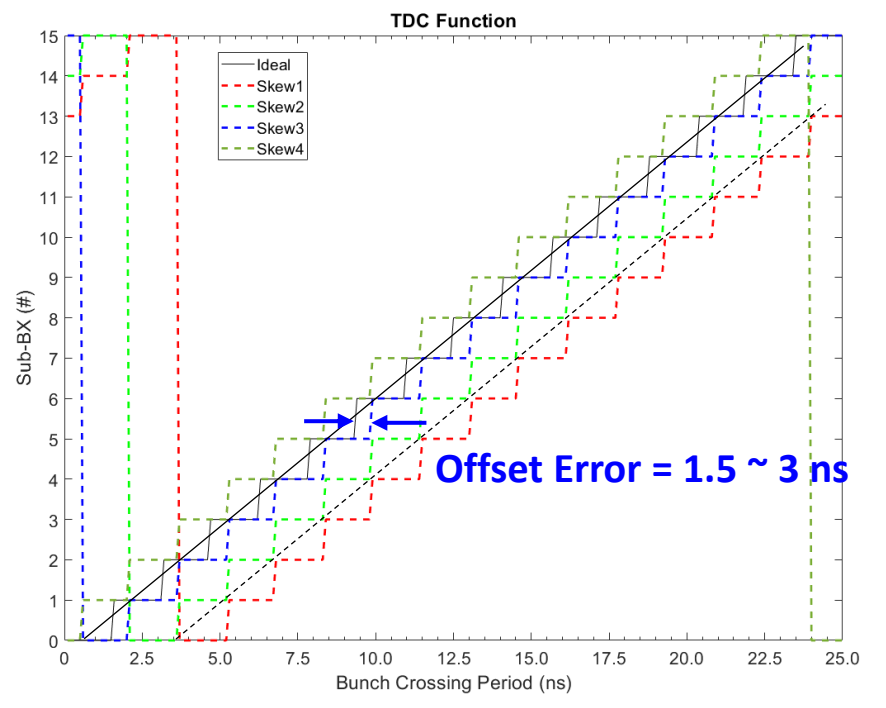
Time-Stamping

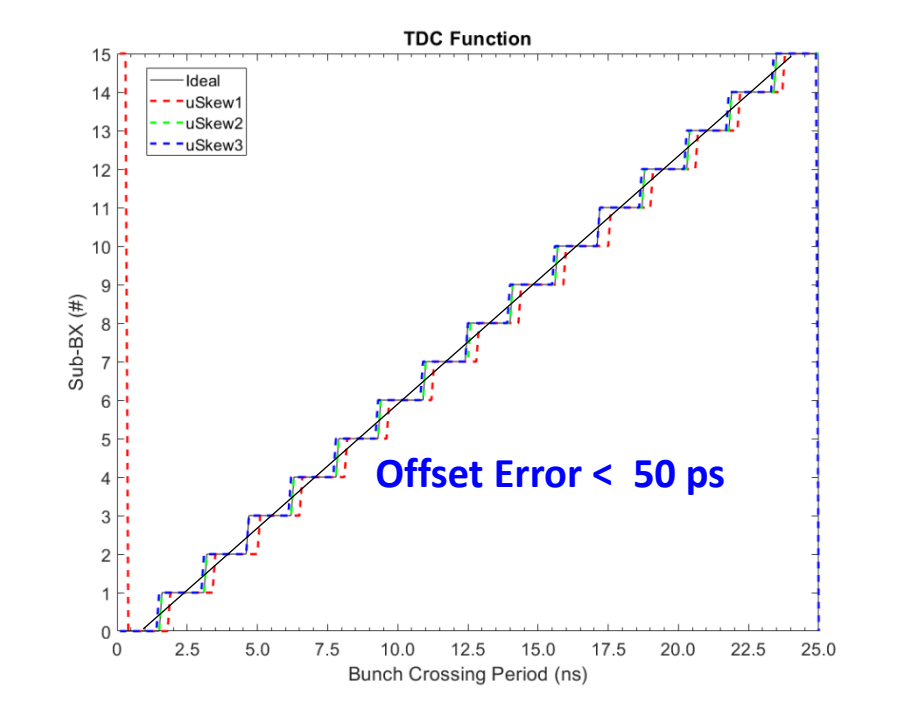
- **RPC signals time Stamp**

  The first step of the RPC signal processing is the measurement of RPC signal arrival time and assignment of this data to the phase compensated LHC/CMS clock (40 MHz).



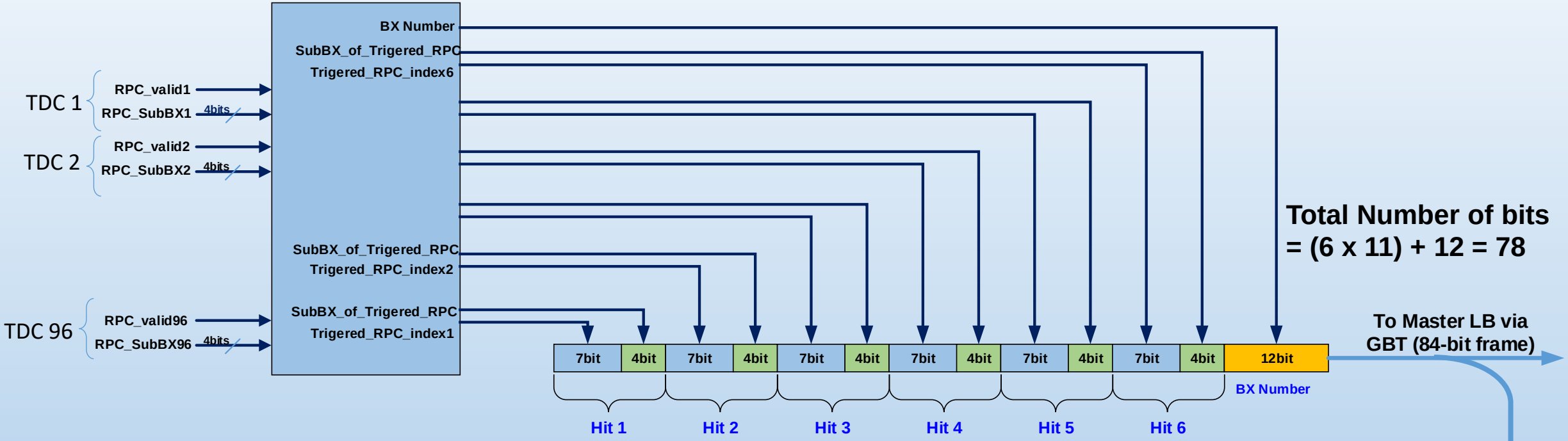
Time-Stamping – TDC Transfer Function



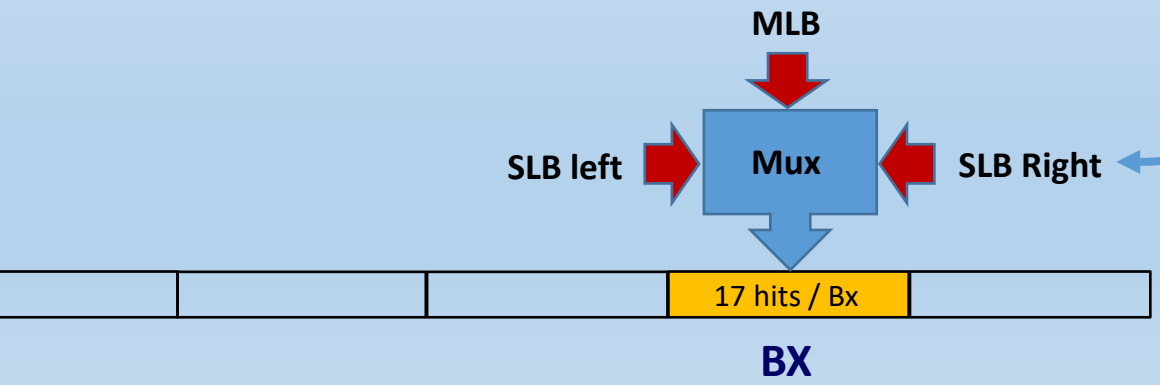


- ✓ **TDC resolution is 1.56 ns. The gain error is zero but the offset error is not.**
- ✓ **TTC clocks and RPC hit signals have delays w.r.t the origin of the LHC clock. This cause a fixed offset error on the TDC transfer function.**
- ✓ **In Link Board, the TDC data is compensated with two parameters; 1) Macro steps: 1.56 ns, and 2) Micro steps: 48 ps. Figure left, Macro step offset error compensation, and Figure right, Macro + Micro steps offset error compensation.**

Data Collector, Multiplexing, and Transmission



- Data of UP to **6 fired strips (activated channels)** are transmitted per BX clock cycle.
- Bursts with up to **42 activated channels** can be transmitted without data loss.
- In Burst cases, channel data are transmitted with a delay.



RPC Signal and Data processing – Data Transmission

- **Frame structure**

Hit-1 … Hit-6

Item	Header + FEC	No. Strip (1..96)	Sub-bx	…	No. Strip (1..96)	Sub-bx	…	No. Strip (1..96)	Sub-bx	…	BCN MLB	BCO SLBR	BCO SLBL
Bit	22	7	4	…	7	4	…	7	4	…	12	6	6

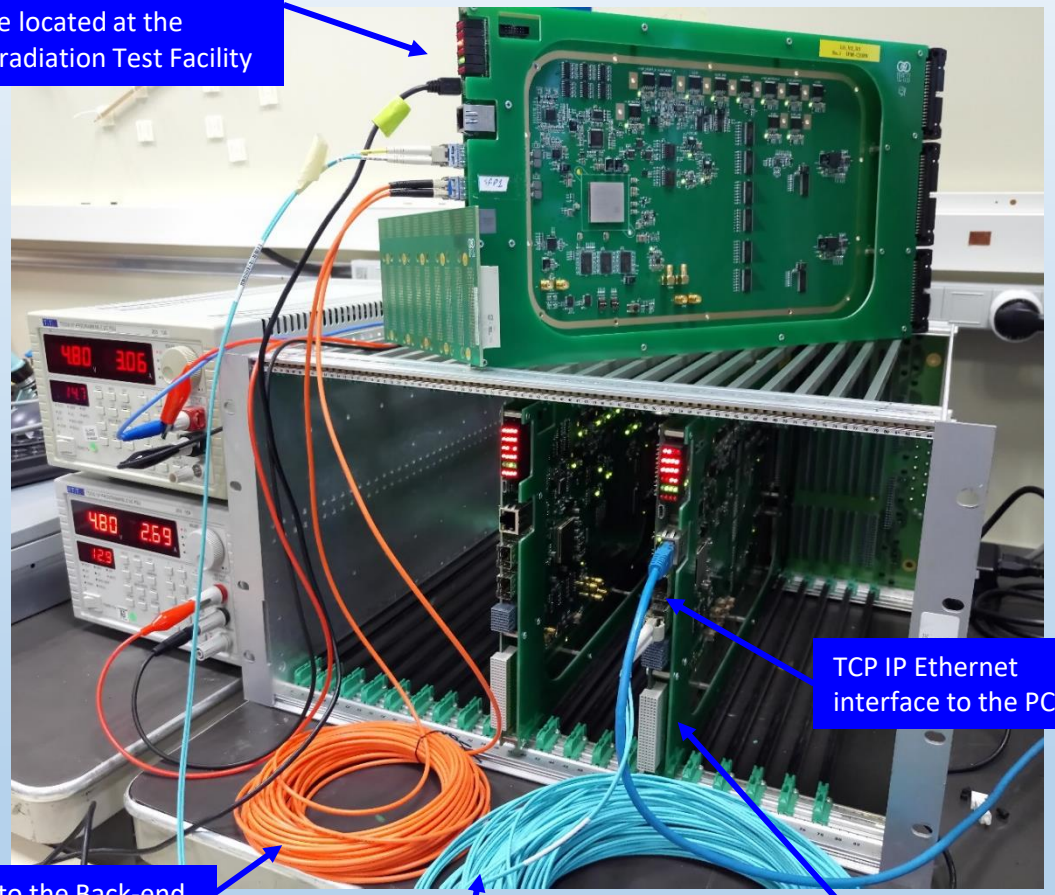
SLB Right (66 bits) MLB (66 bits) SLB Left (66 bits)

- **Frame Fields**
  - **Overhead electronics: Header** (2 bits) + **FEC** (20 bits)
  - **Hit information:**
    - **The number of fired strips could be between strip no. 1 to strip no. 96. Size of this field is 7 bits.**
    - **The Sub-BX** or fractional part of the hit time of a fired strip. The size of this field is 4 bits.
  - **Master LB Bunch Crossing:** Sets as a reference and keeps in the **BCN MLB**.
  - **Bunch Crossing Offsets:** The Bunch crossing in **the Slave LB Right and Left** has an offset w.r.t the Master Link Board bunch crossing. These offsets keep in the **BCO SLBR/SLBL** fields.
  - **Frame size:** 256 bits
  - **Total Number of data bits:** (3 x 66) + 12 + 6 + 6 = 222 bits

Preparation for Irradiation test in Cern 904 Lab

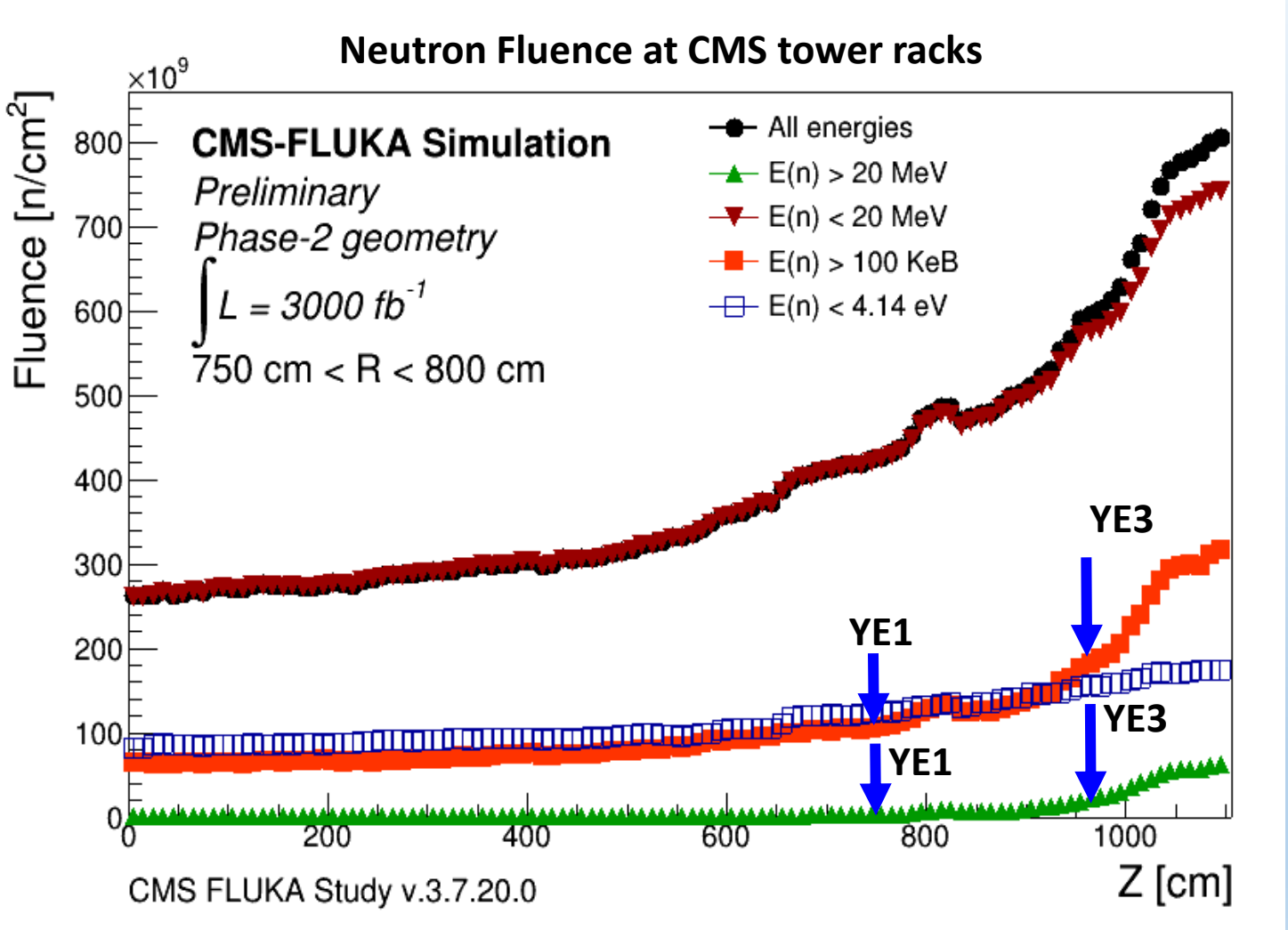
❑ June/July 2022: Preparation for Irradiation Test

- ✓ **Link System Test Setup was tested at 904 Lab.**
- ✓ **System fully stable, responsive during 8 hours continuous run.**
- ✓ **Cold Test was passed. Error injection to the FPGA was done and every errors (virtual SEU) were detected and corrected by FPGA SEM IP core.**



Radiation Consideration in HL-LHC

- **Link System will install on the CMS Tower racks.**
- **Among all racks, the ones in front of the YE3 and YE1 are at higher exposure.**



Epithermal Neutrons Fluence at YE3 tower racks
< 1.6 x 10^{11} n/cm²

20 MeV neutron Fluence at YE3 tower racks
< 2 x 10^{10} n/cm²

Radiation Consideration in HL-LHC

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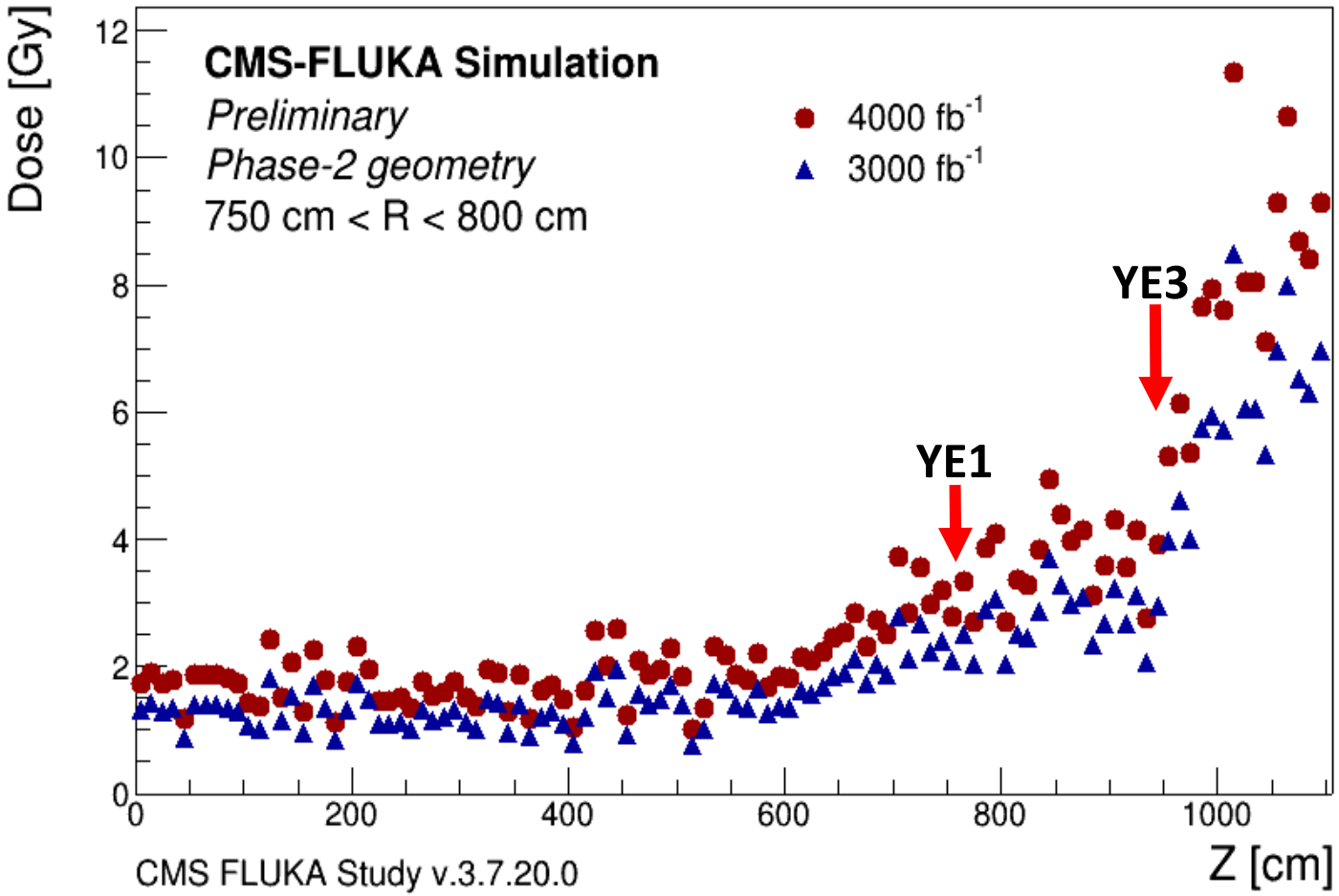
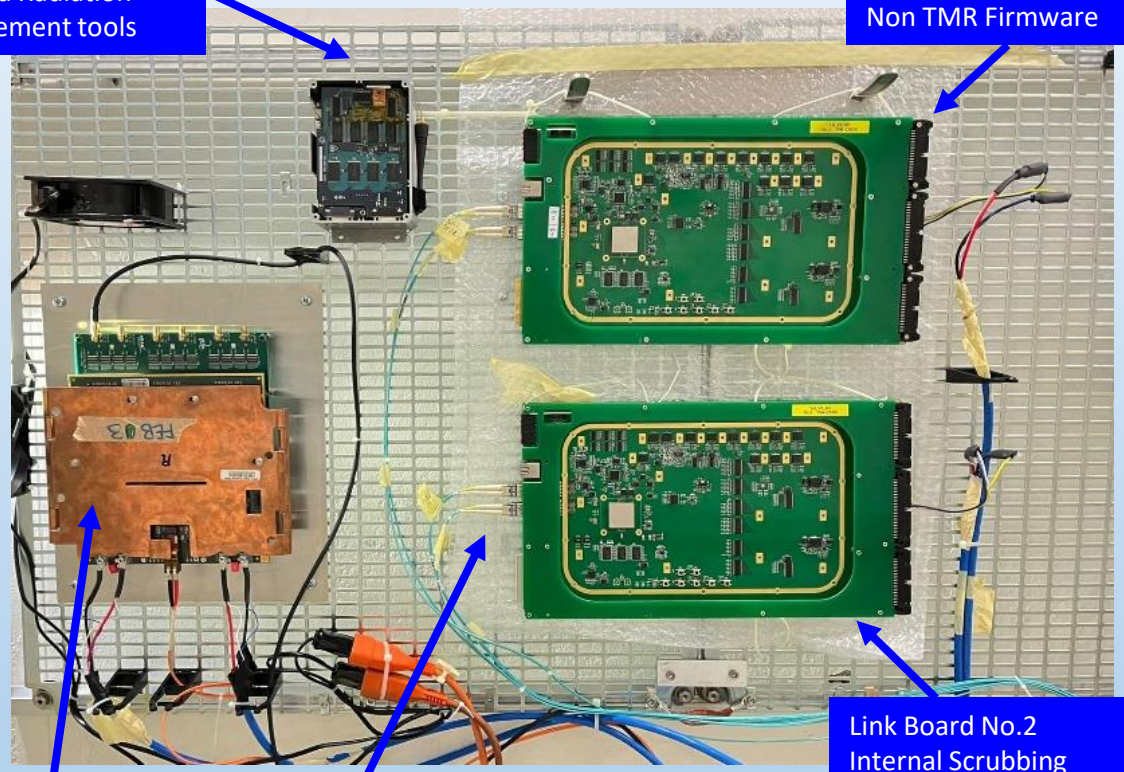


Integrated Dose at YE3 tower racks < 6 Gy

Irradiation Test Setup in CHARM

❑ Oct. 12-Nov. 1st: Irradiation Test for 3 weeks

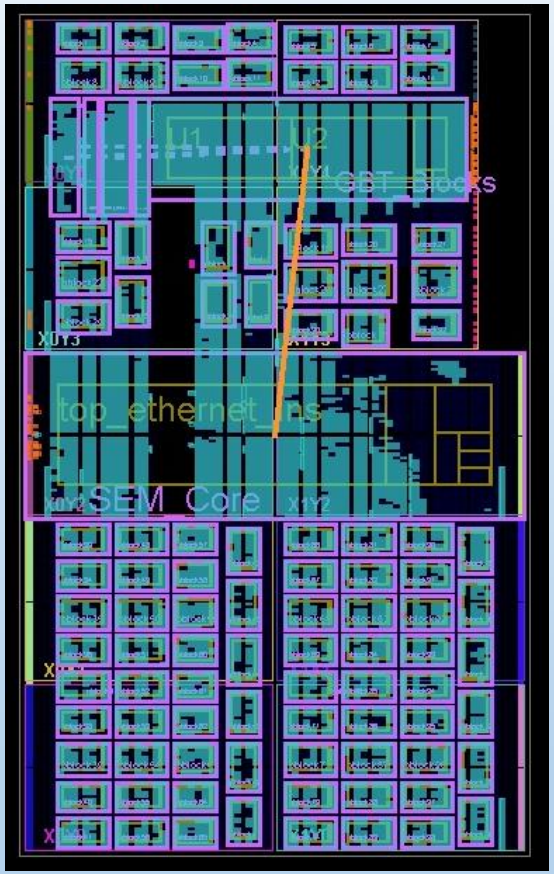
- ✓ CHARM location G0
  - ✓ TID: 3.45 Gy/Day
  - ✓ Thermal neutron flux: 2.7×10^5 (cm^{-2} s^{-1})
  - ✓ High energy hadron flux: 1.4×10^5 (cm^{-2} s^{-1})
- ✓ Target for 10 years HL-LHC
  - ✓ 4000 fb^{-1}
  - ✓ Location of Installation on CMS tower racks
  - ✓ TID < 6 Gy
  - ✓ Total High and Low energy neutron flux < 1.8×10^3 (cm^{-2} s^{-1})
- ✓ Hardware Test Setup on the Charm
  - ✓ Two Link Boards is chosen for this test.
  - ✓ Link Board and Control Board is designed based on the same electronics devices and their circuits are very similar above 90%. For this reason, we decided to test only Link Boards.
  - ✓ Each board has a redundant optical Links and an Ethernet interface (added in week 3rd of the test)
  - ✓ In the Link System, Loss of connection is consider as a failure



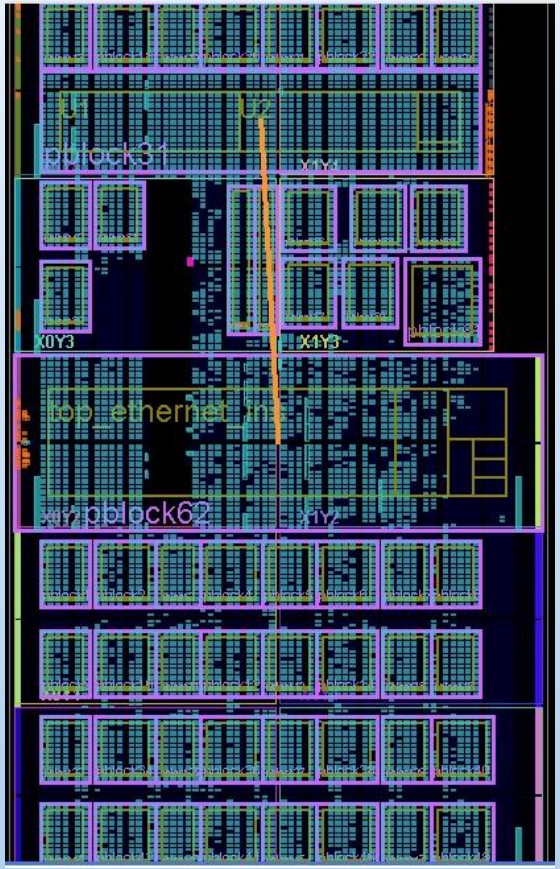
✓ CAEN power module, set a limit on the current to see the over-current and record the latch-up

Irradiation Test – FPGA Firmware

- Link Board firmware covers almost all logics and primitives expected to be used for HL-LHC.
- We have evaluated two mitigation techniques on the Link Board FPGAs (Kintex-7 XC7K160T):
  - Non-TMR + Internal Scrubbing (SEM)
  - TMR + Internal Scrubbing (SEM)
- In both firmware, a test logic block has been replicated over the entire FPGA to increase the chance of the SEUs and precisely evaluate the mitigation methods.
- Ninety-eight test blocks are implemented on the non-TMR firmware, and 37 TMRed test logic blocks are replicated on the TMR firmware.
- Additionally, both firmware comprises two modified GBT-FPGA lanes, automatic link loss detection, and swapping, an Ethernet interface, Clock recovery and Jitter cleaner, and an SEM controller.



Kintex-7, TMR + Internal Scrubbing



Kintex-7, non-TMR + Internal Scrubbing

Irradiation Test – Results

- ✓ No over-current appeared during the test.
- ✓ No permanent damage nor performance degradation detected on the electronics.
- ✓ Electronics test results are fulfilled the HL-LHC requirement with following safety factors:

❑ Oct. 12-Nov. 1st 2022: Irradiation Test Results

- ✓ Electronics running for over three weeks
- ✓ The CHARM dosimetry document Link
- ✓ Total integrated dose (TID): 56.9 Gy
- ✓ Total HEH fluence (cm-2): 1.62 e11
- ✓ Total ThN fluence (cm-2): 3.34 e11
- ✓ No latch-up has been seen on the entire electronics
- ✓ Expected #SEU in FPGA CRAM per minutes: 22.1
- ✓ Expected #SEU in FPGA BRAM per minutes: 2.88
- ✓ Rate of SEU detection and correction by SEM at configuration memory: 0.2 s^{-1} (12 SEU per minute)
- ✓ For the Link Boards, failure is defined as link loss.
- ✓ The power cycling is used to failure recovery
- ✓ MTBF of the Non-TMR firmware + SEM per Link: 250 minutes
- ✓ MTBF of TMR firmware + SEM per link: 250 minutes
- ✓ MTBF extended for HL-LHC condition:
- ✓ $MTBF_{HL\text{-}LHC} = 250\ \text{min} \times \frac{4.23 \times 10^5\ (\text{cm}^{-2}\ \text{s}^{-1})}{1.8 \times 10^3\ (\text{cm}^{-2}\ \text{s}^{-1})} = 40.79\ \text{days}$
- ✓ Redundant links make $MTBF_{HL\text{-}LHC}$ ×2
- ✓ Power Recycling time: 5 sec

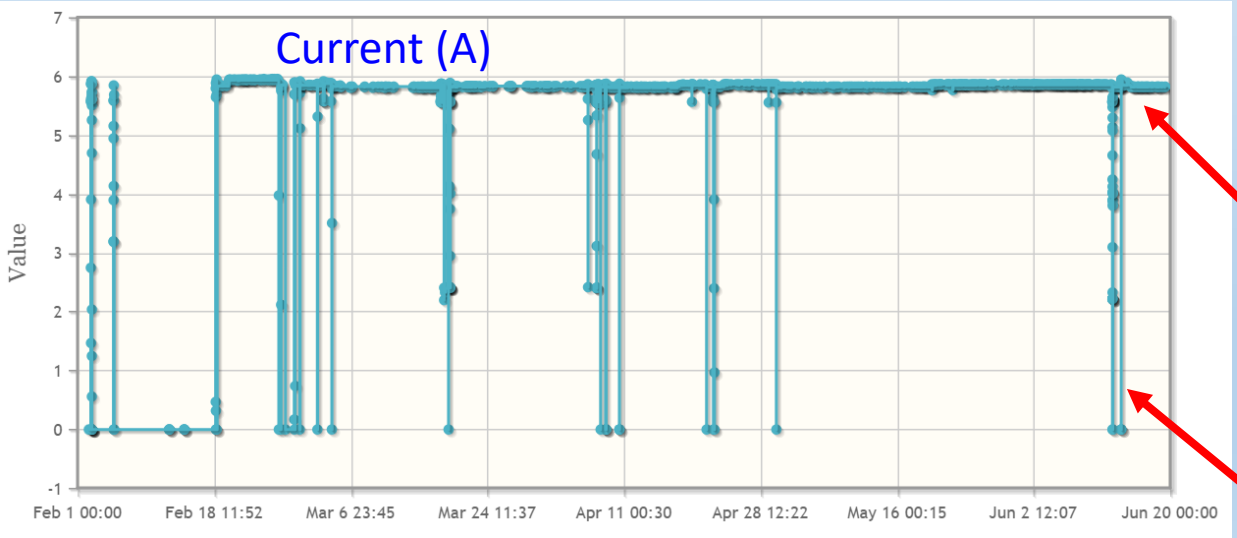
Item	CHARM	HL-LHC	Safety Factor
TID (Gy)	56.9	< 6	> 9.33
Total HEH fluence (cm^{-2})	1.62×10^{11}	$< 2 \times 10^{10}$	> 8.1
Total ThN fluence (cm^{-2})	3.35×10^{11}	$< 1.6 \times 10^{11}$	> 2
Irradiation Flux ($cm^{-2}\ s^{-1}$)	4.23×10^5	1.8×10^3	235
#SEU detection and Correction ($minute^{-1}$)	12	0.14	85
#days between failure	0.17	40.79	
# failure per one HL-LHC year		2.45	
# failure in all HL-LHC years		24.5	
Dead time over HL-LHC (sec)		122.5	

Verification in CMS

RPC Link System status at P5

- ✓ The Link board and Control Board installed on the P5 at the beginning of February 2024 are monitored to see their behavior regarding irradiation, magnetic field, and electrical noises. So far, the Link Board and Control Board are pretty stable in real environmental conditions.

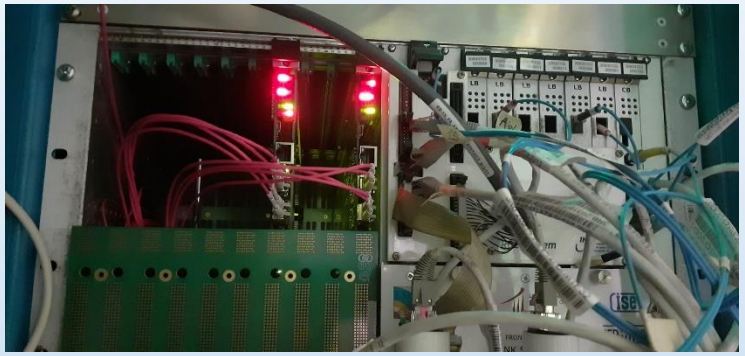
- ✓ The firmware Fine-tuning of the Link Board and Control Board is also in progress using remote programming from Tehran.



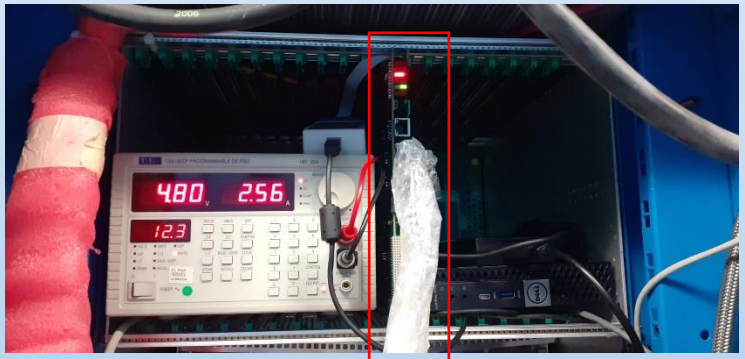
Feb 1st

June 19

New Link System (Left) - Present Link System(Right) Installed at UXC



New Slow Control Emulator located at USC



Stable Current consumption shows stable behavior under real environmental conditions

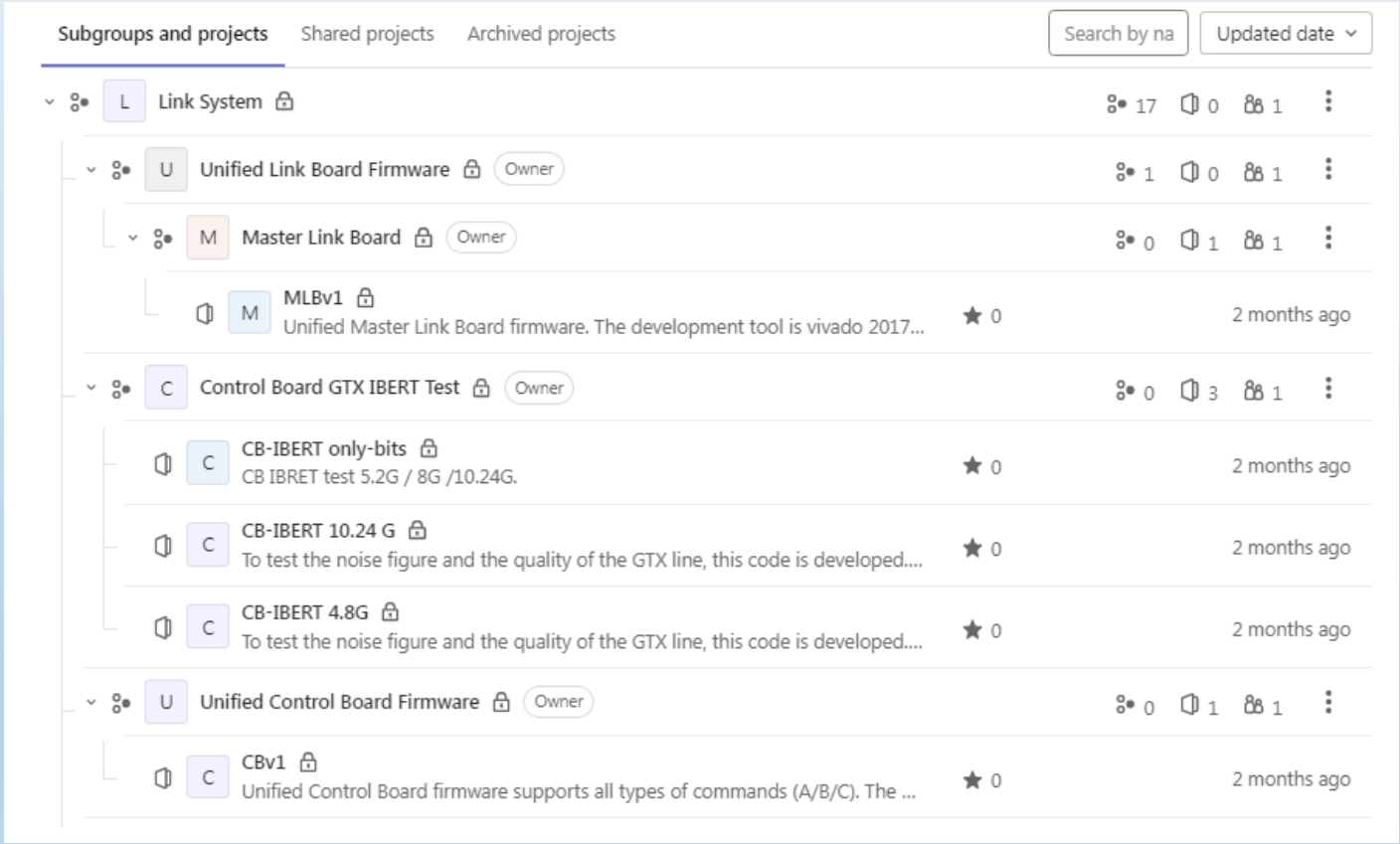
Link System remote programming from Tehran/Cern

RPC Firmware Repository - GitLab

- ***New Link system Firmware***

1. Unified Link Board
2. Unified Control Board
3. Control Board GTX IBERT test
4. Link System Irradiation
5. User Graphic Interface
6. TDC (1.56ns)
7. Diagnostic & Histogramming (LB)
8. GTX and LpGBT transceiver (Xilinx)
9. GTX Fixed Latency data transmission
10. FEB Controller
11. Multi Boot Remote Programming
12. Ethernet LAN
13. DDR3 interface Controller
14. Soft Error Mitigation Engine (SEM)
15. Front Panel Controller
16. TTC Clock Recovery & Phase Shift
17. Jitter Cleaner (State Machine Controller)
18. Control & Diagnostic (CB)
19. Slow Controller Emulator (SCE)
20. GBT-FPGA for the Control Board
21. Triple Modular Redundancy (TMR)

- https://gitlab.cern.ch/cms_rpc_muons_firmware



Summary

- Progress of the Link System Project is well advanced, and Prototypes are finalized.
- Each Board consumes 12 W. Still, there is room for power consumption reduction.
- The latest version of firmware is available on the RPC repository.
- The irradiation test of the Link System is completed, and the results are satisfactory.
- The electronics meet the HL-LHC radiation condition with high safety factors.
- No permanent damage nor performance degradation appeared on the electronics.
- Number of failures per board for 10 HL-LHC years is 24.5, which means 122.5-sec dead time over 10 HL-LHC years. The overall dead time for full system is 168560-sec.
- This number even would be better by using redundant links.
- The project schedule is protected with well enough floating time.

- **Thank you!**

Backup Slides

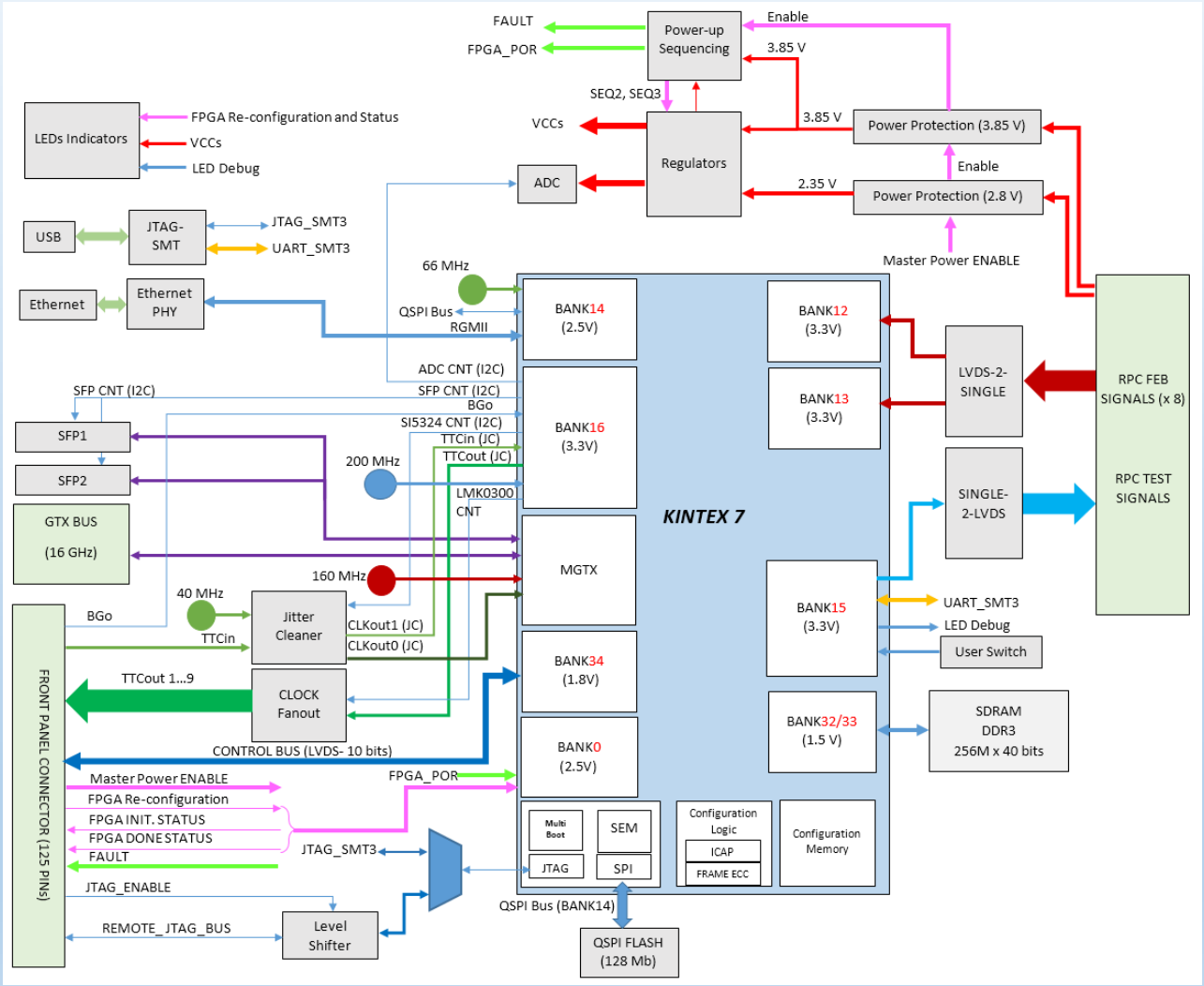
Link Board

1. 14 Layers PCB – FR4
2. 96 Input Channels. 15 kV ESD protected.
3. Twenty-four output channels to inject a signal in the FEB(s) for calibration, a test of the flat cables and connectors.
4. Detector Diagnostic and monitoring:
   a. Full/Adjustable window Histograms
   b. RPC Data logging
   c. Timing Histogram
5. Muon Hit time information with a time resolution of 1.5 ns.
6. Collects 42 hits per Bunch Crossing without any buffer overflow and data loss.
7. Transmit 18 hits per Bunch, Crossing to the L1T through a 10 G optical Link.

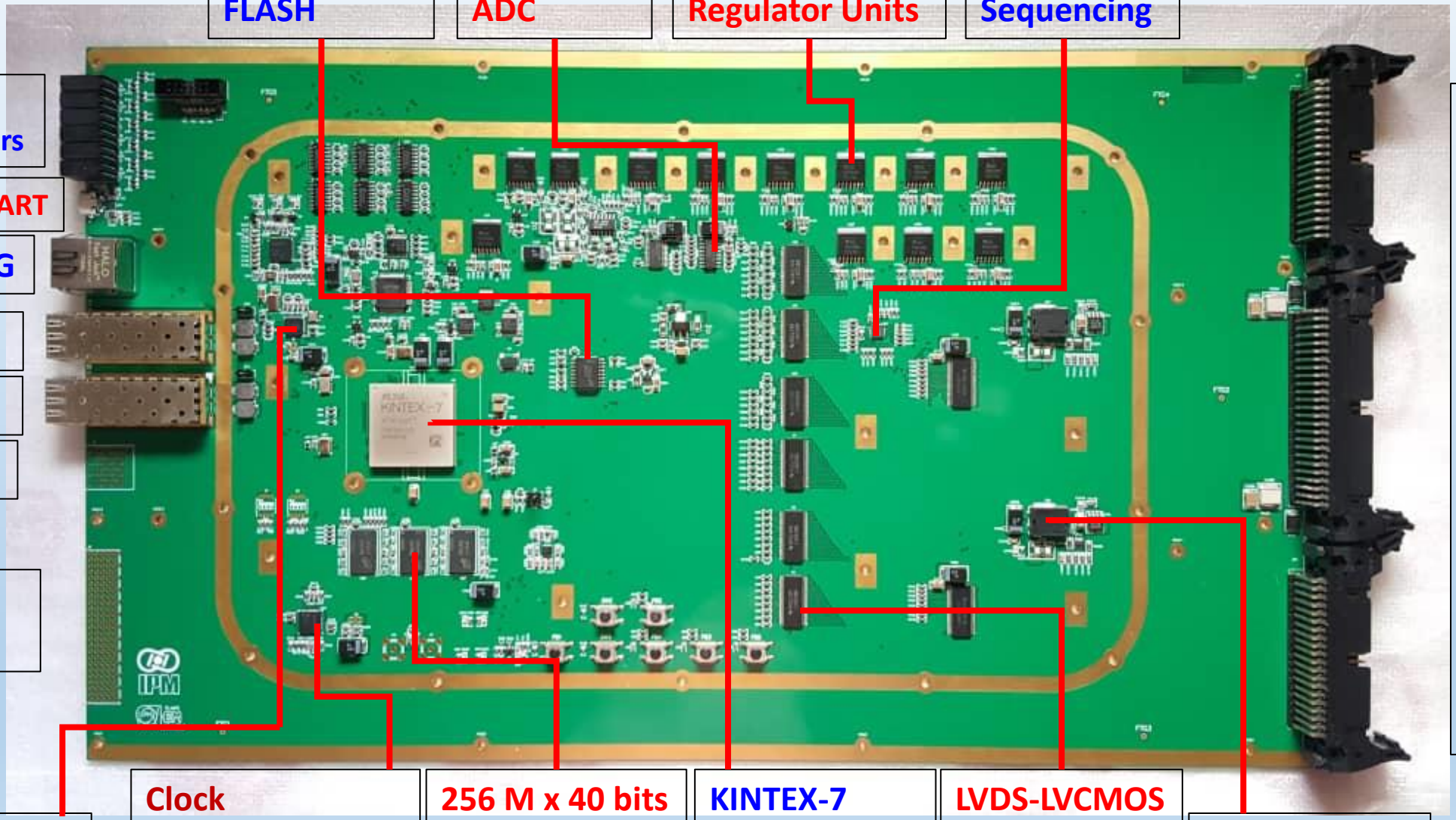
New Link Board Hardware Architecture

- **The design specifications and components:**

1. **FPGAs are KINTEX7, XC7K160T-2FFG676I.**
2. **Fully support 10.3 Gbps data transmission. FPGA Chip is equipped with a heat sink.**
3. **High-resolution TDCs (at the steps of 1.56 ns) implemented into the Kintex7 FPGA**
4. **Two Redundant optical data transmission lines at the data rate of 10.24 Gbps**
5. **Ethernet link for the debugging and onboard JTAG programmer**
6. **256 M x 40 bits of SDRAM-DDR3 for data buffering and debugging**
7. **Data transmission with adjacent slave link boards through the SAMTEC back-plane type connector with a bandwidth of 16 GHz and front panel PCB board.**
8. **Radiation Mitigation is based on Triple Modular Redundancy (TMR) techniques and Soft Error Mitigation (SEM) IP core from Xilinx.**
9. **Voltage Regulators selected from low dropout linear regulator families have already been tested under radiation.**



Hardware Prototype of New Link Board(V2.r0)



Hardware Prototype of New Link Board (V2.r1)

External SPI FLASH

External ADC

LV Linear Regulator Units

Power-up Sequencing

Front Panel LED Indicators

USB JTAG/UART

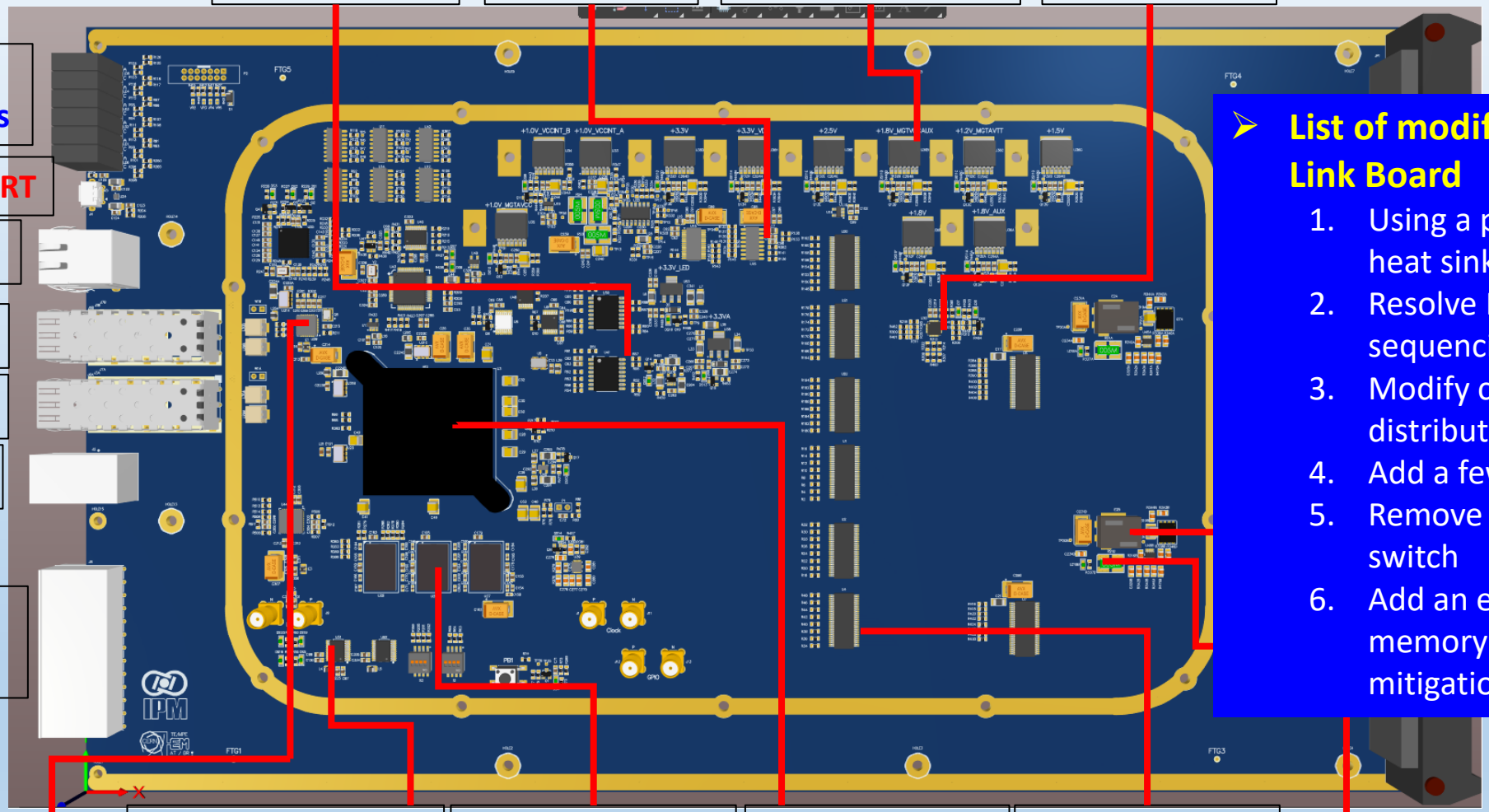
Ethernet 1G

SFP+ (10G)

SFP+ (10G)

GTX BUS

Low speed BUS



- **List of modification on Link Board**
  1. Using a proper size of heat sink
  2. Resolve Power-up sequencing issue
  3. Modify clock distribution schema
  4. Add a few SMAs
  5. Remove user micro switch
  6. Add an extra Flash memory to make a SEU mitigation very fast

Jitter Cleaner

Clock Distribution Unit

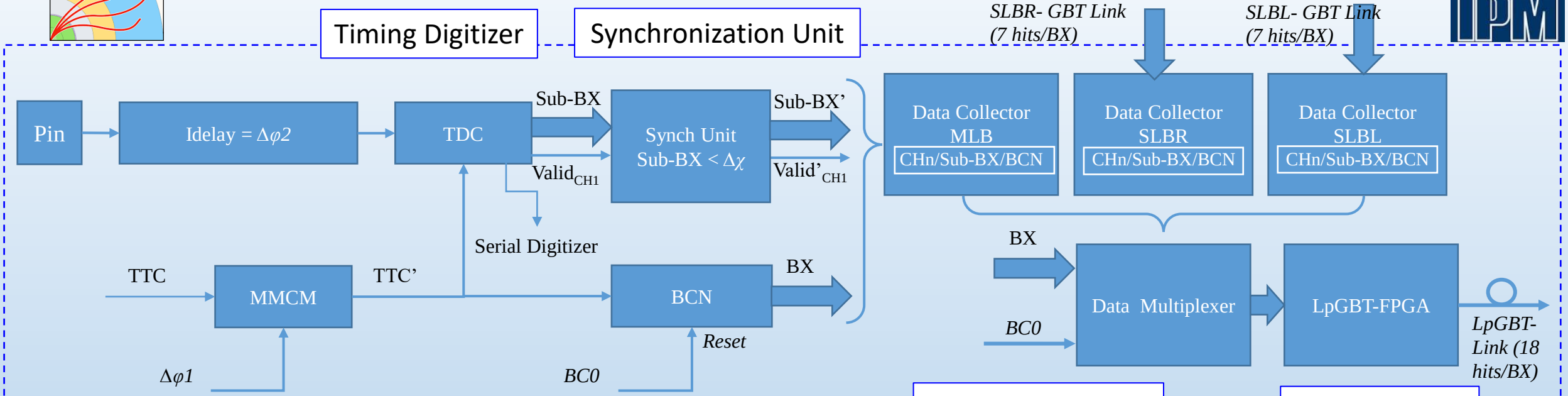
256 M x 40 bits DDR3

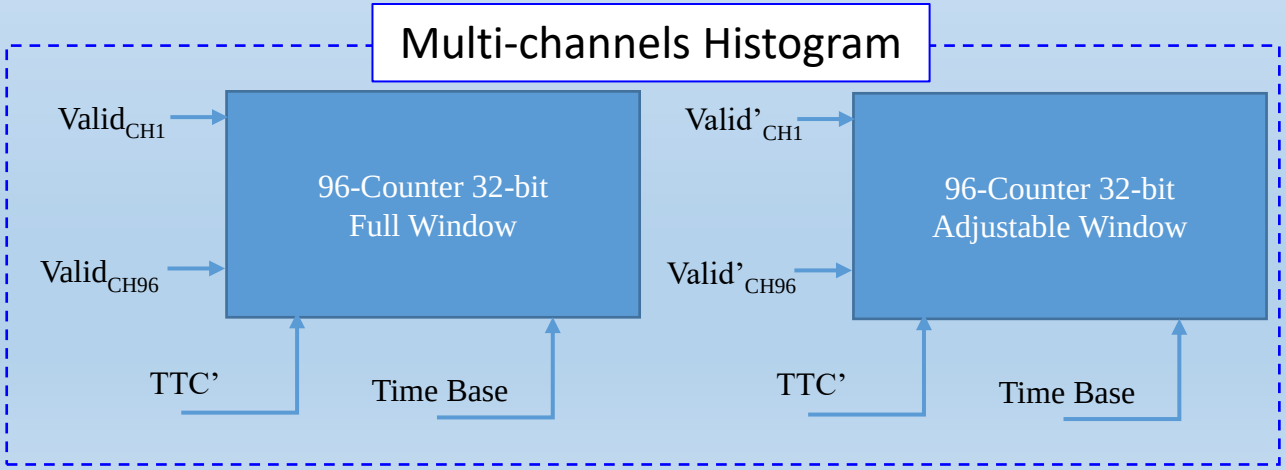
KINTEX-7 (XC7K160T-2I)

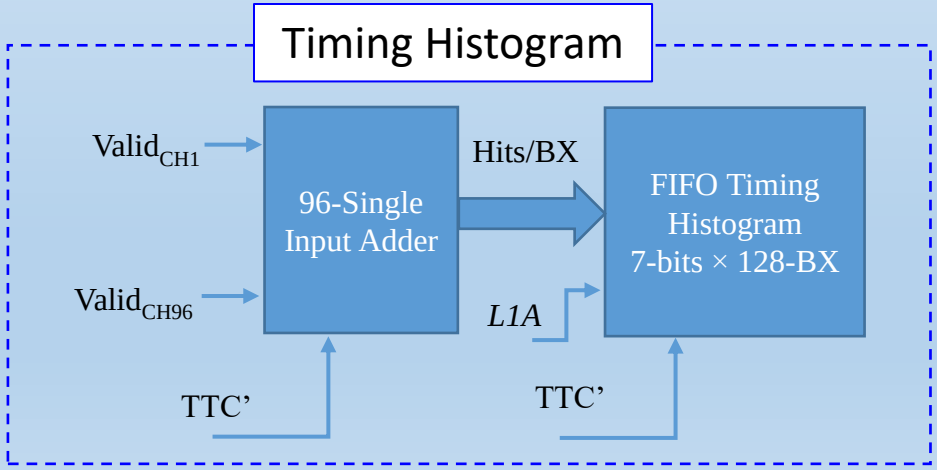
LVDS-LVCMOS Converters

LV Protection

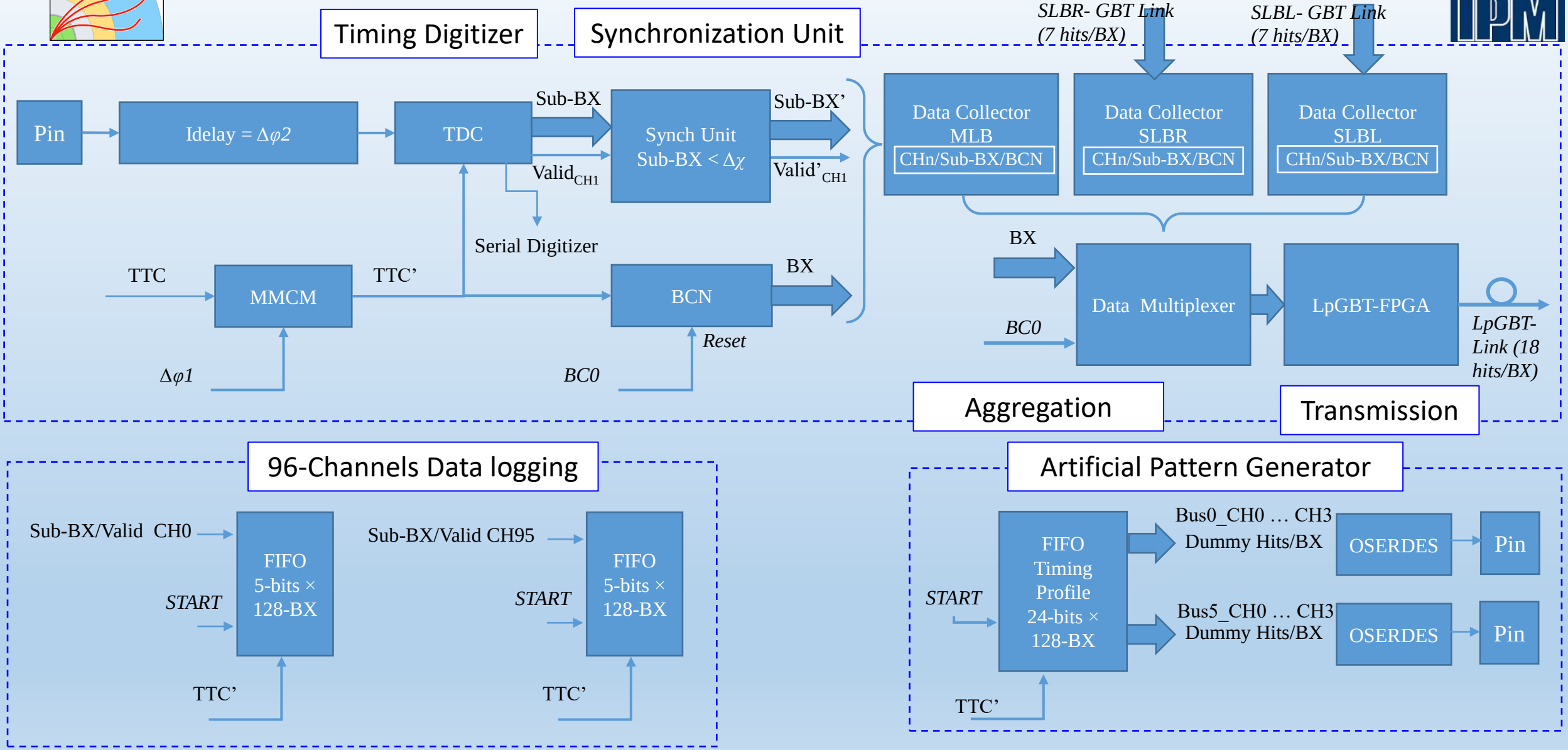
RPC data processing - RPC signal time tagging



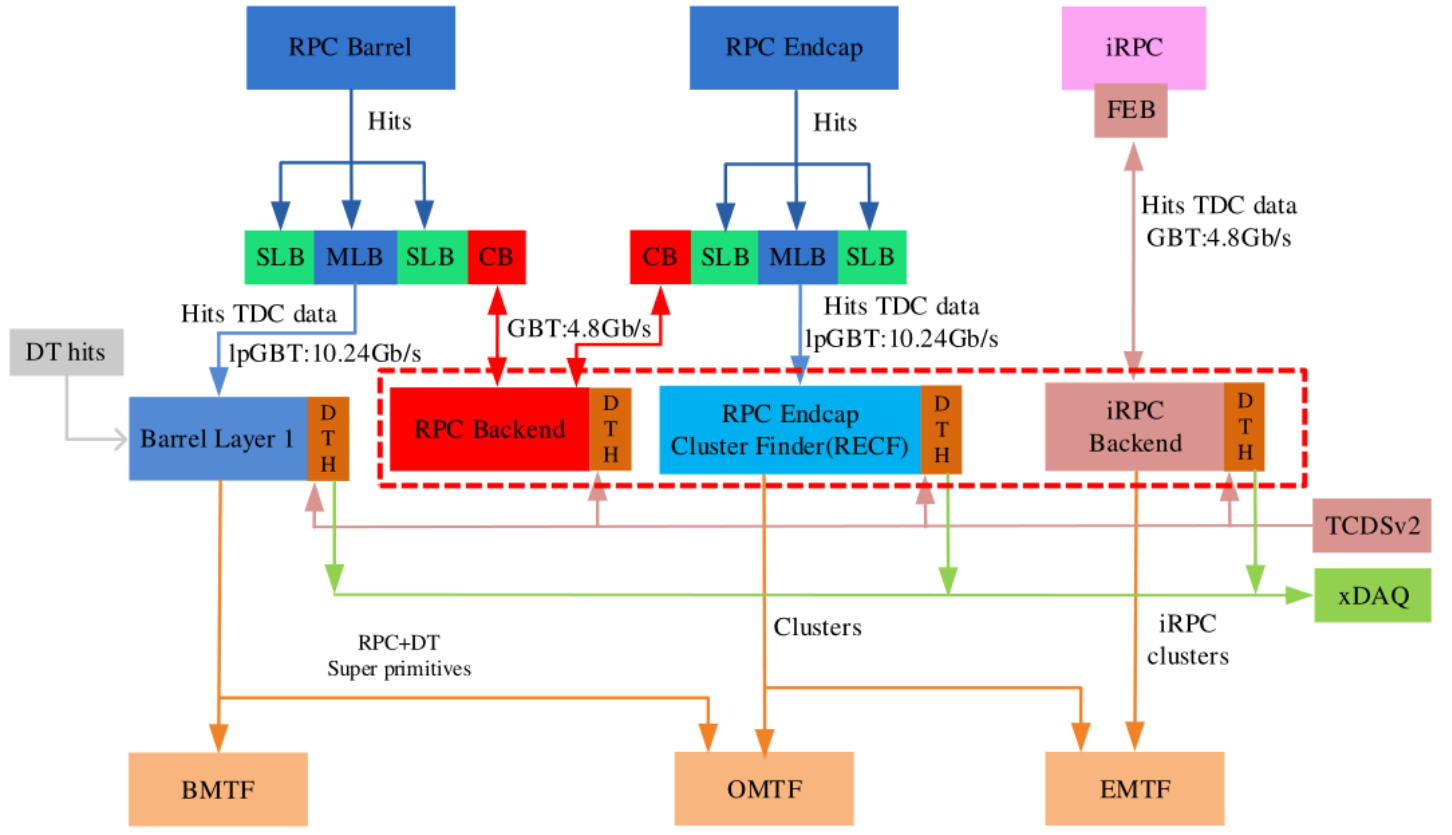


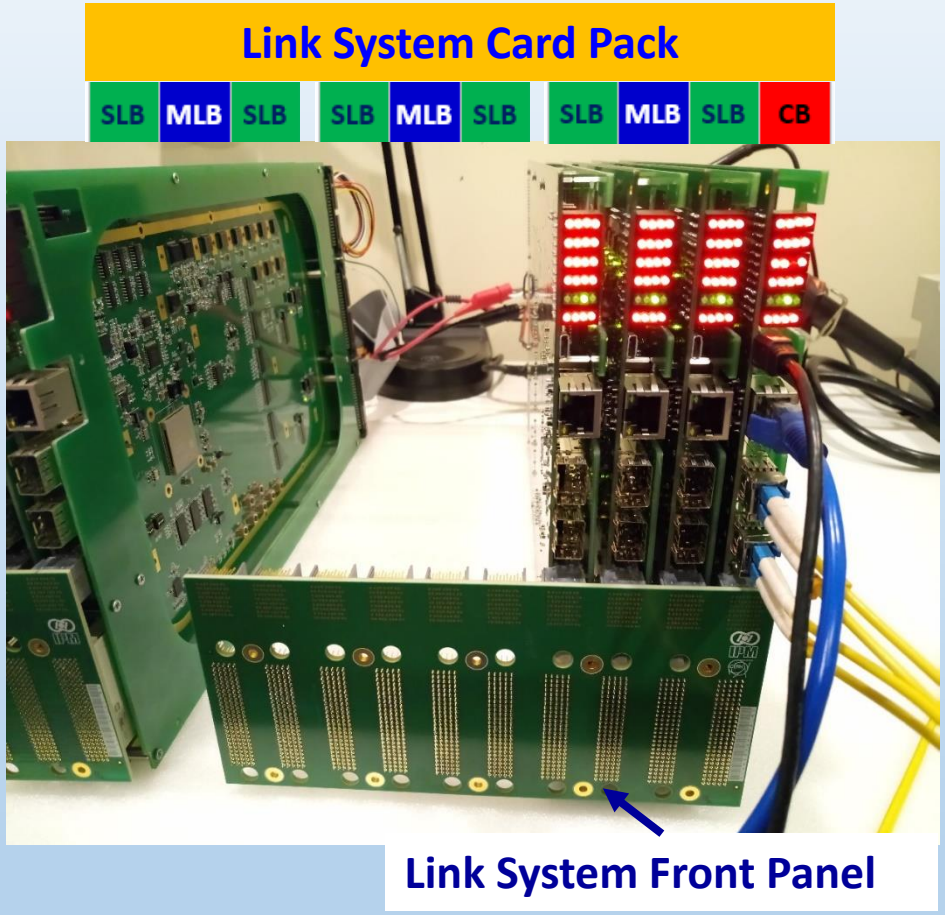


RPC data processing - RPC signal time tagging



RPC Phase-2 Upgrade Architecture and Layer-1

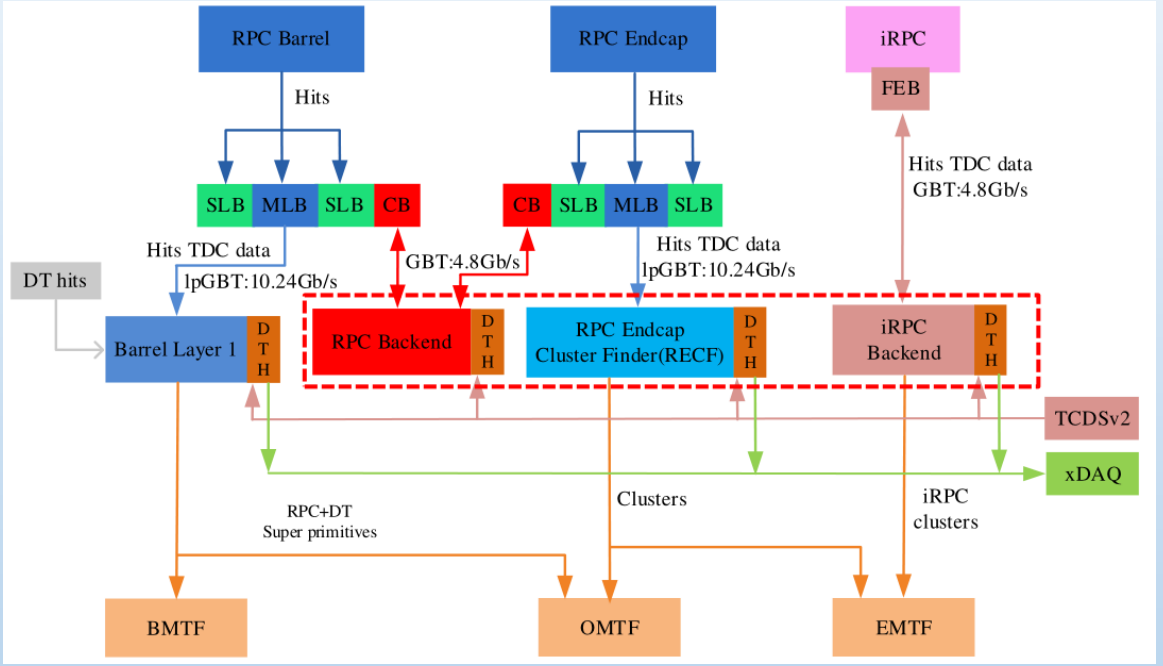




SLB: Slave Link Board
MLB: Master Link Board
CB: Control Board
B/O/E MTF: Barrel/ Overlap/ Endcap Muon Track Finder

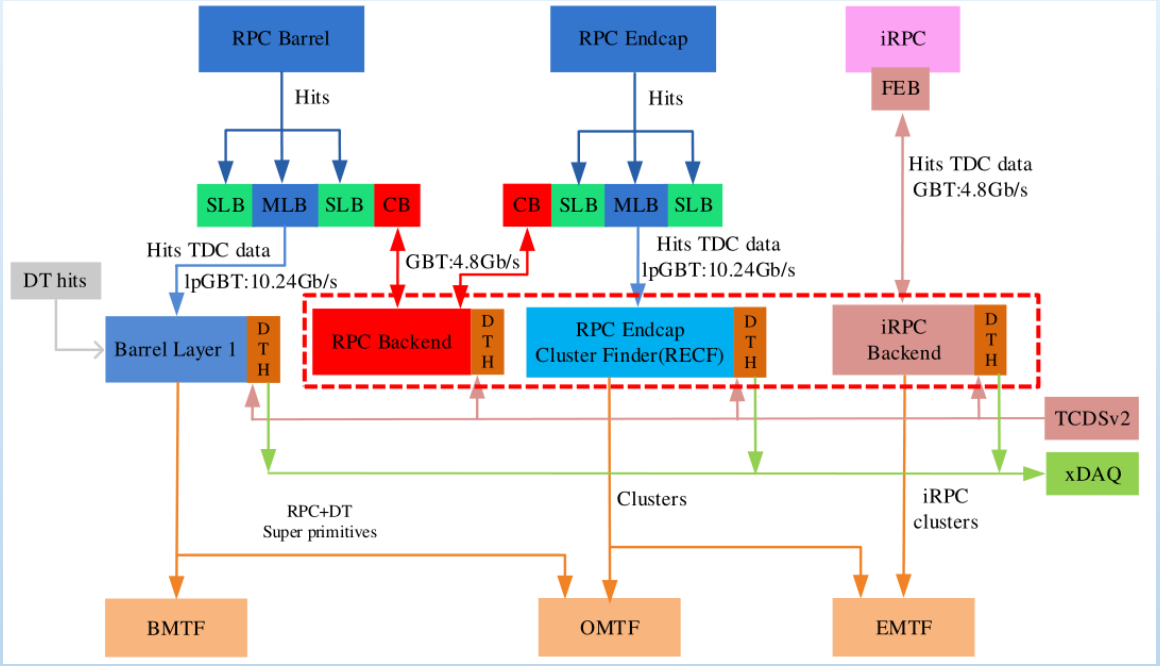
RPC LB Link structure

- Latency
  - RPC + Cable = 9 BX,
  - LB = 11-20 BX,
  - Fiber 110m = 22 BX.
- Optics
  - Standard Short Range 10G-SR-SFP+.
  - Fiber type = OM4.
- Protocols (low-level data)
  - Optical encoding (bits) = FEC 5.
- General Frame specs
  - Size = 256 bits
  - Header = 2 bit.
  - FEC5 = 20 bit.
  - User data = 234 bit.



RPC Link structure in the Barrel

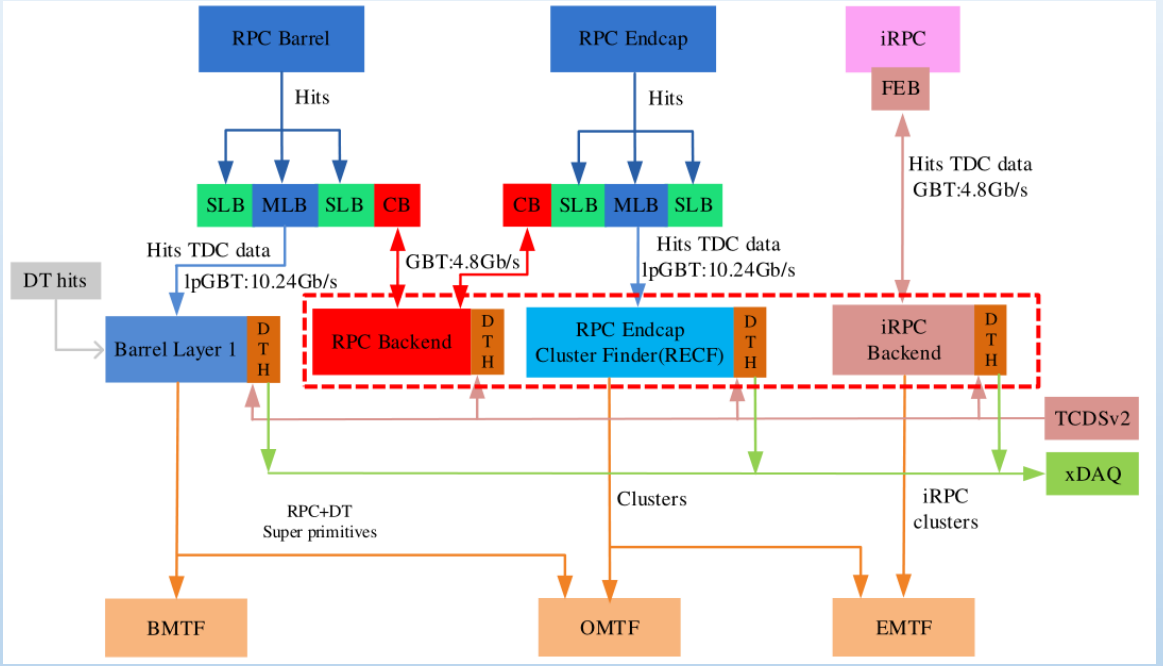
- The link between RPC to BMT-L1
  - one-way direction.
  - Total number of Links = 300.
  - Number of links per sector = 5.
  - The link bandwidth = 10.24 Gbps.
  - Data transmission Protocol = LpGBT.
  - Firmware = Customized version of LpGBT-FPGA.
  - Type of data synchronization = Asynchronous.
  - Type of FEC = FEC 5.



- Object
  - Object name = hit.
  - Object size = 11 bits.
  - Object fields name = Fired Strip number (7 bits), Sub-BX (4 bits)

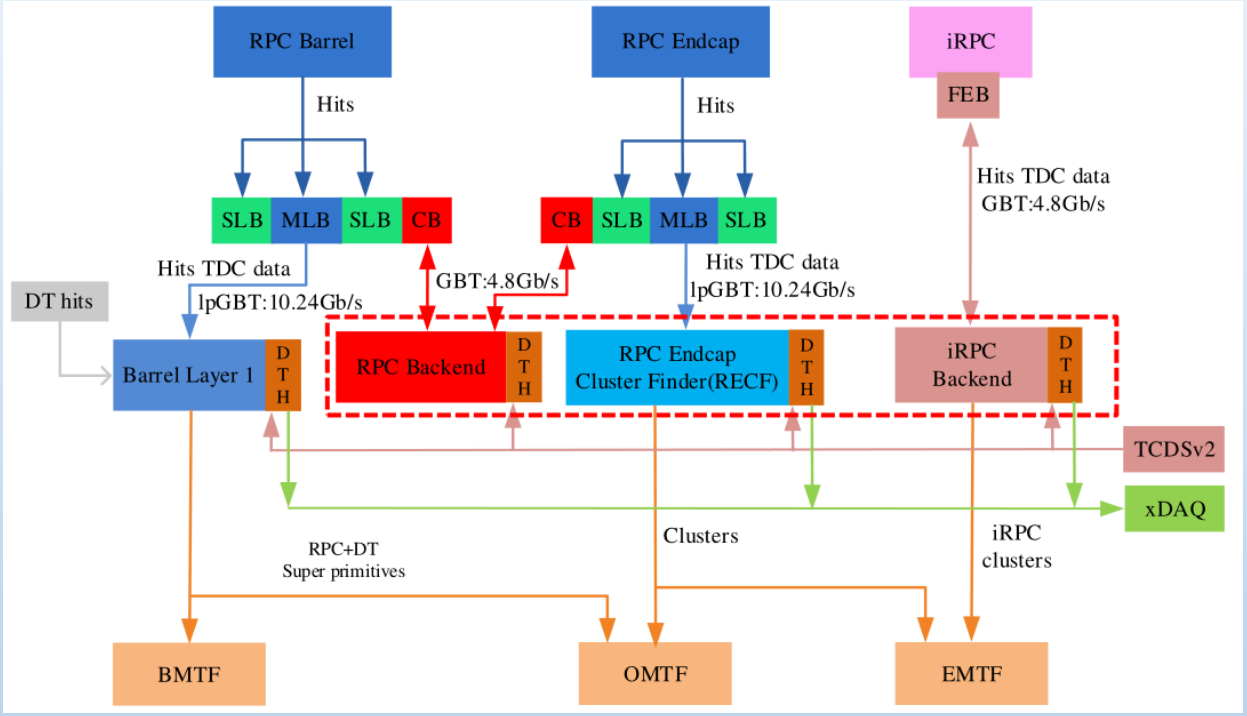
RPC Link structure in the Endcap

- The link between MLB to RECF
  - one-way direction.
  - Total number of Links = 192.
  - The link bandwidth = 10.24 Gbps.
  - Data transmission Protocol = LpGBT.
  - Firmware = Customized version of LpGBT-FPGA.
  - Type of data synchronization = Asynchronous.
  - Type of FEC = FEC 5.
- Object
  - Object name = hit.
  - Object size = 11 bits.
  - Object fields name = Fired Strip number (7 bits), Sub-BX (4 bits)



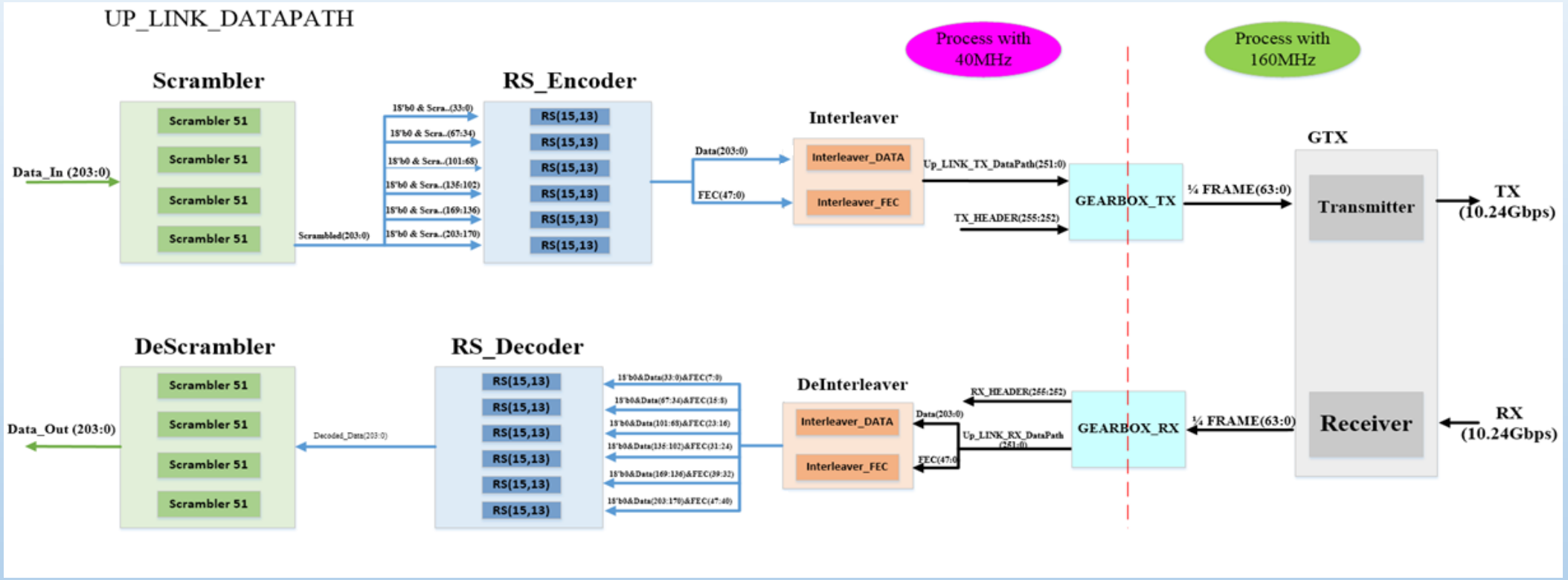
The RPC Data Payload to Layer-1

- **Payload on the Barrel**
  - Maximum payload per Link = 0.811 Gbps
  - Maximum Payload per Sector = 4.055 Gbps
  - Maximum Payload in Barrel = 243.3 Gbps
- **Payload on the Endcap**
  - Maximum payload per Link = 0.546 Gbps
  - Maximum Payload in Endcap = 104.8 Gbps
- **Fiber Mapping**
  - The same as present Link System



RPC Link System for Phase-2

- **Transceiver Architecture**



- ✓ In the scrambler avoiding long sequences of bits of the same level helps GTX distinguish each bit's boundary.
- ✓ Using Reed-Solomon, by adding redundancy to each packet, will have the possibility to correct defects.
- ✓ Using Interleaver by distributing defects in a frame makes FEC more robust.

Total Number of CBs, MLBs, SLBs in Barrel
Required Optical Links for Link System Phase-2 Upgrade

				Number of Master Link Boards in Each Sectors														
3	WHEEL	Chambers	SECTORS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		Total Number of MLB	Optical Links (SX)
4	RB+2	96	12	5	5	5	5	5	5	5	5	5	5	5	5		60	60
5	RB+1	96	12	5	5	5	5	5	5	5	5	5	5	5	5		60	60
6	RB0	96	12	5	5	5	5	5	5	5	5	5	5	5	5		60	60
7	RB-1	96	12	5	5	5	5	5	5	5	5	5	5	5	5		60	60
8	RB-2	96	12	5	5	5	5	5	5	5	5	5	5	5	5		60	60
9		480															300	300
10				Number of Salve Link Boards in Each Sectors														
11	WHEEL	Chambers	SECTORS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		Total Number of SLB	
12	RB+2	96	12	8	8	8	10	8	8	8	8	8	10	8	8		100	
13	RB+1	96	12	8	8	8	10	8	8	8	8	8	10	8	8		100	
14	RB0	96	12	8	8	8	10	8	8	8	8	8	10	8	8		100	
15	RB-1	96	12	8	8	8	10	8	8	8	8	8	10	8	8		100	
16	RB-2	96	12	8	8	8	10	8	8	8	8	8	10	8	8		100	
17																	500	
18				Number of Control Boards in Each Sectors														
19	WHEEL	Chambers	SECTORS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		Total Number of CB	Optical Link (DX)
20	RB+2	96	12	2	2	2	2	2	2	2	2	2	2	2	2		24	24
21	RB+1	96	12	2	2	2	2	2	2	2	2	2	2	2	2		24	24
22	RB0	96	12	2	2	2	2	2	2	2	2	2	2	2	2		24	24
23	RB-1	96	12	2	2	2	2	2	2	2	2	2	2	2	2		24	24
24	RB-2	96	12	2	2	2	2	2	2	2	2	2	2	2	2		24	24
25																	120	120

SX = Single Fiber

MLB OUTPUTS

DX = Double Fibers

CB Control Link

Total Number of CBs, MLBs, SLBs in Endcap
Required Optical Links for Link System Phase-2 Upgrade

				Number of Master Link Boards in Each Sectors												
30																
31	DISK	chambers	SECTORS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Total Number of MLB
32	RE+4	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
33	RE+3	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
34	RE+2	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
35	RE+1	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
36	RE-1	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
37	RE-2	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
38	RE-3	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
39	RE-4	72	12	2	2	2	2	2	2	2	2	2	2	2	2	24
40		576														192
41																
42				Number of Slave Link Boards in Each Sectors												
43	DISK	chambers	SECTORS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Total Number of SLB
44	RE+4	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
45	RE+3	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
46	RE+2	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
47	RE+1	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
48	RE-1	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
49	RE-2	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
50	RE-3	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
51	RE-4	72	12	4	4	4	4	4	4	4	4	4	4	4	4	48
52		576														384
53				Number of Control Boards in Each Sectors												
54	DISK	chambers	SECTORS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Total Number of CB
55	RE+4	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
56	RE+3	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
57	RE+2	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
58	RE+1	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
59	RE-1	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
60	RE-2	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
61	RE-3	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
62	RE-4	72	12	1	1	1	1	1	1	1	1	1	1	1	1	12
63		576														96

SX = Single Fiber

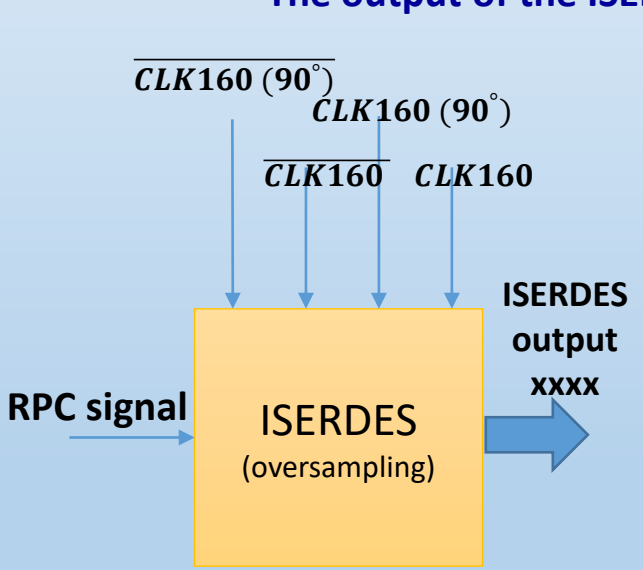
MLB OUTPUTS

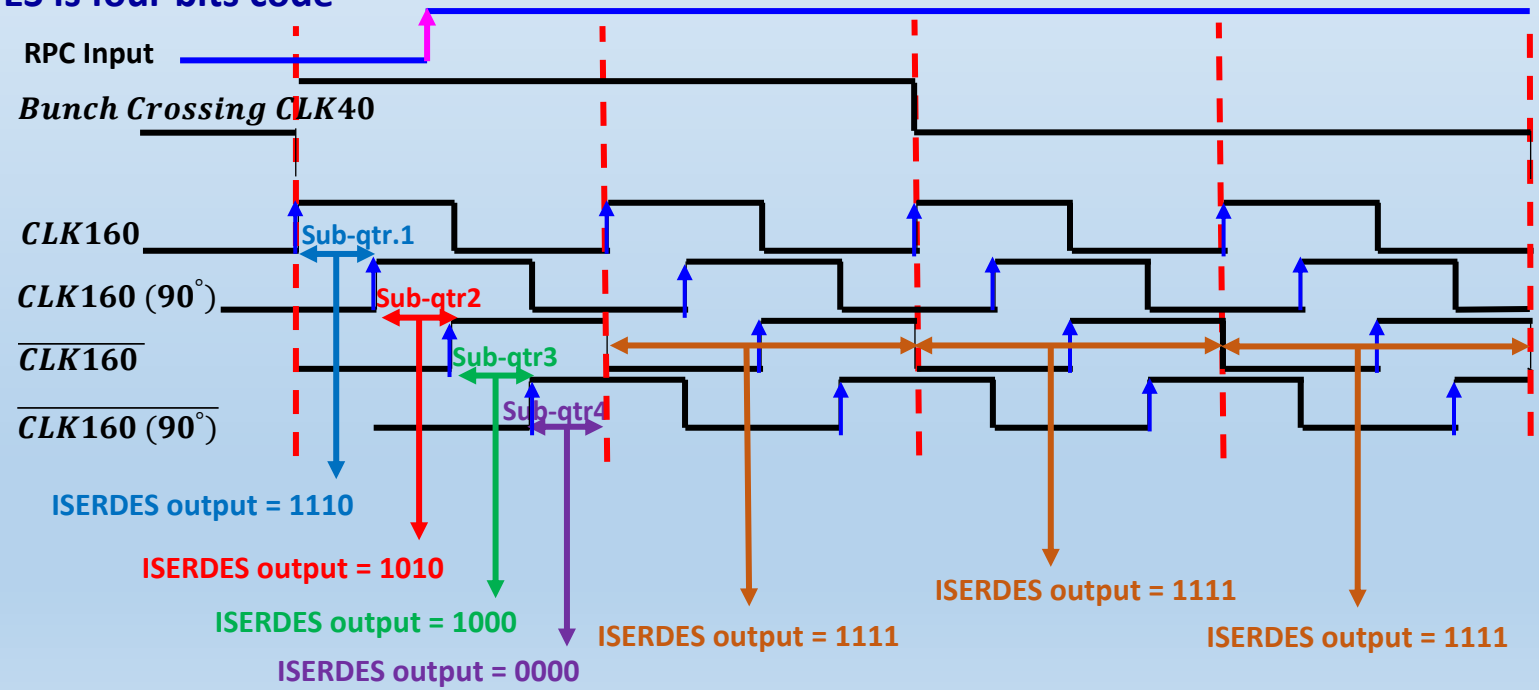
DX = Double Fibers

CB Control Link

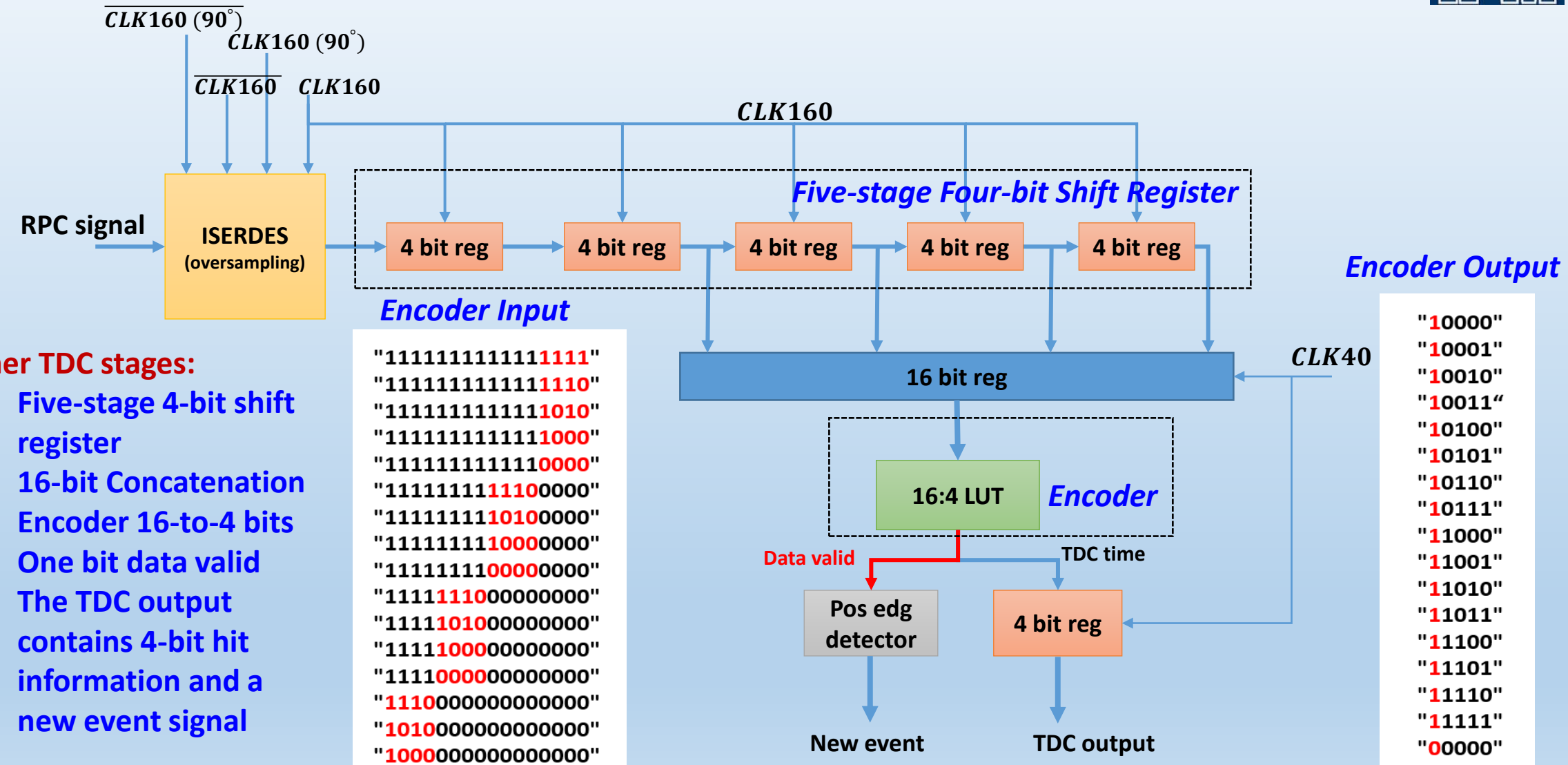
RPC data processing – Time-Stamping

- **RPC signals time-Stamping on RPC hits**
  - Time-to-Digital Converter (TDC)
  - In TDC the first stage is the Input Serial/De-serial (ISERDES) DIGITIZAER unit.
  - It needs four Clocks, four times higher than the reference clock (Bunch Crossing). Take four samples on every quarter of the reference Clock
  - ISERDES is a hardware built-in component inside the FPGA
  - The main function of ISERDES is to serialize the RPC input signal at the specific sampling rate
  - The output of the ISERDES is four bits code





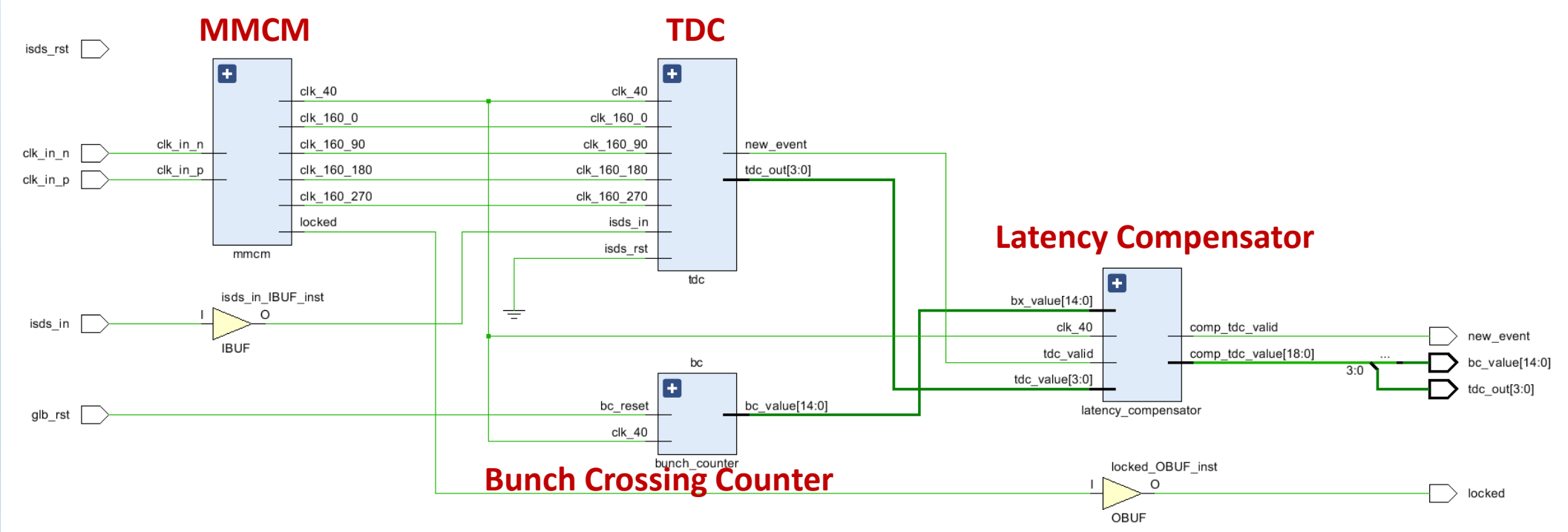
RPC data processing – Time-Stamping



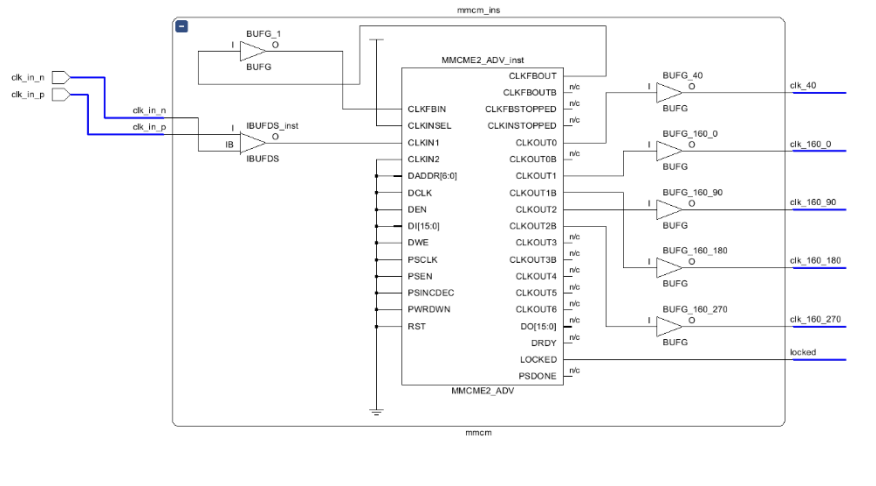
- **Other TDC stages:**
  1. Five-stage 4-bit shift register
  2. 16-bit Concatenation
  3. Encoder 16-to-4 bits
  4. One bit data valid
  5. The TDC output contains 4-bit hit information and a new event signal

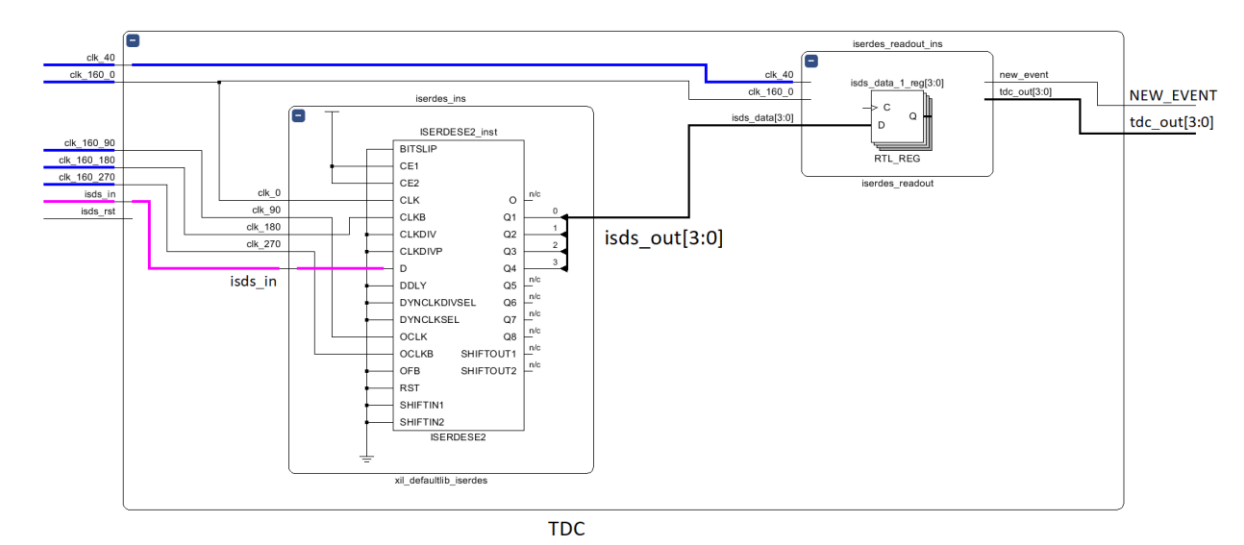
Time-Stamping – FPGA Implementation

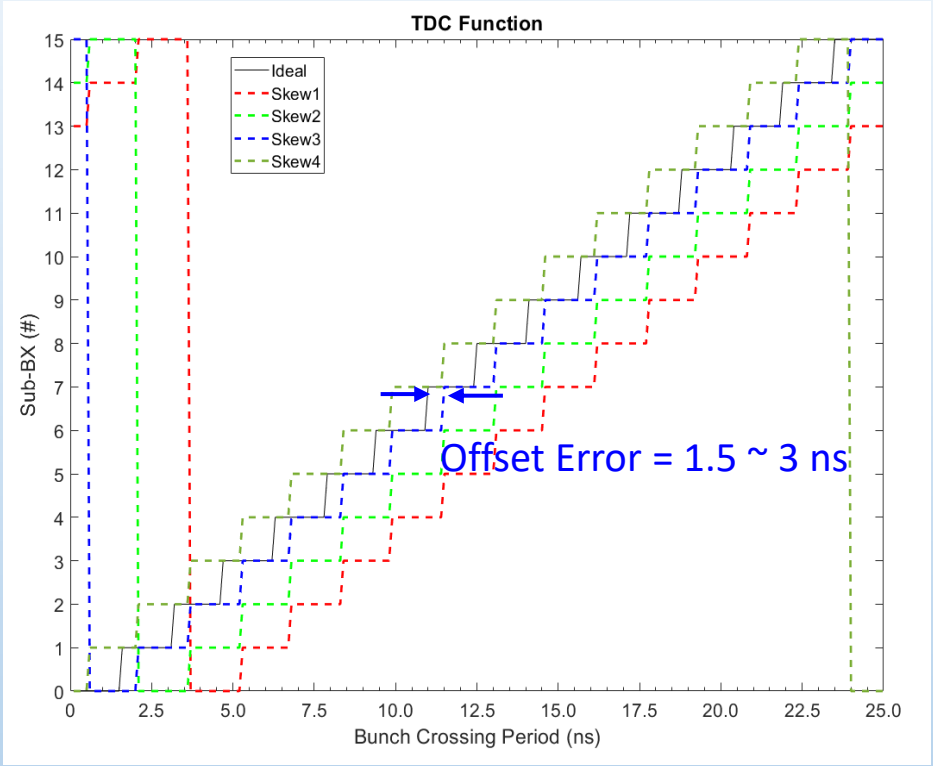
- **Time-Stamping stages in FPGA:**
  1. MMCM generate four-phase shifted clocks at frequency of 160 MHz
  2. Time-to-Digital Converter, fine-time measurement.
  3. Bunch Crossing Counter is implemented by a 15-bit Counter, coarse time measurement.
  4. TTC Clock Latency and RPC signal propagation delay are compensated by the Latency Compensation unit.



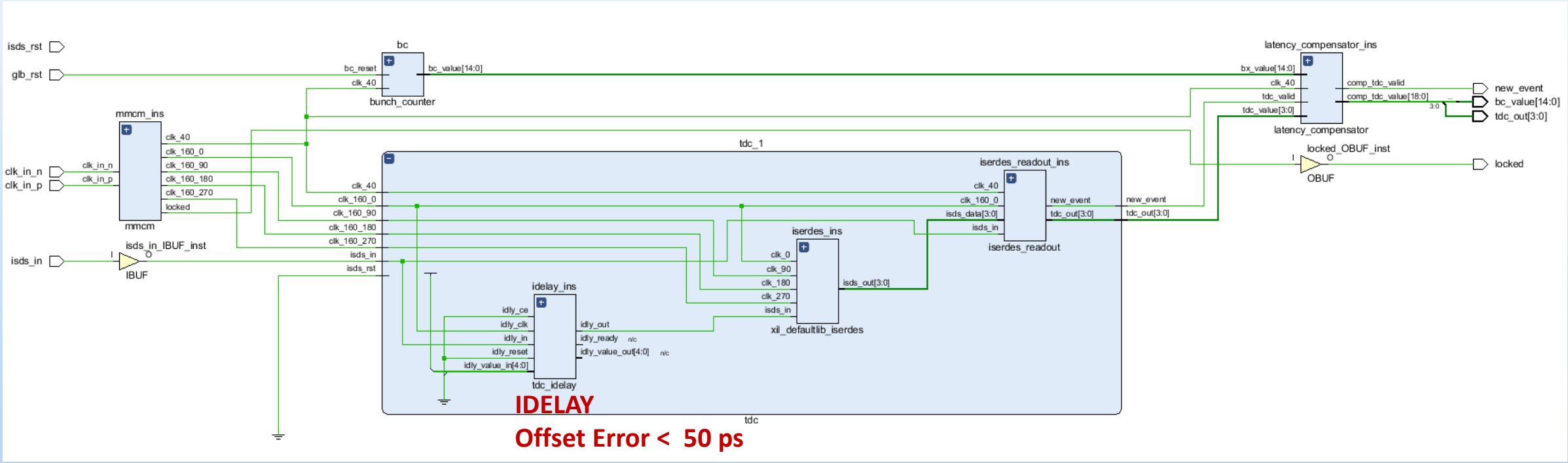
Time-Stamping – TDC Transfer Function



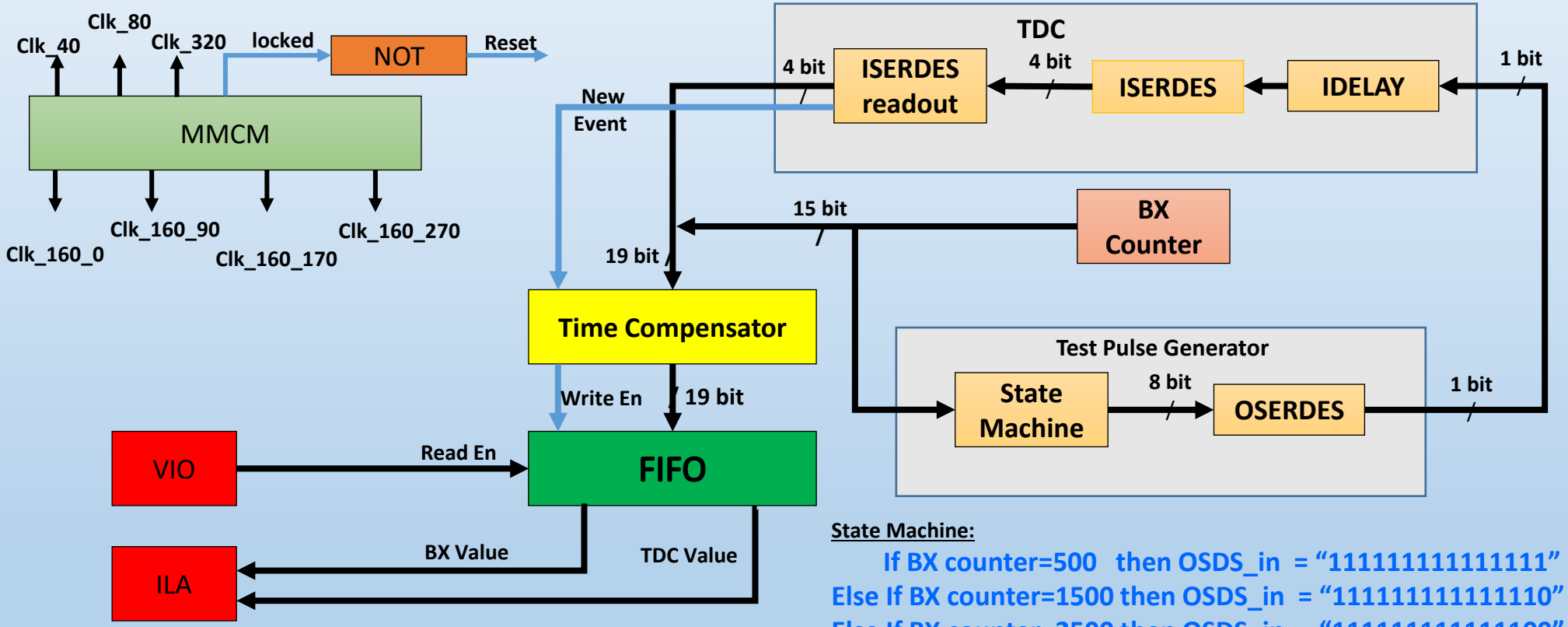




Time-Stamping – TDC Transfer Function



Time-Stamping – Validation

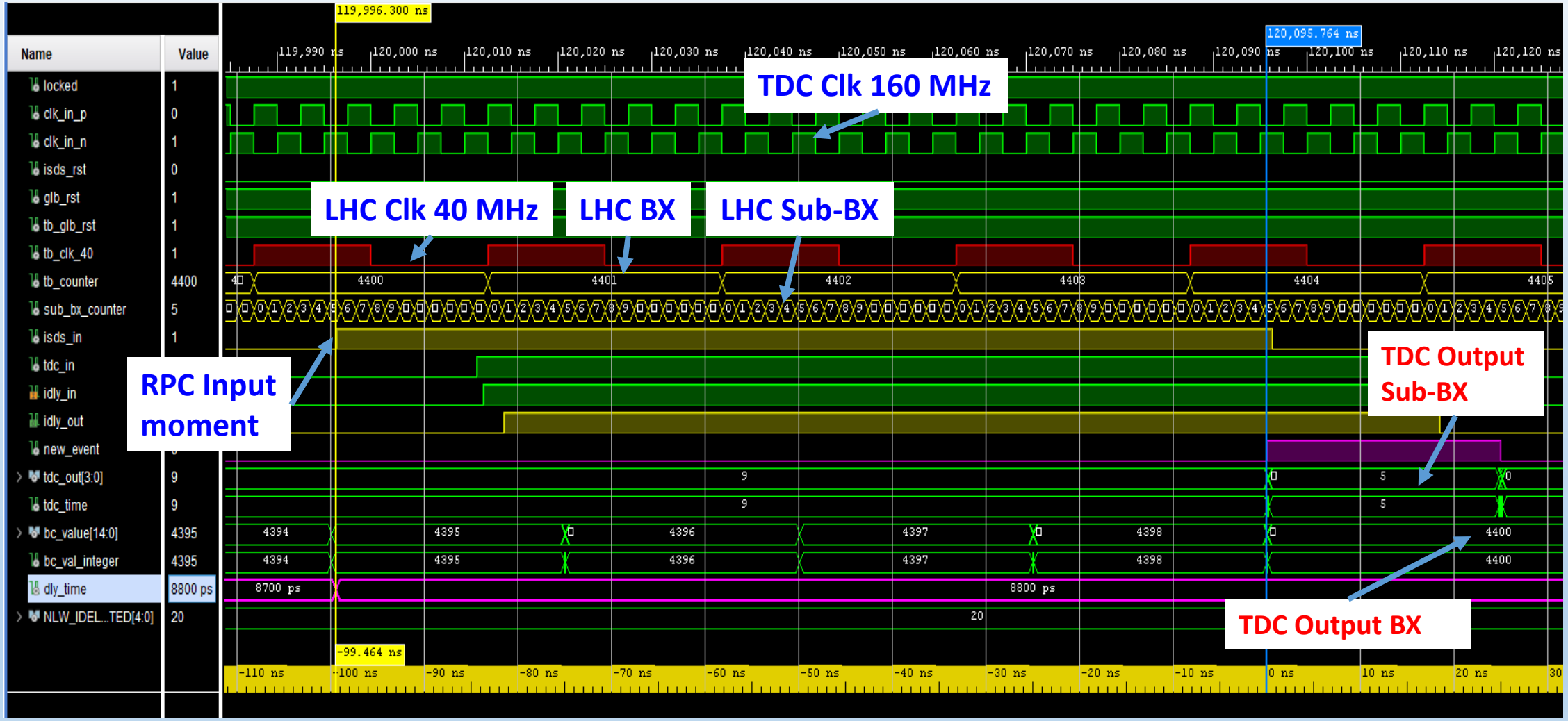


State Machine:

If BX counter=500 then OSDS_in = "111111111111111"
Else If BX counter=1500 then OSDS_in = "111111111111110"
Else If BX counter=2500 then OSDS_in = "111111111111100"

.
.
.

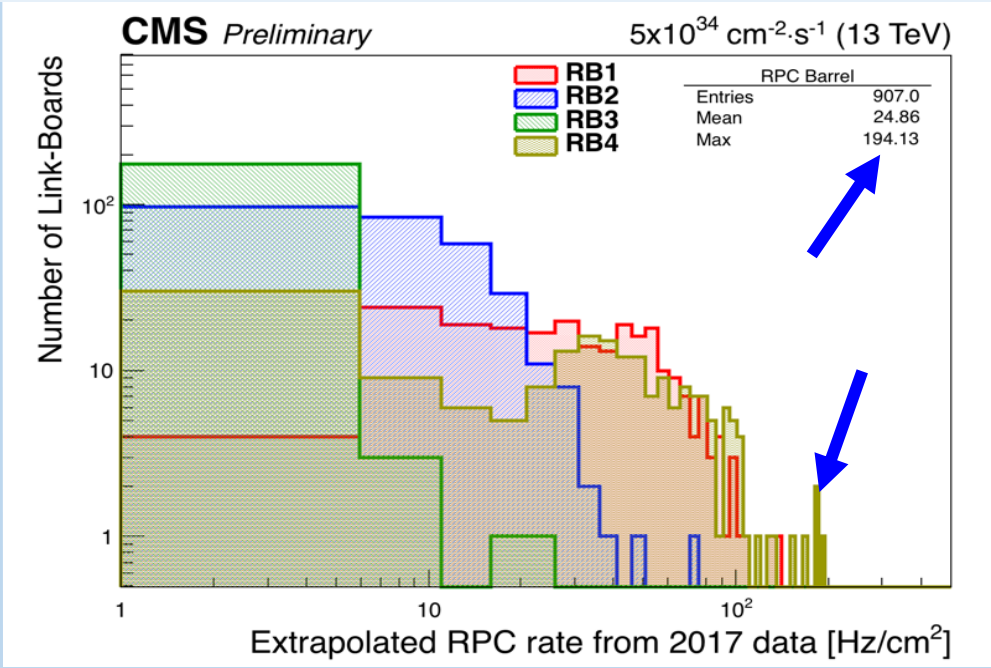
Time-Stamping – Validation



Maximum Expected Event payload in the Barrel

- Expected Max hit rate in Barrel in HL-LHC , safety factor 3: 600 $cm^{-2}. s^{-1}$
- Biggest Strip surface area : 120 × 3 cm^2
- Average cluster size: -
- Number of Strip per chamber : 96
- Max Single hit in one LB per BX : 600 x (120 x 3) x 96 x 25 X 10^{-9}= 0.52 hit /LB x bx
- One Link covers three Link Boards
- Max Single hit on Link per bx : 0.52 × 3 = 1.56 hit /Link . BX
- Size of hit : 13 bits/hit (Yellow box)
- MLB Max. Event Payload: 13 bits/hit × 1.56 hits/Link . BX = 20.28 bits /Link . BX
- $= 20.28 \times 40 \times 10^6$ bit/s $= 0.811 \times 10^9$ bit/s
- Total number of link in the Barrel : 300
- Total number of event payload in the Barrel : 6084 bits /BX = 760.5 Byte /BX
- Maximum throughput : $20.28 \times 300 \times 40 \times 10^6$ bit/s
  $= 0.24336 \times 10^{12}$ bit/s

One Event = Size of the data corresponding to one bunch crossing



Item	Header + FEC	No. Strip (1..96)	Sub-bx	...	No. Strip (1..96)	Sub-bx	...	No. Strip (1..96)	Sub-bx	...	BCN MLB	RBCN SLBR	RBCN SLBL
Bit	22	7	4	...	7	4	...	7	4	...	12	6	6

Maximum Expected Event payload in the Endcap

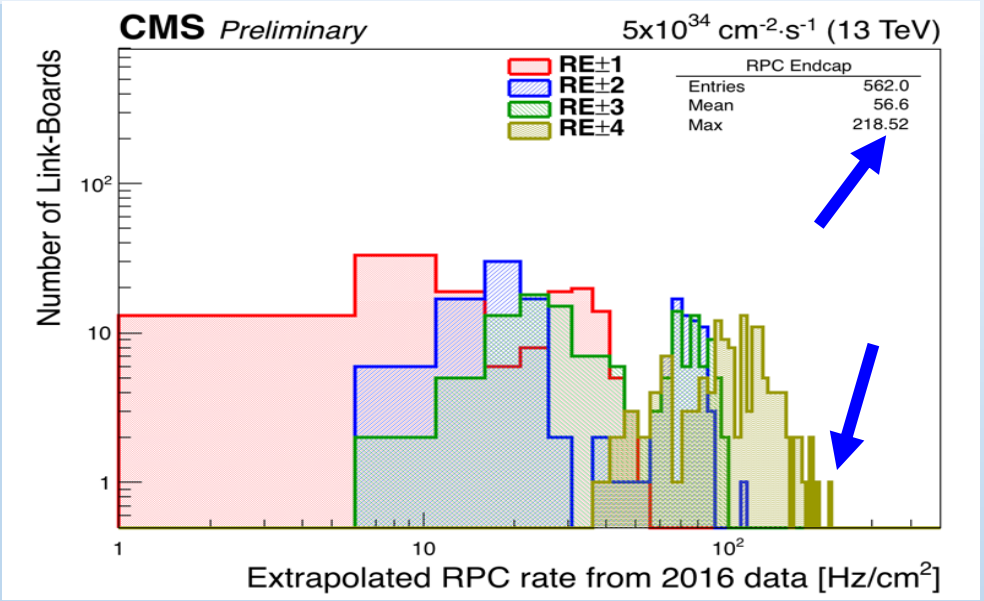
- Expected Max hit rate in Endcap in HL-LHC , safety factor 3: 700 $cm^{-2}. s^{-1}$
- Biggest Strip surface area : 66 × 3.125 cm^2
- Average cluster size: -
- Number of Strip per chamber : 96
- Max Single hit in one LB per BX : 700 x (66 × 3.125) × 96 × 25 × 10^{-9} = 0.35 hit /LB . BX
- One Link covers three Link Boards
- Max Single hit on Link per bx : 0.35 × 3 = 1.05 hit /Link . BX
- Size of hit : 13 bits/hit (Yellow box)
- MLB Max. Event Payload: 13 bits/hit × 1.05 hits/Link . BX = 13.65 bit / Link . BX

$$= 13.65 \times 40 \times 10^6 \text{ bit/s} = 0.546 \times 10^9 \text{ bit/s}$$

- Total number of link in the Endcap : 192
- Total number of event payload in the Endcap = 2620 bit/BX = 327 Byte/BX
- Maximum throughput = $13.65 \times 192 \times 40 \times 10^6$ bit/S

$$= 0.1048 \times 10^{12} \text{ bit/S}$$

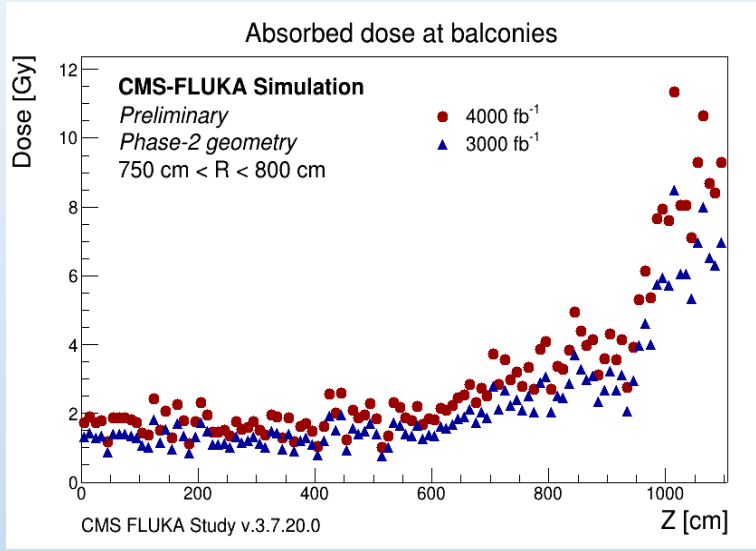
One Event = Size of the data corresponding to one bunch crossing

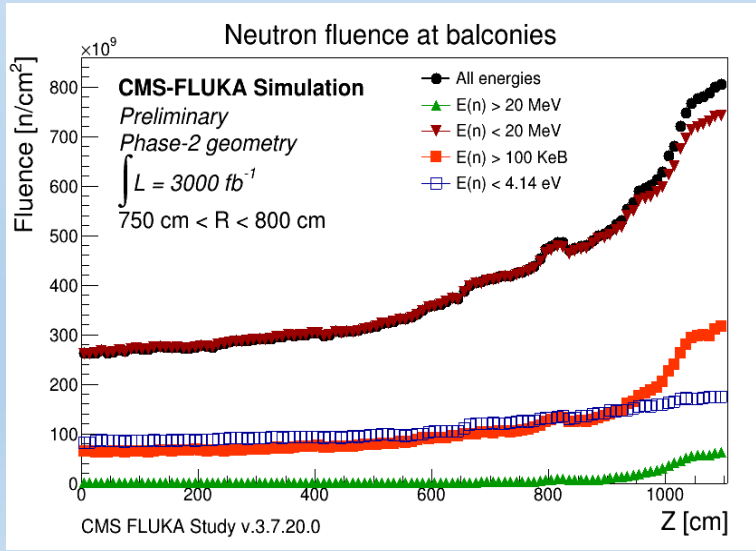


Item	Header + FEC	No. Strip (1..96)	Sub-bx	...	No. Strip (1..96)	Sub-bx	...	No. Strip (1..96)	Sub-bx	...	BCN MLB	RBCN SLBR	RBCN SLBL
Bit	22	7	4	...	7	4	...	7	4	...	12	6	6

Radiation Consideration

- The **Link system** will be installed on the **Balcony of CMS**, where the rates are even lower than what we have at the periphery of the detector.
- **Total Irradiation Dose at most** is **10 Gy** @ **3000fb^{-1}**
- **Neutron Flux** at the **CMS Balcony** is **1x10^{4} cm^{-2}s^{-1}** **@5 x 10^{34} cm^{-2}s^{-1}**
- **Neutron Fluence for 10 HL-LHC years is 8x10^{11} cm^{-2}**
- The new Link board components has been chosen from COTS which are validated for radiation at the level of **300 Gy**
- The FPGA TID KINTEX-7 (XC7K160T) is **3400-4500 Gy**
- **Scrub Time of entire FPGA (Real time SEU detection and Correction) : 13ms**
- The Single Event upset (SEU) rate on **configuration memory** is **1 SEU every 413 sec.** and **1 SEU every 1695 sec. at Block RAM**
- **TMR and Configuration Scrubbing will mitigate the SEUs**



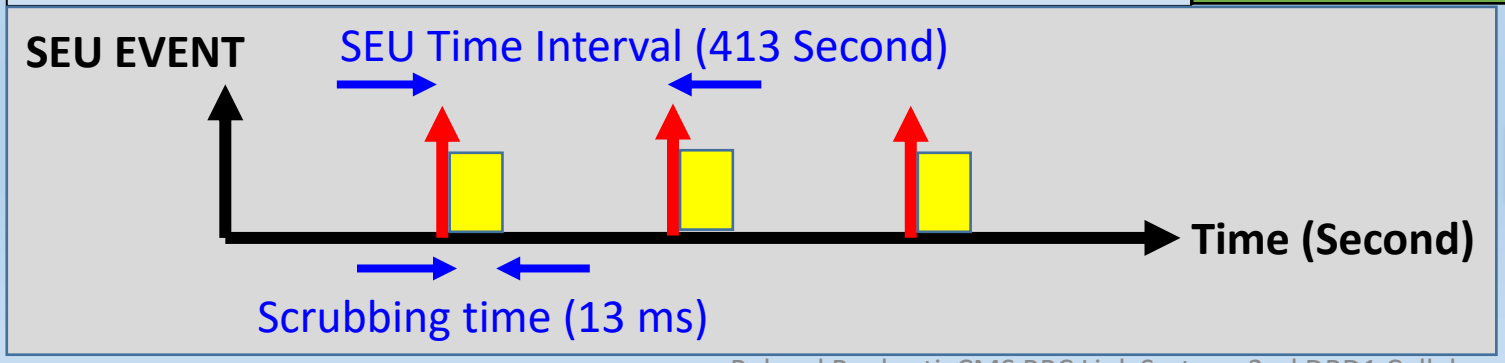


Radiation Consideration

Estimation of SEU on the KINTEX-7 XC7K160T Configuration and BRAM Memories

- *Number of Errors* = $\sigma_{CRAM} \times Flux \times T_{irrd} \times N_{CRAM}$
- σ_{CRAM} = Cross section of the Single Event upset of each bit at the configuration Memory ($cm^2\ bit^{-1}$)
- Flux = Number of Neutron pre squire centimeter per second
- T_{irrd} = Irradiation Time
- N_{CRAM} = number of bits at the Configuration Memory

Integrated Errors due to SEU at the Configuration Memory of KINTEX-7 XC7K160T	Integrated Errors due to SEU at the BLOCK RAM Memory of KINTEX-7 XC7K160T
$\sigma_{CRAM} = 4.52 \times 10^{-15}\ cm^2\ bit^{-1}$ Flux = $1 \times 10^4\ cm^{-2}\ s^{-1}$ Time of Exposure = 1 sec N_{CRAM} = 53,540,576 bits	$\sigma_{BRAM} = 5.07 \times 10^{-15}\ cm^2\ bit^{-1}$ Flux = $1 \times 10^4\ cm^{-2}\ s^{-1}$ Time of Exposure = 1 sec N_{BRAM} = 11,700,000 bits
E_{CRAM} = 0.00242 at 1 second E_{CRAM} = 0.1452 at 1 minute E_{CRAM} = 8.712 at 1 hour	E_{BRAM} = 0.00059 at 1 second E_{BRAM} = 0.036 at 1 minute E_{BRAM} = 2.135 at 1 hour
1 SEU every 413 seconds	1 SEU every 1694 seconds



SEU Time Interval >> Scrubbing time

RPC Link System- CHARM Irradiation result

Irradiation test: 12 Oct. – 1 Nov. 2022

	TID	HeH	N1MeV	ThN	POT	DD/TID	Rfactor
1) RUN #28 (USER)	19.1 Gy	5.35e+10 cm^{-2}	-2.86e+07 cm^{-2}	1.17e+11 cm^{-2}	1.44e+16	-1.49e+06 $cm^{-2}Gy^{-1}$	2.189445
2) RUN #29 (USER)	16.9 Gy	4.89e+10 cm^{-2}	2.20e+11 cm^{-2}	9.95e+10 cm^{-2}	1.42e+16	1.30e+10 $cm^{-2}Gy^{-1}$	2.033706
3) RUN #30 (USER)	17.9 Gy	5.05e+10 cm^{-2}	2.90e+11 cm^{-2}	1.00e+11 cm^{-2}	1.46e+16	1.62e+10 $cm^{-2}Gy^{-1}$	1.980232
Final value	54.0 Gy	1.53e+11 cm^{-2}	5.11e+11 cm^{-2}	3.17e+11 cm^{-2}	4.33e+16	9.74e+09 $cm^{-2}Gy^{-1}$	2.067794

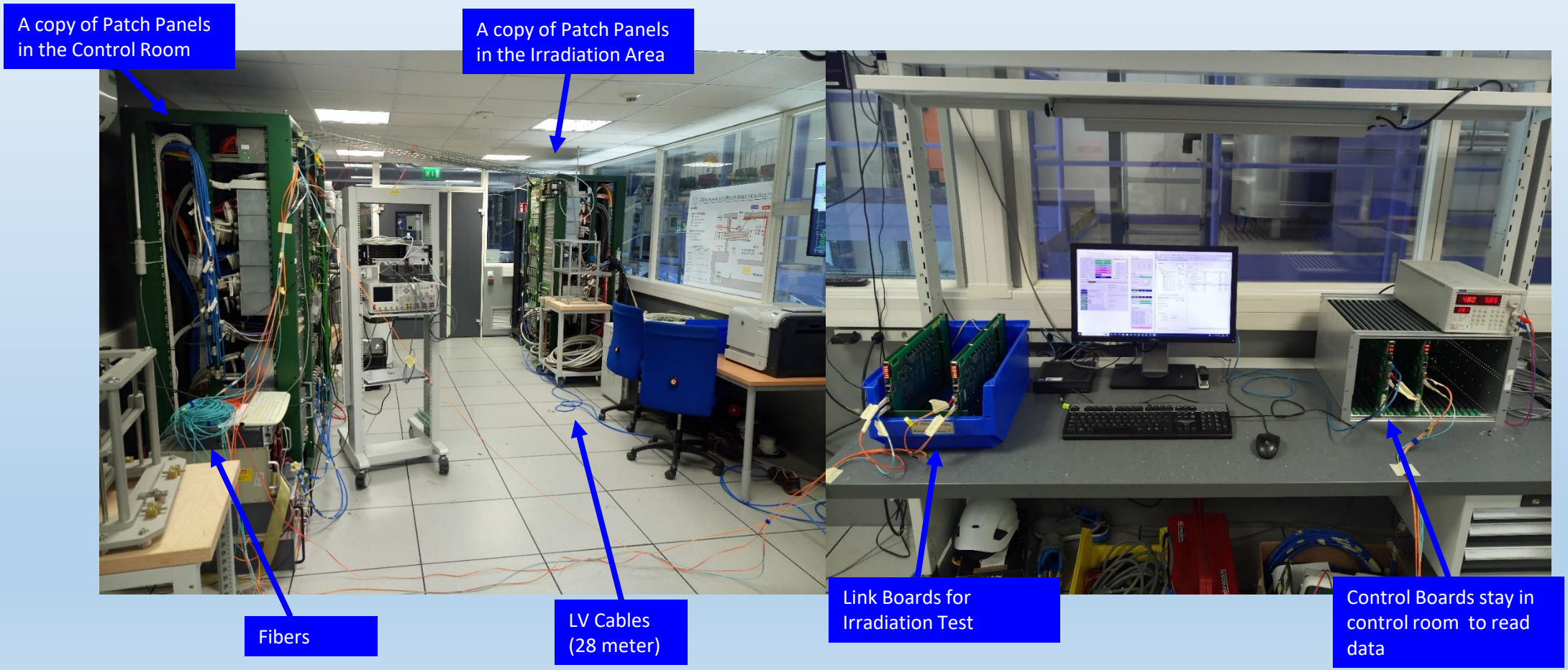
RPC Link System- Installation in Control Room at CHARM

- Two Redundant readout
- In this setup two Control Boards emulate the Backend electronics functionalities

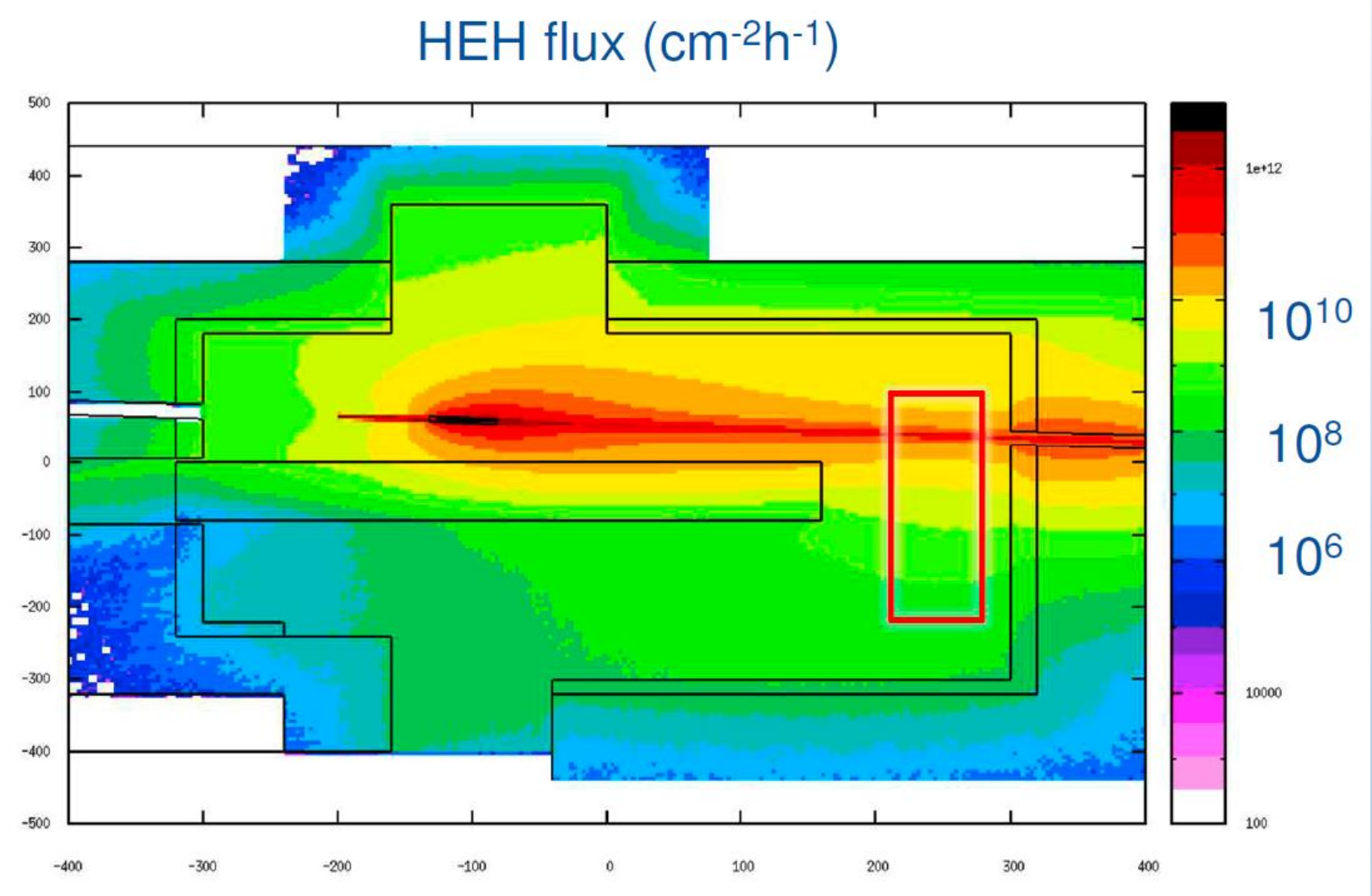
Wall grid (Position G0)

CHARM Preparation Area

- **September 2022: Dry-Run test for one week**



The CHARM Radiation Environment



In the downstream locations (10-13) HEH fluxes of **~10^{10} $cm^{-2}h^{-1}$** (roughly one year in the LHC tunnel) can be reached in one hour

The CHARM Radiation Environment

of the mixed-field environment, is that of a quasi-uniform spill lasting roughly 350 ms, which is repeated every 10 seconds. Although this would indeed be a pulsed beam for

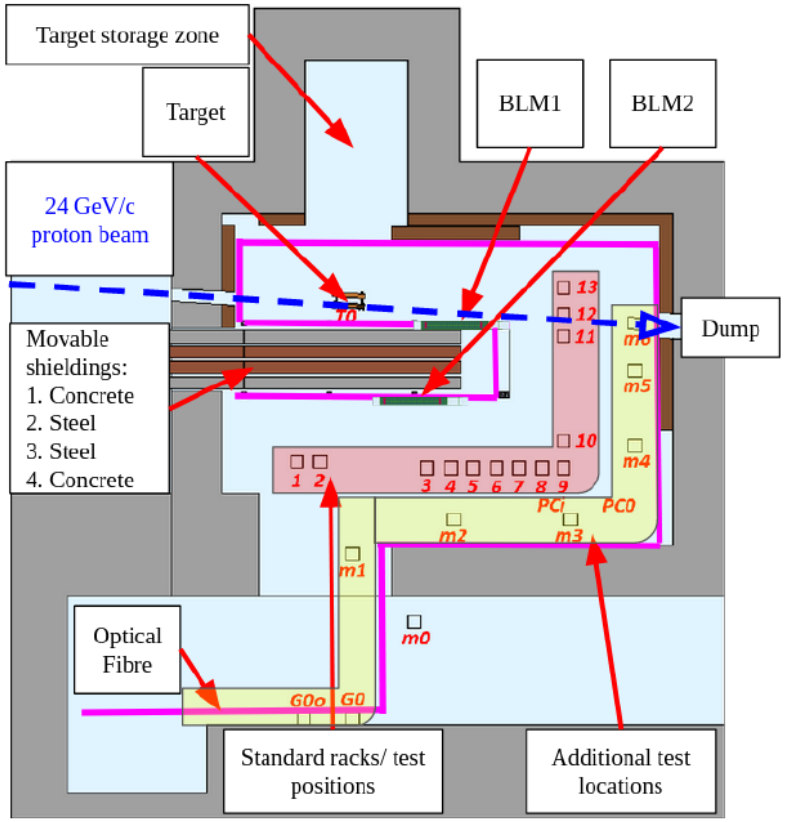
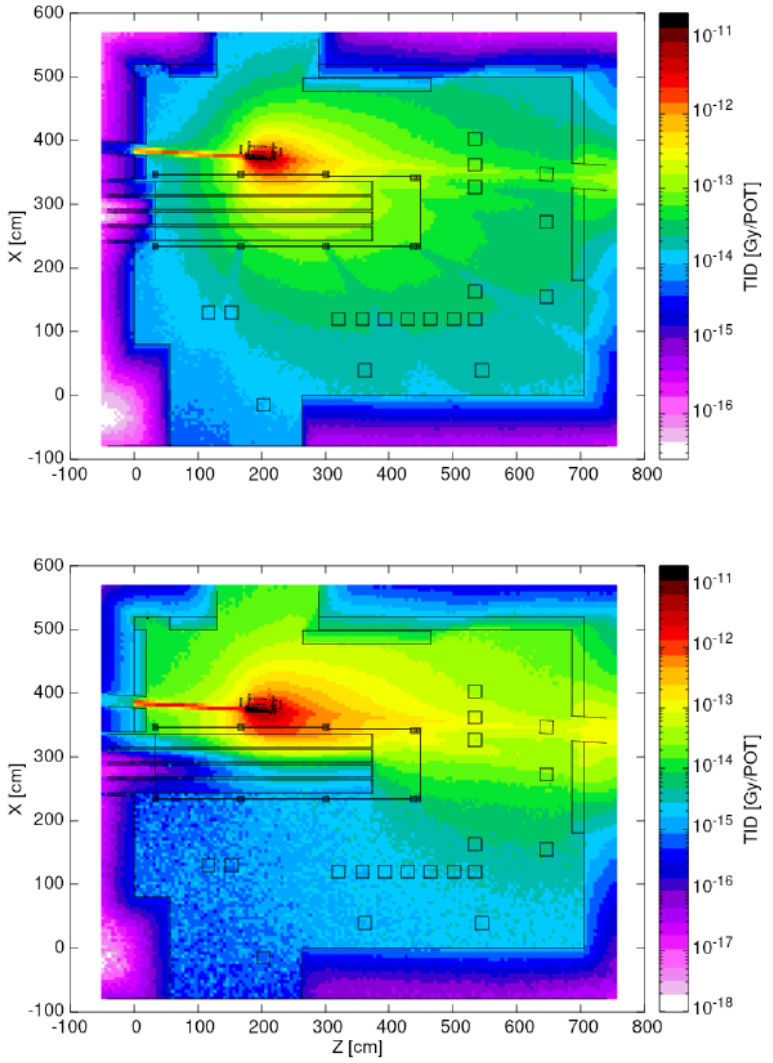


Fig. 1: Top view of FLUKA geometry of the CHARM test area. Two BLMs are installed at 1 m above beam height, one next to the target and one behind the movable shieldings. There



The simulated 2D TID distribution at beam height is shown for two configurations: CuOOOO (top) and CuCSSC (bottom).

[Paper Link]

The CHARM Radiation Environment

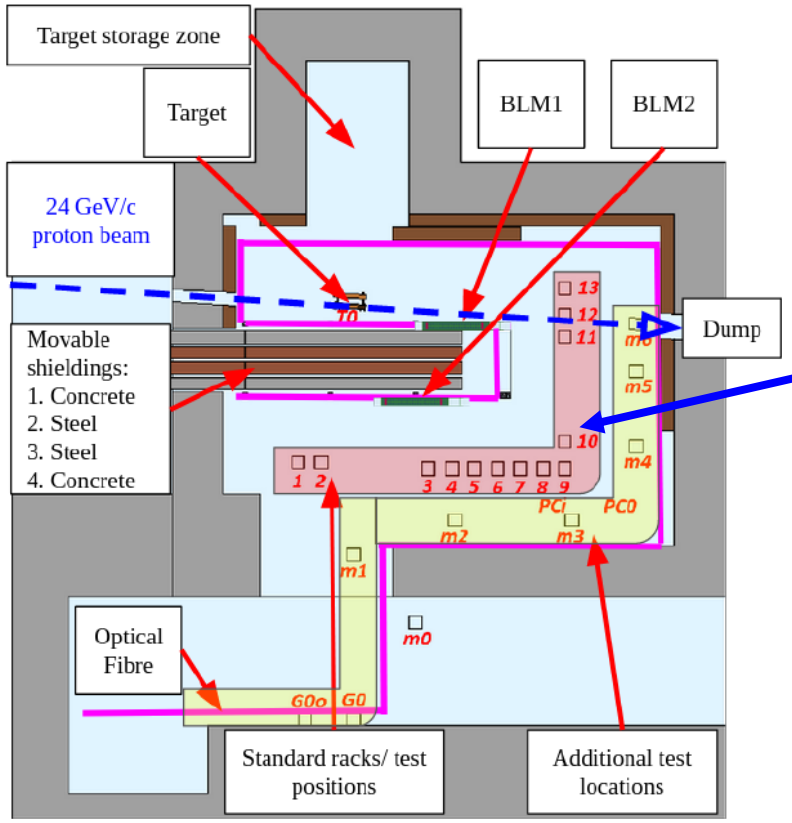


Fig. 1: Top view of FLUKA geometry of the CHARM test area. Two BLMs are installed at 1 m above beam height, one next to the target and one behind the movable shieldings. There

TABLE I: Maximum and weekly maximum integrated rates at CHARM for the Total Ionizing Dose, and the thermal neutron equivalent and high-energy hadron Fluences, obtained at the R10 location based on FLUKA simulations.

Quantity	Maximum Rate	Integrated Rate (per week)
Total Ionizing Dose	2.70 Gy/h	360 Gy
Thermal neutron fluence	3×10^{6} cm^{-2}s^{-1}	1.5×10^{12} cm^{-2}
High-energy hadron fluence	1.5×10^{6} cm^{-2}s^{-1}	8×10^{11} cm^{-2}