MAX-PLANCK-INSTITUT
FÜR PHYSIK

DEVELOPMENT OF A NEW ASD-ASIC FOR DRIFT-TUBE AND STRAW DETECTORS

N. Bangaru, D. Cieri, F. Fallavollita, O. Kortner, S. Kortner, H. Kroha, G. Proto, R. Richter, E. Voevodina, Y. Zhao

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Drift-tube and straw-tube detectors at the FCC

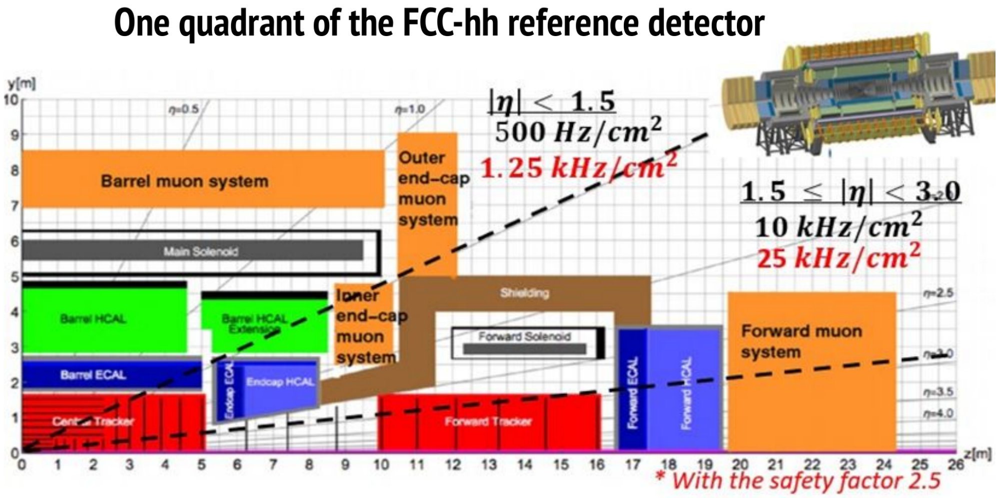
FCC-ee

- In order to achieve $\sim 1‰$ momentum resolution for charged particles up to 50 GeV, a combination of low X_0 silicon and gaseous detectors is envisaged.
- One option for the gaseous detector: straw-tubes with diameters $\sim$ 10 mm.

FCC-hh

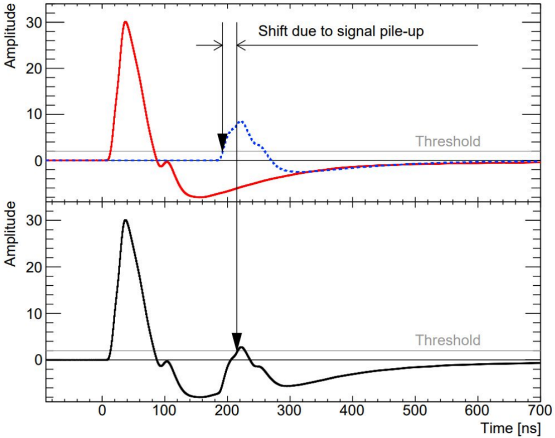
- Baseline muon system instrumented with single layer of small diameter muon drift-tube (sMDT) chambers up to $|\eta| = 3.0$.
- Target angular resolution: 70 μrad achieved by placing two quadruple layers of 15 mm diameter tubes at 1.5 m distance.

Operating conditions at the FCC-hh



⇒ Counting rates up to 1 MHz/tube expected.

Performance limitations from the read-out electronics



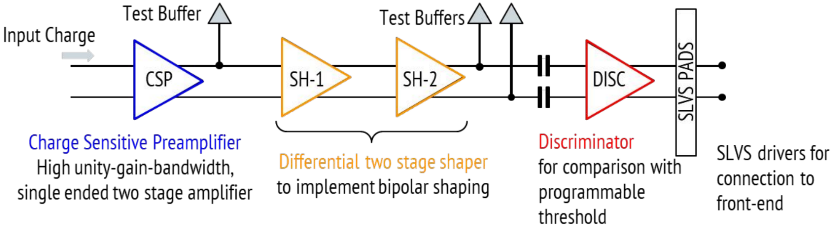
Reference: ATLAS phase-II electronics

- ASD ASIC in 130 nm GF CMOS technology.
- 12 ns peaking time with bipolar shaping.
- Background hits mask muon hits with the dead time of the electronics leading to reduced muon efficiencies.
- Signal pile-up deteriorates the spatial resolution at high background rates.

New ASD chip

- 65 nm TSMC CMOS technology.
- Faster baseline recovery of the bipolar shaping scheme to reduce the pile-up effect.

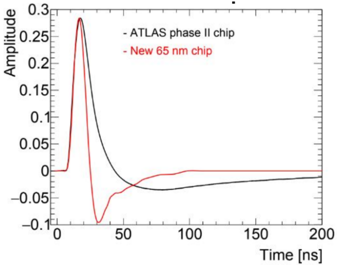
New ASD chip in 65 nm CMOS technology



- Four-channel Amplifier Shaper Discriminator designed by the MPI for Physics and fabricated in 65 nm TSMC CMOS technology.
- Bipolar shaping selected to avoid baseline shifts at high background hit rates.
- Discriminator with LVDS output.
- Power consumption per channel 12.8 mW (61% lower than the power consumption of the ATLAS phase-II ASIC).
- 0.235 mm^2 area/channel.

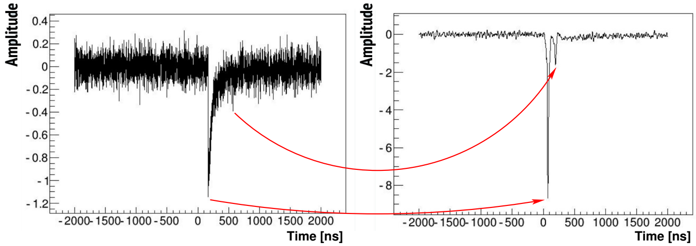
Response of the new ASD chip

δ response functions



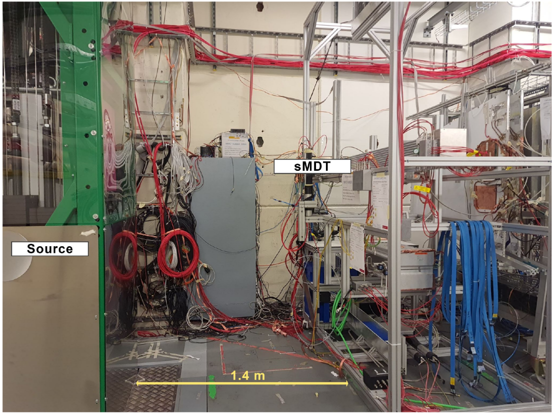
- Same peaking time of the new chip as the ATLAS phase-II chip.
- Faster baseline recovery of the new chip.

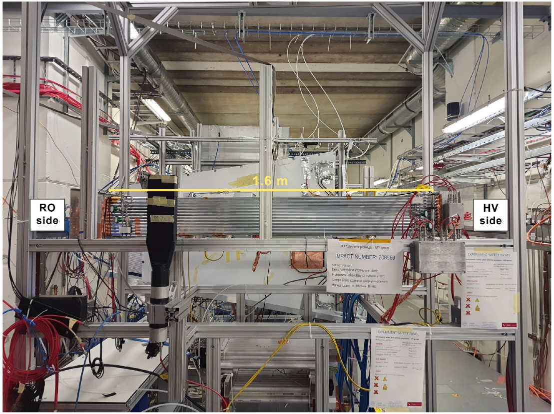
Simulated muon pulse before and after shaping



- Fast pulse shaping of the new chips allows us to destinguish different primary ionization clusters.

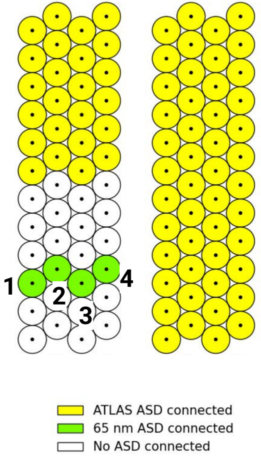
Test of the new chip on an sMDT chamber in the GIF++

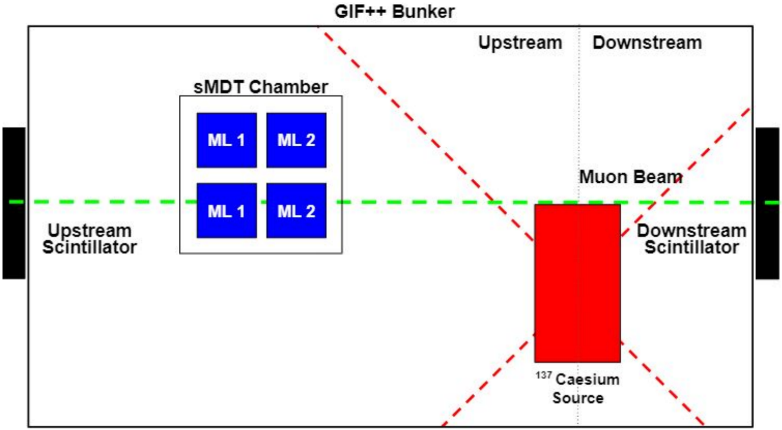




Test-beam set-up

Electronics Connected to the sMDT Chamber

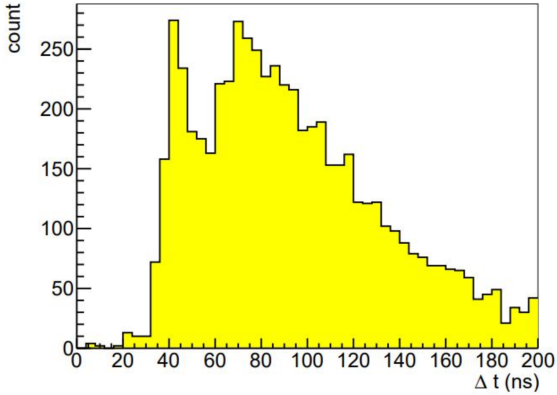




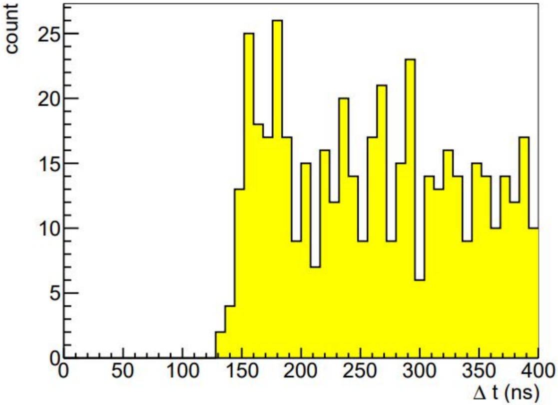
- One 65 nm ASD chip on a prototype PCB connected to 4 tubes.
- Rest of the tubes read out with the ATLAS phase-II chip.
- Coincidence of GIF++ scintillators used as beam trigger.

Dead time comparison

New chip

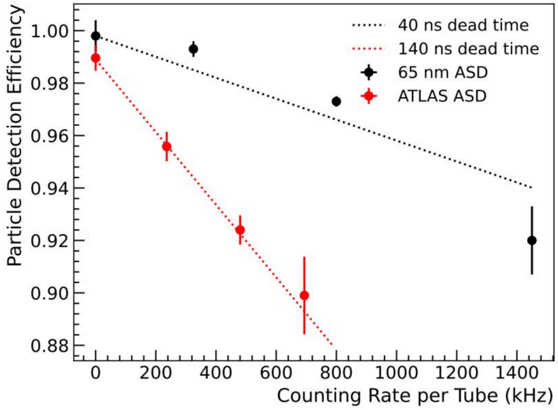


ATLAS phase-II chip



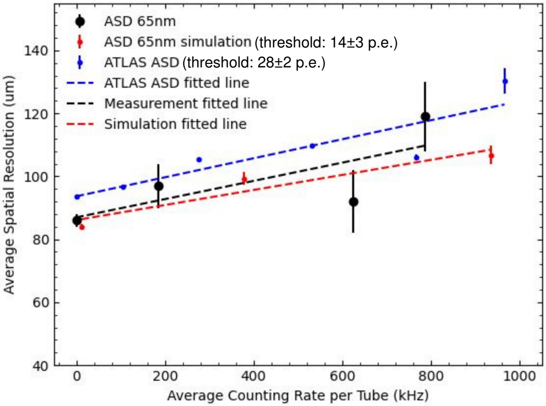
- The distributions of the time difference of two consecutive γ hits shows that the new chip has a much shorter dead time than the ATLAS phase-II chip: 40 ns vs 140 ns.

Muon detection efficiency comparison



- Much higher efficiency obtained with the new chip than with the ATLAS phase-II chip thanks to the reduced dead time.
- Slightly higher efficiency of the new chip at 0 background rates due to a lower discriminator threshold.

Spatial resolution comparison



- Measured spatial resolution values compatible with the prediction from the Garfield simulation.
- Resolution achieved with the new ASD chip about 10 μm better than with the ATLAS phase II chip (mainly thanks to the lower discriminator threshold).
- 100 μm spatial resolution even at 1 MHz background count rate.

Conclusions and outlook

- A new ASD chip with fast baseline recovery and reduced dead time has been developed.
- Test of this chip on a chamber in the GIF++ shows excellent performance of the new chip in terms of muon detection efficiency and spatial resolution.
- Next steps:
  - Use the chip for the read-out of straws.
  - Optimize the shaping for the read-out of straws.