Progress on Timing Electronics for the T-SDHCAL

Weihao Wu

Shanghai Jiao Tong University

On behalf of Calice Group

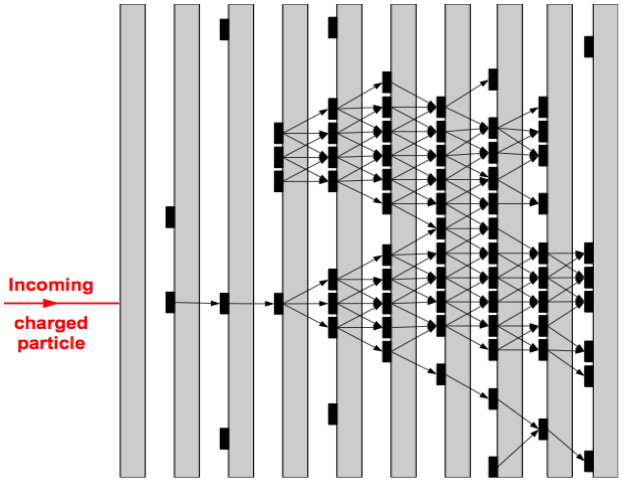
WP7B Meeting, 2024 6/17

Outline

Semi-Digital Hadronic CALorimeter

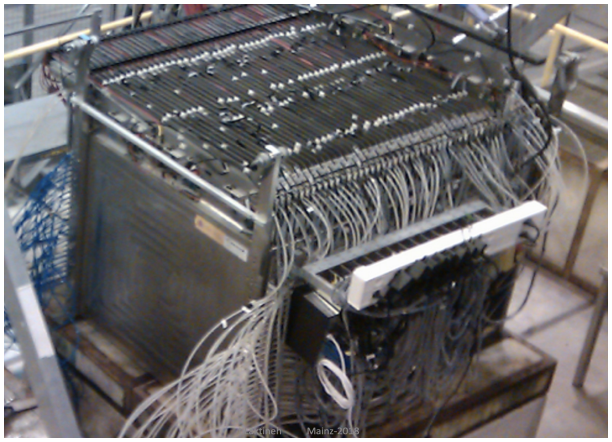
One of the high granularity PFA (Particle Flow Algorithm) calorimeters

- Connect first hits and then their clusters using distance and orientation information.
- The energy information helps to optimize the connections of hits belongs to the same shower.

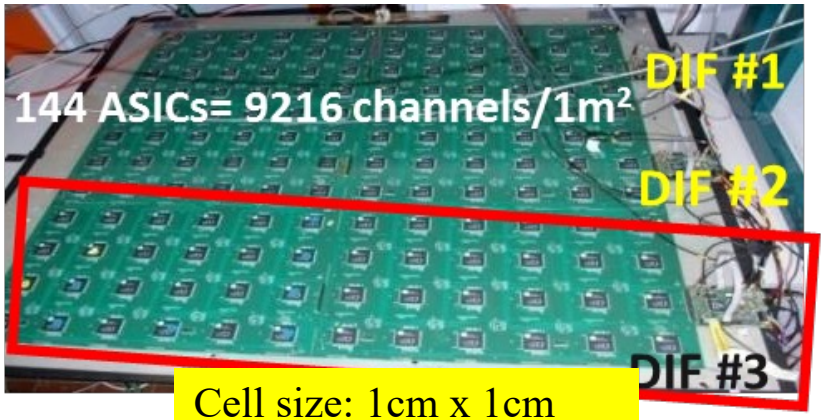


A SDHCAL prototype built based on Glass RPC

Semi-digital readout： three different thresholds



SDHCAL prototype at testbeam in 2015



Cell size: 1cm x 1cm
Power: 1mW/ch

Timing-SDHCAL

Timing information can be very helpful to separate close-by showers and reduce the confusion for a better PFA application.

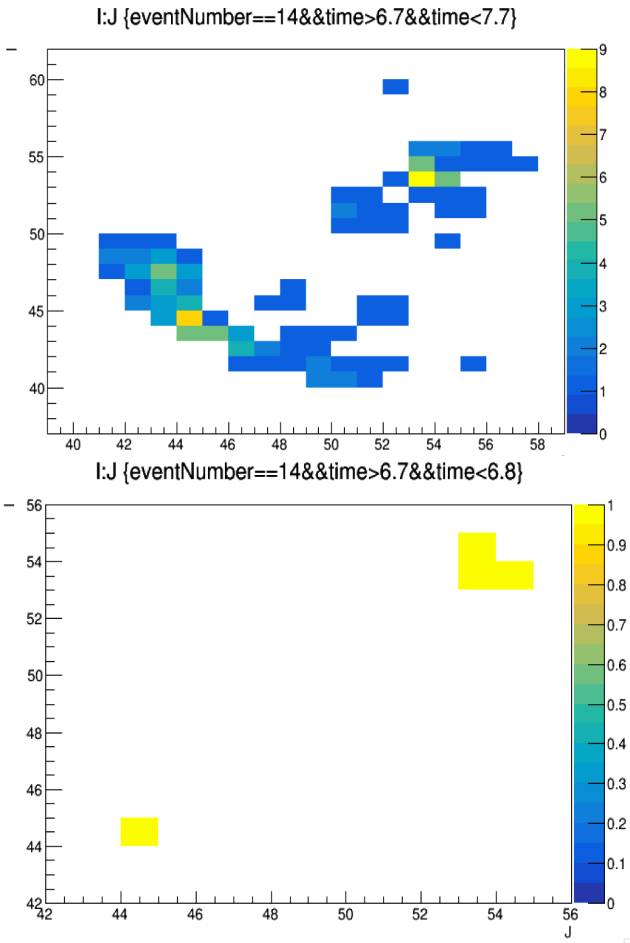
Add some mRPC layers in the SDHCAL

- Fast timing detectors (<100 ps)

Front-End Electronics for mRPC readout

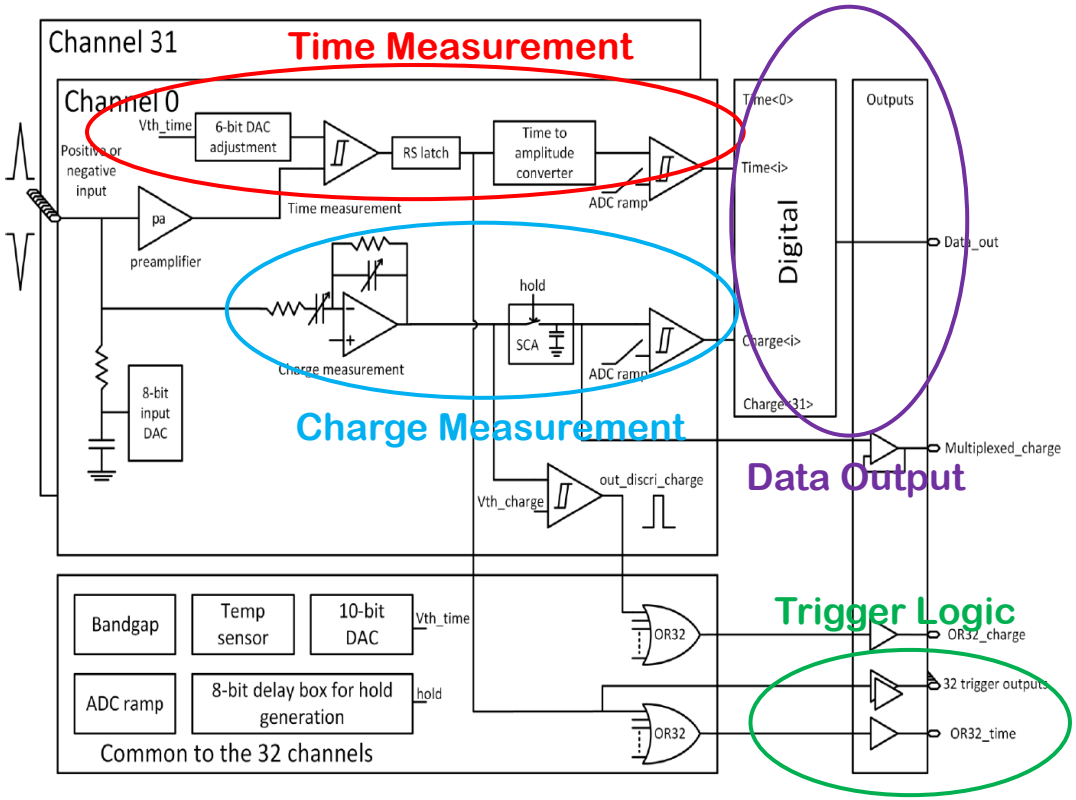
- High resolution timing measurement (<100 ps)
- High-granularity => large channel density
- Low power consumption

The HARDROC ASIC doesn't support high timing measurement.



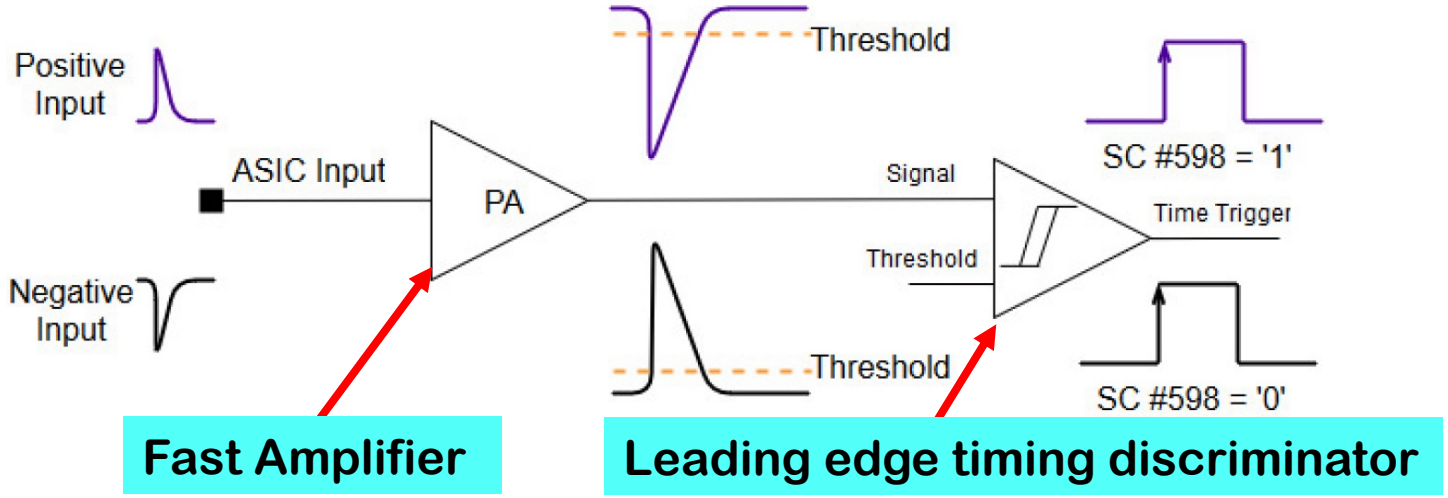
Example: Pi-(20 GeV), K-(10 GeV) separated by 15 cm

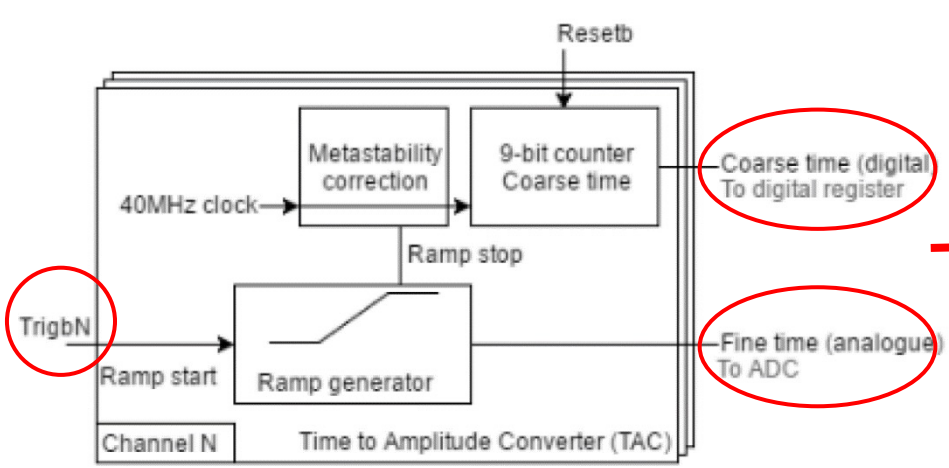
PETIROC ASIC from Weeroc

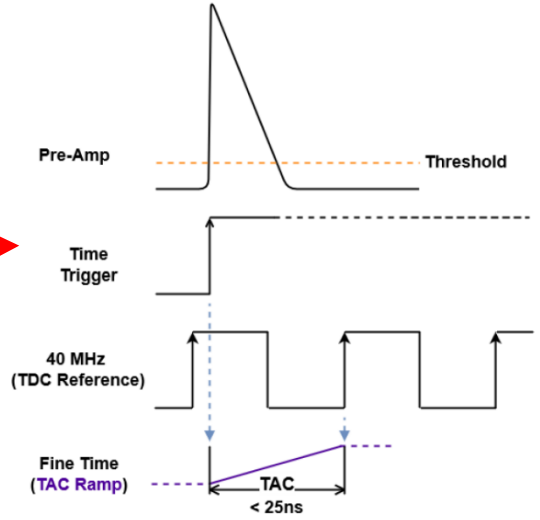


- A 32-channel front-end ASIC designed for SiPMs readout
- Charge and timing measurement
- 40 ps bin size of on-chip TDC
- Readout time: 12us
- Fast trigger line output
- Dynamic Range 0-480 pC i.e. 3000 photoelectrons @ 10^6 SiPM gain
- Power consumption 6mW/channel

Timing measurement @ PETIROC2A







Front-end electronics board

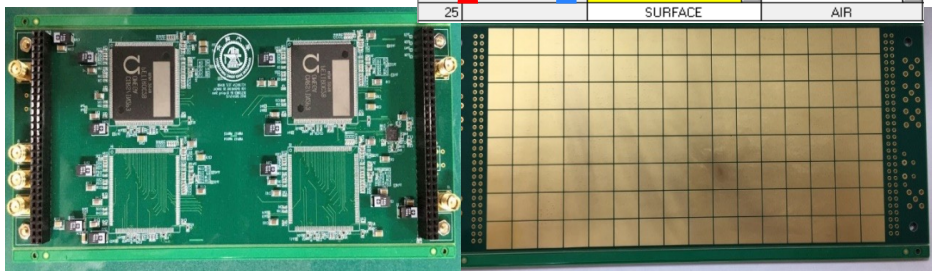
A small FEB prototype

- 12 layer structure
- Laser-drilled via-in-pad
- Buried vias

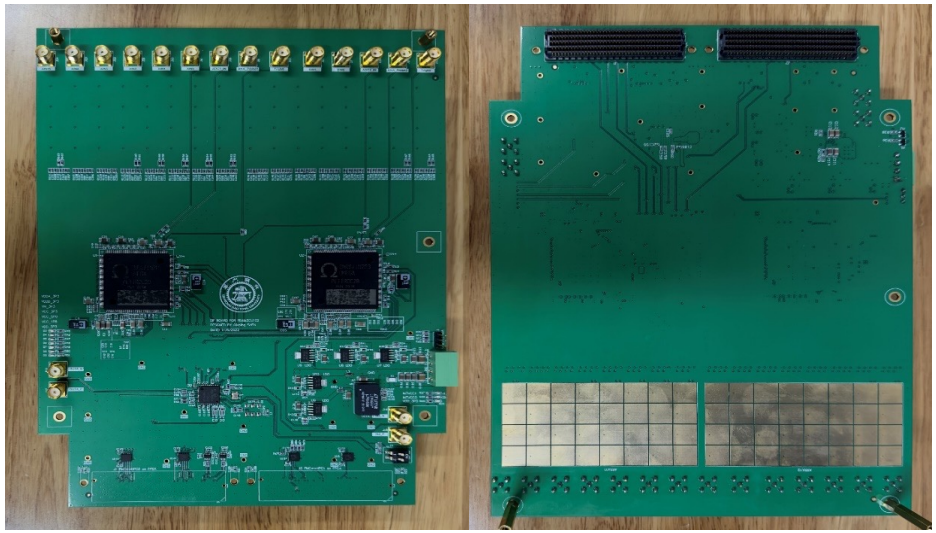
2nd-version of FEB has been designed and fabricated

- 2 Petirocs on-board
- Power rails designed on board
- 64-channel input pads
- Crosstalk issue in injection tests has been fixed

		SURFACE	AIR
1			
2	TOP	CONDUCTOR	COPPER
3		DIELECTRIC	FR-4
4	GND1	CONDUCTOR	COPPER
5		DIELECTRIC	FR-4
6	SIG1	CONDUCTOR	COPPER
7		DIELECTRIC	FR-4
8	SIG2	CONDUCTOR	COPPER
9		DIELECTRIC	FR-4
10	GND2	PLANE	COPPER
11		DIELECTRIC	FR-4
12	VDDA	PLANE	COPPER
13		DIELECTRIC	FR-4
14	VDDD	PLANE	COPPER
15		DIELECTRIC	FR-4
16	GND3	PLANE	COPPER
17		DIELECTRIC	FR-4
18	SIG3	CONDUCTOR	COPPER
19		DIELECTRIC	FR-4
20	SIG4	CONDUCTOR	COPPER
21		DIELECTRIC	FR-4
22	GND4	CONDUCTOR	COPPER
23		DIELECTRIC	FR-4
24	BOTTOM	CONDUCTOR	COPPER
25		SURFACE	AIR

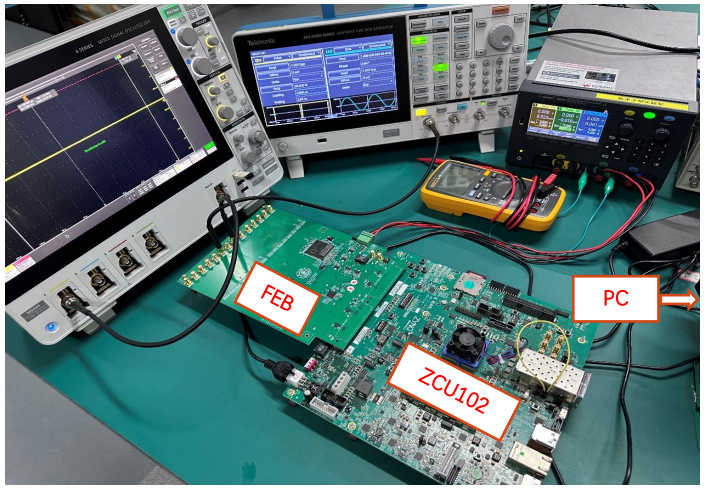


FEB v1

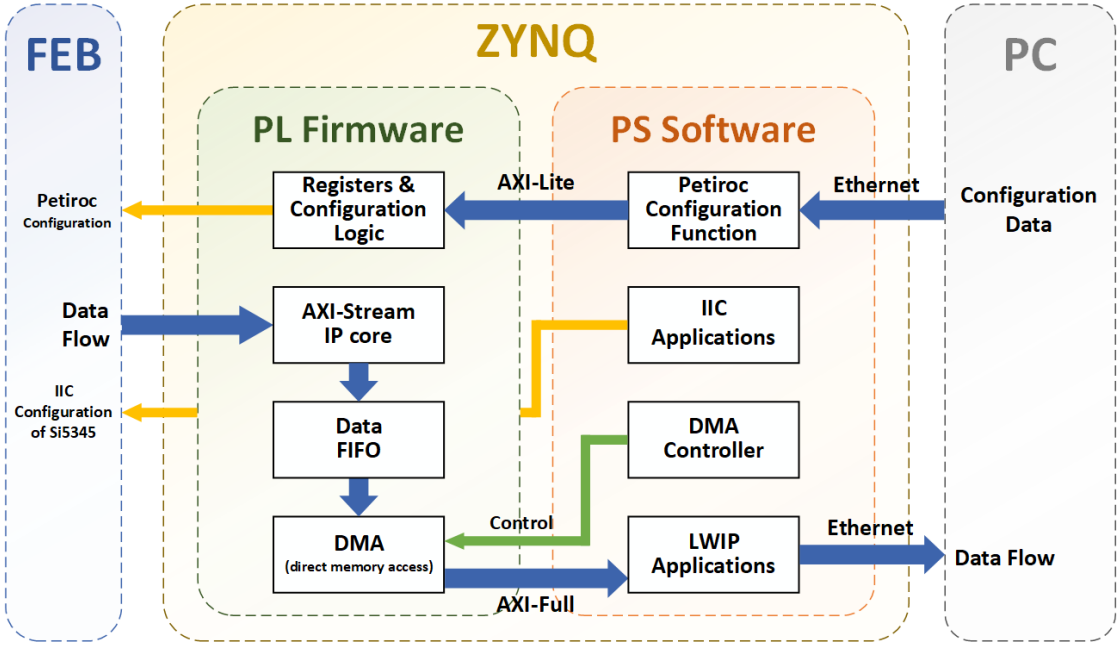


FEB v2

FPGA system



The DAQ system based on commercial FPGA evaluation board: ZCU102

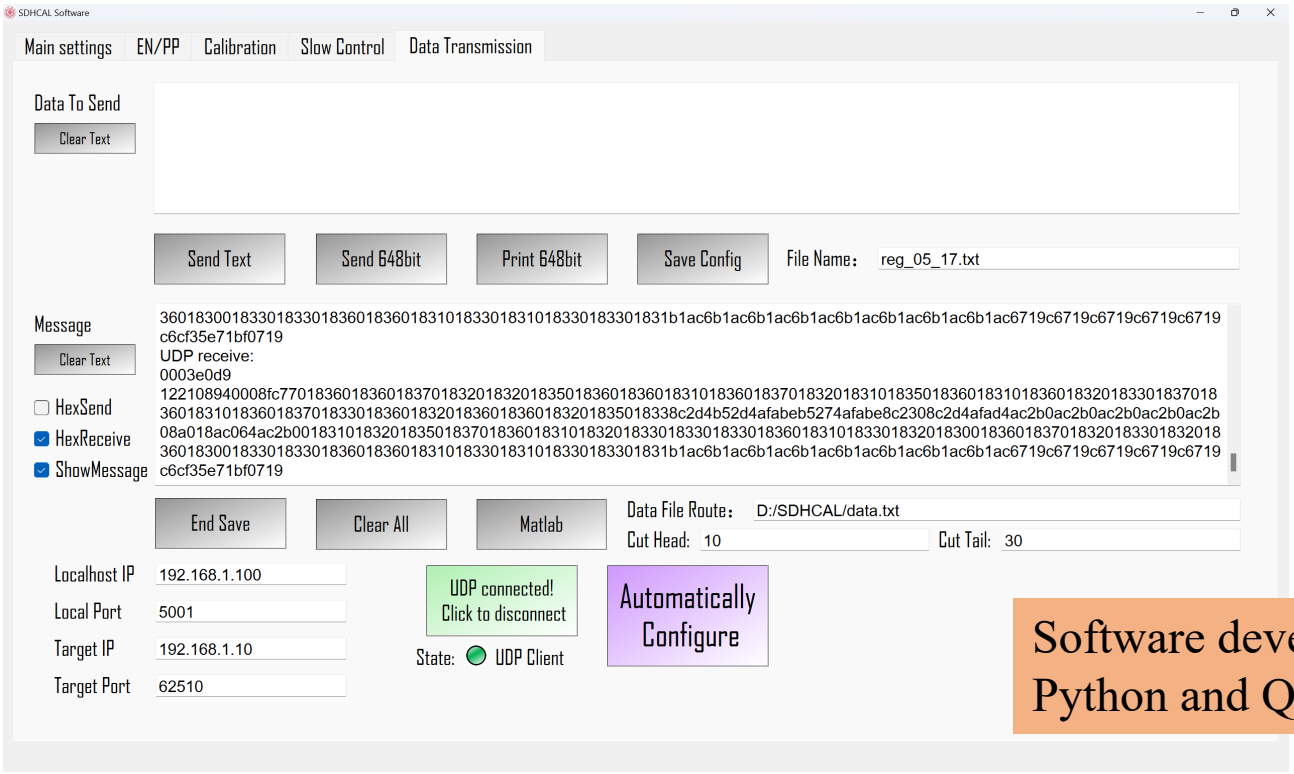


Hardware is based on ZCU102 evaluation board with Zynq UltraScale+ SoC

LWIP data transmission based on processing system (PS)

Other logic cores in programmable logic (PL) for configuration and data transmission

GUI software



Software developed with Python and Qt5

Generating 648-bit configuration data flow and send through Ethernet

Receive and decode data from FEB

Tune the threshold of each channel to enhance the uniformity

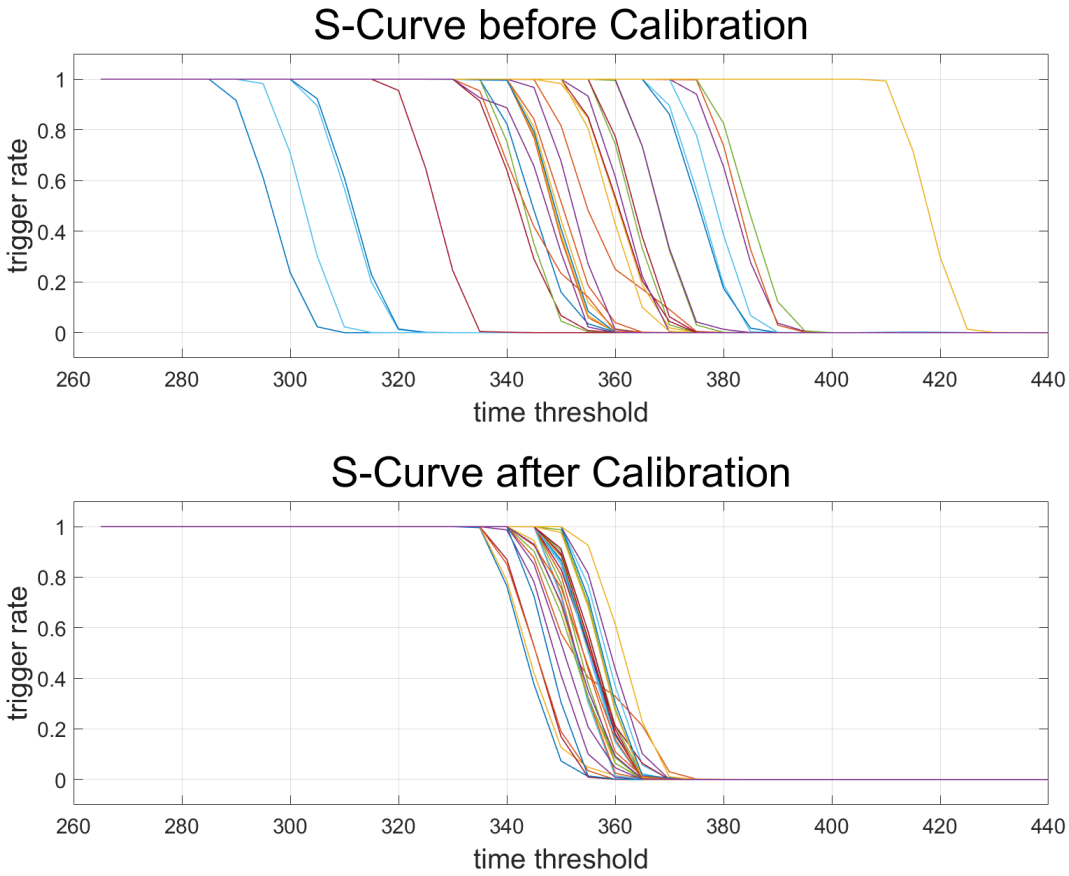
Calibration

The threshold of each channel can be dispersive

S-curve test based on the pre-amplifier baseline

Tune the threshold for each channel through a local 6-bit DAC

The RMS of 50% trigger rate threshold reduces from 25.3 DAC to 4.56 DAC



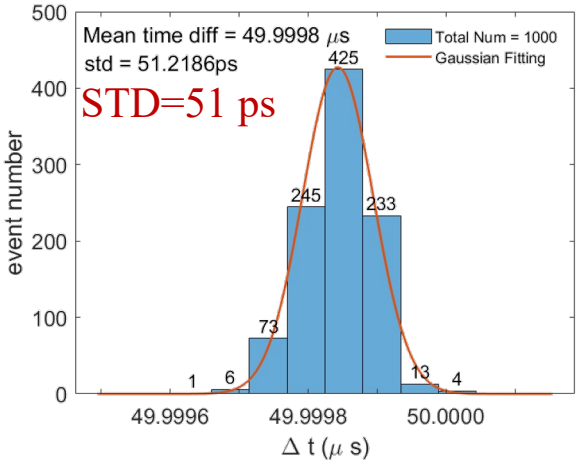
Injection test for timing evaluation

Single channel injection

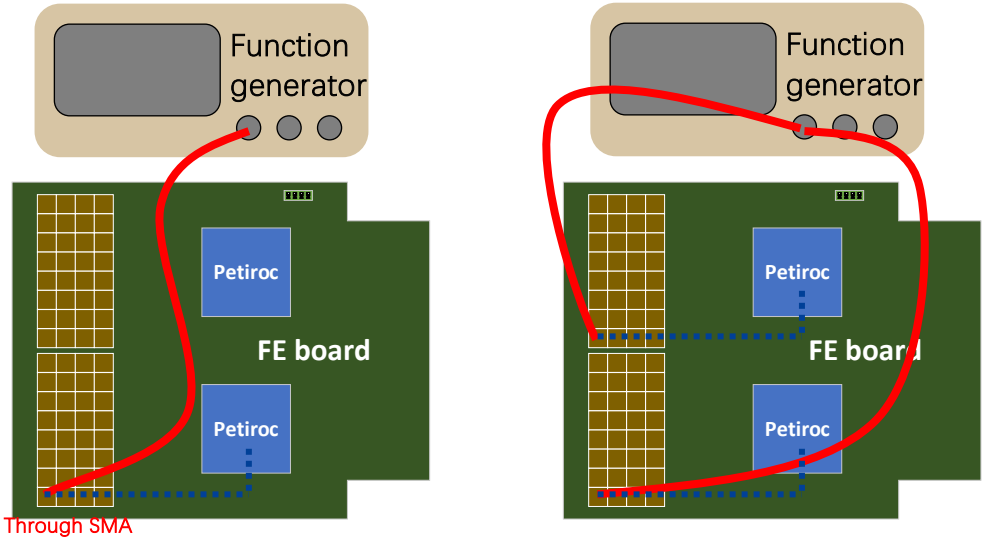
Inject periodic signal into one channel, measure the time differences of every neighbor hits

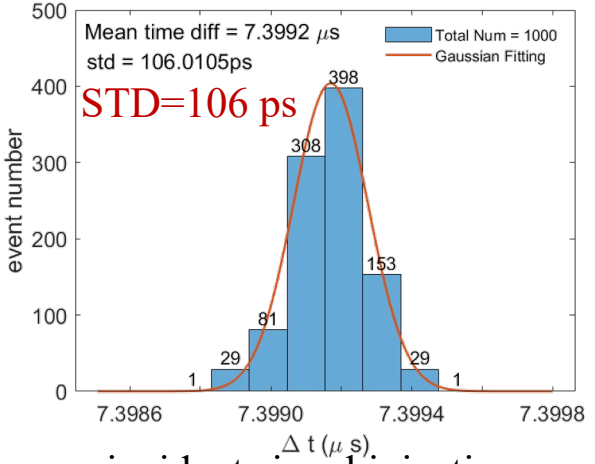
Coincident signal injection

Inject identical signals into two ASICs, measure the time differences of the identical hits between two ASICs



single channel injection





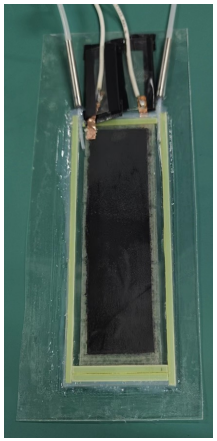
coincident signal injection

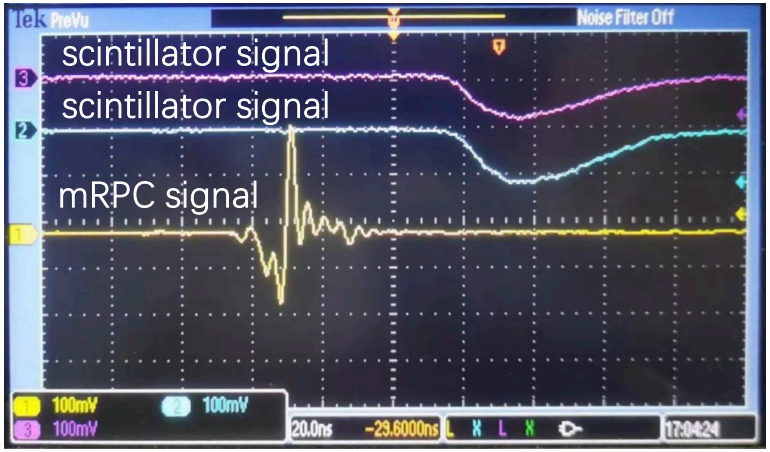
Tests with mRPC（ongoing）

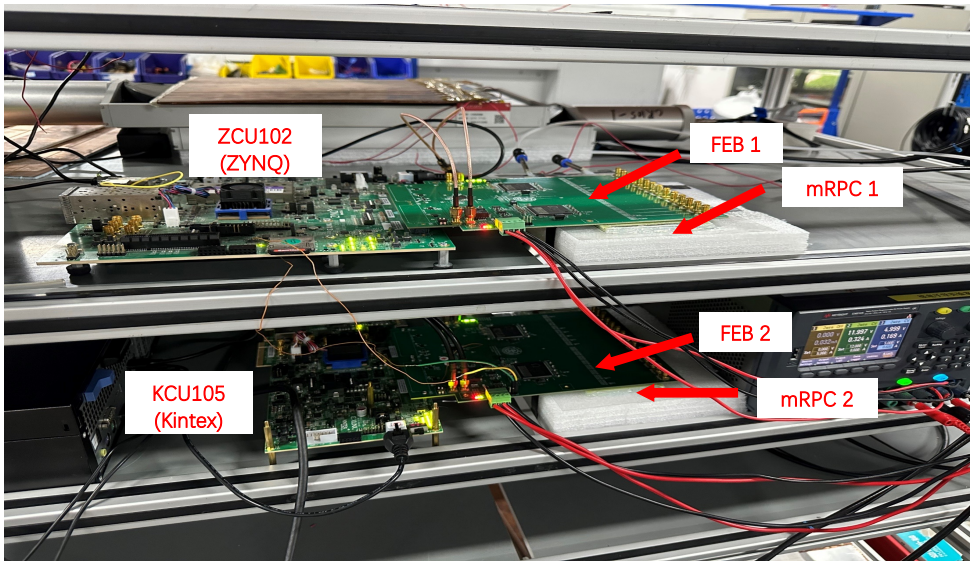
Use copper strips and oscilloscope to read out mRPC signals.

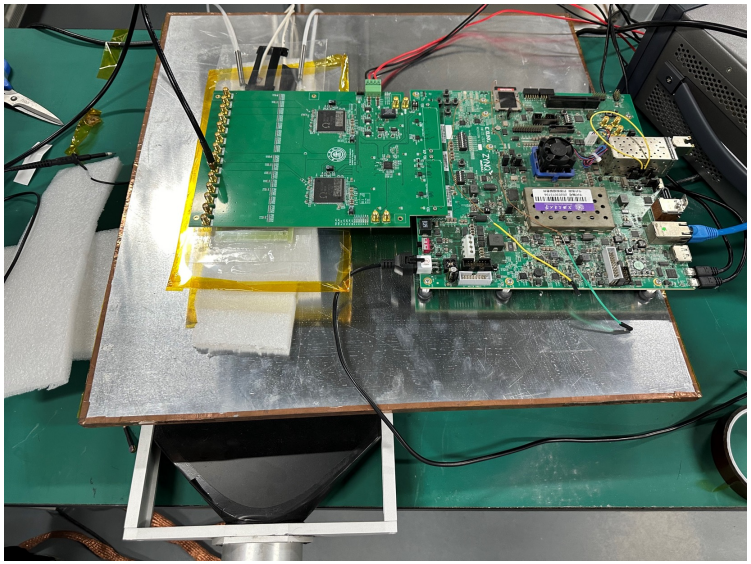
The mRPC signals is quite noisy.

We're still debugging on this.









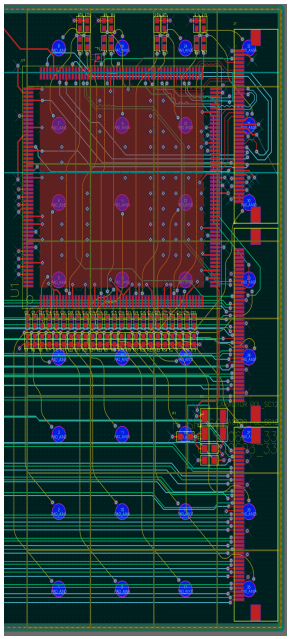
Large-sized prototype (ongoing)

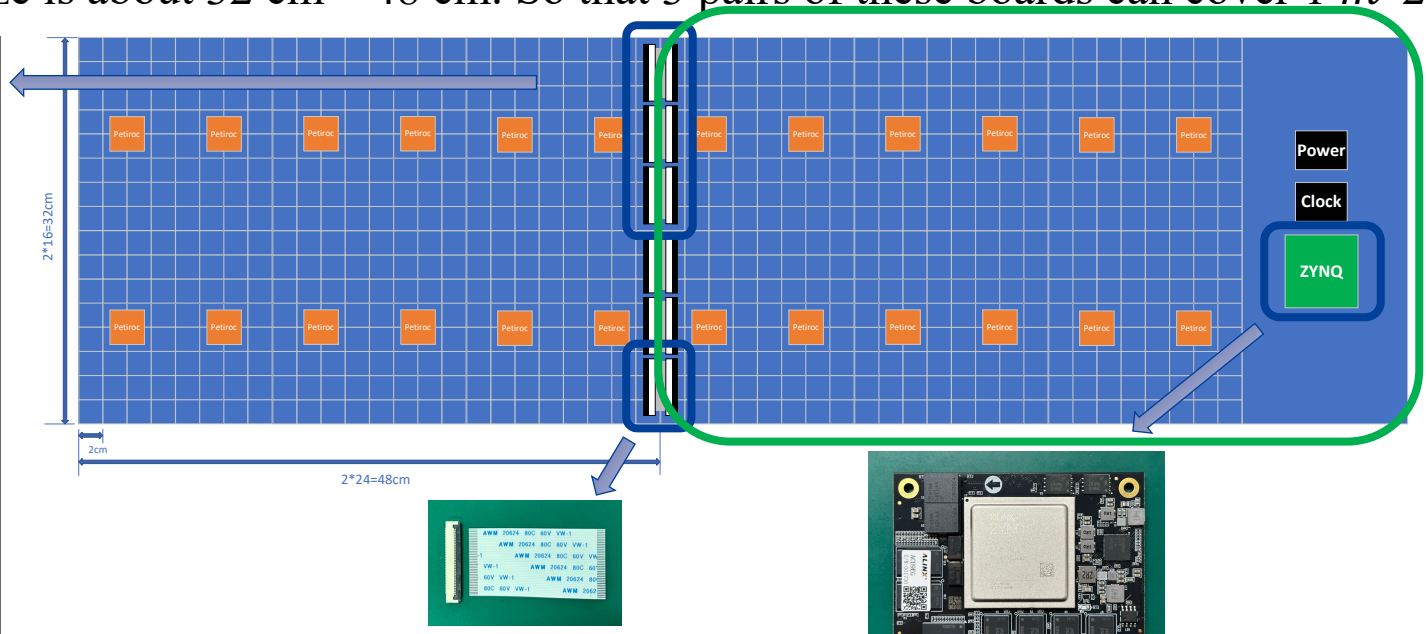
Design two boards, which are connected together by tiny connectors.

The length of each PCB board should be <75cm, limited by the PCB technology

Each PCB board has 12 Petirocs (384 channels).

The size is about 32 cm * 48 cm. So that 3 pairs of these boards can cover 1 m^2

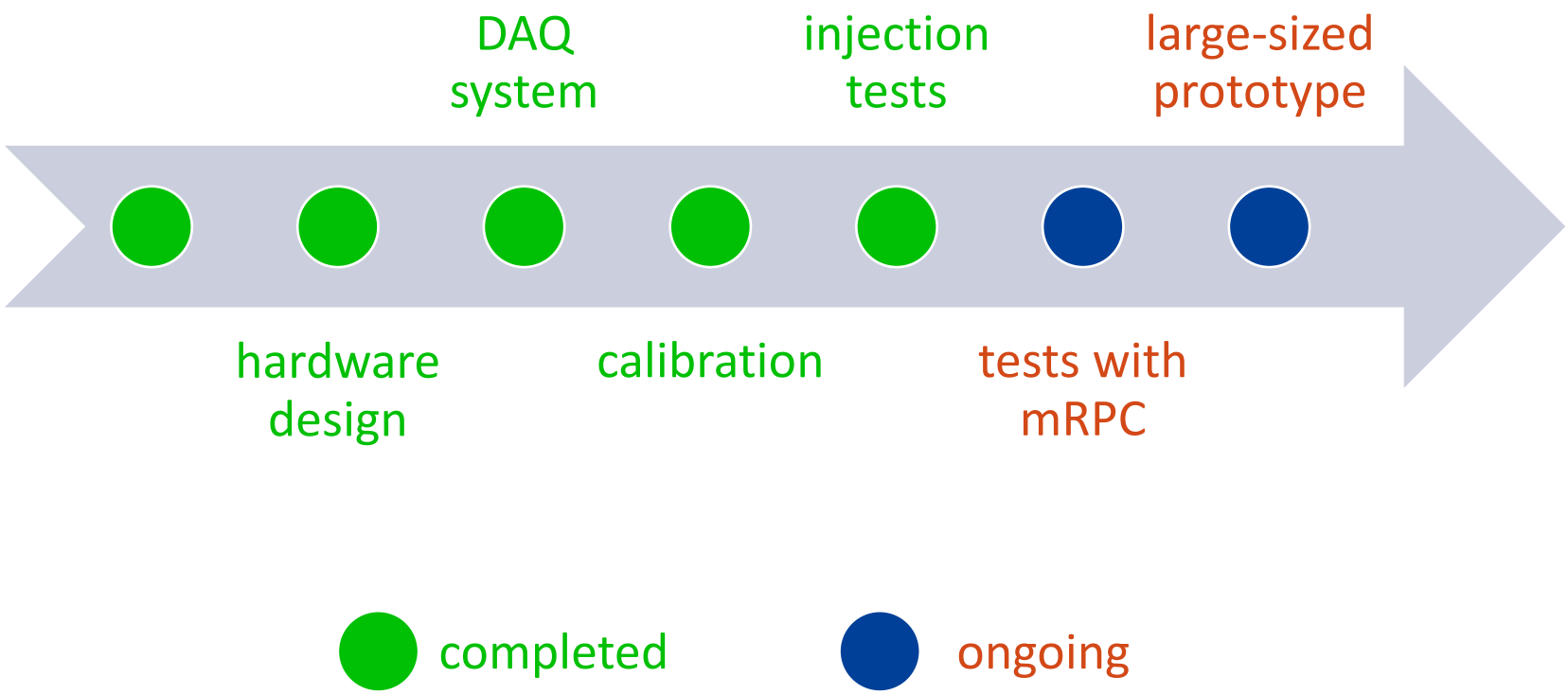




Tiny connectors with a height = 2mm

FPGA core board, already bought

Timeline of the prototype



Summary

Timing information can help event build in SDHCAL.

The timing electronics are designed based on Weeroc Petiroc ASIC.

A small prototype of electronics has been developed.

- The front-end board has two Petirocs.
- The DAQ system based on Zynq FPGA has been developed.
- A GUI software has been developed.

The performance evaluation tests validate the electronics system.

The commissioning test with mRPC is ongoing.

A larger size prototype is been developed.

Thanks!