Manufacturing of High Rates Resistive Micromegas (RHUM* Project)

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DRD1 Collaboration Meeting

18 June 2024 CERN

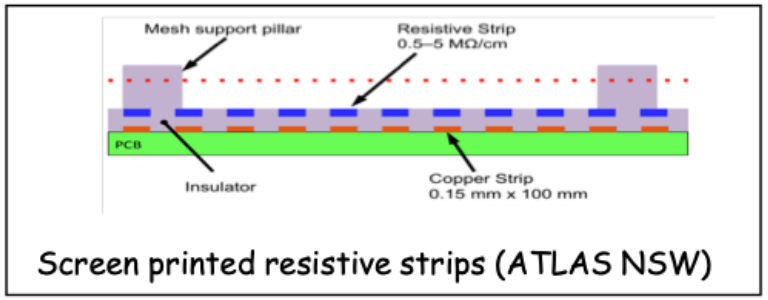
* Resistive High granUlarity Micromegas

Recent developments on resistive Micromegas

One-slide summary from Rui De Oliveira (RD51 MPGD School – December 2023)

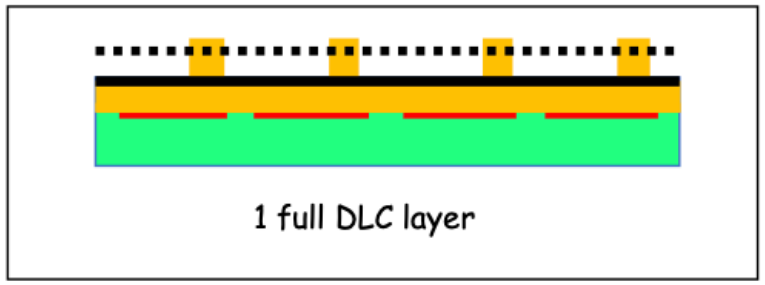
All Resistive MM structures

Medium-rate detectors 100kHz/cm2
Side evacuation of the charges



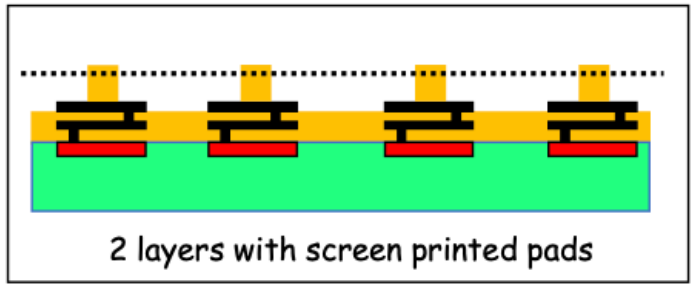
Screen printed resistive strips (ATLAS NSW) — 2013

or



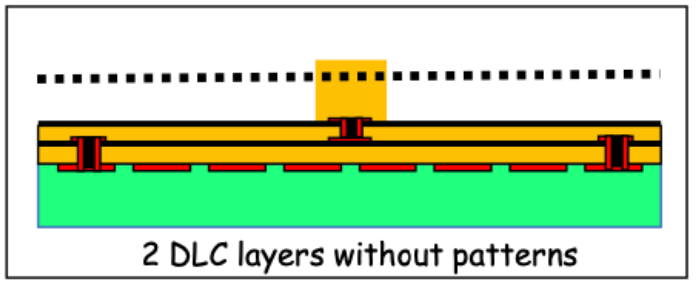
1 full DLC layer — 2015

High-rate detectors 10Mhz/cm2
Charge evacuation inside active area



2 layers with screen printed pads — 2015

or

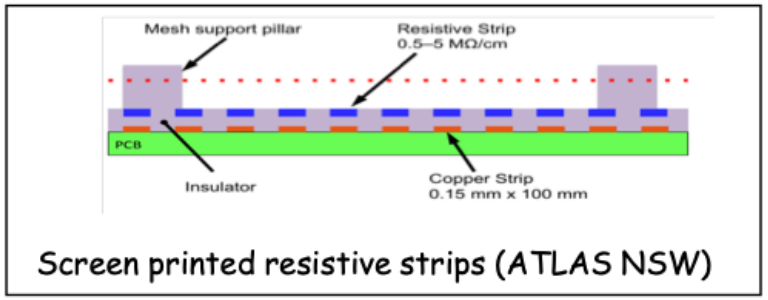


2 DLC layers without patterns — 2020

Recent developments on resistive Micromegas

All Resistive MM structures

Medium-rate detectors 100kHz/cm2
Side evacuation of the charges



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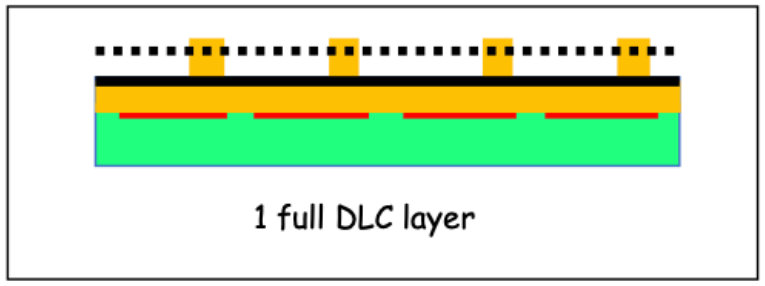

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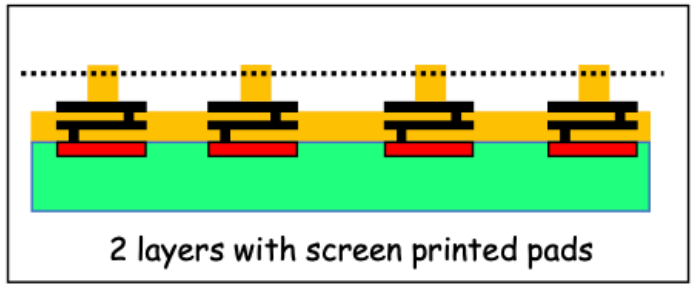

2 layers with screen printed pads — 2015

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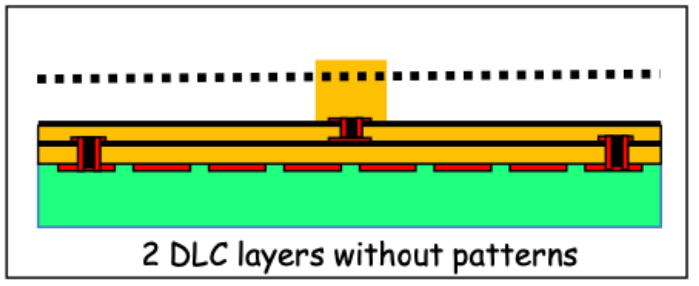


2 DLC layers without patterns — 2020

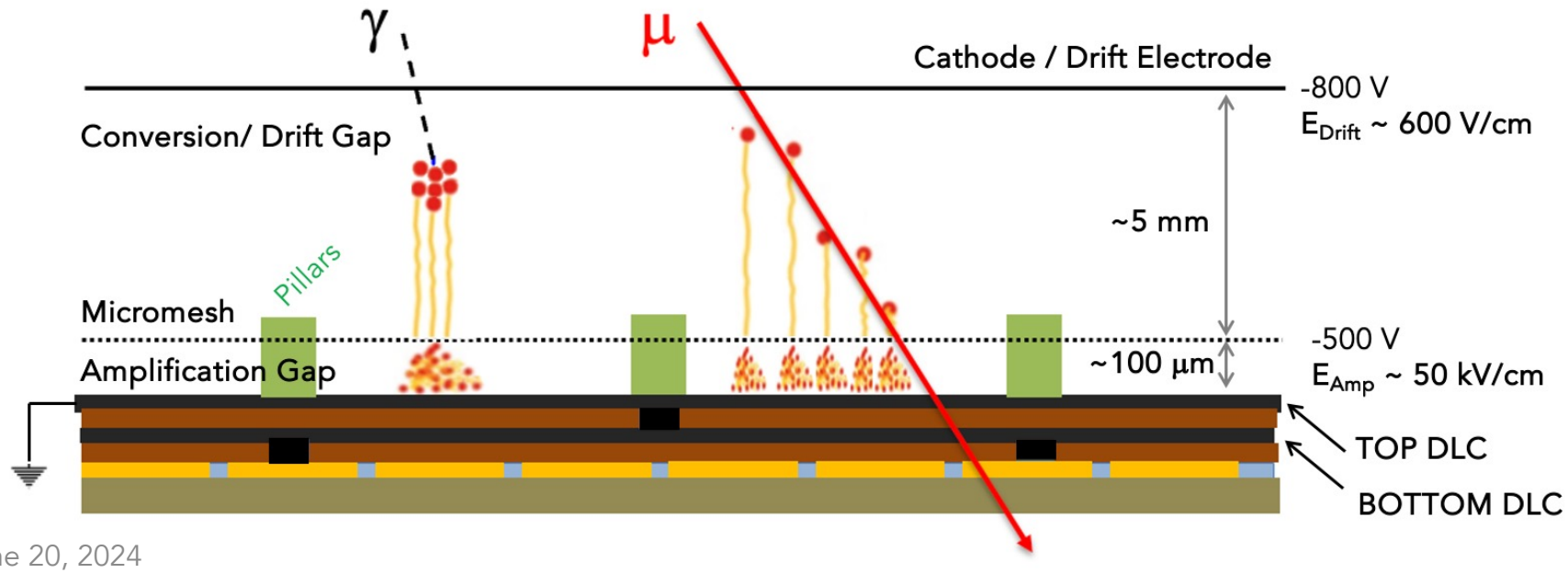
This is the journey of the RHUM project

Double DLC layer Micromegas Concept

- Configuration inspired by G. Bencivenni and co-authors (applied to uRWell) (JINST 12 (2017) 06, C06027)
- Readout pads are covered by a **double layer of DLC** with a grid of staggered interconnecting vias for rapid charge evacuation → Charge evacuation inside the active area, through "vertical dots"
- First generation: Grounding connection vias "filled manually"
- Second generation: the sequential build up technique (SBU) was implemented exploiting copper-clad DLC foils. It allows best alignment of vias and connections by plating techniques. Fully compatible with PCB manufacturing techniques
  (Rui De Oliveira at INSTR 2020)

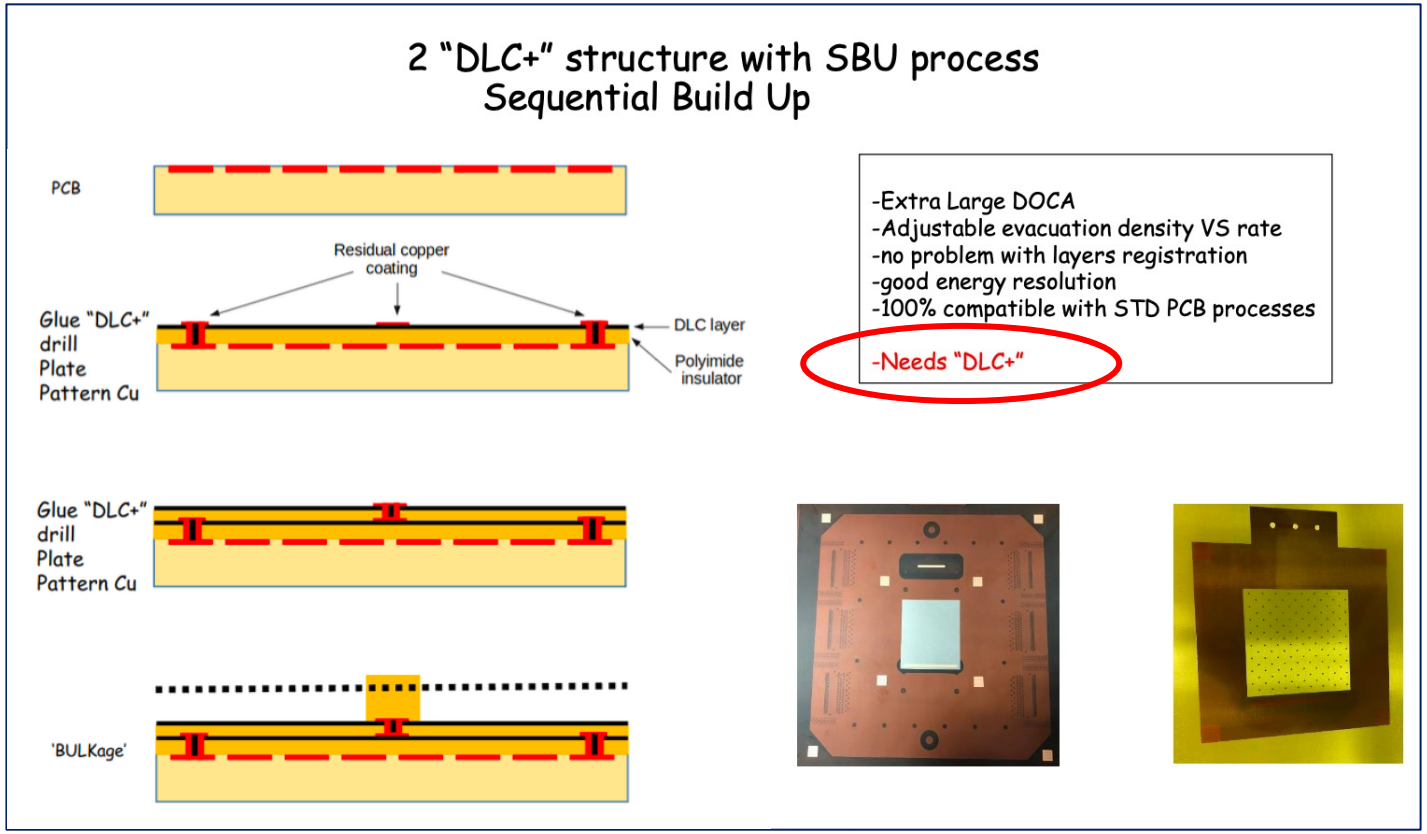
Typical (optimal) DLC resistivity for high rates:

20 – 40 MΩ/sq



Double DLC layer Micromegas Manufacturing

Rui's talk at INSTR 2020



Double DLC layer Micromegas Manufacturing

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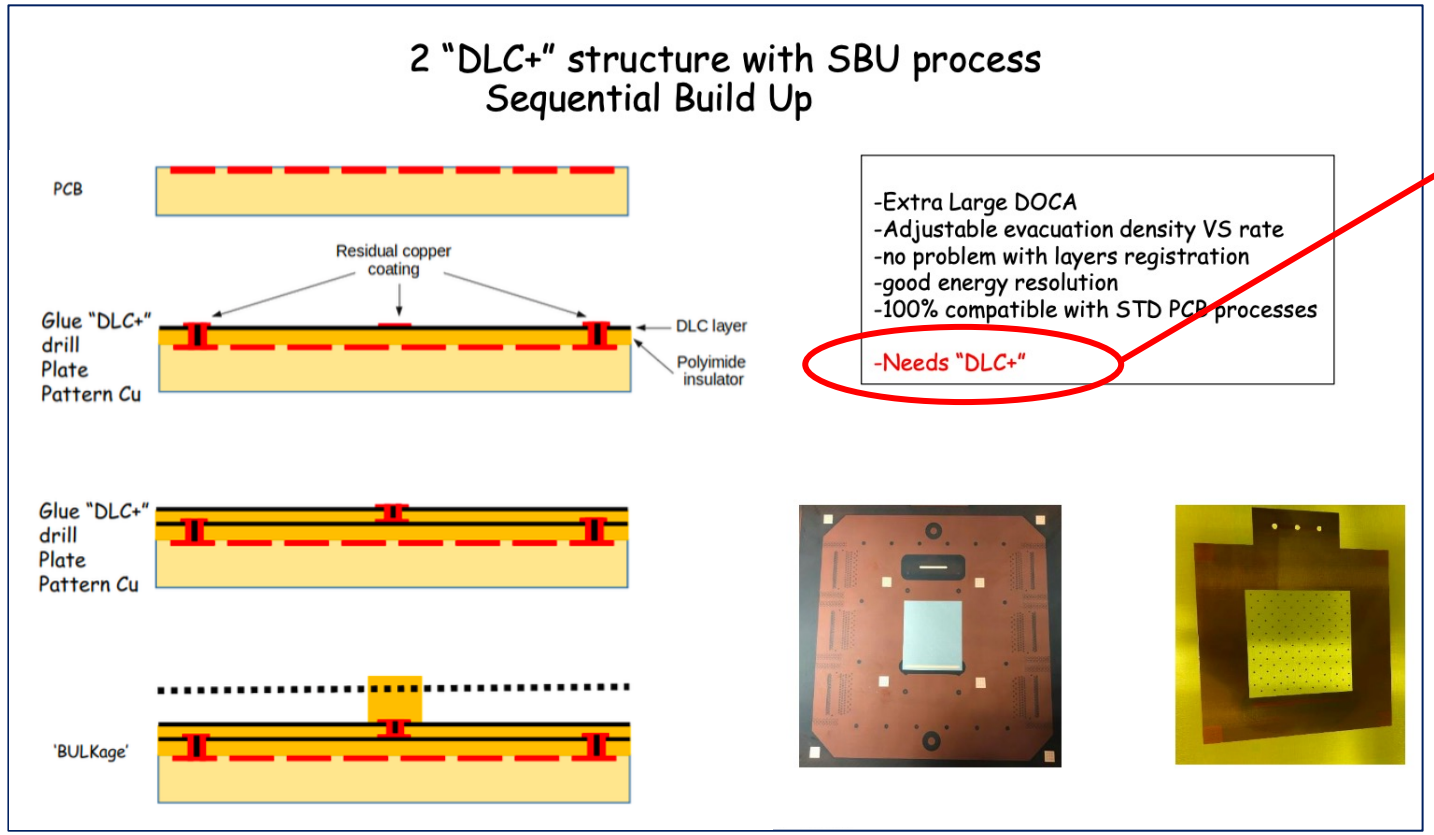


CERN-INFN Sputtering Machine @ CERN

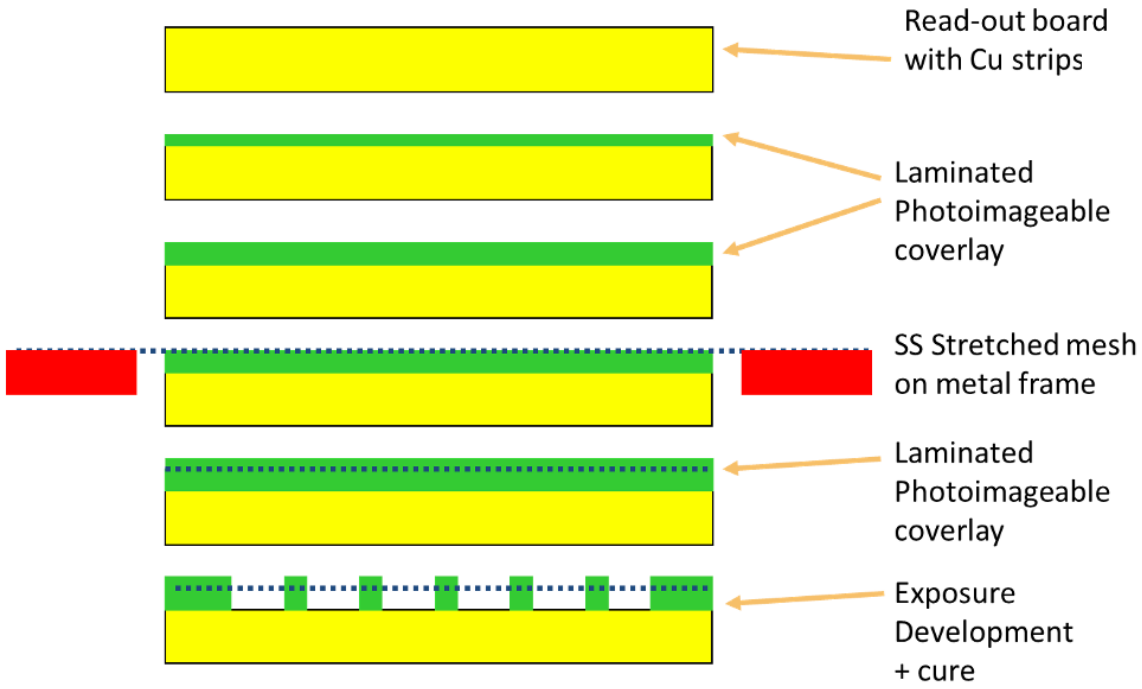
See Rui's talk today
and G. Morello 1st DRD1 Collab Meeting

Currently in these weeks a CERN-INFN team is carrying on new tests.

Very advanced production of large foils of copper clad "*DLC+*"

The "bulkage" i.e. how to trap and sustain the mesh in the pillars

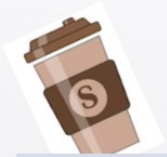
- The bulkage is a non-standard PCB process
- Needs manual work
- It is among the more expensive steps in the MM production.
- Simple in principle, however, faces significant challenges when applied to industrial contexts.



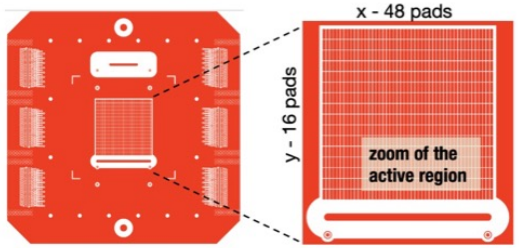
MATERIAL

- Photo imageable coverley
  was Pyralux → now Dynamask
- Stretched mesh:
  - Frames
  - Stretching process
  - Clean, high-quality mesh (18/45)

Our Production at CERN - Towards Large Area



small size prototypes

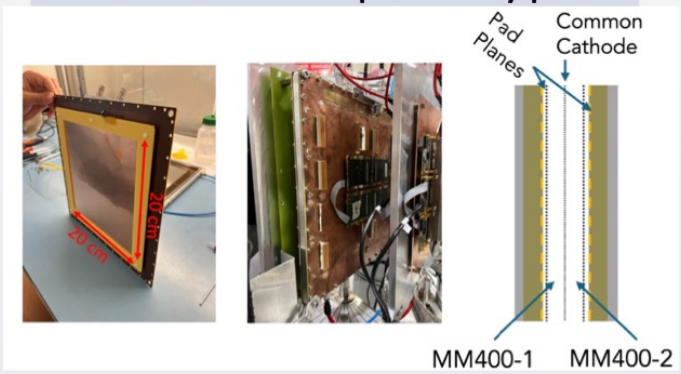


active area : 4.8cm x 4.8 cm

segmented in 48 x16 readout pads

pad size: 1 x 3 mm^2

medium size prototypes

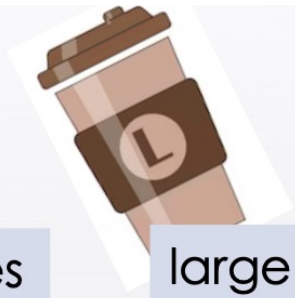


Two detectors Paddy400-1 and Paddy400-2

active area : 20 cm x 20 cm (40% readout in central part)

Anode plane pad size: 1x 8 mm^2

also tested in sandwich config sharing the same cathode



large size prototype

"The Big one"
Paddy-2000: 50 x 40 cm^2

Readout central region 6.4x6.4 cm^2 with1x8 mm^2 pads

Surrounding area – 2048 pads, 10x10 mm^2

Taken from M. Biglietti's talk on Monday

Critical steps in the resistive bulk MM manufacturing

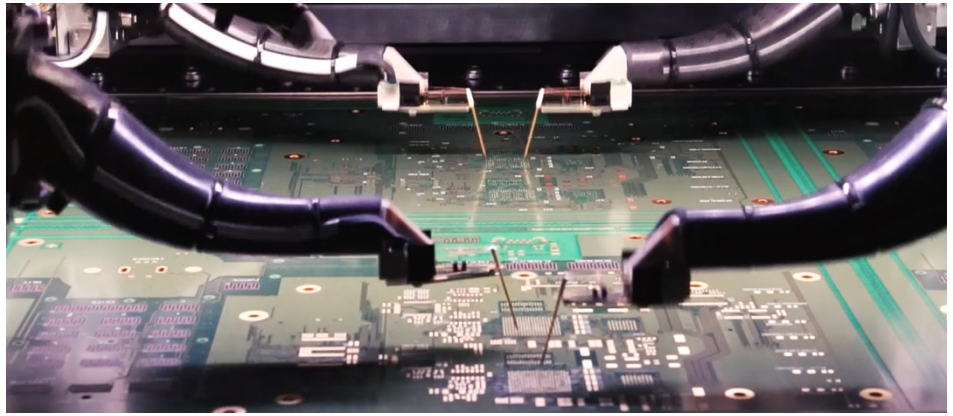
- High quality PCB manufacturing: easy to find at industry
  → caveat: Large size (multilayer) PCBs significantly reduce the market
- DLC with copper-clad: will be done "in house" with the magnetron sputtering machine available at CERN → more studies needed to launch production – ….almost got there!
- High quality mesh procurement and stretching on frames *(huge experience at Institutes from ATLAS)*
- "Bulkage"

For large productions (and for large requests of R&D prototypes) it is mandatory to:

- Transfer the technology of the most critical steps to the industry
- Keep the same level of quality/reliability/easy interaction as we are used with the MTP Workshop at CERN (very challenging!)
- Simplify, automatise, **reduce the costs $$$**

A step-by-step approach towards complete production at ELTOS SpA has been initiated

Micromegas Manufacturing at ELTOS



Preparation

Materials supplied by us :

- Design of the detector (Gerber files of PCB, DLC, coverlay, ..)

  Simplified version:

  - 10 x10 cm^2 active area, pad-size: 1x8 mm^2
  - Single DLC foil without dot evacuation vias
- One roll of photo imageable material – Dynamask - foils 45 μm thick
- Stretched mesh on frames
- Patterned DLC foils

→ Construction of two "identical" prototypes

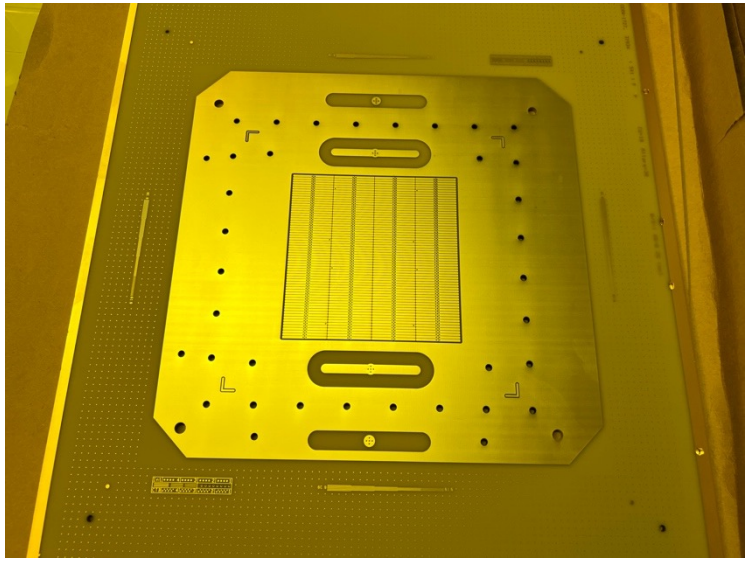
June 11-13, 2024

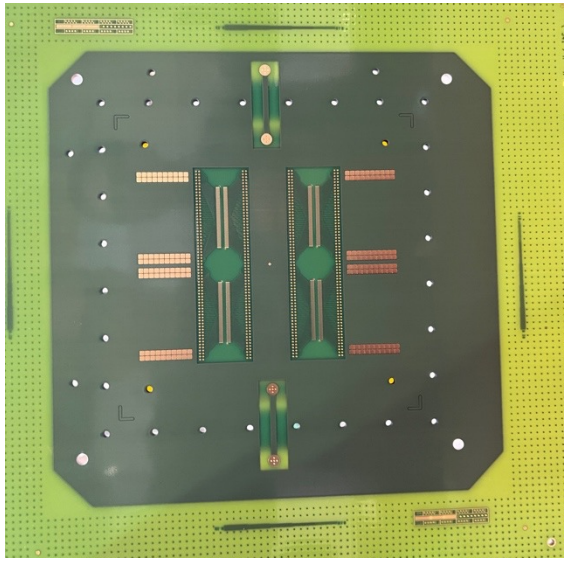
Micromegas Manufacturing at ELTOS

Main Steps of manufacturing at ELTOS

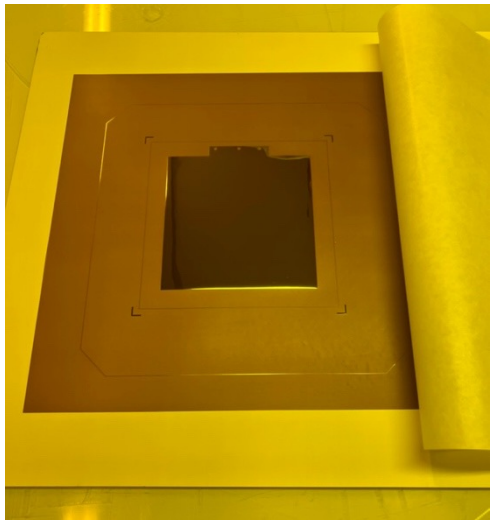
- PCB production(*)
- DLC foil inspection measurement and gluing/pressing on the PCB
- Bulkage: Lamination of Dynamask + mesh, exposure, development
- Quality checks and Metrology

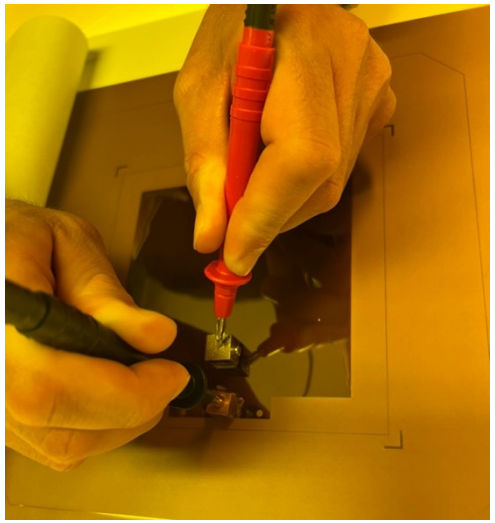
(*)





DLC Foils

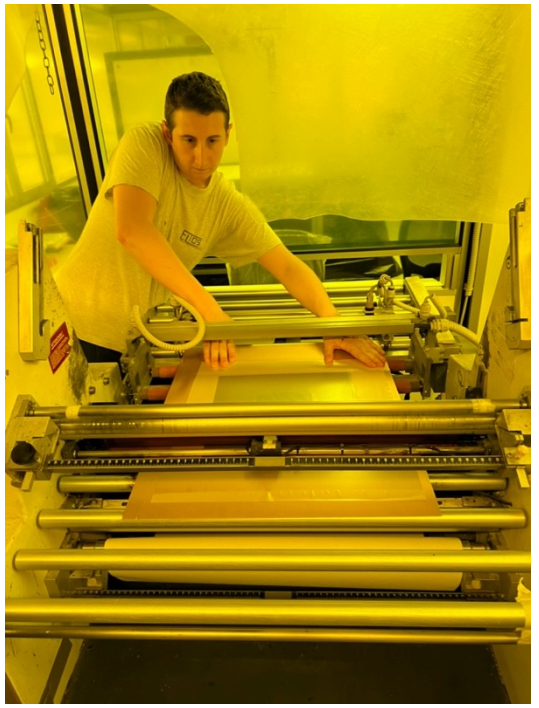


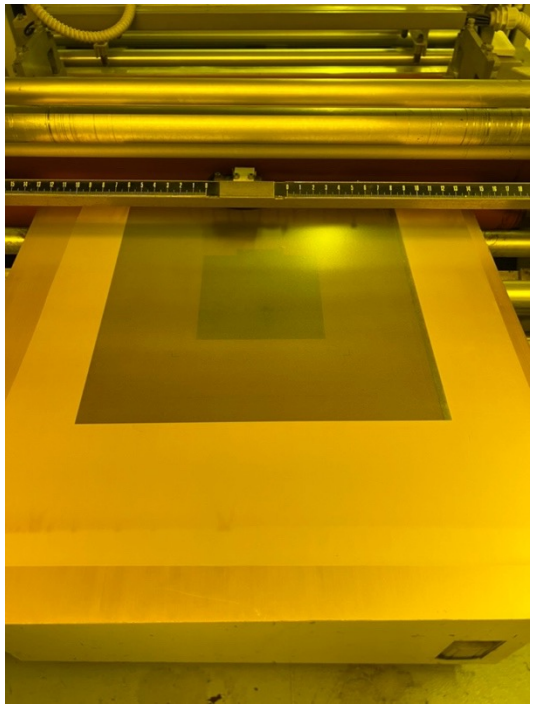


Resistivity map

- Avg DLC1: 29 MOhm/sq
- Avg DLC2: 32 MOhm/sq

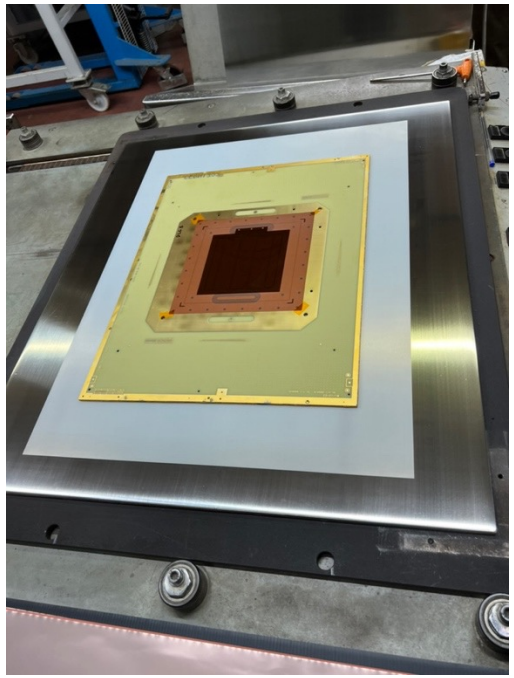
Glue lamination



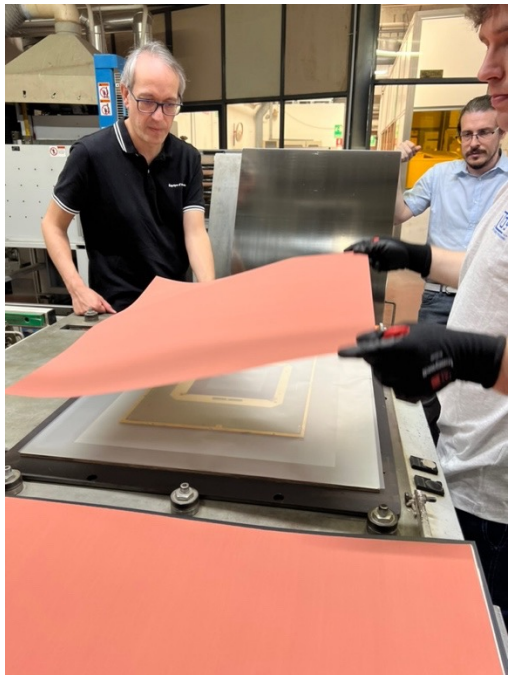


Glue: Akaflex, thickness 25 μm

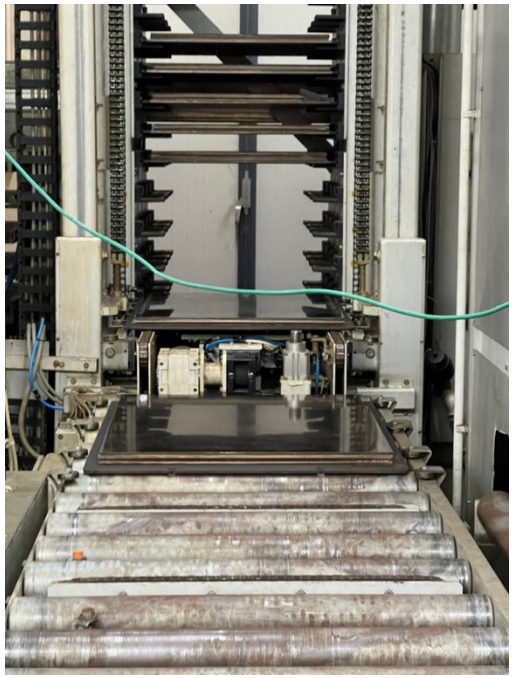
DLC pressing



DLC positioned on the PCB

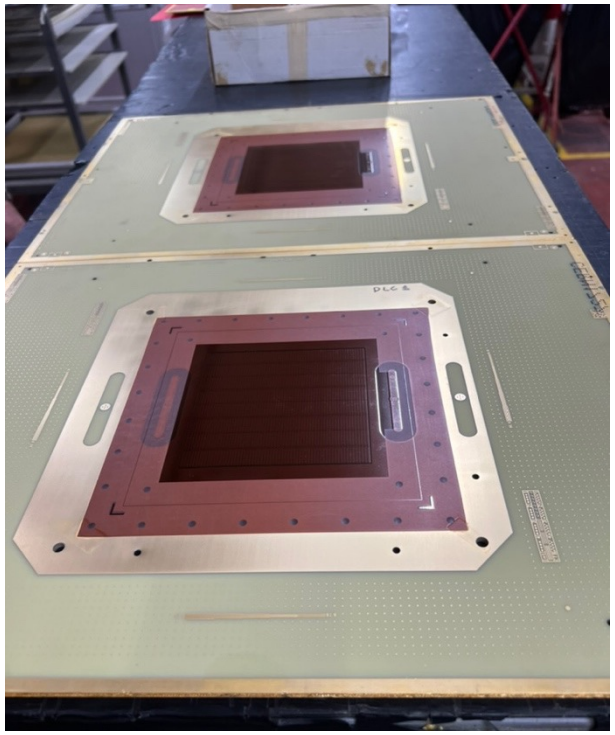


Pressing stack preparation with layers of: copper, conformable layer (pacoflex), cushions, …



Sent to press and curing

DLC Foils

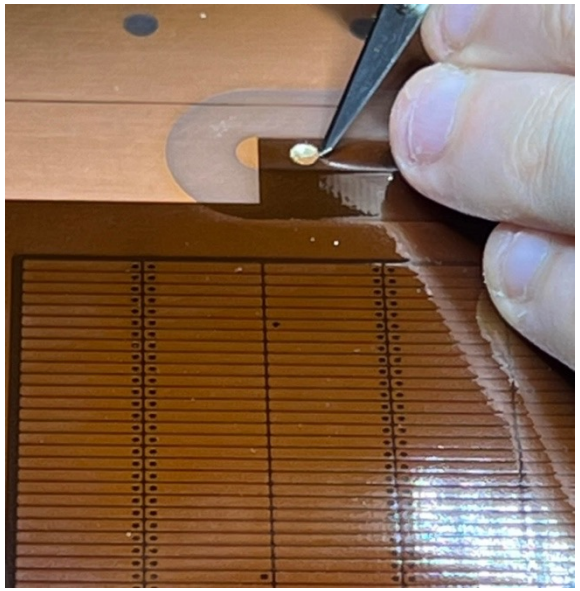


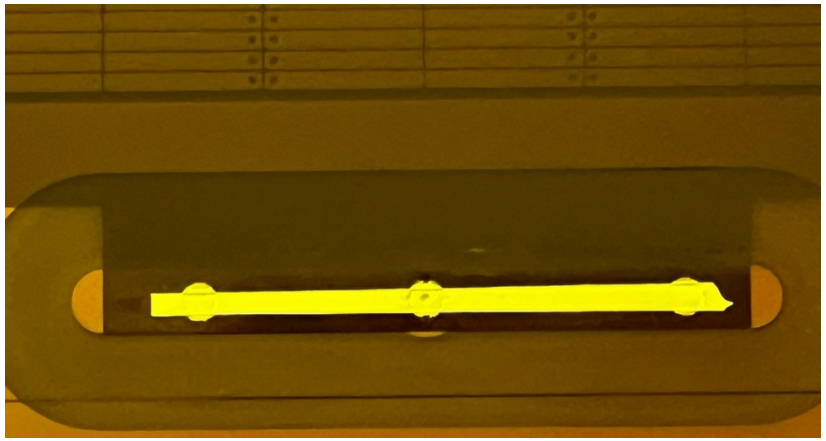
Resistivity map after pressing and curing:

- Avg DLC1: 38 MOhm/sq (was 29 → +30%)
- Avg DLC2: 36 MOhm/sq (was 32 → +12%)

(an increase is expected if DLC is not completely stabilised)

HV Connection with silver glue

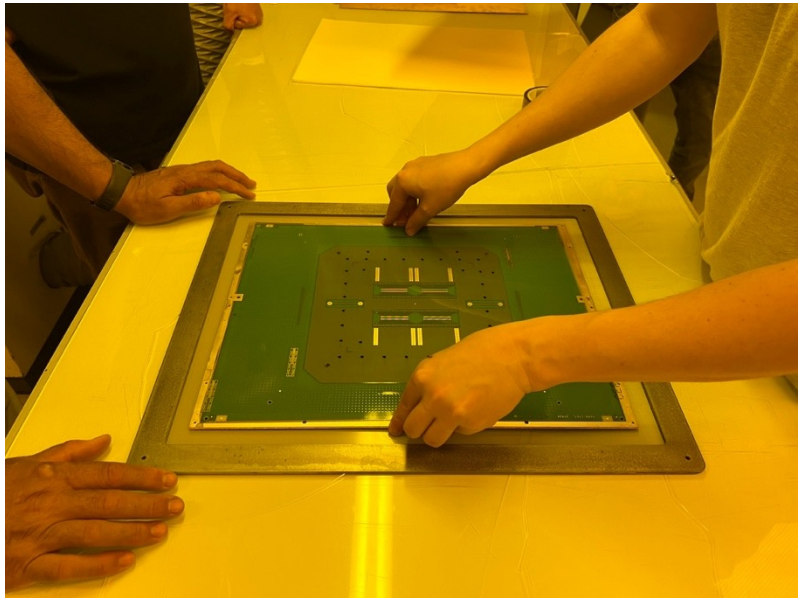




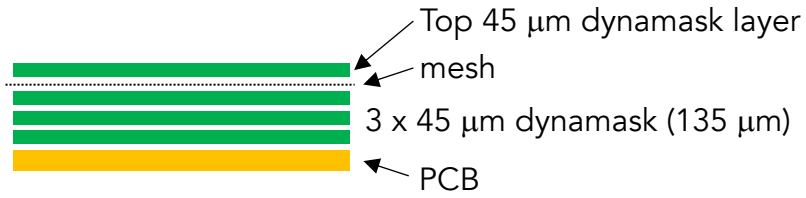
Manual intervention.
Can be simplified

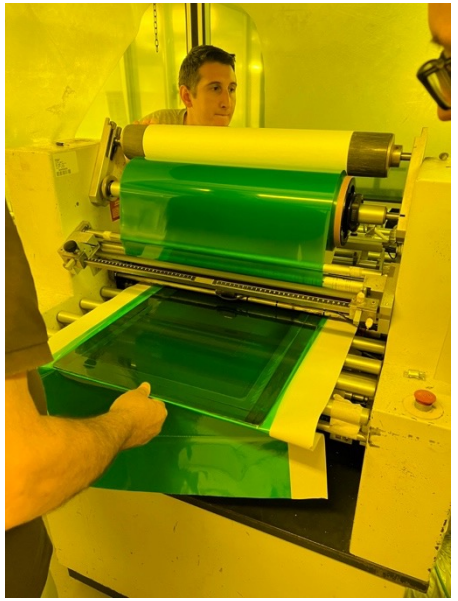
BULKAGE – lamination with Dynamask

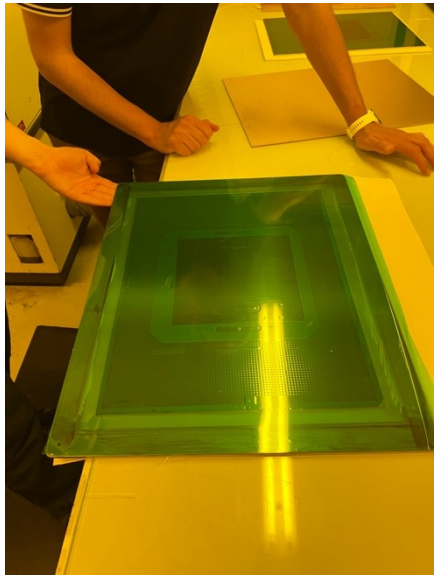
Dynamask thickness: 45 μm → 3 layers + mesh + top layer



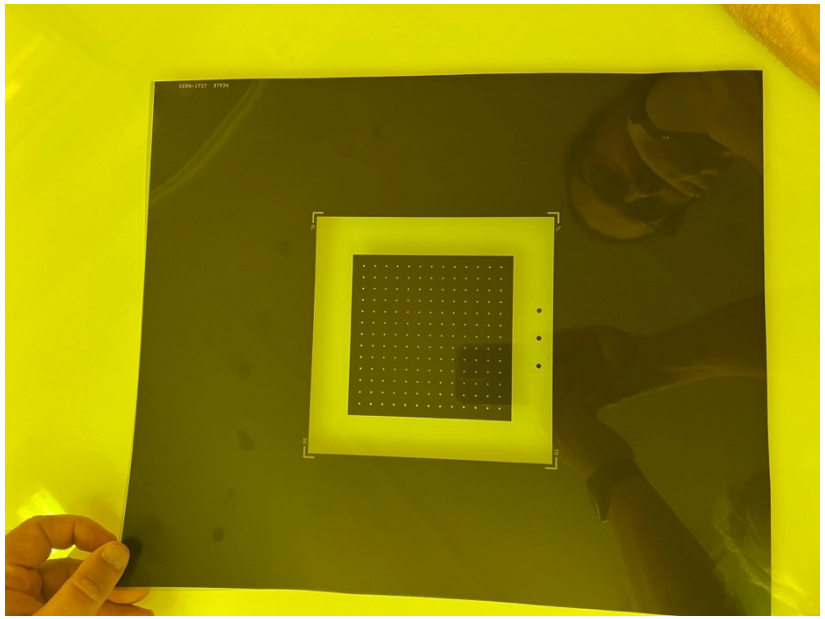
Laminated PCB positioned on the mesh before last (top) lamination

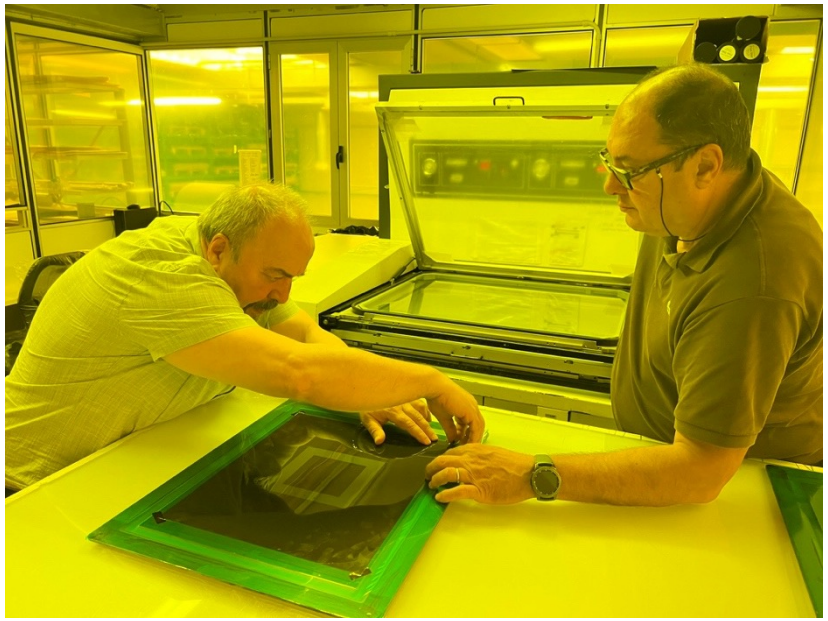






Bulkage – UV exposure



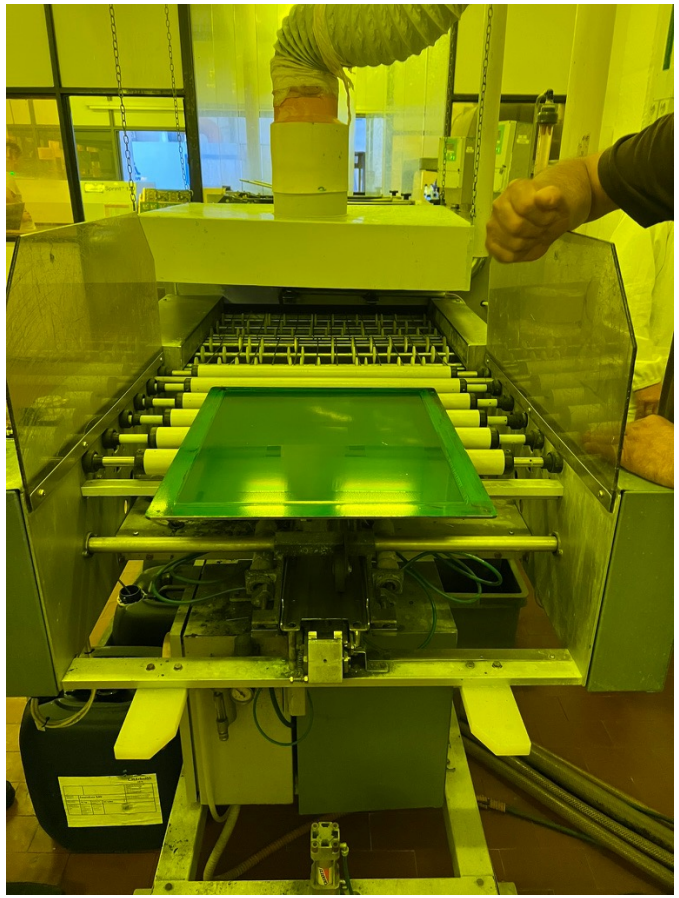


Mask with patterned coverlay and circles for pillars in the active area

Exposure: 900 mJoule

Bulkage - development

Transport in a diluted soda Solvay bath



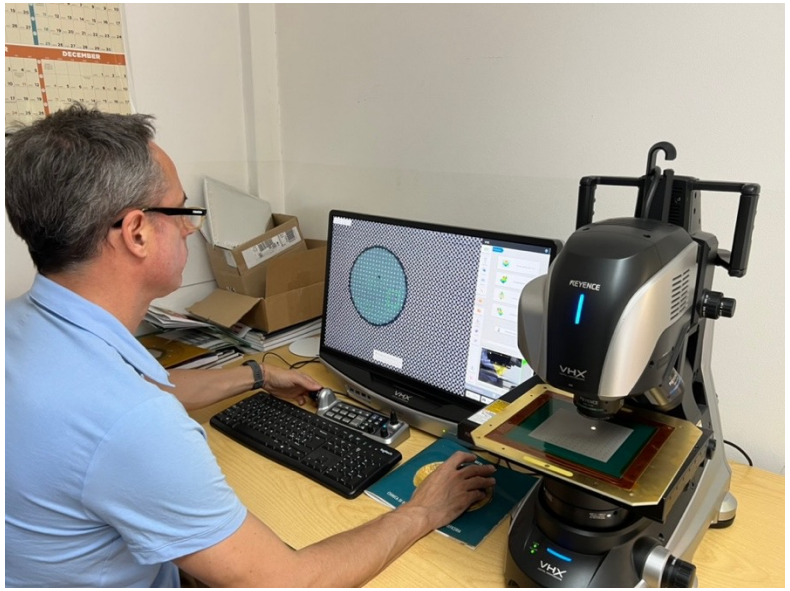
Bulkage – final curing

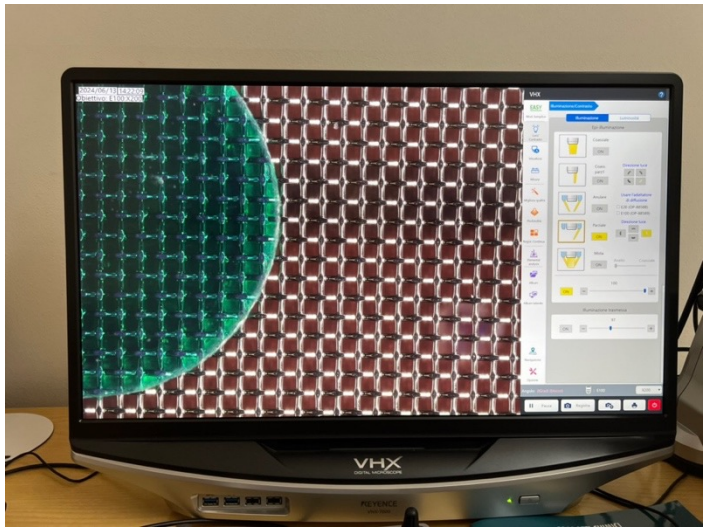
In the oven…

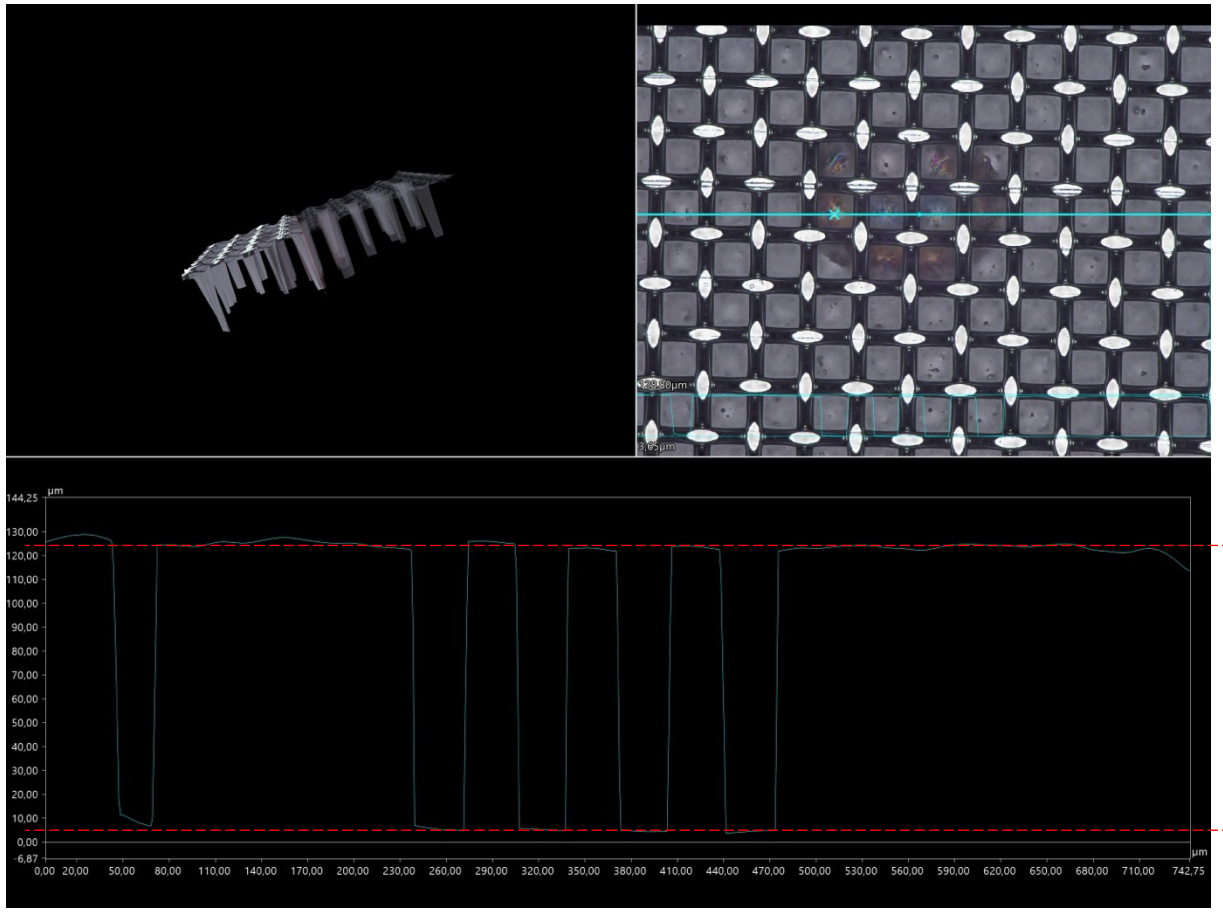
…DONE !

Metrology – a few examples

Estimate of the amplification gap size with the Keyence microscope







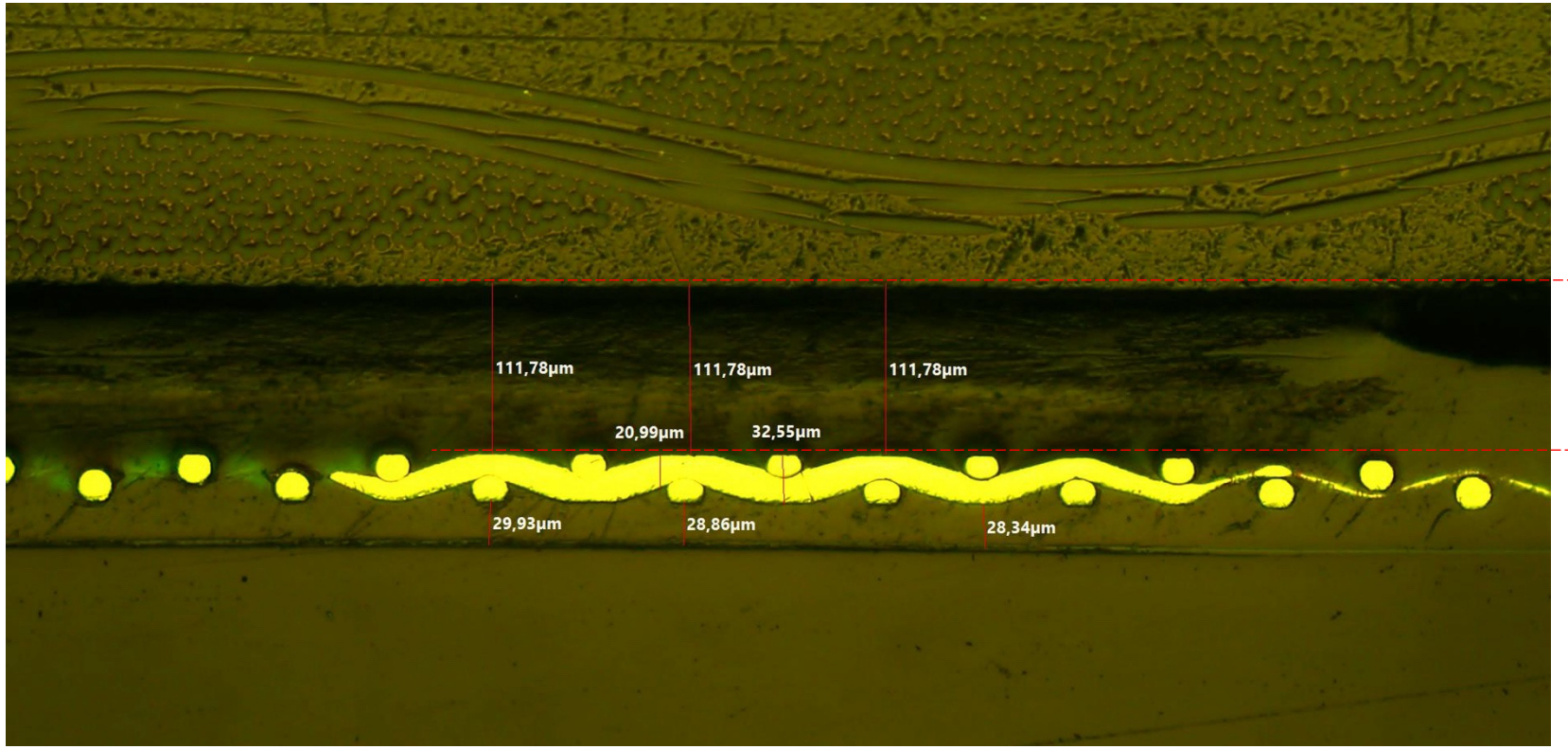
From the outer side of the mesh to the pad plane

→ **~102 µm** considering the wires thickness

As expected, the nominal thickness of 3x45 = 135 um of gap shrinks to a lower value.
However, ~102 um (accounting for 18 um of wire thickness in woven mesh) seems a bit too low ! …will investigate further

Metrology – a few examples

Estimate of the amplification gap size with metallography



~112 µm

From the pad plane (top in the photo) to the inner side of the mesh

As expected, the nominal thickness of 3x45 = 135 um of gap shrinks to a lower value.
A value of ~112 um is in line with expectations
(need to check the consistency of the two measurements – however we believe the metrology is a more accurate measurement)

Summary

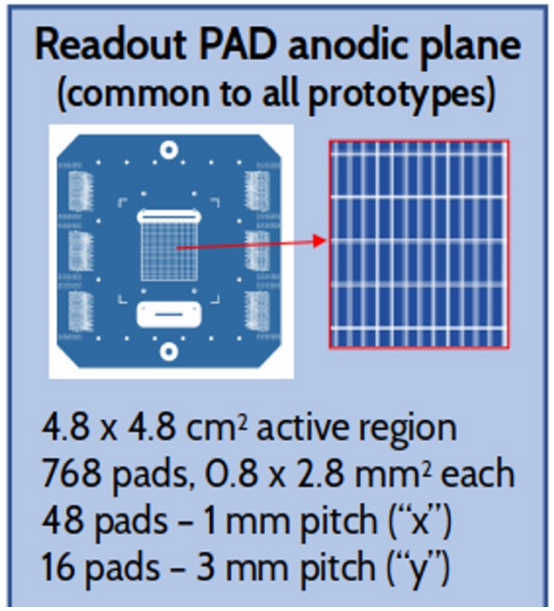
- The production of Double-Layer DLC Resistive Micromegas at CERN has reached an established high-quality standard and reliability, even for large sizes.
- Due to the large number of requests, the MPT Workshop is experiencing extended delay times.
- R&D of new configurations can hardly be done outside CERN.
- For large-scale production, the cost of this technology needs to be reduced.
- The transfer of manufacturing technology to industries is essential.
- After the experience gained with ATLAS production, ELTOS S.p.A. is in a good position to face new, more complex productions (including bulk).
- The tests carried out at ELTOS last week are promising. ELTOS is interested in our developments, and we need to strengthen this collaboration, progressing towards large-scale and full industrial production.

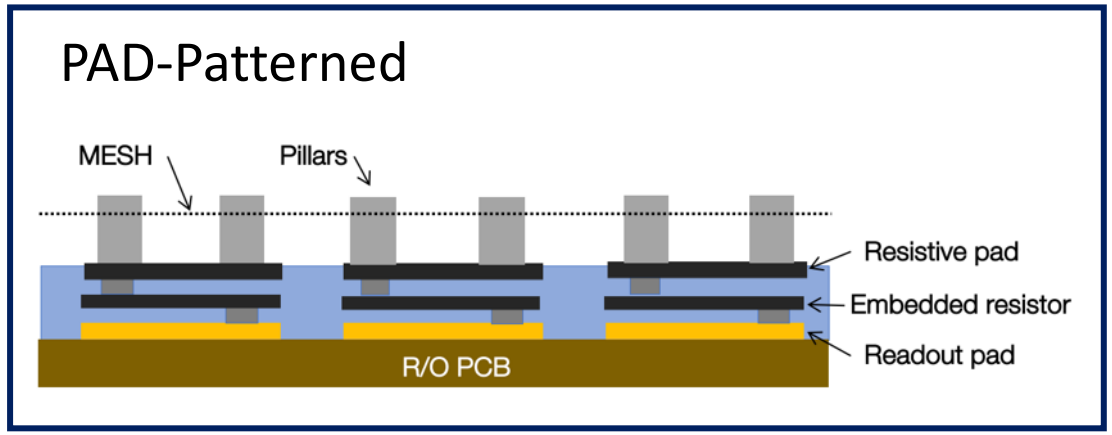
Thank you!

Additional Material

The start (2015): Resistive Pad-Patterned Micromegas

- Configuration inspired by (1 cm^2 pad resistive MM) by M. Chefdeville and co-authors [1], [2], and by (non-resistive GEM + MM hybrid) detector in COMPASS [D. Neyret, et al.]
- Push the technology to high rates - Main changes/improvements:
  - Combine a resistive scheme to a high granularity readout for stable operation at high gain (G~10^4 and beyond) and high rates (up to 10 MHz/cm^2)
  - Improve and ease the production technique





Readout pads 0.8x2.8 mm^2

PAD-P

- EMBEDDED RESISTORS between resistive and readout copper pads
- Each pad completely independent from neighbours

The Resistive Pad-P Micromegas - manufacturing

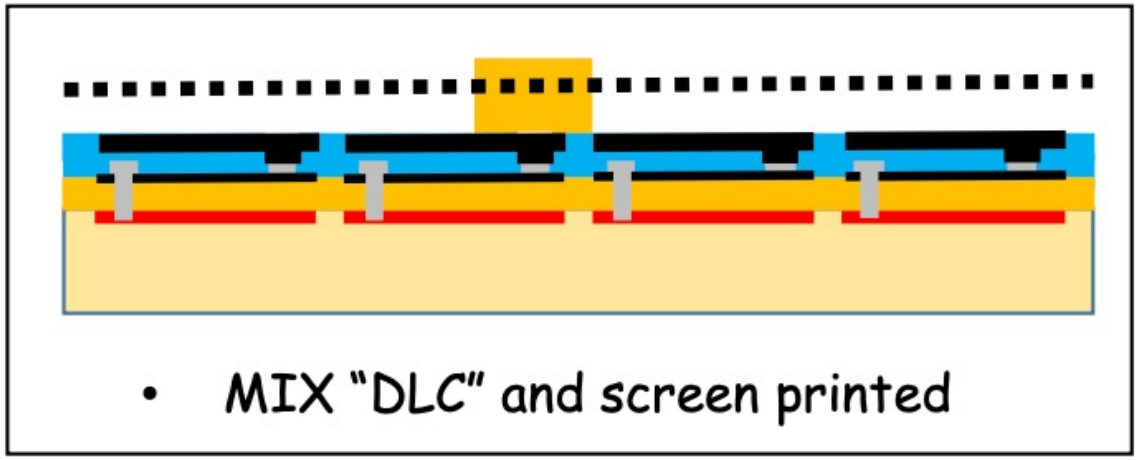
(see Rui's talk at INSTR 2020 and slide in backup)

- **First Prototype**: Full screen-printing (including the insulation layer)
  → failed due to sparks caused by (unavoidable?) micro-holes in the insulation layer;
- **Second generation**: 2 layers screen printed resistors on Kapton → partially successful: for small pads, the embedded resistors are difficult to shape with high enough resistance
- **Third generation:** a "MIX" technique was adopted: the screen printing is still used for the top layer while the embedded resistors were obtained by **patterning a DLC layer on Kapton**
  Thanks to the higher resisivity of DLC ($\mathcal{O}$(MΩ/sq)) with respect to the screen-printing paste (around 10 kΩ/sq), this solution allows for easier patterning of small pads with high resistance

→This is the solution adopted to build
our latest PAD-Patterned detector

Excellent results in terms of stability
Not fully satisfactory for some performance results

(see M. Iodice – RD51 https://indico.cern.ch/event/1327482)



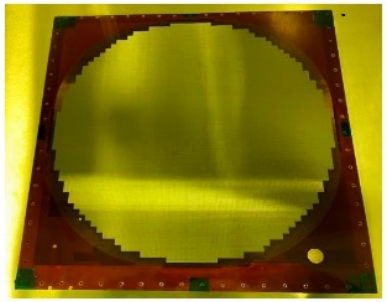
Printed Pad-Patterned with embedded resistors

Rui's talk at INSTR 2020

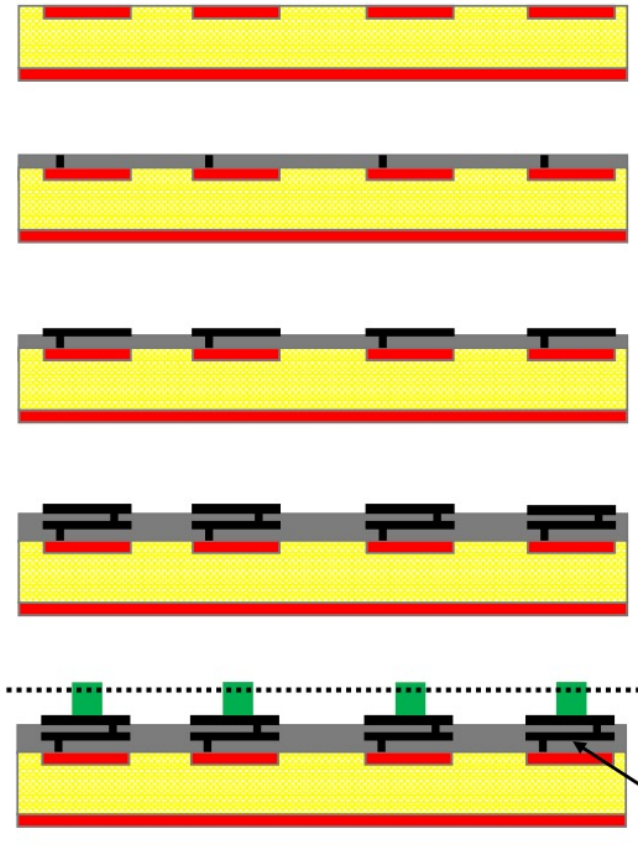
2 Printed layers

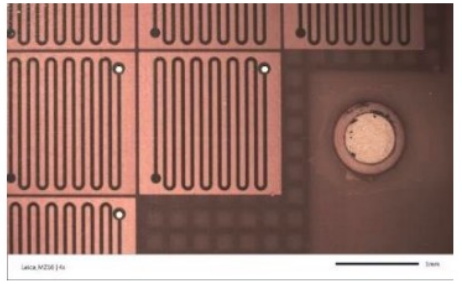
-Extra Large DOCA
-Accurate layers registration in large size
-No DLC needed
-High rate detectors

-Embedded Res should be less than 10KOhms/square
-Large pads only
-low energy resolution

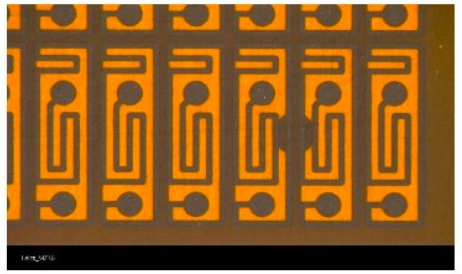


5 ILC DHCAL
50cm diameter
pads 1cm x 1cm
5M/Pad





1cm x 1cm pad→ Ok
There is space to create a
2 Mohms Resistor
with 10K/sqr paste



1mm x 3mm pad→ Bad result
There is no space to create a
2 Mohms Resistor
with 10k paste