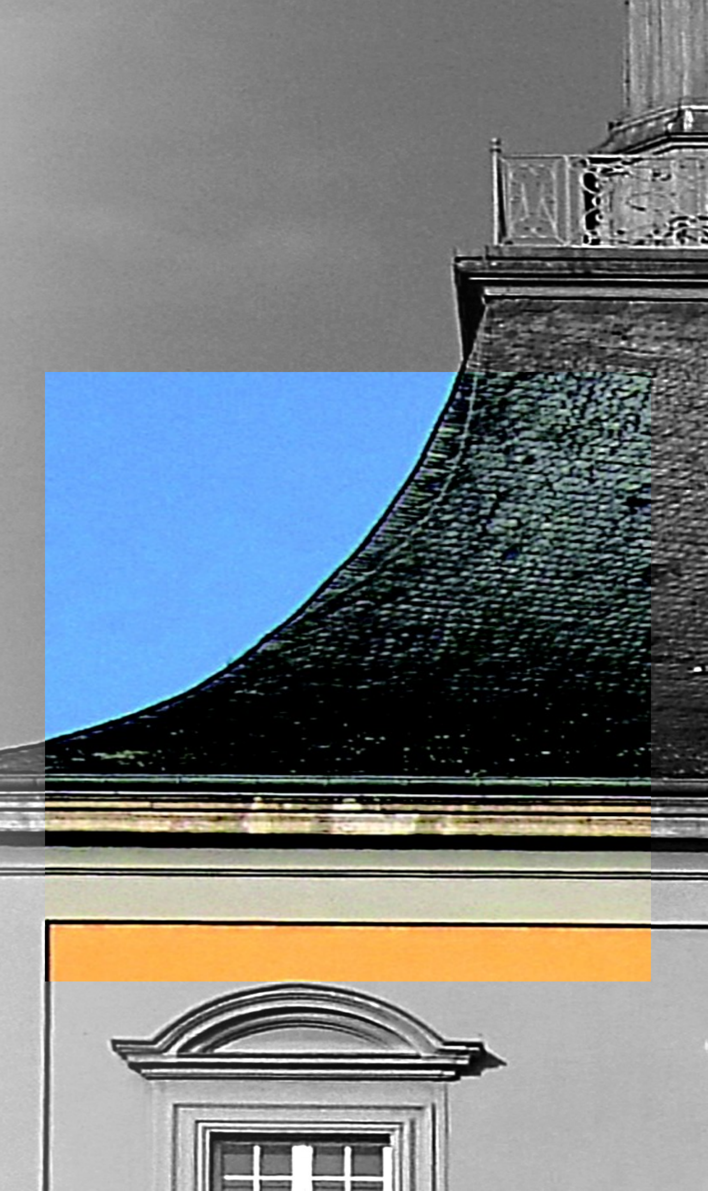
Close-out

Michael Lupberger

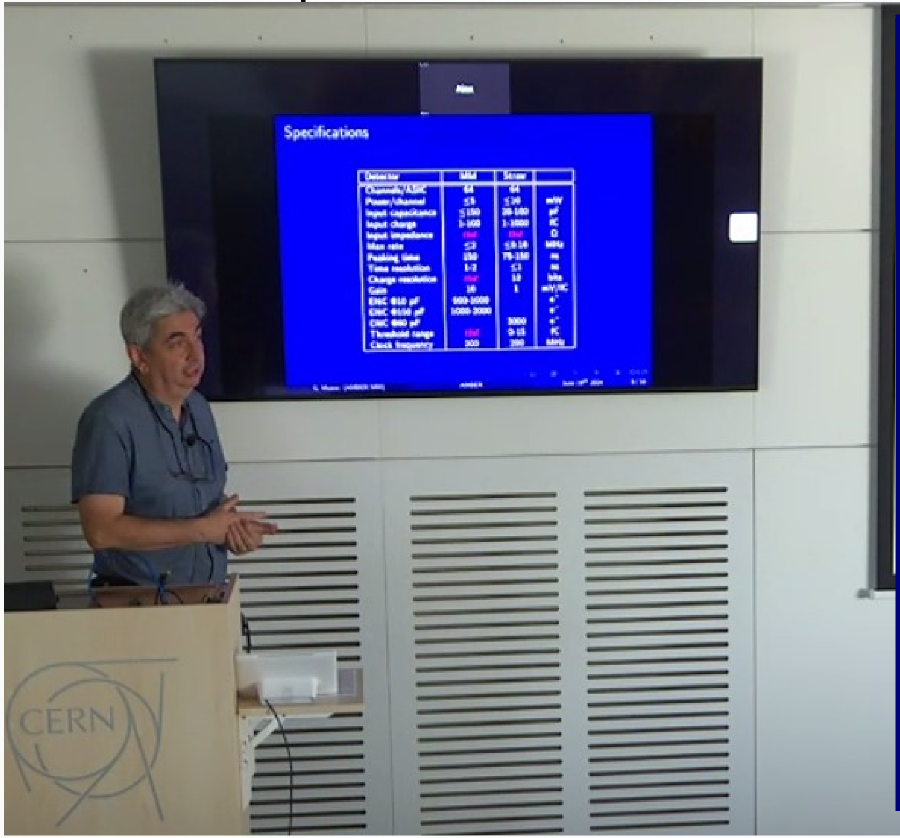
Topical Workshop on Electronics for Gaseous Detectors
2nd DRD1 Collaboration Meeting

19.06.2024 CERN



CONTRIBUTION FLASH: GIANNI MAZZA

ASIC developments for the AMBER MM experiment



Detector	MM	Straw	
Channels/ASIC	64	64	
Power/channel	$\leq$5	$\leq$10	mW
Input capacitance	$\leq$150	20-100	pF
Input charge	1-100	1-1000	fC
Input impedance	*tbd*	*tbd*	Ω
Max rate	$\leq$2	$\leq$0.18	MHz
Peaking time	150	75-150	ns
Time resolution	1-2	$\leq$1	ns
Charge resolution	*tbd*	10	bits
Gain	10	1	mV/fC
ENC @10 pF	500-1000		e^-
ENC @150 pF	1000-2000		e^-
ENC @60 pF		3000	e^-
Threshold range	*tbd*	0-15	fC
Clock frequency	200	200	MHz

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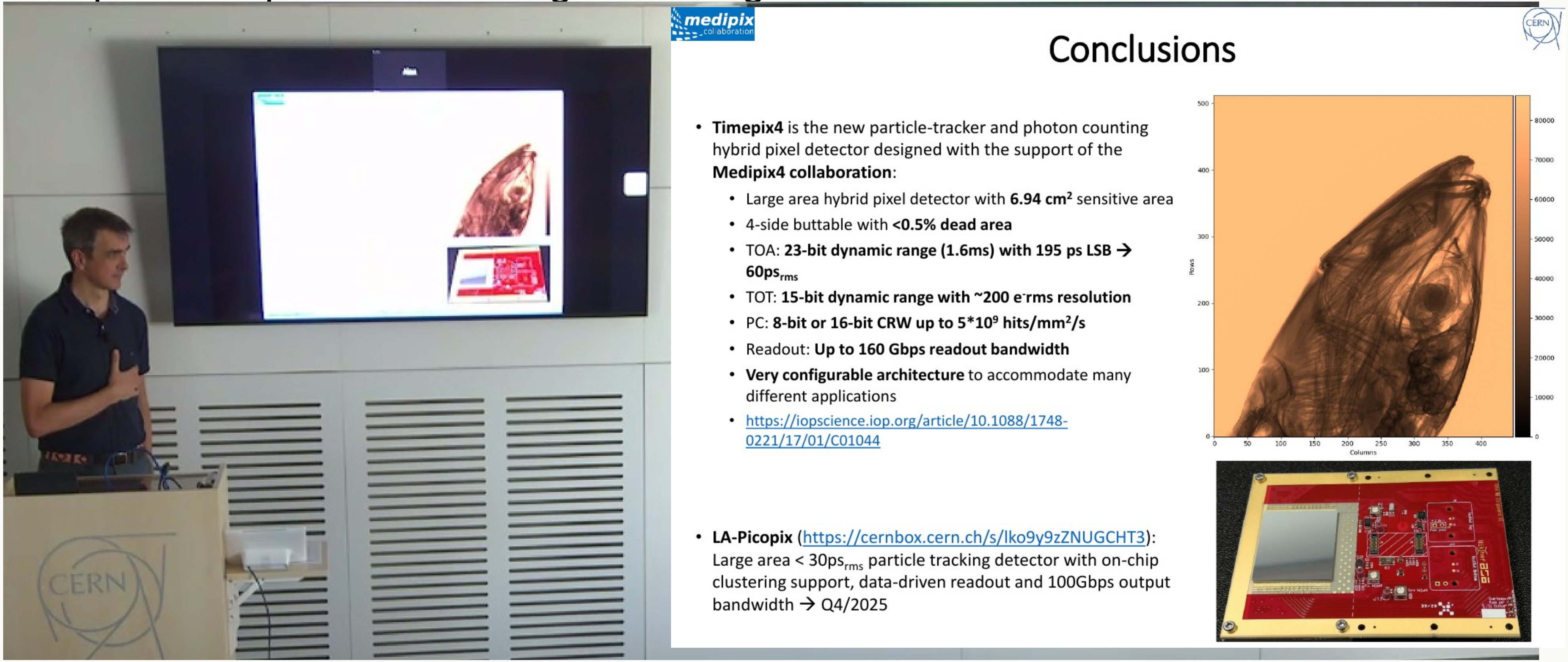
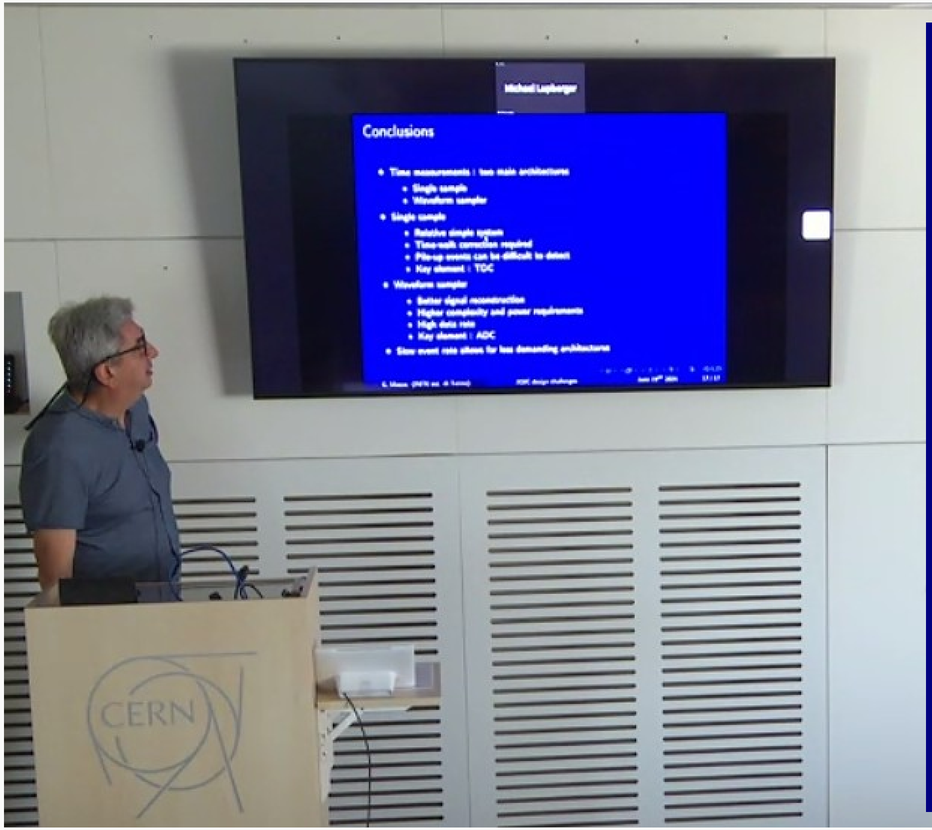
CONTRIBUTION FLASH: XAVIER LLOPART

Timepix4 and pixel ASIC design challenges



CONTRIBUTION FLASH: GIANNI MAZZA

ASIC design challenges - with a focus on precise timing

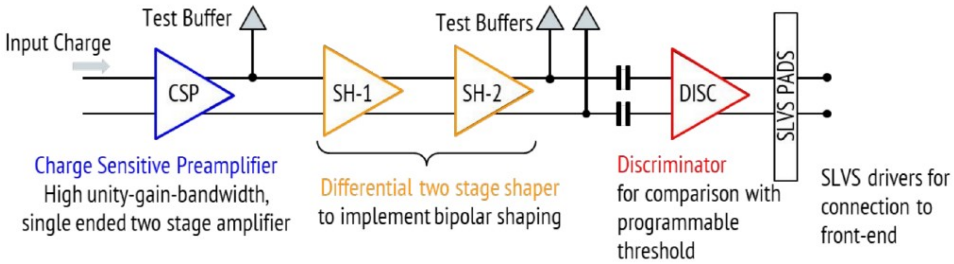


- Time measurements : two main architectures
  - Single sample
  - Waveform sampler
- Single sample
  - Relative simple system
  - Time-walk correction required
  - Pile-up events can be difficult to detect
  - Key element : TDC
- Waveform sampler
  - Better signal reconstruction
  - Higher complexity and power requirements
  - High data rate
  - Key element : ADC
- Slow event rate allows for less demanding architectures

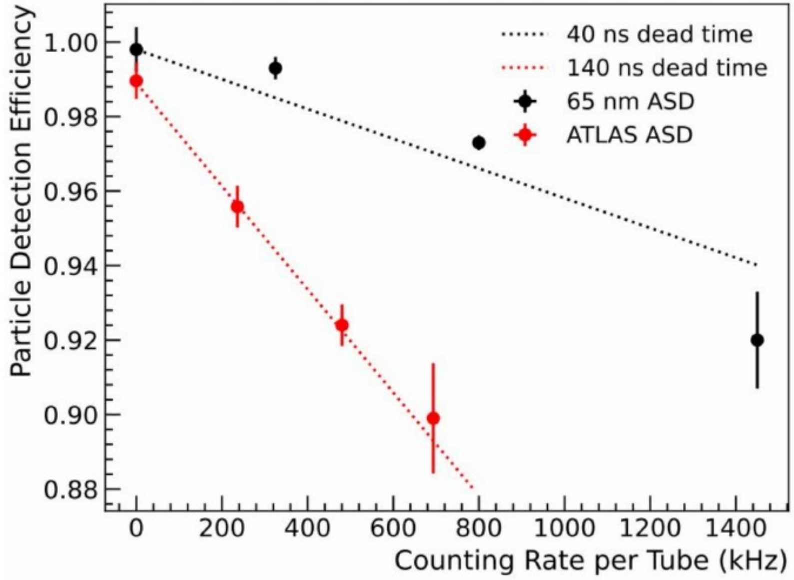
CONTRIBUTION FLASH: OLIVER KORTNER

Development of a new ASD-ASIC for drift-tube and straw detectors

New ASD chip in 65 nm CMOS technology

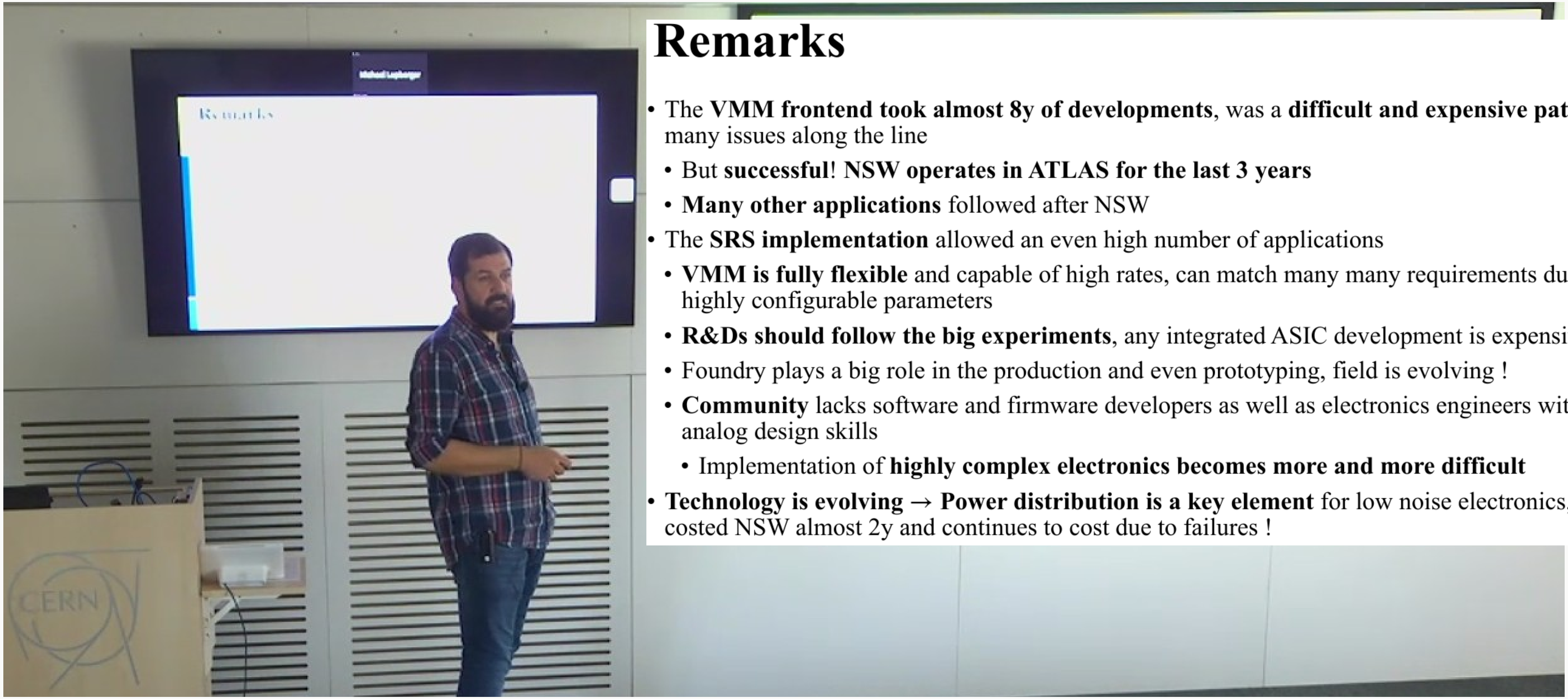


- Four-channel Amplifier Shaper Discriminator designed by the MPI for Physics and fabricated in 65 nm TSMC CMOS technology.
- Bipolar shaping selected to avoid baseline shifts at high background hit rates.
- Discriminator with LVDS output.
- Power consumption per channel 12.8 mW (61% lower than the power consumption of the ATLAS phase-II ASIC).
- 0.235 mm^2 area/channel.



CONTRIBUTION FLASH: GEORGE IAKOVIDIS

MPGD Electronics - From R&D to ATLAS NSW



Remarks

- The **VMM frontend took almost 8y of developments**, was a **difficult and expensive path** with many issues along the line
  - But **successful**! **NSW operates in ATLAS for the last 3 years**
  - **Many other applications** followed after NSW
- The **SRS implementation** allowed an even high number of applications
  - **VMM is fully flexible** and capable of high rates, can match many many requirements due to its highly configurable parameters
  - **R&Ds should follow the big experiments**, any integrated ASIC development is expensive !
  - Foundry plays a big role in the production and even prototyping, field is evolving !
  - **Community** lacks software and firmware developers as well as electronics engineers with analog design skills
    - Implementation of **highly complex electronics becomes more and more difficult**
- **Technology is evolving → Power distribution is a key element** for low noise electronics, it costed NSW almost 2y and continues to cost due to failures !

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CONTRIBUTION FLASH: MAREK IDZIK

Short status on DRD7 ADC and TDC activities (plus few slides on front-end ASICs)

- Overview of DRD7.3a

  "High performance TDC and ADC blocks at ultra-low power"

  - DRD7.3a is one of three DRD7.3 projects

  - DRD7.3 (4D & 5D techn.) is one of seven DRD7 packages

  find the DRD7 proposal at 3rd meeting of the DRDC

  https://indico.cern.ch/event/1406007/

- Few examples of existing low-power front-end ASICs (~DRD6)

AGH

Introduction to TDC&ADC in DRD7.3a

- Project Target and Vision:

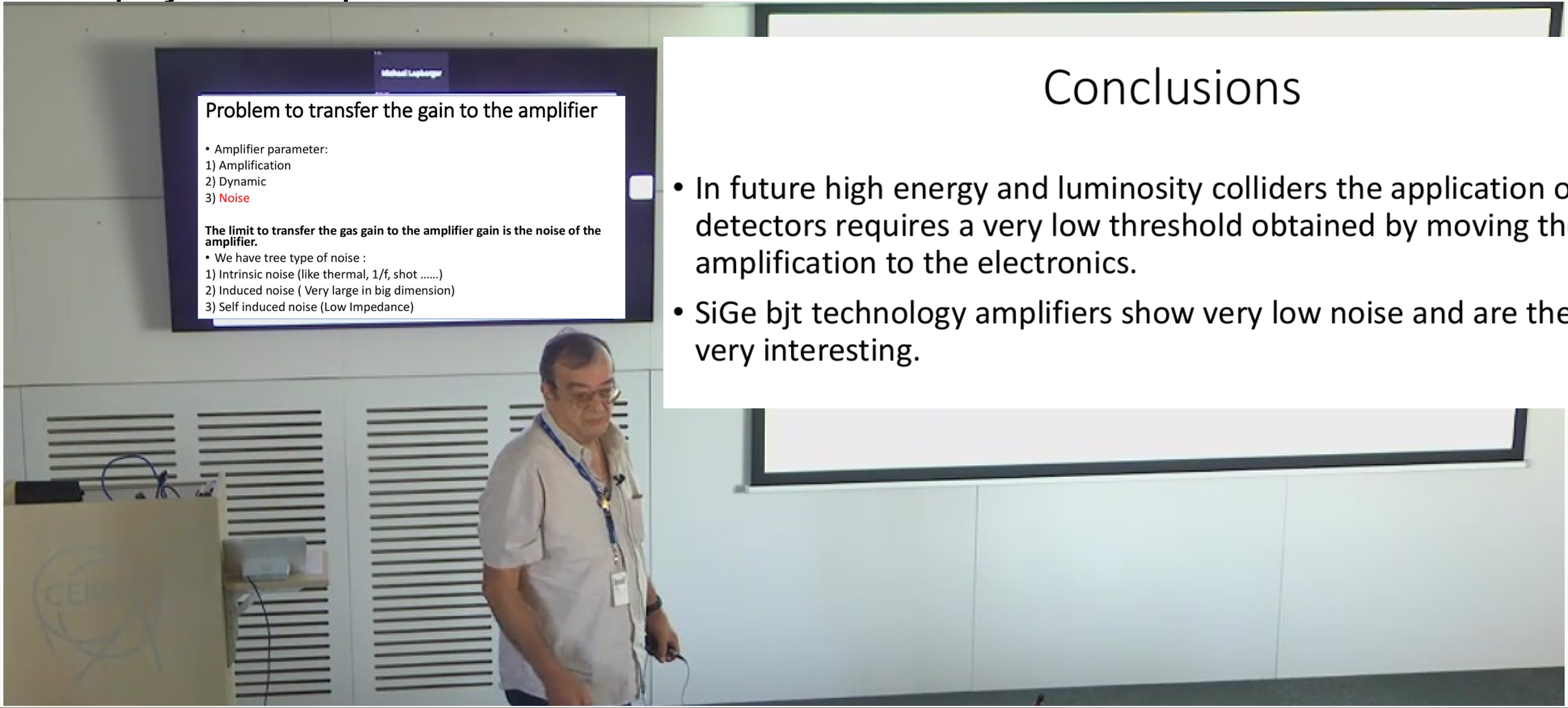
  High resolution (~10ps) TDC and medium-high resolution (10-14 bits) fast sampling (>40MSps) ADC blocks. High performance, especially ultra-low power consumption, should be confirmed with a very good Figure of Merit, compared to the state-of-the-art solutions in the same CMOS technology and with similar parameters

  The ADC&TDC blocks in advanced CMOS technologies should be ready to be deployed as key components of SoC readout ASICs

- Contributors: AGH (PL), CEA IRFU (FR), CPPM (FR), DGIST (KR), ICCUB (ES), IP2I (FR), OMEGA (FR), SLAC (US), TU GRAZ (AT)

CONTRIBUTION FLASH: ROBERTO CARDARELLI

RPC physic and performance v.s. low threshold



Conclusions

- In future high energy and luminosity colliders the application of gas detectors requires a very low threshold obtained by moving the gas amplification to the electronics.
- SiGe bjt technology amplifiers show very low noise and are therefore very interesting.

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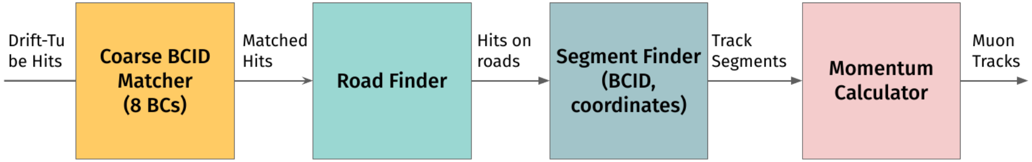
CONTRIBUTION FLASH: DAVIDE CIERI

Development of a self-seeded drift-tube chamber trigger

The Design

- (Very) preliminary FPGA architecture for the standalone trigger design
  - Efficiency and rate performance to be studied
  - Idea is to estimate resource usage, to see if it could fit in current system
- Concept study applied to a muon spectrometer with standard drift-tubes with radius of 15mm (max. Drift-time of 800ns)

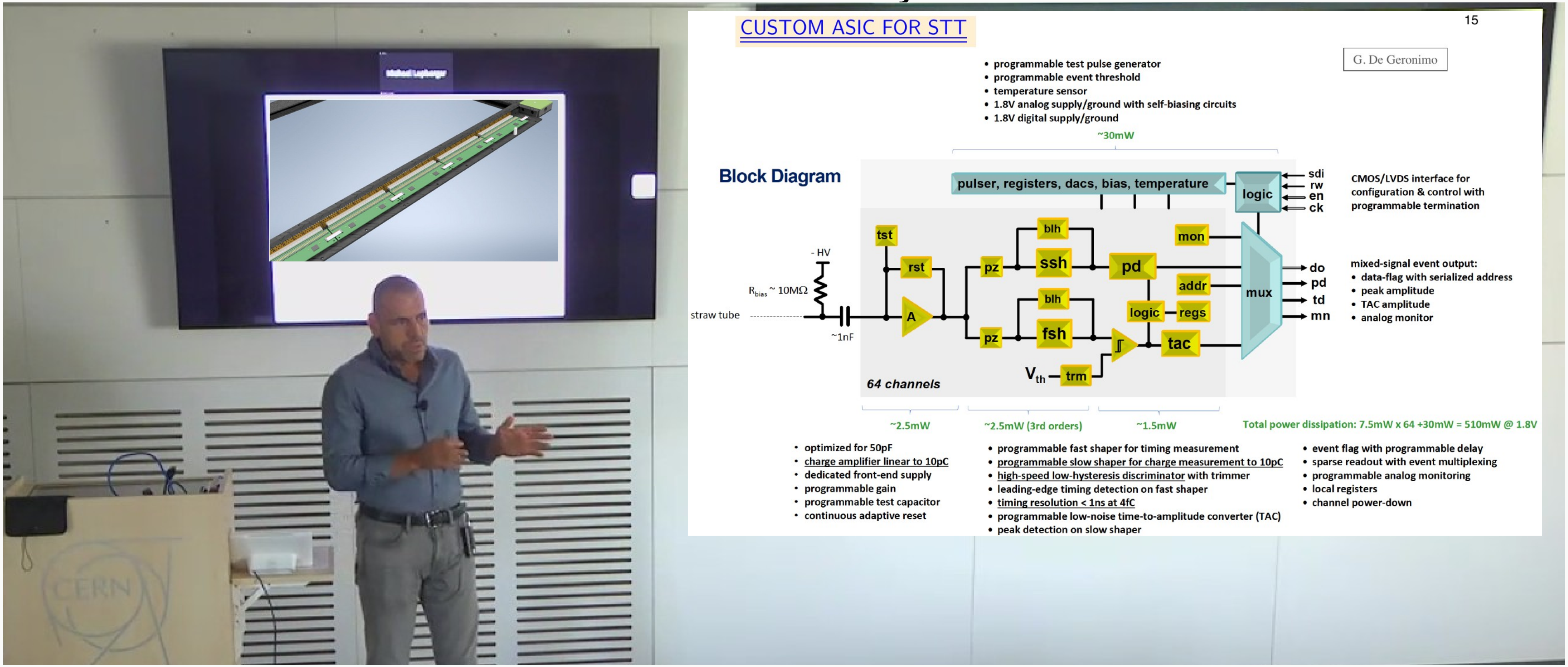


Conclusions

First study of a self-seeded drift-tube trigger. Design could be operated with available state-of-the-art technology.

Performance analysis still to be done.

Readout of Straw Tube Tracker for Neutrino Physics



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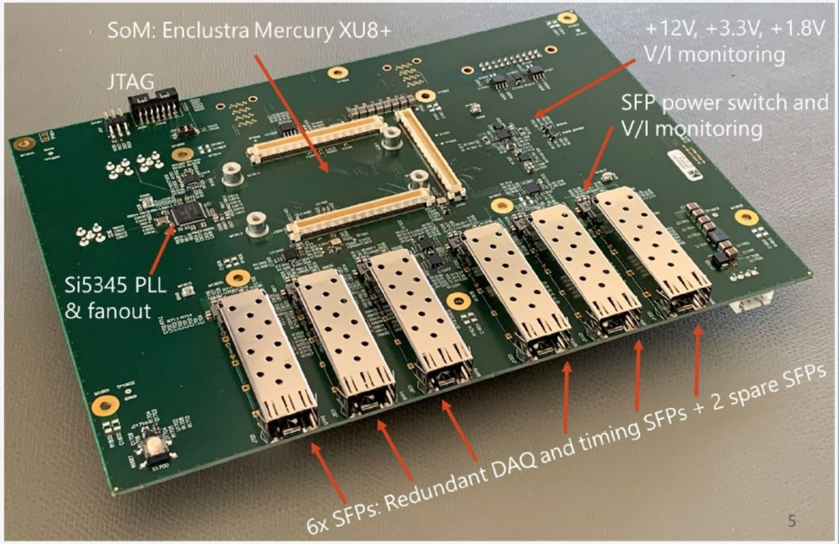
CONTRIBUTION FLASH: CURRO (JOSE FRANCISCO TOLEDO ALARCON)

Contribution to SRSe design – the eFEC module

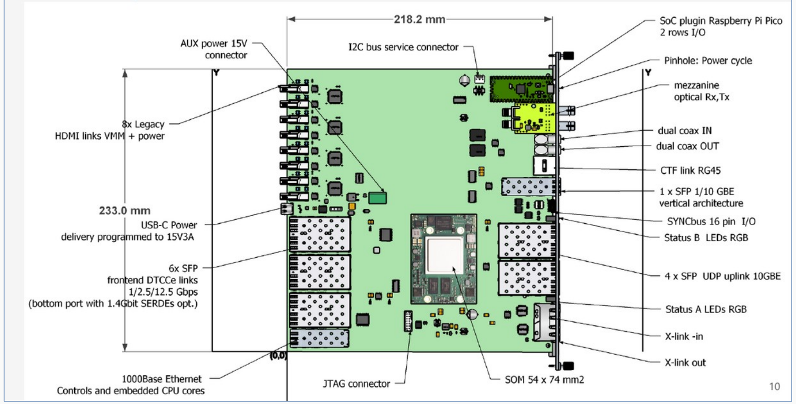
UPV group activities

- Hyper-Kamiokande: currently developing the DPB module in the FE box, inner detector.

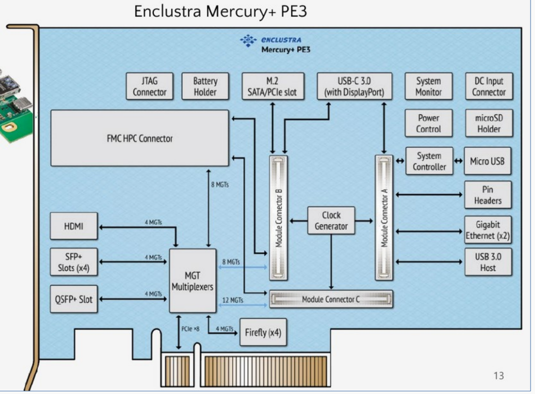
- Based on SoM
- Zynq Ultascale+ SoC
- Petalinux
- DDR4 buffer (data flow)
- Several GbE I/O
- Redunancy&High reliability



eFEC conceptual view

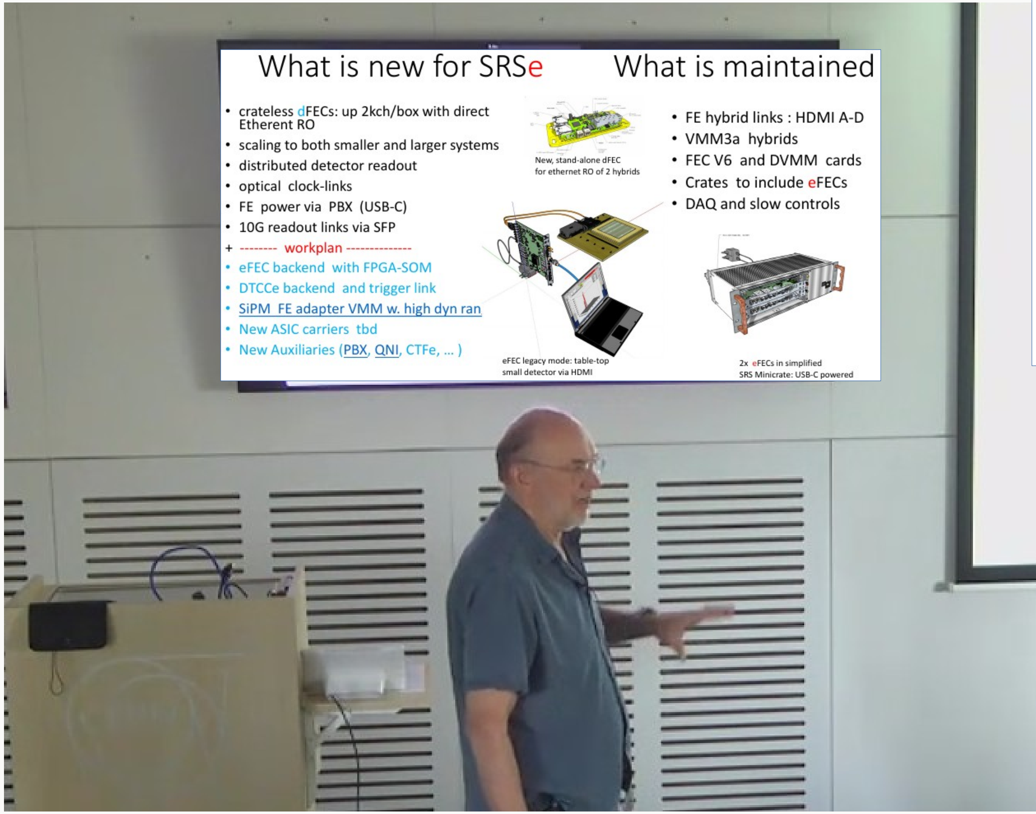


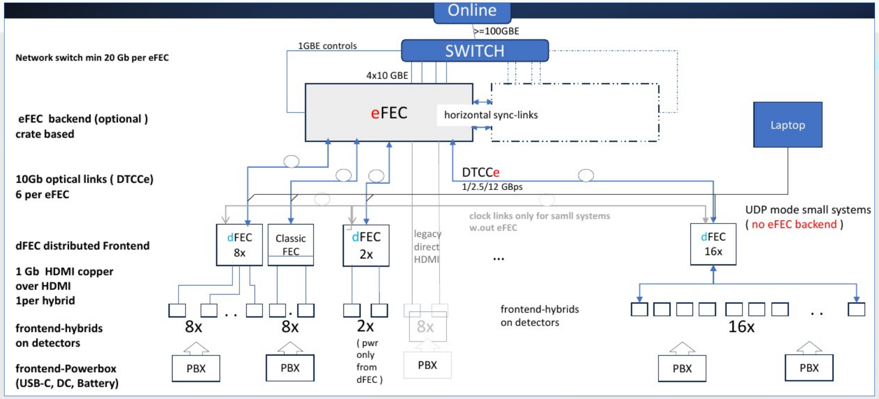
eFEC prototyping



CONTRIBUTION FLASH: HANS MÜLLER

Update on eFEC backend project





SRSe project draft, call for DRD1 teams

FE -HW	FW / Scripts	DAQ & Slow Controls SW
-VMM3a 128 ch (standard) -SAMPA 128 ch (proto) -HGCRoc study case	-VMM3a Spartan7 (standard) -SAMPA see talk G. A. de Souza IF-USP	-VMM3a self triggered (standard) -VMM3a triggered mode-> Jin-Hee Chang / FRIB
dFEC-HW uROC 256 ch -> see talk A.Rusu MaxiROC 2k ch under design	dFEC -FW uROC 256 ch -> see talk A.Rusu MaxiROC 2k ch -> see talk D.Pfeiffer	dFEC DAQ Ethernet uROC 256ch -> see talk A.Rusu MaxiROC 2k -> see talk D.Pfeiffer
PBX power box (in production)	PBX V-Monitor via RP (uPython)	Clock-Trigger-EvNr distribution TLU ? under investigation
Clock link mezzanine (under design)	dFEC Clock synchronizer (tbd)	
eFEC-HW New SOM concept-> see talk J.Toledo Co-design CERN/UPV	eFEC FW DTCCe coder- decoder (tbd) 10GB Ethernet cores **ZU9CG** Template triggers (tbd)	eFEC Linux for **ZU9CG ARM core** <-> DDR4 UPV Valencia DAQ choice & integration (tbd)

CONTRIBUTION FLASH: DAMIEN NEYRET

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SALSA: a new versatile readout chip for MPGD

SALSA CHIP TARGET SPECIFICATIONS, COMPARED TO EPIC MPGD REQUIREMENTS

Versatile front-end characteristics → EPIC MPGD needs

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1 nF → **200 pF**
- Large range of peaking times: 50-500 ns → **100-200 ns**
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC → **0-250 pC**
- Large range of input rates, up to 100 kHz/ch with fast CSA reset → **< 25 kHz**
- Both polarities (depends on kind of detector) → **negative**

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s → **50 MS/s**
- Integrated DSP for internal data processing and size reduction, treatment processes to be configured according to user needs → **all processes**
- Continuous readout, triggered mode also available → **continuous readout**
- Several 1 Gb/s output data links → **1 gigabit link used at EPIC**

General characteristics

- ~1 cm^2 die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, > 300 Mrad, > 10^{13} n_{eq}/cm^2) → **10 krad, 10^{11} n_{eq}/cm^2**

CONCLUSIONS AND PROSPECTS

Present status

- Specifications almost finalized. Still open to suggestions
- SALSA0 and PRISME prototypes with promising performance measurements; helpful to fix bugs, and verify simulations
- SALSA1 prototype (front-end + ADC) designed and submitted
- SALSA2 prototype (fully featured, reduced number of channels) development ongoing: DSP architecture and features
- Grant from EIC eRD109 R&D program
- Grant from French and Brazilian research agencies requested

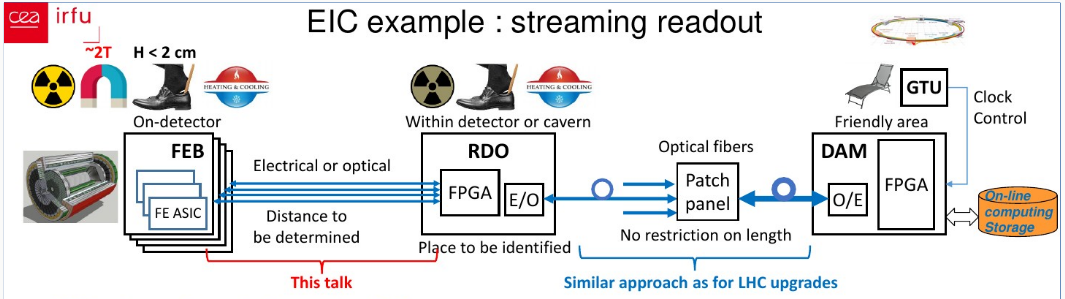
Next steps

- Completion of tests on PRISME prototype, radiation tests
- Tests of SALSA1 from Autumn 2024
- Submission of SALSA2 in 2^{nd} quarter 2025
- Design of SALSA3 pre-serial ASIC in 2025, production and tests in 2026
- Full production in 2027, 4000 ASICs foreseen for EPIC, probably more produced for other projects
- Compatible with the EIC project timeline
- Expressions of interest welcome !

CONTRIBUTION FLASH: IRAKLI MANDJAVIDZE

Salsa ASIC: Interfaces

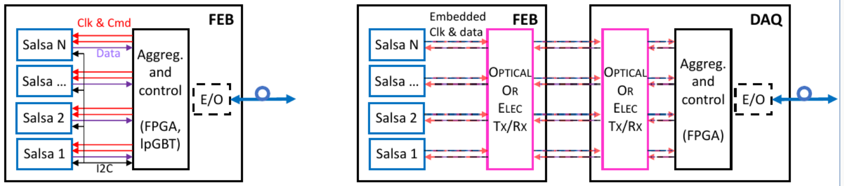
EIC example : streaming readout



- FEB – frontend board with readout ASICs
  → Sub-detector specific
- RDO – readout module – first stage of FEB data aggregation, last stage to dispatch clock & control
  → Mostly common design framework between sub-detectors, different form factor
- DAM – data aggregation module – interface with computing and global timing and control unit (GTU)
  → Common design for all sub-detectors
- Downstream towards detector : clock, control, monitoring
- Upstream towards storage : physics, calibration, monitoring data

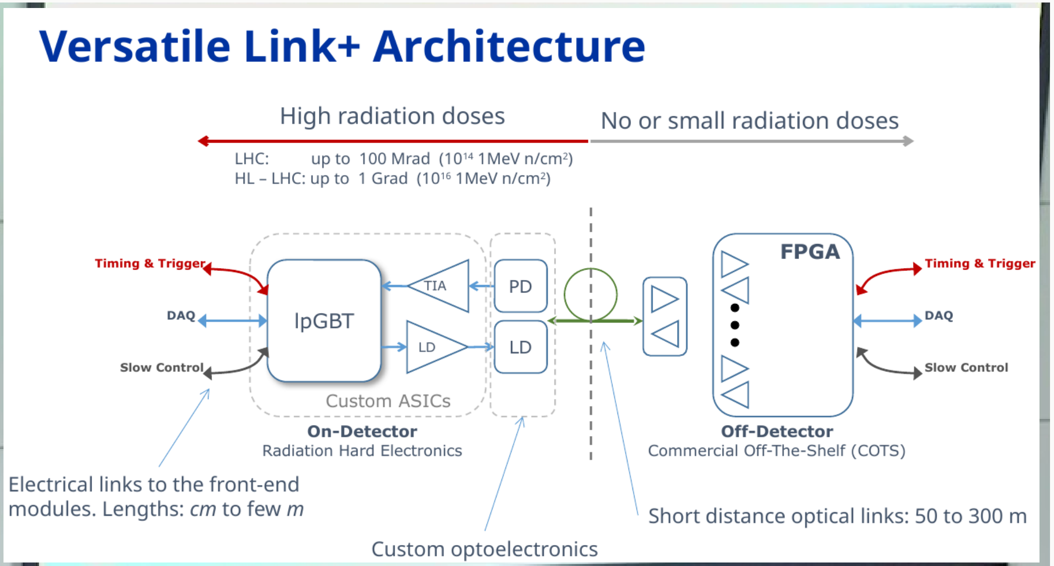
Summary

- If successful, flexibility in Salsa integration
  → Support for **local companion ASIC** as well as **remote intelligence** schemes



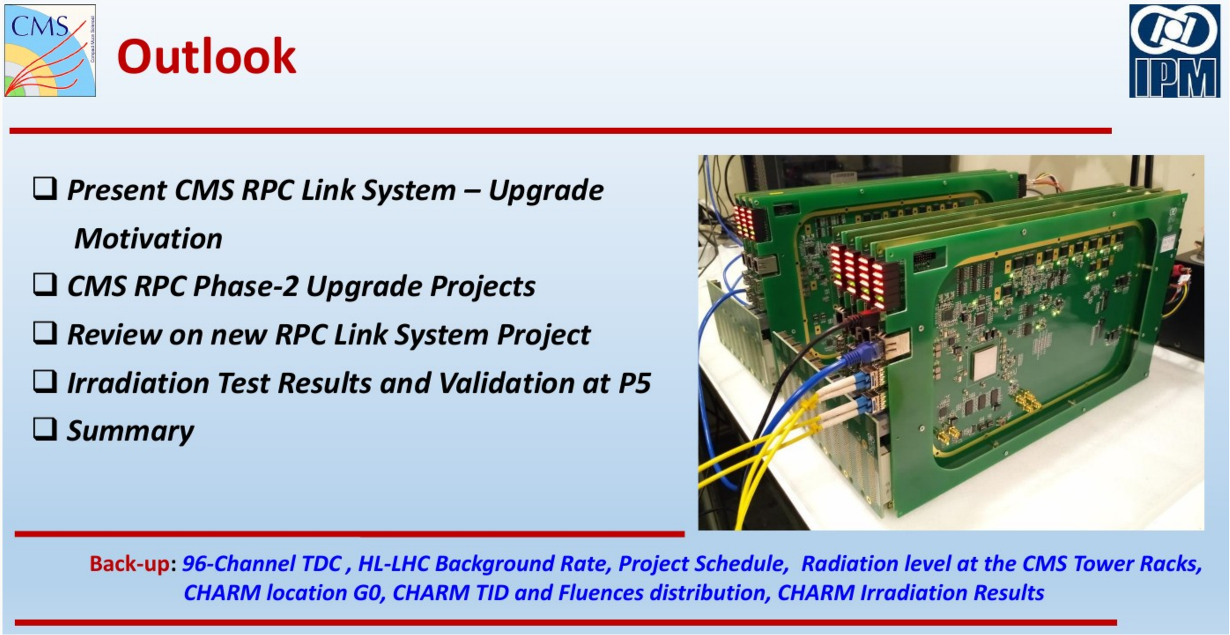
  → Low pin count unified interface : potential to control and aggregate data from a large number of ASICs
  → Less than 1 Gbit/s links to interface with standard FPGA IOs and SERDES IPs
  → Wide range of system clock choices with Prisme mixed analog-digital PLL IP
    - 40 – 120 MHz with aimed recovered clock jitter better than 10 ps RMS
- Work well advanced to fix specifications
- Prototypes under development and tests
- Appeal to DRD1 collaboration to understand the access conditions to the CERN radiation facilities
  → Validate radiation tolerance of the design

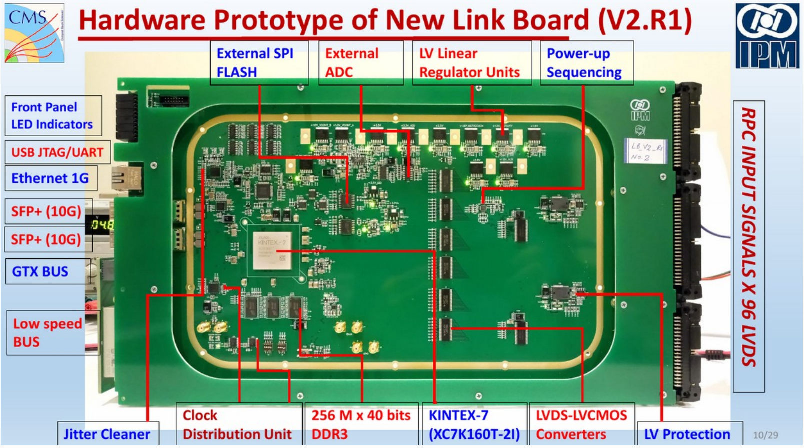
Versatile Link+ / lpGBT overview

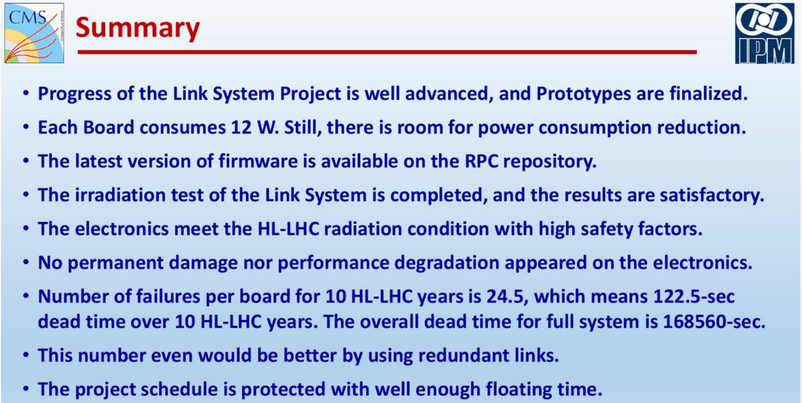


CONTRIBUTION FLASH: BEHZAD BOGHRATI

CMS RPC Link System

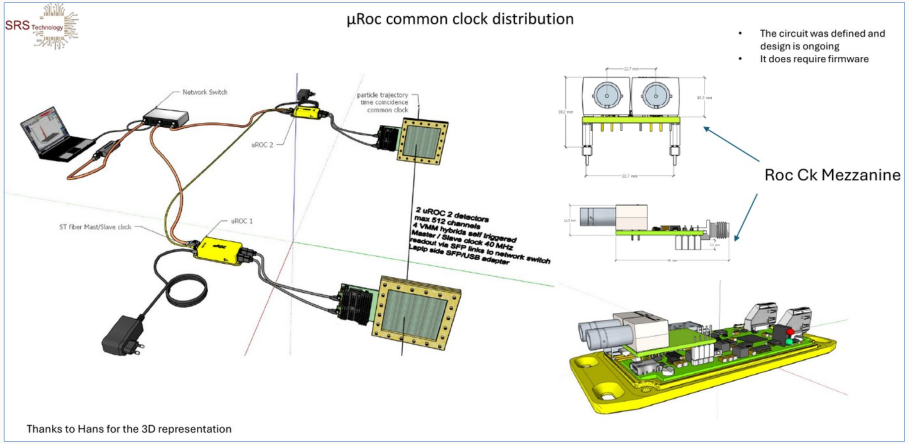






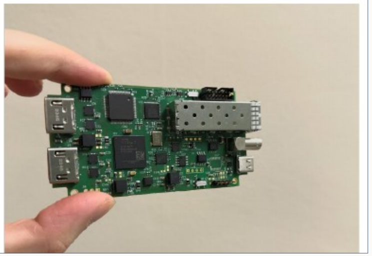
CONTRIBUTION FLASH: ALEXANDRU RUSU

uRoc Concentrator for VMM Front End's



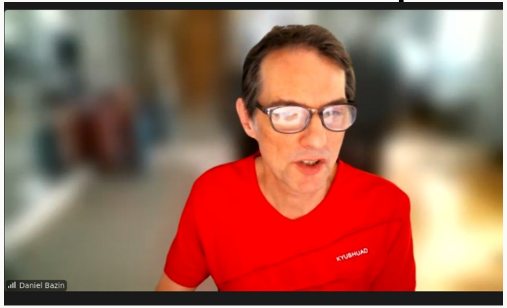
Size comparison between
VMM Hybrid and µRoc

- First 2 prototypes have been built
- The firmware for the board is completed
- A second revision of the board is mandatory.
- The revision is ongoing and explorations are done for a production of larger batch.



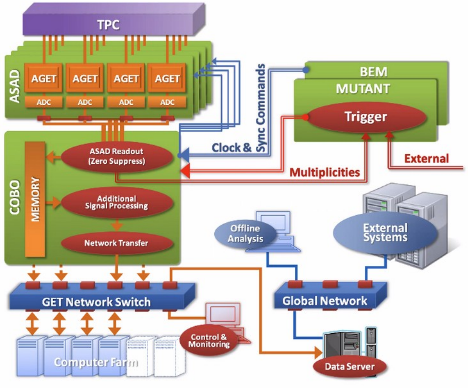
CONTRIBUTION FLASH:DANIEL BAZIN

Electronics requirements for a low-energy nuclear physics TPC



The GET Electronics

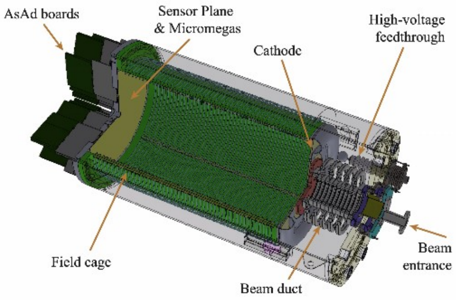
- Main characteristics
  - *High density (256 channels per AsAd)*
  - *Based on 64 channel ASIC using SCA technology*
  - *12 bit ADCs to serial lines*
  - *Parallel architecture to maximize throughput*
- Special features
  - *Possibility to generate real time trigger based on channel multiplicity*
  - *Zero suppression of baseline on a channel basis*



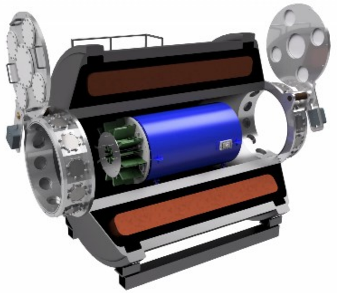
AGET Data Sheet, IRFU, Saclay, France

AT-TPC @ SOLARIS

Active Target Time Projection Chamber



Solenoidal Spectrometer Apparatus for Reaction Studies



U.S. Department of Energy Office of Science
National Science Foundation
Michigan State University

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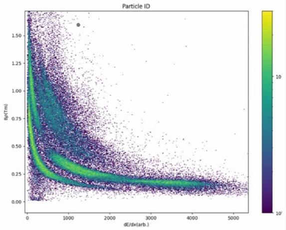
D. Bazin, Topical Workshop on Electronics for Gaseous Detectors, CERN, June 19, 2024 2

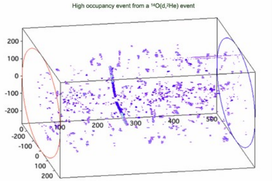
Active Target issue: dynamic range

- Very large dynamic range
  - *Large variations of particle energies*
    - *Inverse kinematics*
    - *Detection of both target-like and beam-like particles*
  - *Large variations of particle energy losses*
    - *Energies much lower than minimum ionization regime*
    - *Large variations of atomic charge of particles*
- Larger dynamic range needed (factor ~ 10)
  - *Logarithmic preamplifiers?*



Active Target issue: data throughput

- Data reduction performed at the back-end level (CoBo)
  - *CoBo buffer memory of 256 Mbytes*
  - *FPGA performs data reduction before TCP/IP broadcast*
- Data throughput limitations
  - *AGET SCA readout frequency is 25 MHz*
  - *Serial lines between AsAd and CoBo take about 16 ms per event (full buffer of 512 samples)*
  - *Dead time grows substantially above 50 events per second*
  - *Highly selective trigger needed*
- Better throughput needed (factor ~ 5)



CONTRIBUTE TO WG5!

Subscribe to our mailing list:
https://e-groups.cern.ch/e-groups/EgroupsSubscription.do?egroupName=drd1-wg5
→ receive e.g. invitations to WG5.1 meetings (SRS/VMM realated developments)

Many opportunities to contribute to presented projects

You can trigger new common developments e.g. based on WP needs

Offer your presentations at WG5 sessions on future DRD1 meetings!

Or we will ask you

THANKS

Co-oranisers of this Topical Workshop (1st of DRD1 Collaboration):
Marco Bregant, Maxime Gouzevitch, Sorin Martoiu, Hans Muller, Lucian Scharenberg, Michael Lupberger

Fruitful discussion, trust in us to organise this workshop:
CB Chair Anna Colaleo; SPs Maksym Titov, Eraldo Oliveri

Your contributions:
All the 17(!) speakers

Your attendance, the fruitful discussion and questions:
All participant