Monolithic Pixel Detector with SOI technology

June. 27, 2011

@CERN, PH-ESE Electronics Seminar

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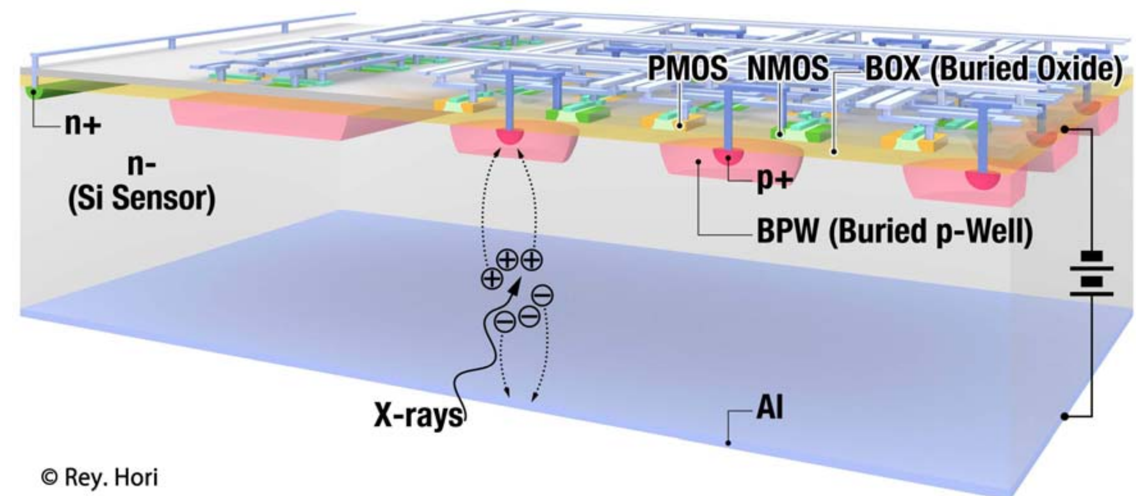
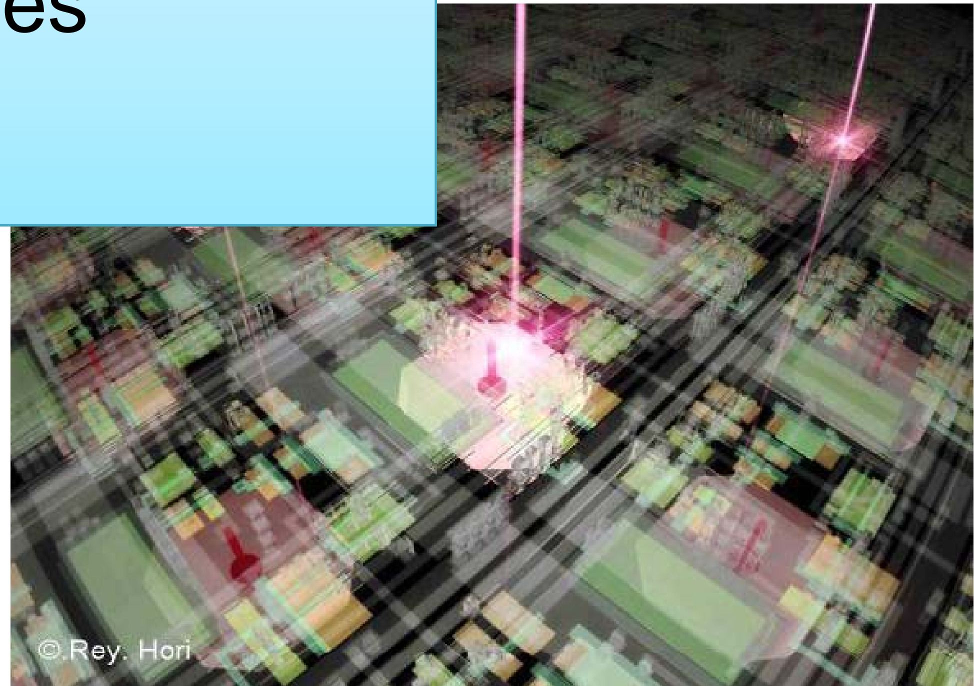
http://rd.kek.jp/project/soi/



OUTLINE

- Introduction of SOI Pixel Project
- SOI Detectors
- Developing Techniques
- Summary



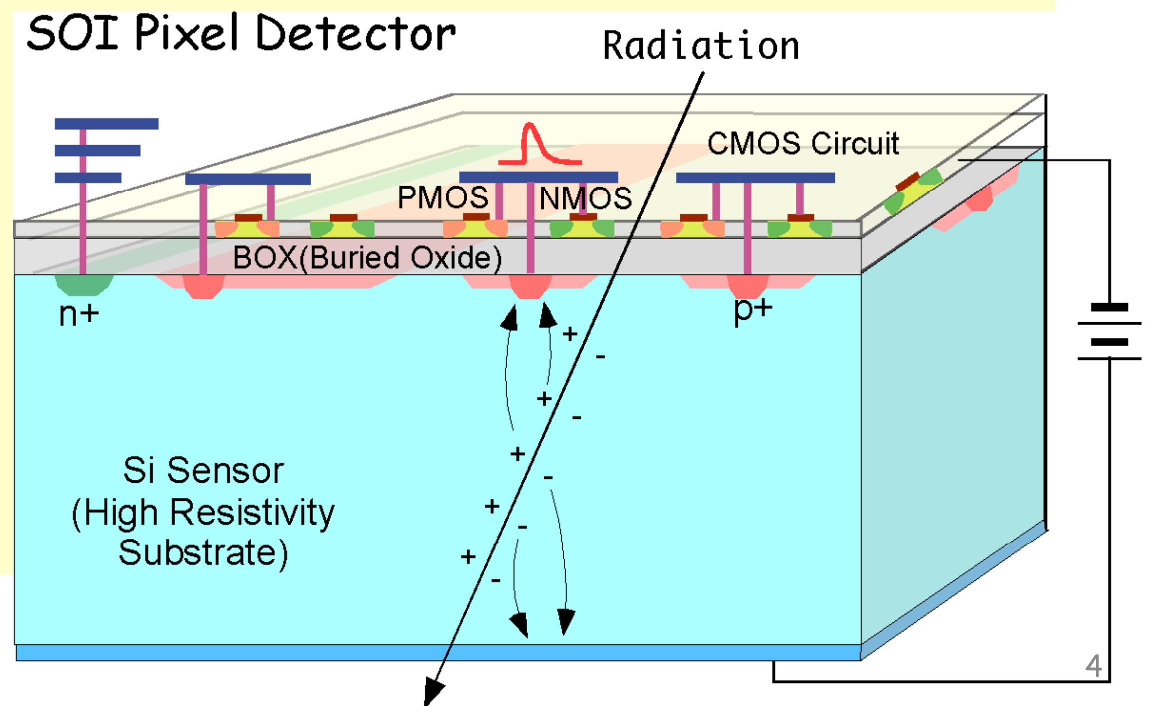
SOI Wafer (UNIBOND™)
(1995, LETI -> SOITEC)

SmartCut(1991)
(Michel. Bruel)

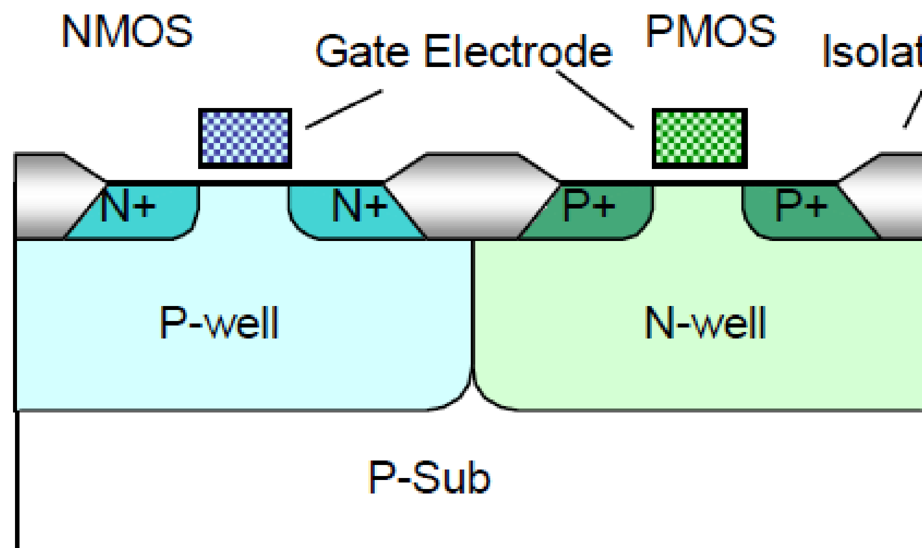
1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
7. Split-off wafer A is recycled, becoming the new wafer A or B

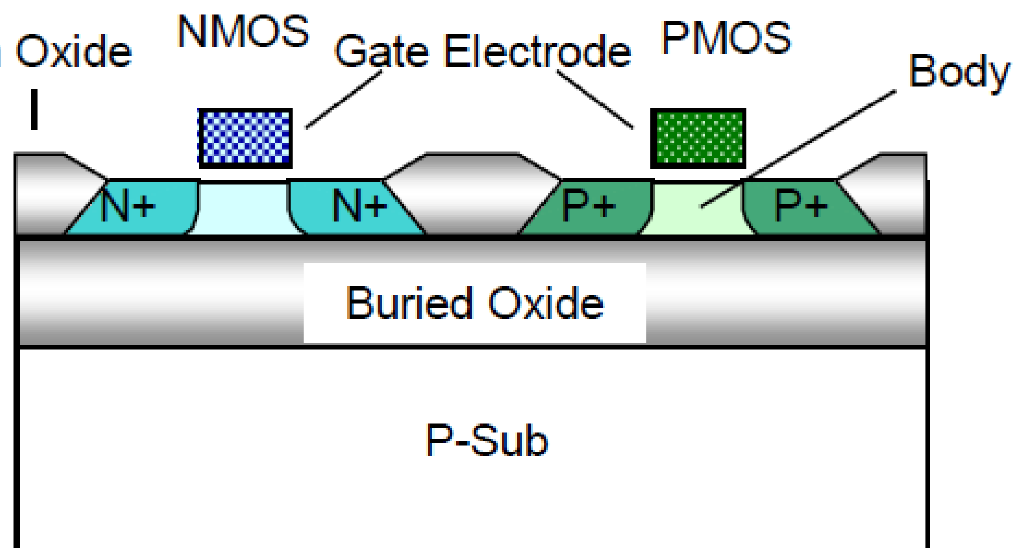
Features of SOI Pixel Detector

- Bonded wafer : High Resistivity (Sensor) + Low Resistivity (CMOS) .
- Truly Monolithic Detector (-> High Density, Low material, Thin Device).
- Standard CMOS can be used (-> Complex functions in a pixel).
- No mechanical bump bonding (-> High yield, Low cost).
- Fully depleted sensor with small capacitance of the sense node (~10fF, High conversion gain, Low noise)
- Based on Industrial standard technology (-> Cost benefit and Scalability)
- No Latch Up, Low SEE σ.
- Low Power
- Operate in wide temp (4K-300C) range.
- ...

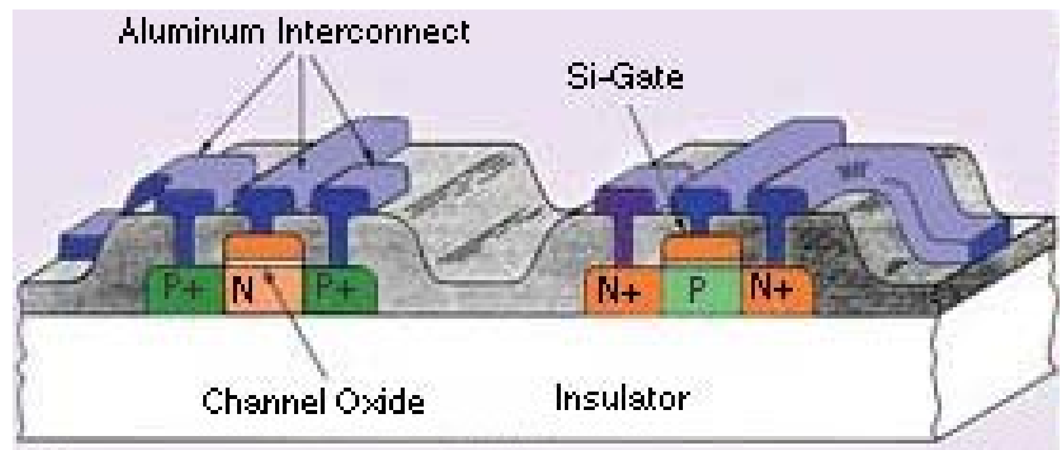


Bulk CMOS vs. SOI CMOS

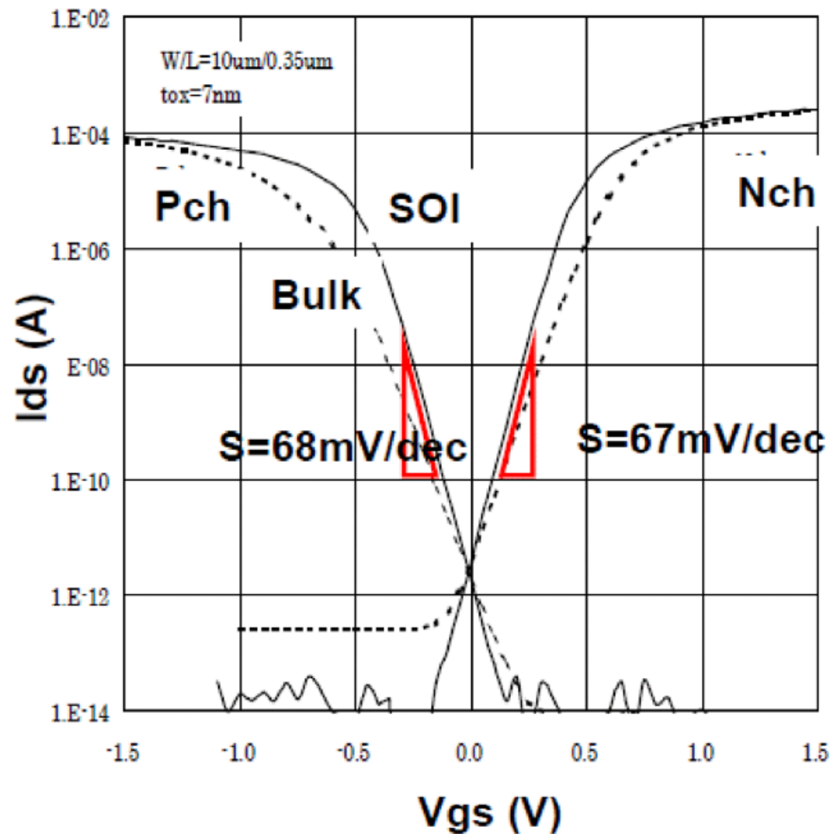


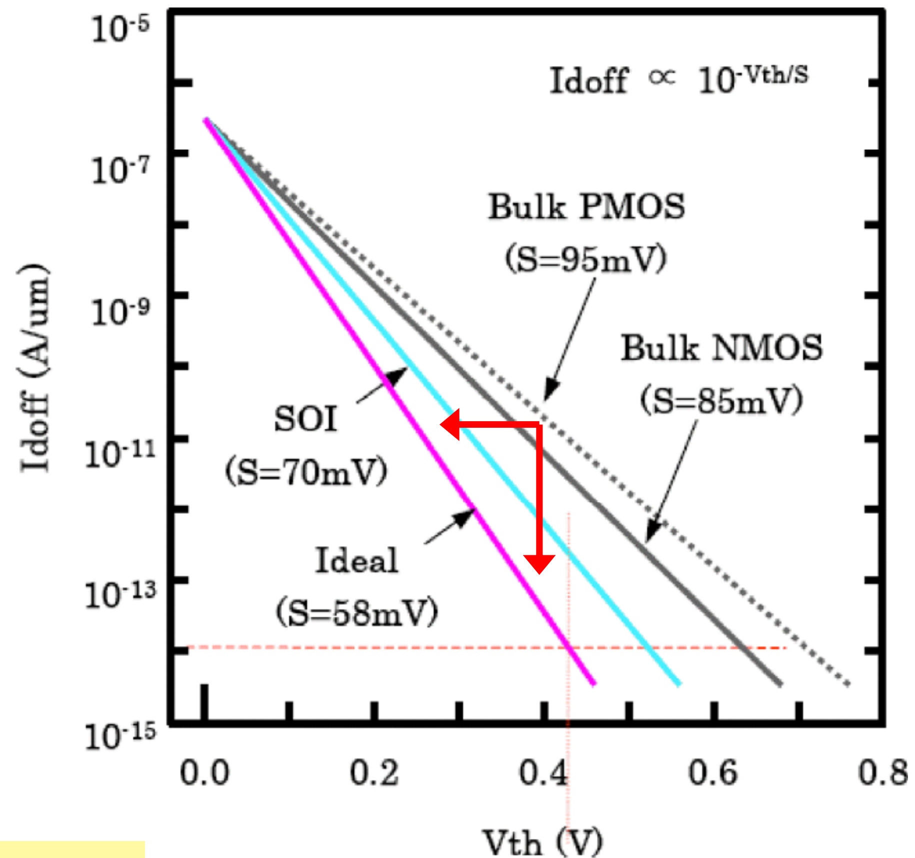


In SOI, Each Device is completely isolated by Oxide.



Steep Sub Threshold Slope





F.Ichikawa et al., SSDM, 2004

Gate voltage is not wasted to deplete the bulk.

Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).

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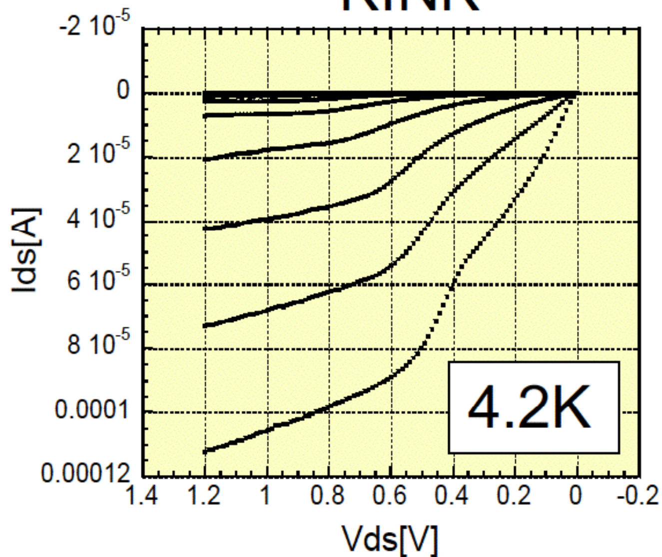
Operation at Cryogenic Temperature

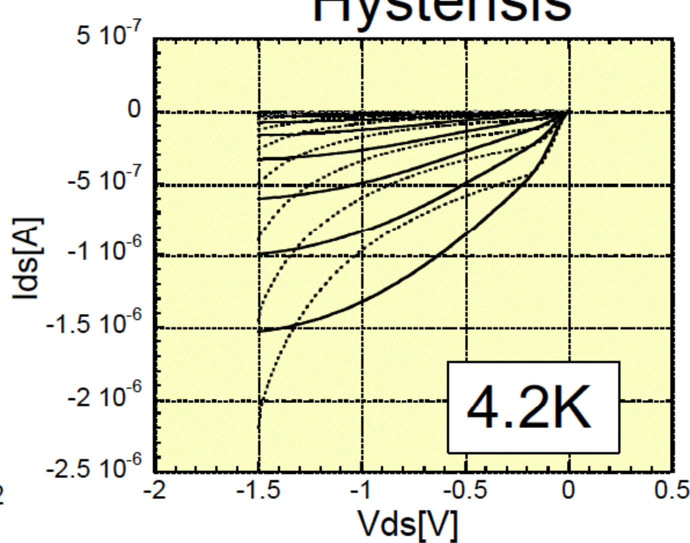
gate
source
drain
channel
n-type
n-type
depletion layer
holes produced by the impact ionization
can't escape through the body
if the temperarure is below 30K.(freeze out)
p-type Substrate

Bulk MOS

gate
source
drain
n-type
channel
n-type
depletion layer
40nm
Buried Oxide (BOX)
holes produced by the impact ionization
can't penetrate BOX, and escape into the channel
Substrate

SOI MOS

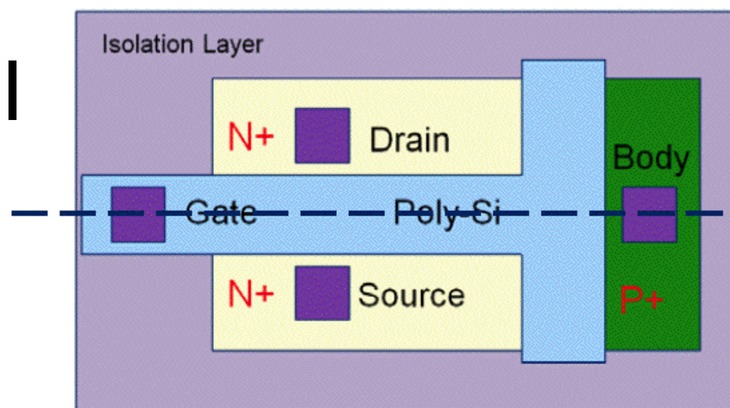


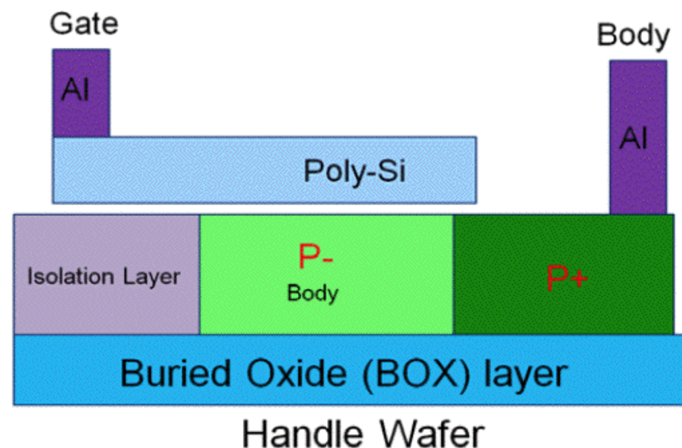


IV characteristics at cryogenic temperature

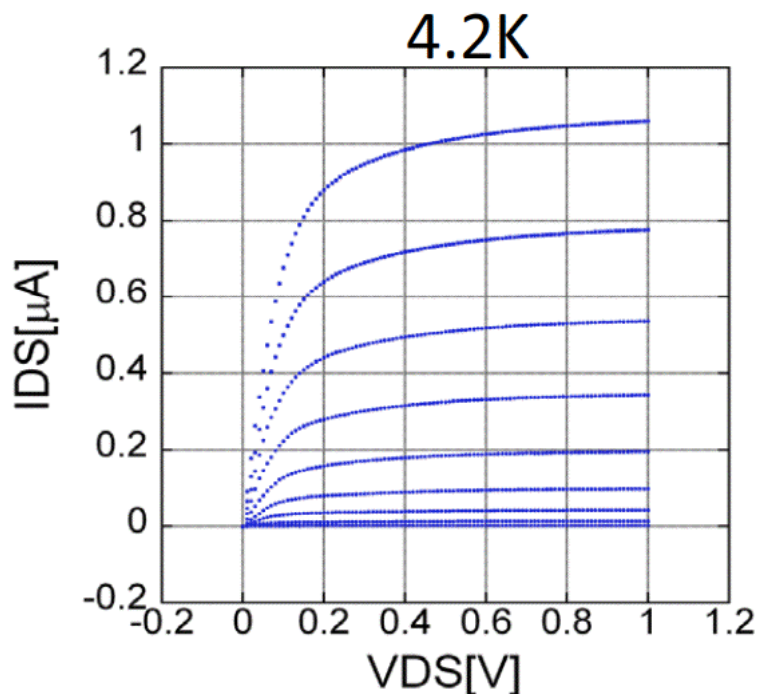
Body tie type

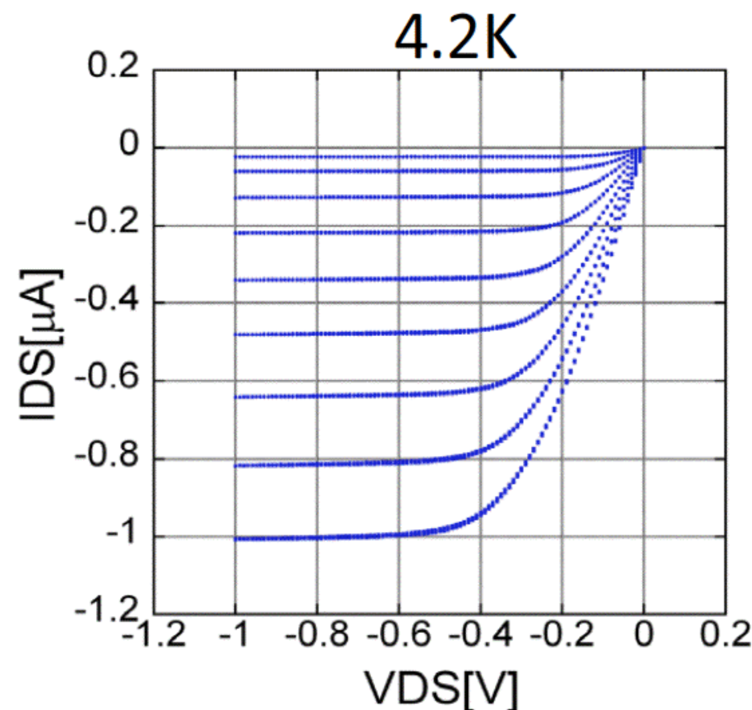
SOI





Body-tied W(μm)/L(μm)=0.5/10





The kink effects do not occur for |VDS|≤1.0V (L=10 μm)

SOI Pixel Project Brief History

'05. 4 : Proposed to KEK Detector Technology Project.
(Generic R&D)

'05. 7 : Start Collaboration with OKI Semiconductor.

'05.10 : 1st Submission in VDEC 0.15 um MPW.

'06.12 : 1st (and last) 0.15 um KEK MPW run.

'07.3 : 0.15 um lab. process line was closed.

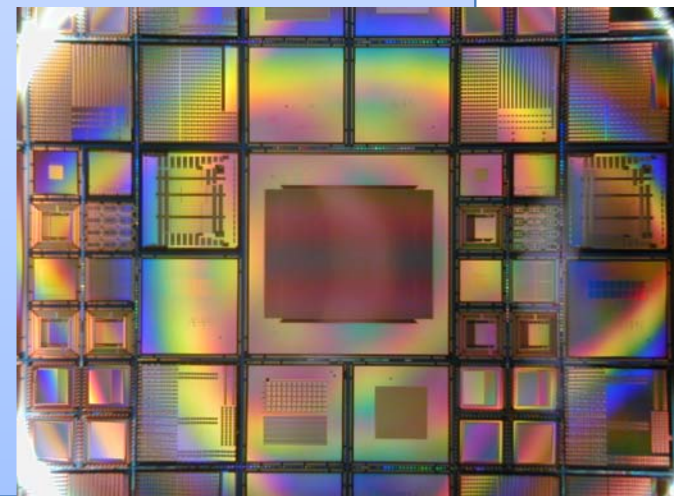
→ move to 0.2 um mass production line at Miyagi.

'08.1 : 1st 0.2 um KEK SOI-MPW run.

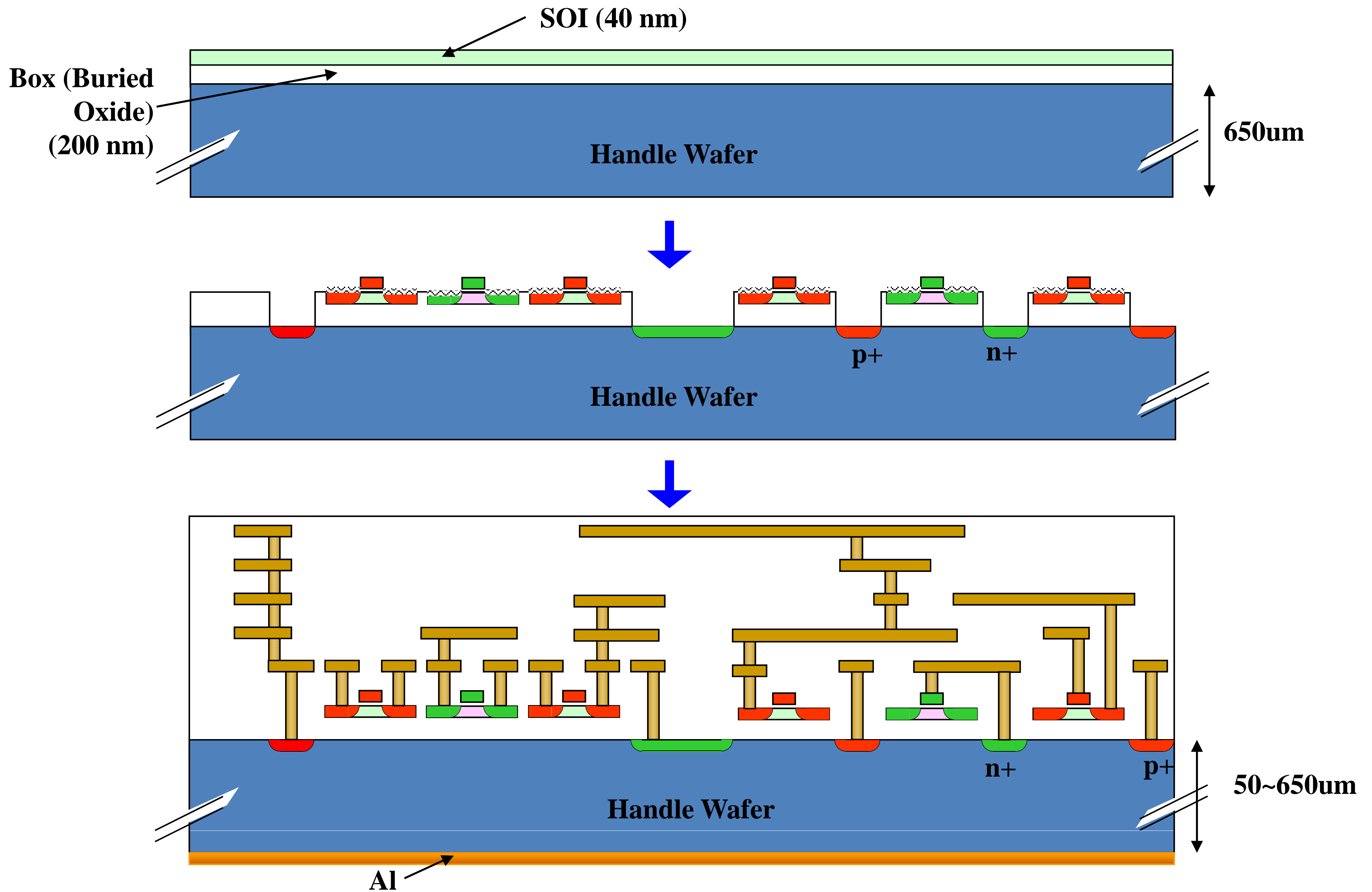
'08.10 : OKI is owned by ROHM Co. Ltd.
(Lehman Shock)

:

'11.1: 6th KEK SOI-MPW run



SOI Pixel Process Flow



OKI semi/ROHM 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) ~7k Ω-cm, FZ(p) ~40 k Ω-cm
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

MPW (Multi Project Wafer) run

We are operating MPW runs Twice / year.
(Next MPW run is Oct. 3rd.)

Louvain-la-Neuve Univ.

U. of Hawaii

Riken

INP Krakow

FNAL

FNAL

IHEP China

LBNL

LBNL

U. Heidelberg

U. Tohoku

CNTPIX4

INTPIX
3C

CNTPIX5

Kyoto Univ.

JAXA/ISAS

KEK

KEK
MPI

Krakow

3D_L

3D_U

Tsukuba Univ.

INTPIX4

KEK

JAXA

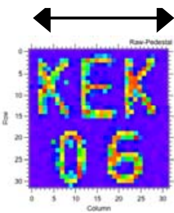
KEK KEK

AIST

SOI Pixel Detectors

2006

0.64 mm

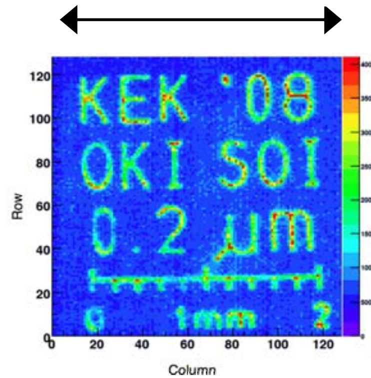


32x32

Vbias~10V

2008~9

2.56 mm

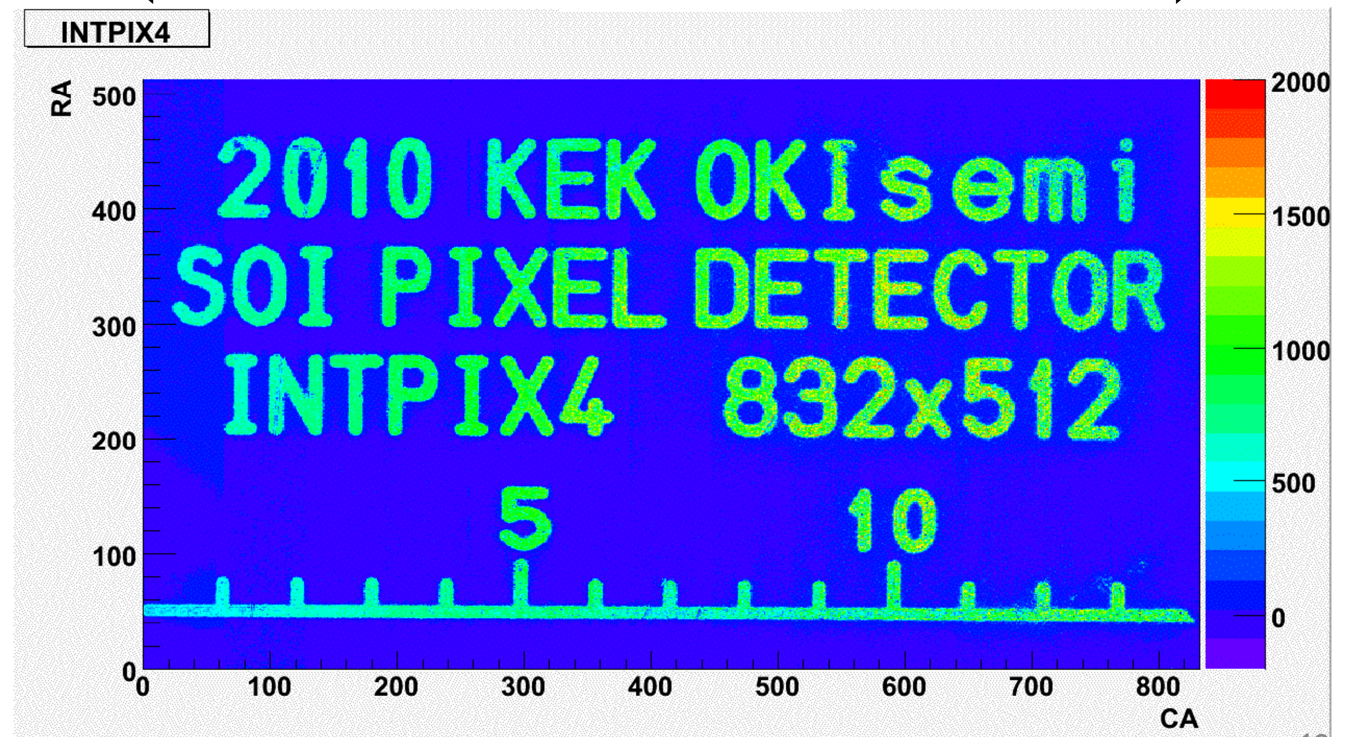


128x128

Vbias~100V

2010

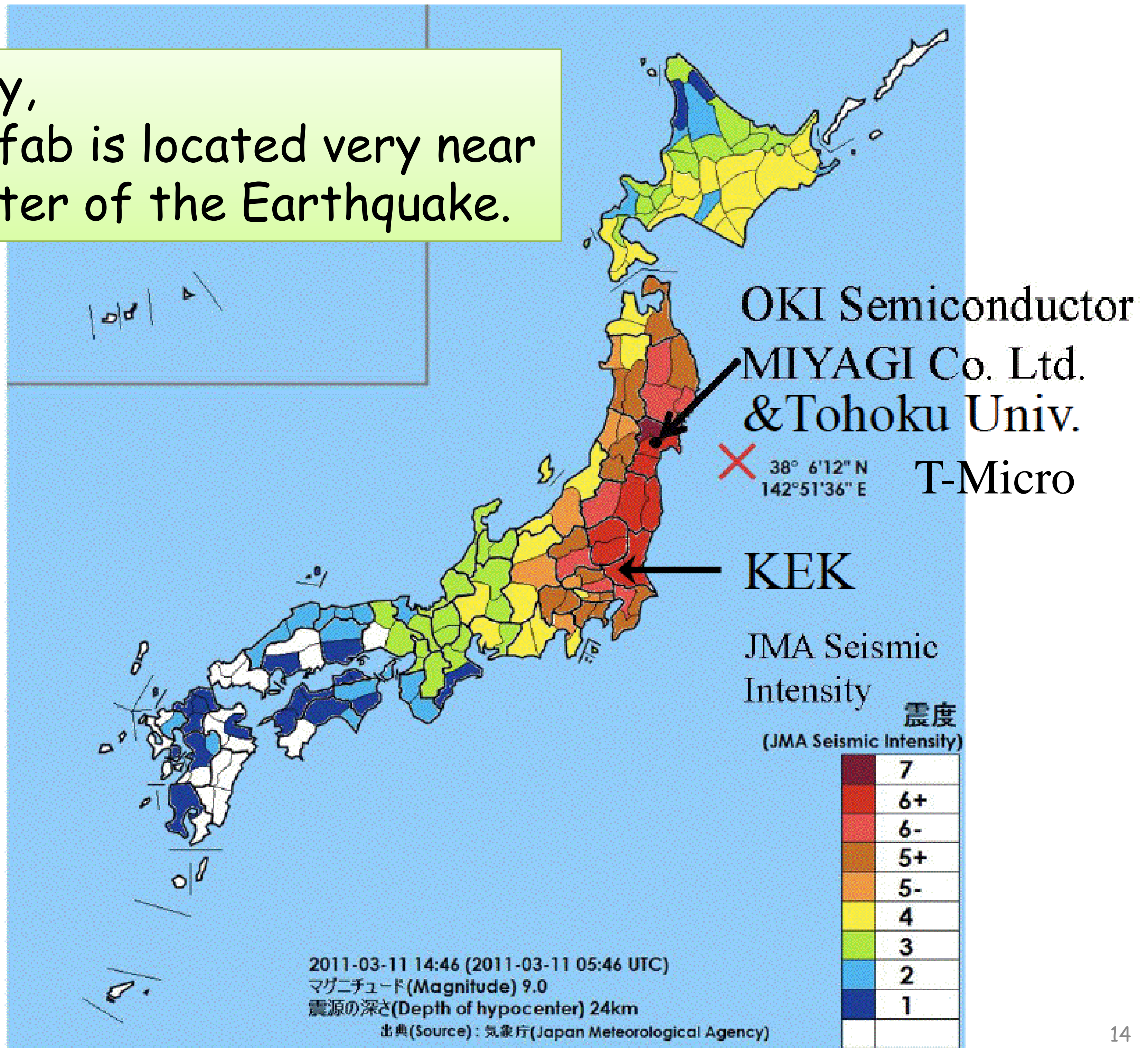
13.8 mm



832x512

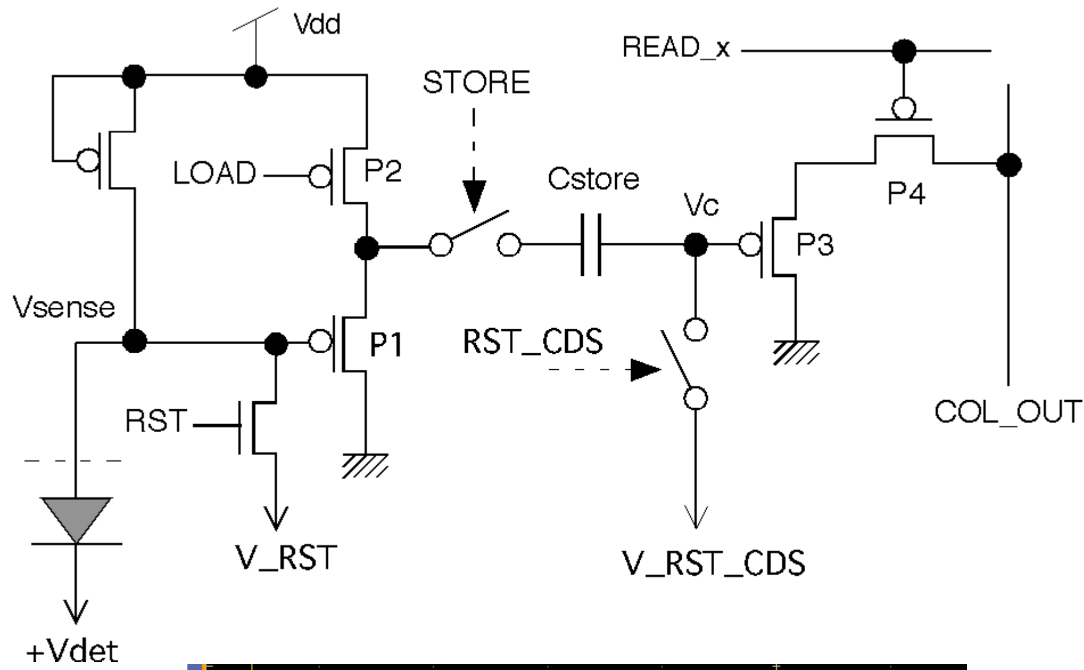
Vbias~250V

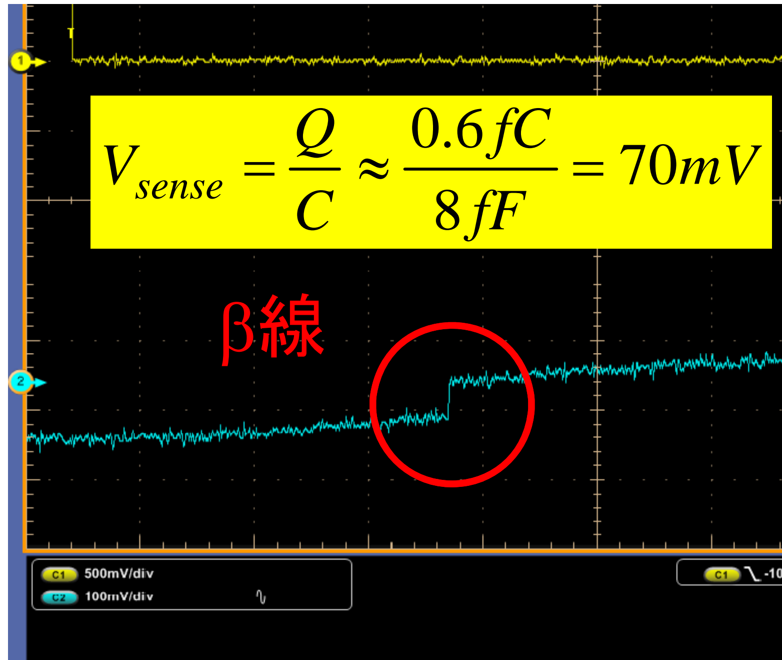
By the Way,
OKI Semi fab is located very near to the Center of the Earthquake.

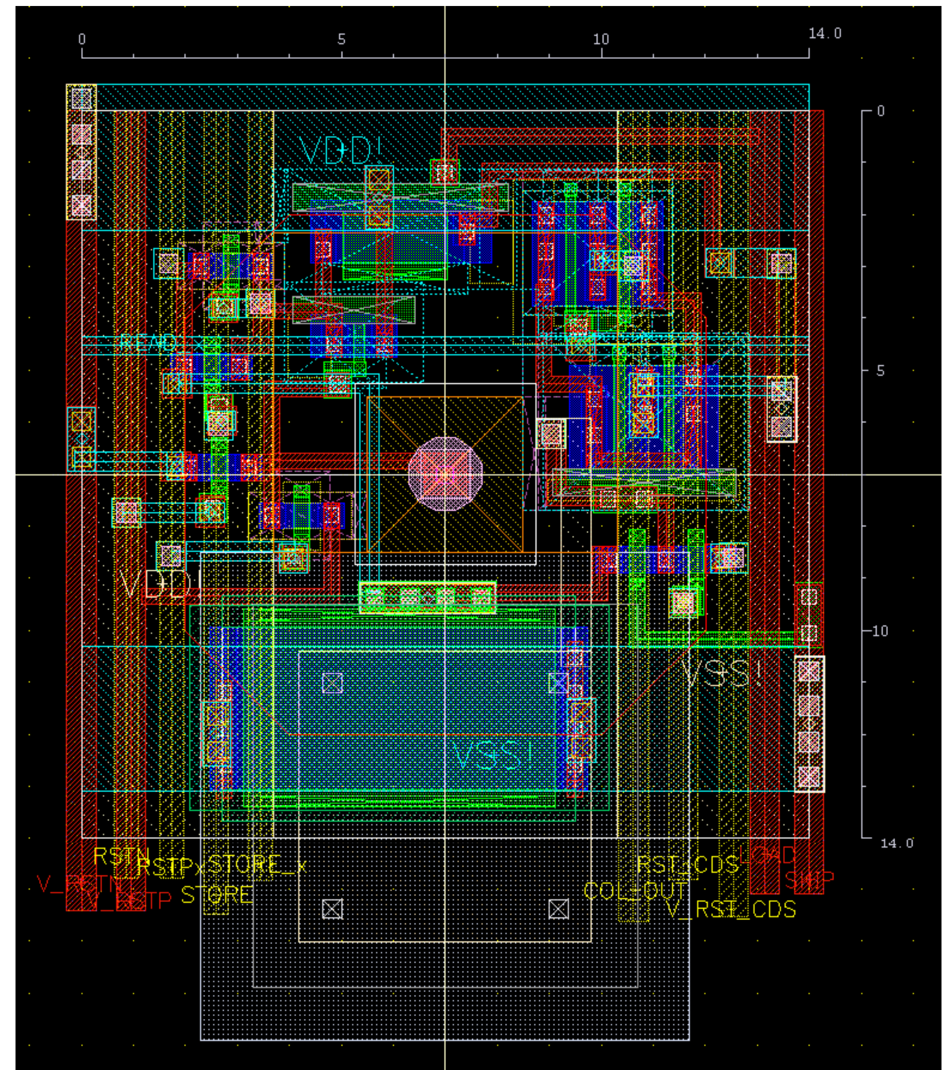


SOI Detectors

Integration Type Pixel (INTPIX)







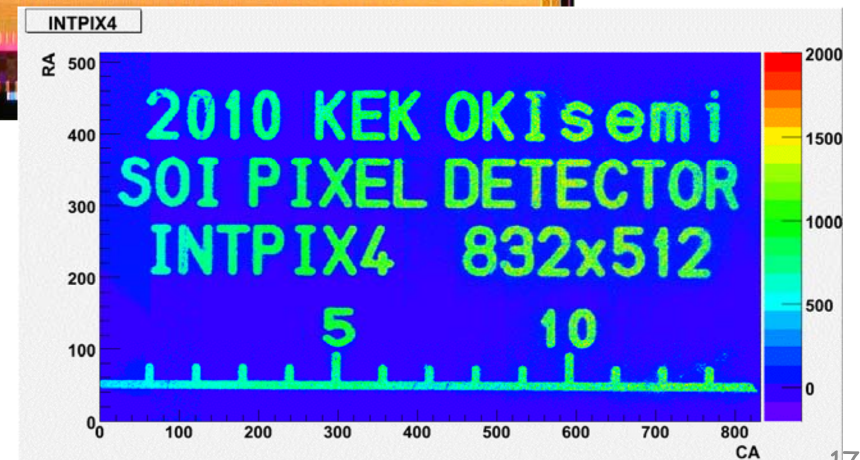
Size : 14 μm x 14 μm
with CDS circuit

Integration Type Pixel (INTPIX4)

Largest Chip so far.

10 mm

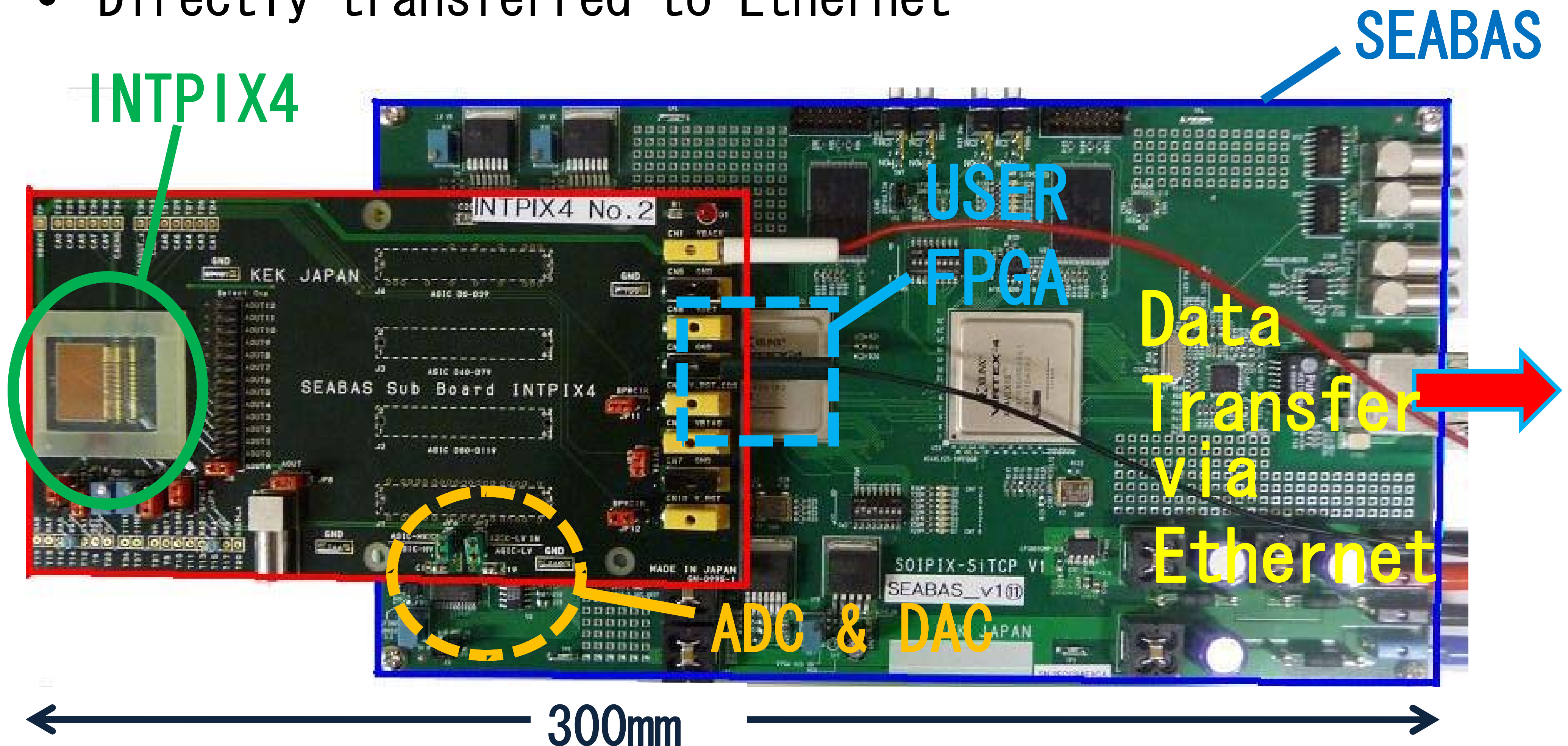
15 mm



17x17 μm, 512x832 (~430k) pixels、13 Analog Out、CDS circuit in each pixel.

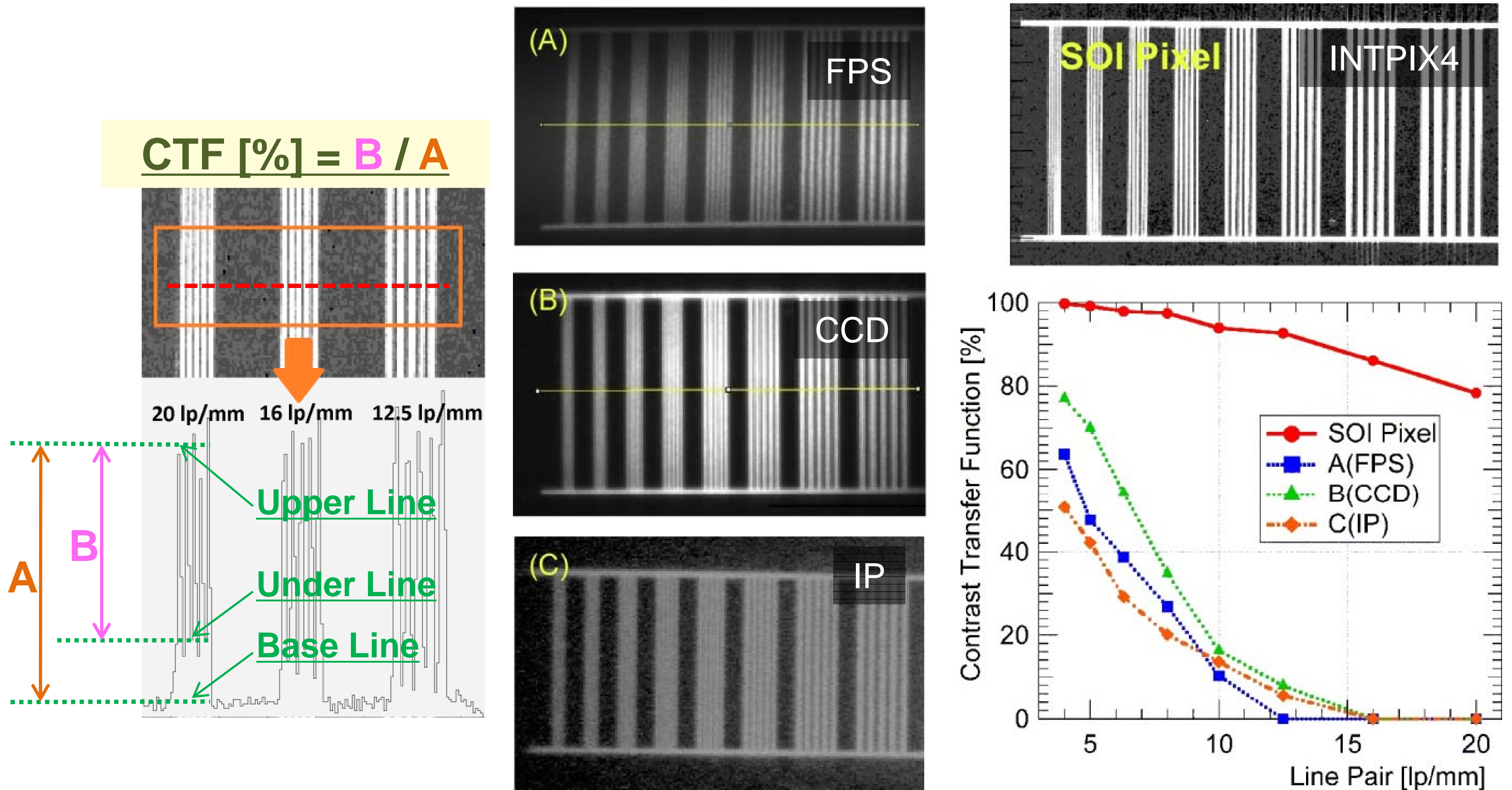
Data Acquisition Board

- Soi EvAluation BoArd with Sitcp(SEABAS)
- A FPGA controls the SOI Pixel chip
- Directly transferred to Ethernet



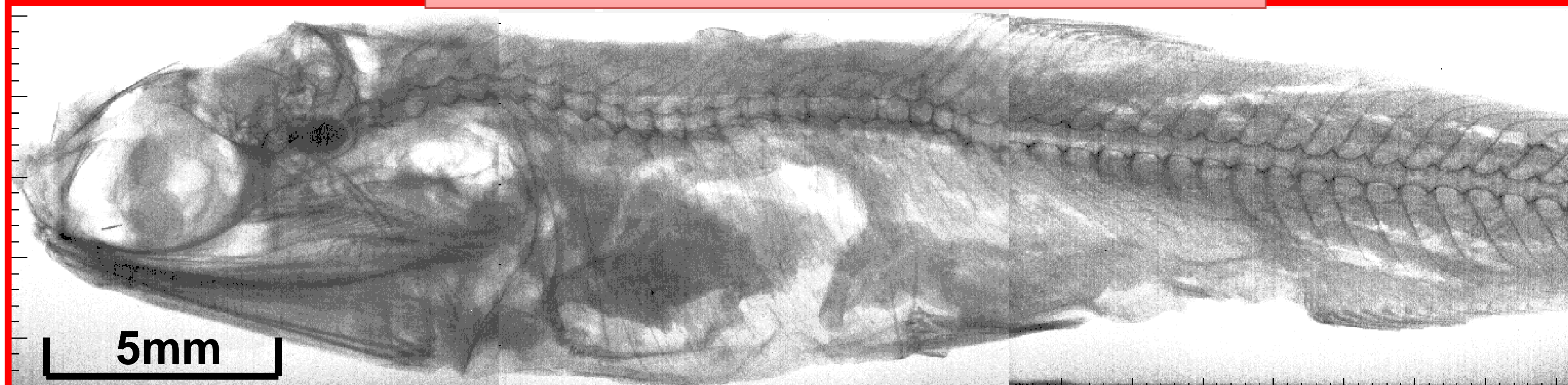
Spatial Resolution (Contrast Transfer Function)

- Comparison of contrasts with commercial X-ray devices.
  - SOI Pixel : INTPIX4, **F**lat **P**anel **S**ensor (FPS), CCD, and **I**maging **P**late (IP)



INTPIX4
Pixel Size : 17 um x 17 um
No. of Pixel : 512 x 832 (= 425,984)
Chip Size : 10.3 mm x 15.5 mm
Vsensor=200V, 250us Int. x 500
X-ray Tube : Mo, 20kV, 5mA

Fine resolution & High Contrast

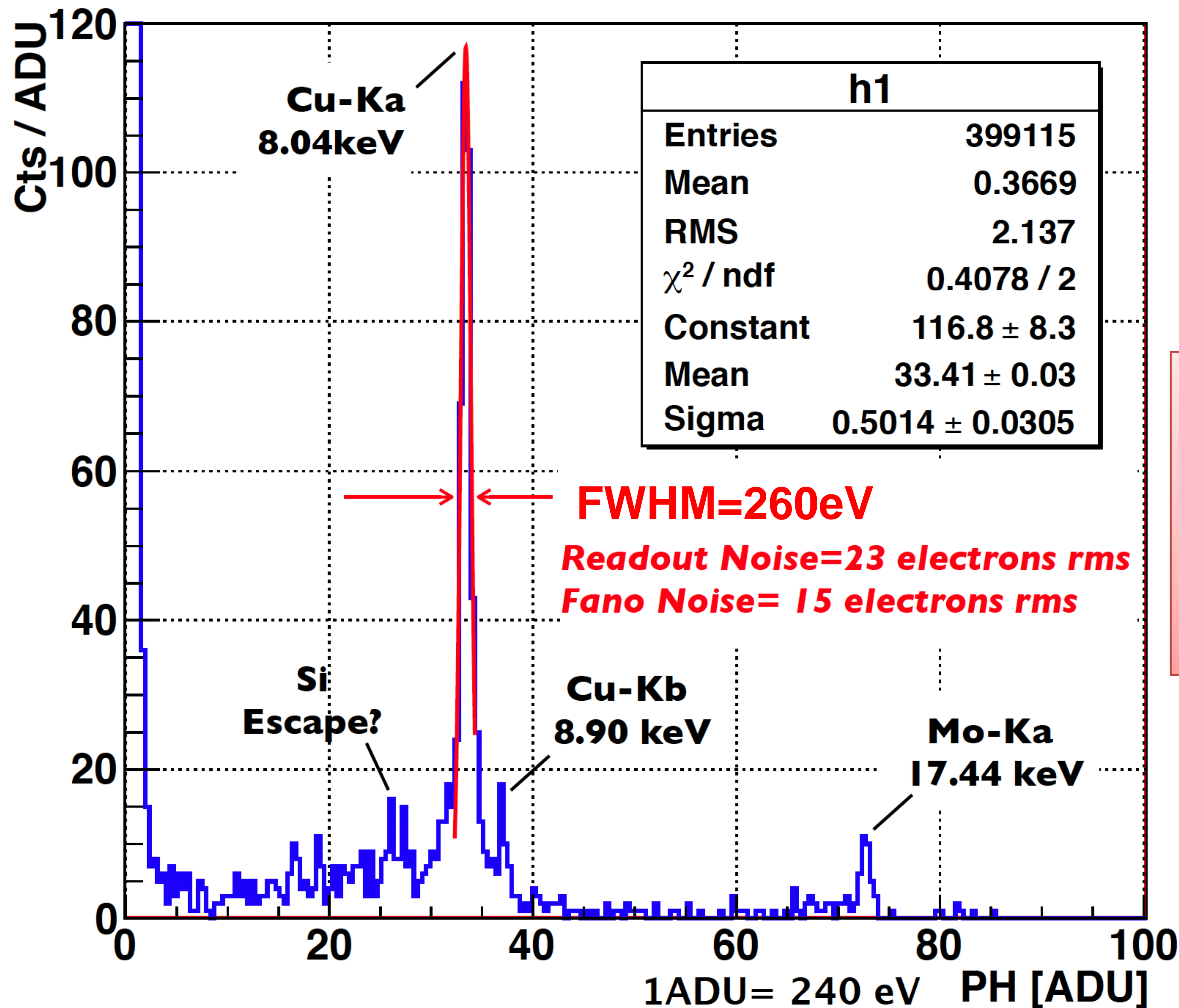


X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).

(A. Takeda)

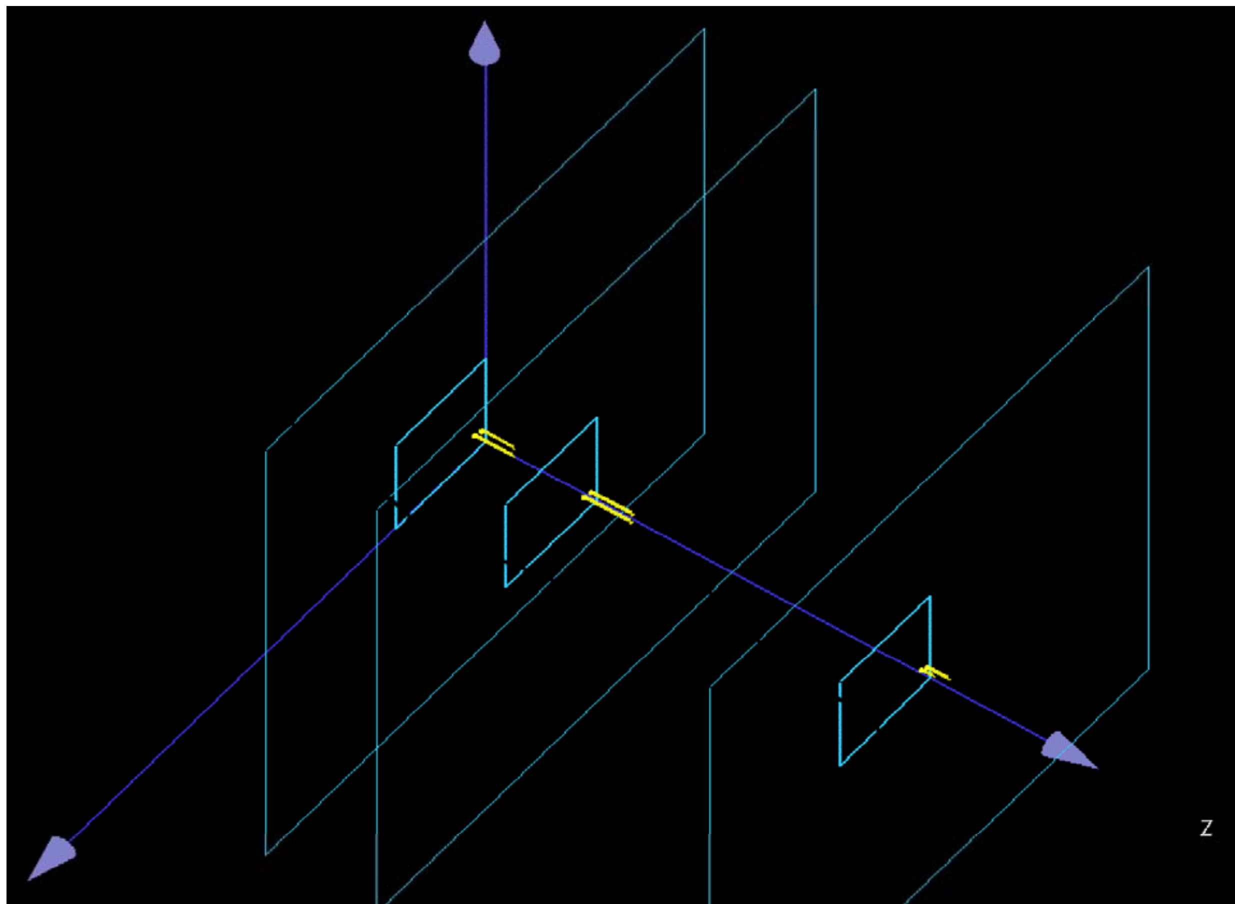
XRPIX1

◎ XRPIX1-CZ Correlated Multi Sampling 試験 2011/02/10@-50℃,100Vb
◎ 39D (ST&BT Type) Single Pixel (25,25) Spectrum (Target: Cu + Mo)

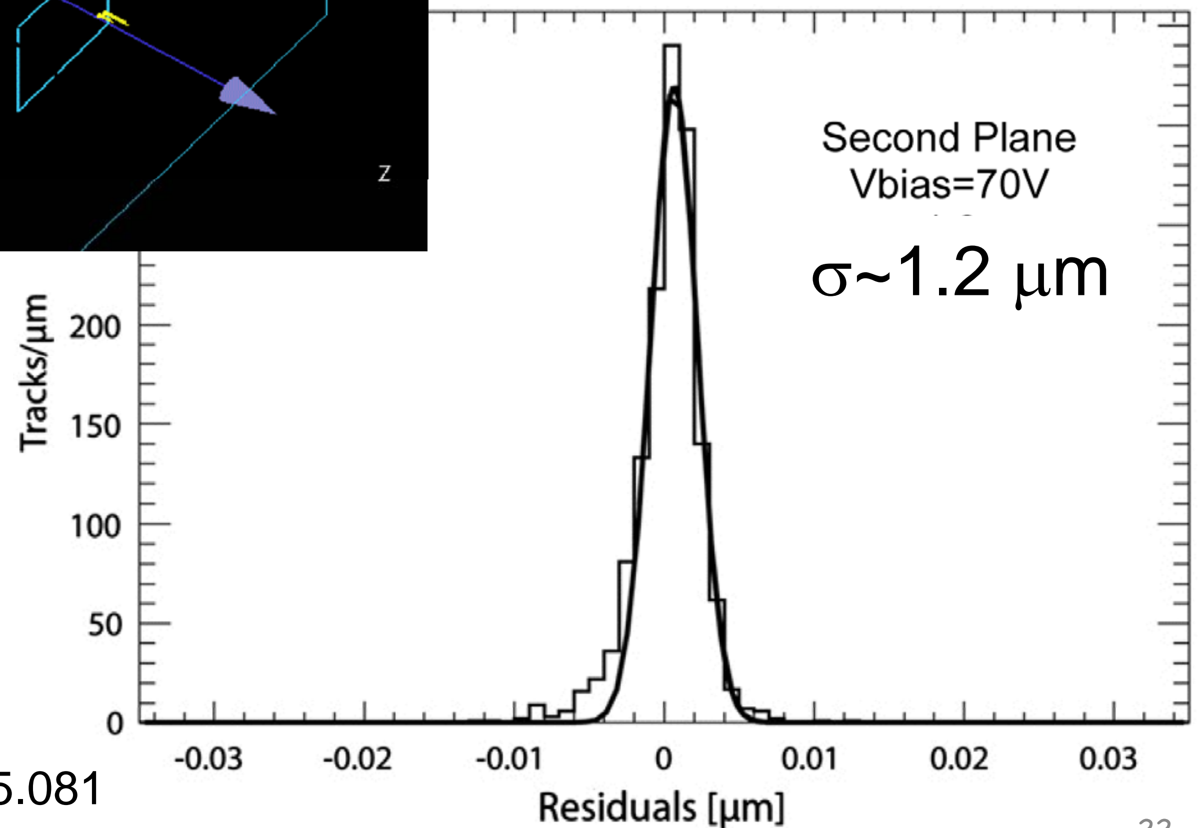


Cu Kα and Kβ is separated
Noise ~ 23e⁻
@-50°C

(Kyoto Univ.)



CERN SPS
200GeV/C π^- beam

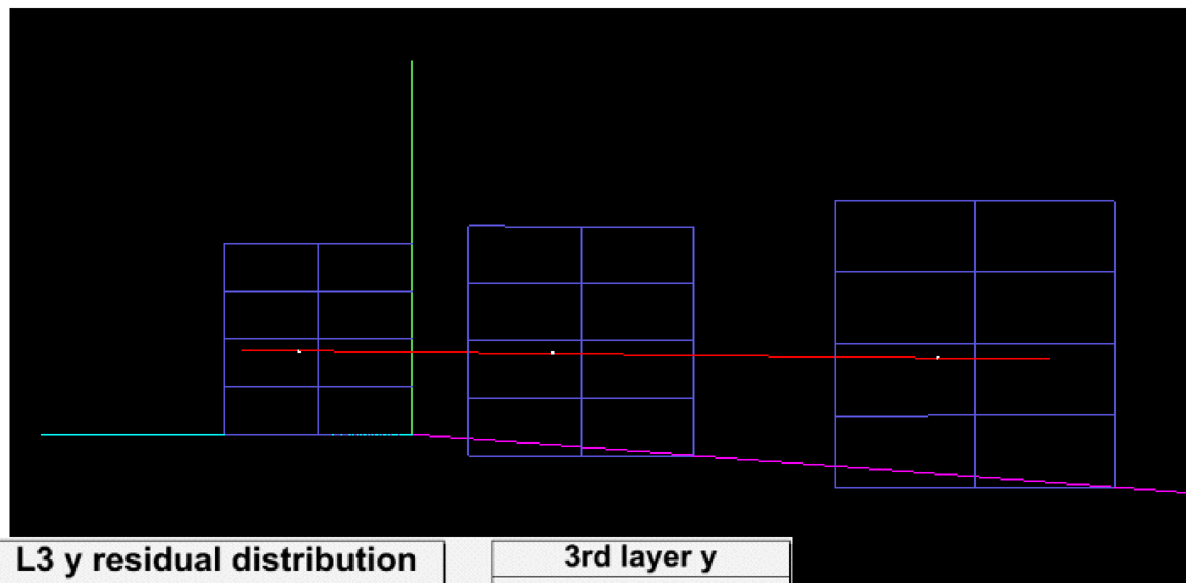


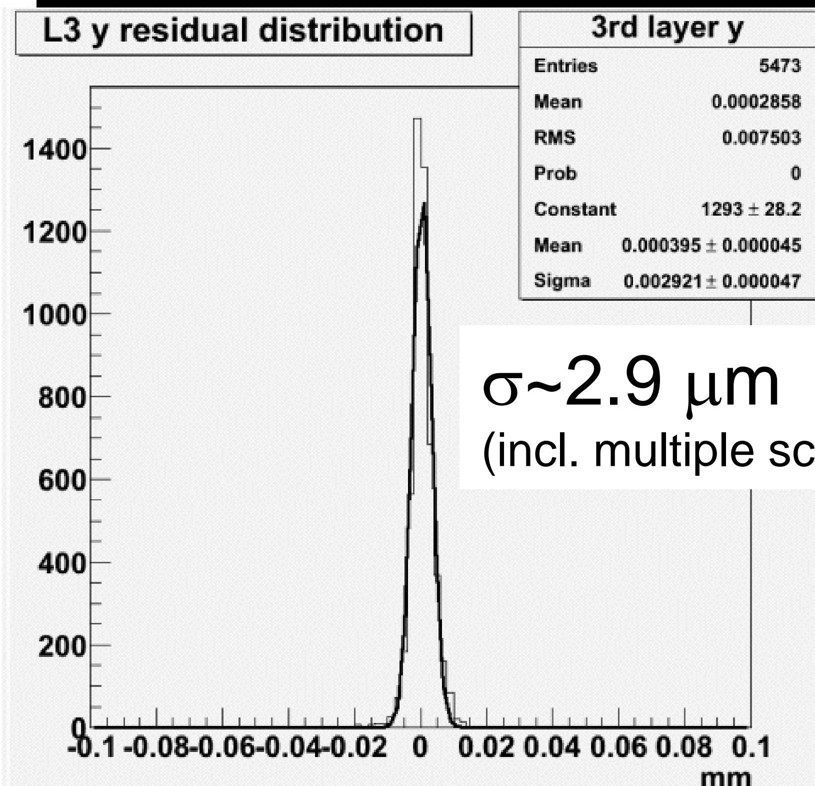
LBNL & Padove

NIM A, M. Battaglia et al.,
http://dx.doi.org/10.1016/j.nima.2011.05.081

e+ Beam Test at Tohoku Univ.

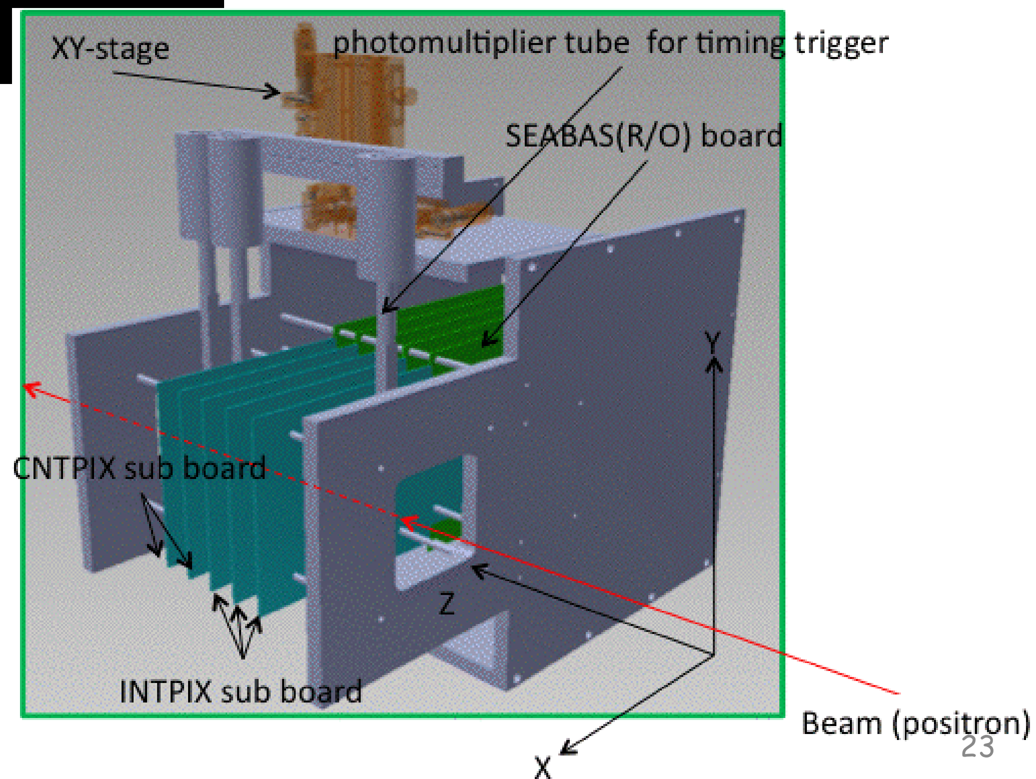
SOI beam test 2010 collaboration





σ~2.9 μm
(incl. multiple scattering)

e+ Beam ~673MeV/c



Counting Type Pixel (CNTPIX)

CNTPIX5 Pixel

Vfb

Dual Discri

from/to
other
3 pix

VthH

Window

Counter
Control
Logic

Programable
Counter

9 bit
9 bit

Charge
Amp

Shaper

VthL

fine DAC_H
3bit

18

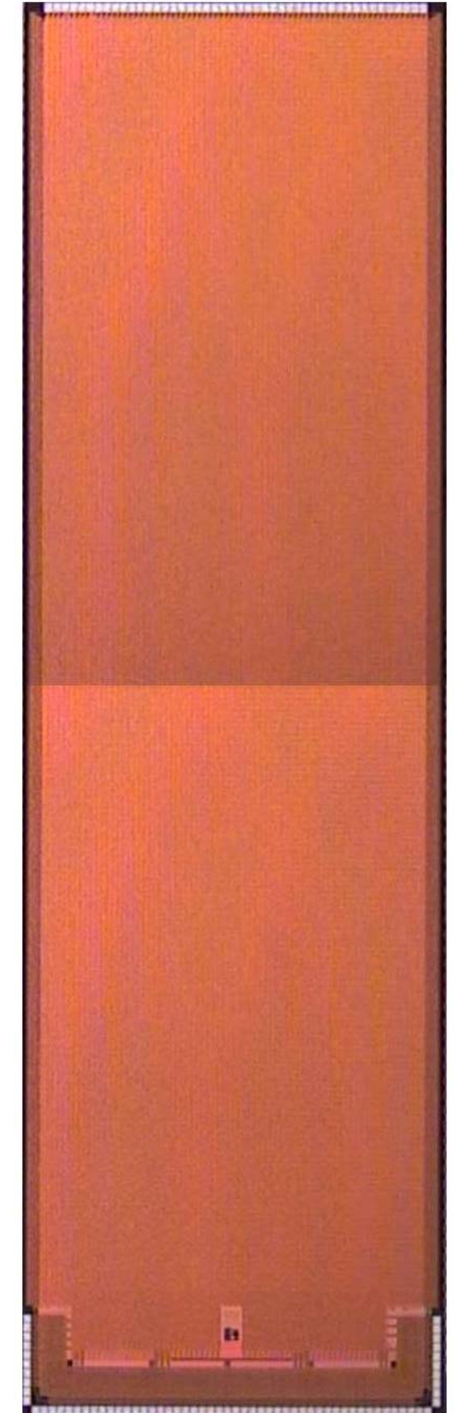
Control
Registers

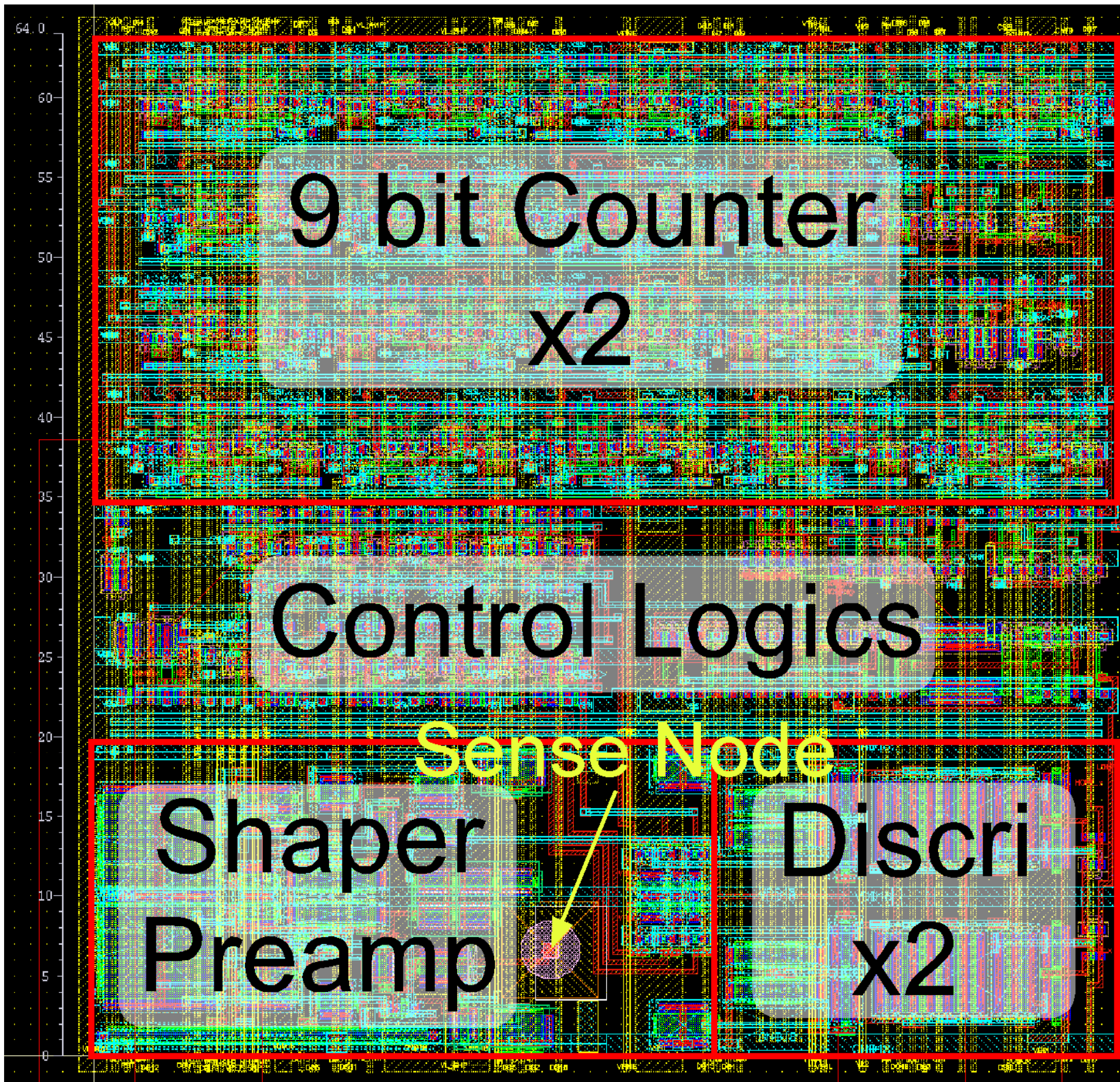
fine DAC_L 3bit

+Vdet

Energy selection and
Counting in each pixel.
4 pixels can be
combined.

5 x15.4 mm^2
72 x 272 pixels
64um x 64 um pixel





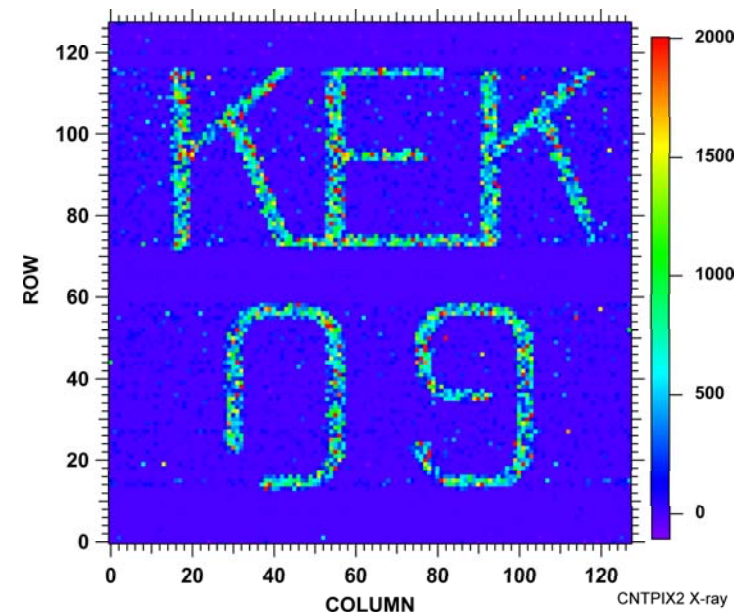
CNTPIX5
Pixel Layout

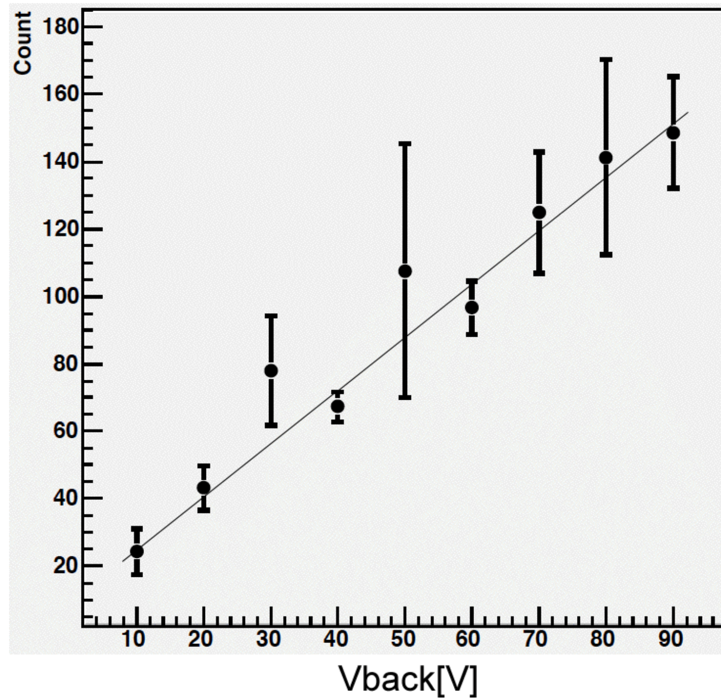
64x64 um²

~600 Tr/pix
x 72 x 212
= 10 M Trs

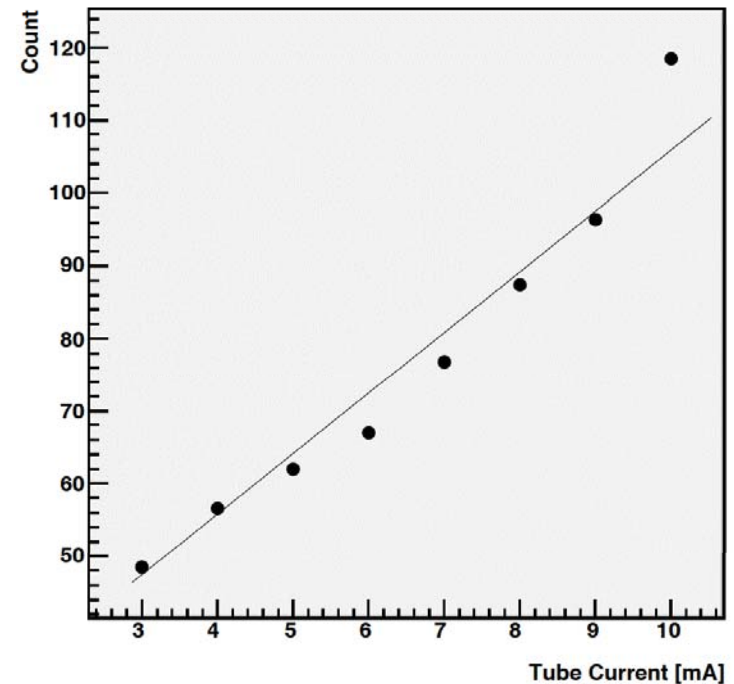
CNTPIX X-ray Test

Pixels are working but some crosstalks are observed.



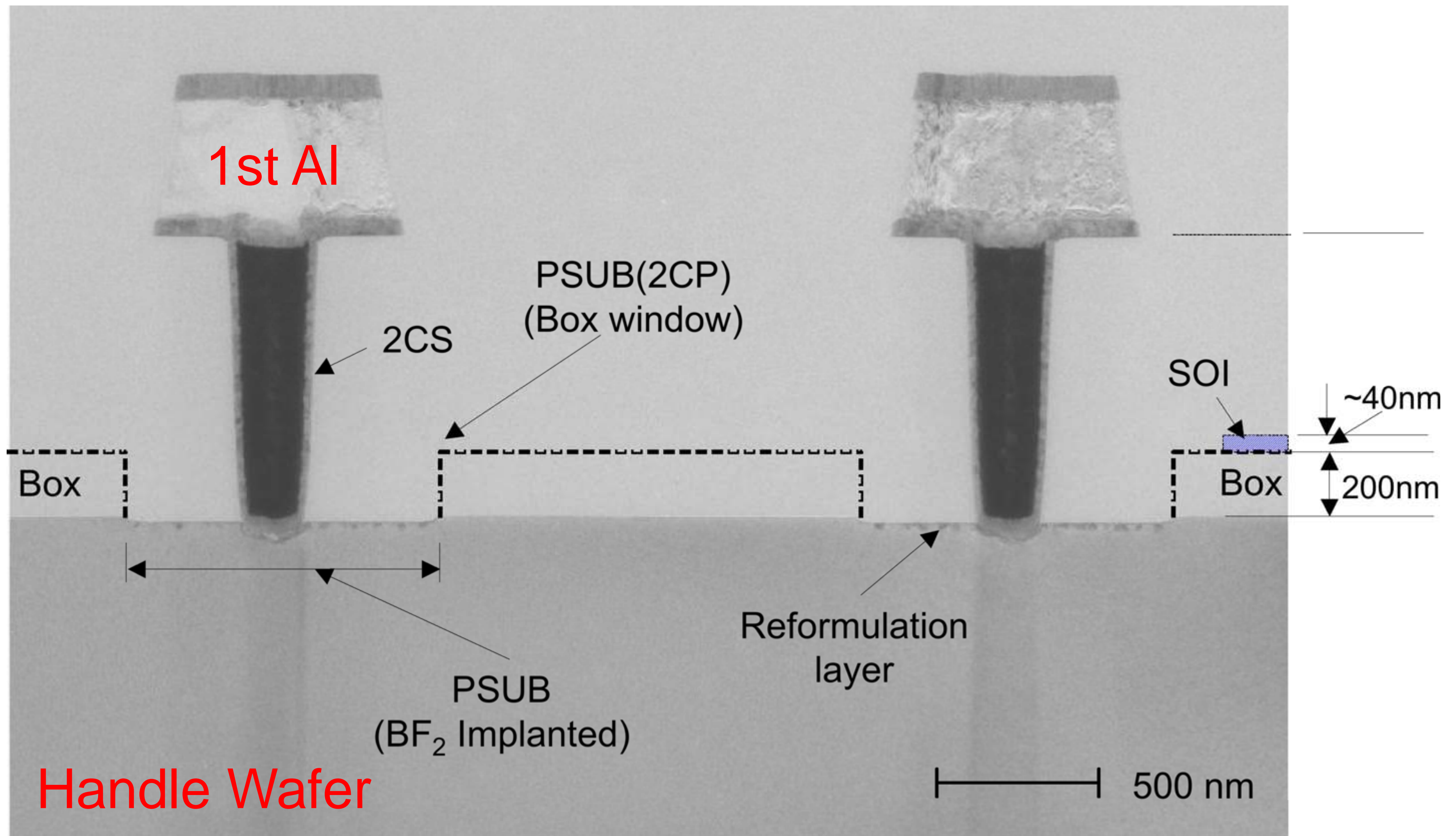


Count v.s. sensor bias.

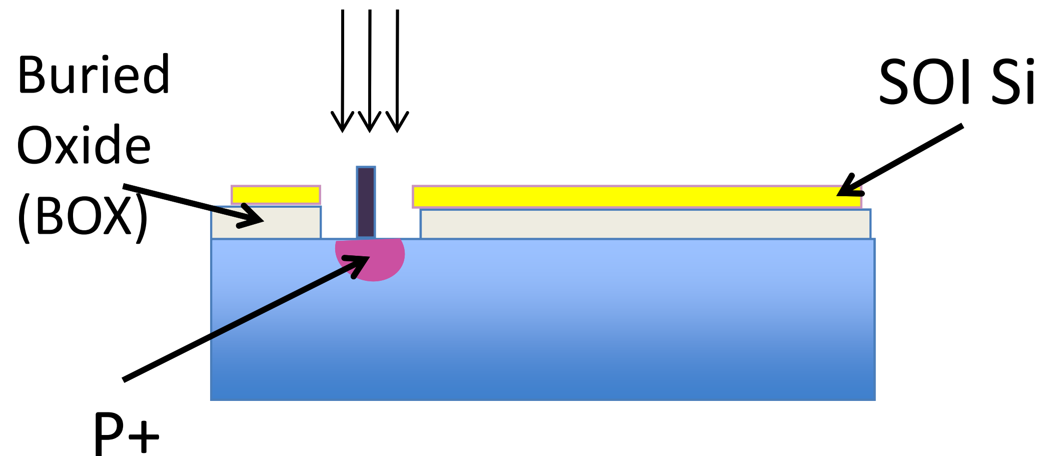


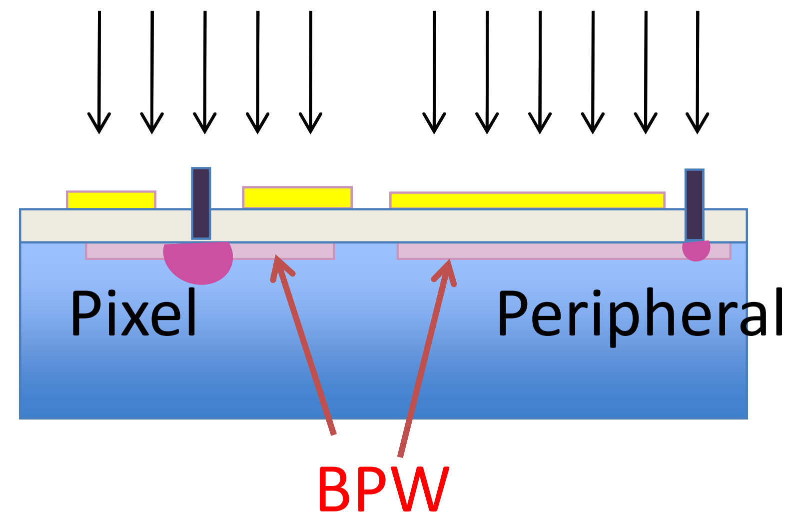
Count v.s. X-ray Tube Current

Developing Techniques



Buried p-Well (BPW)





- Cut Top Si and BOX
- High Dose

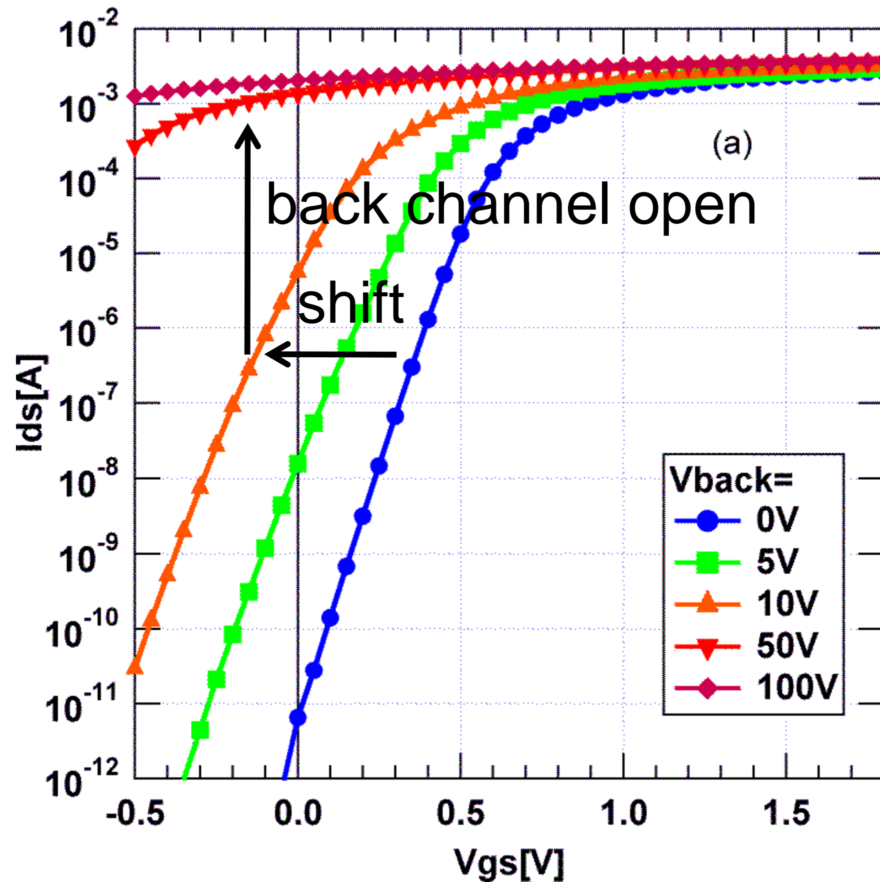
- Keep Top Si not affected
- Low Dose

- Suppress the Back Gate Effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which improve radiation hardness.

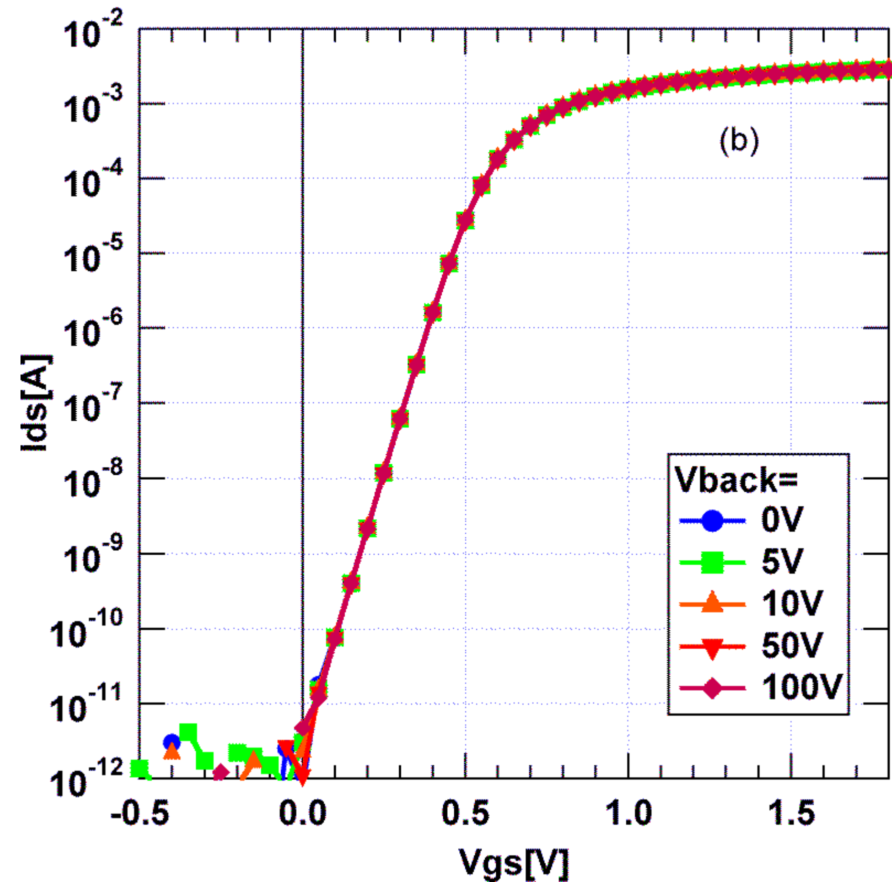
I_d-V_g and BPW

NMOS

w/o BPW



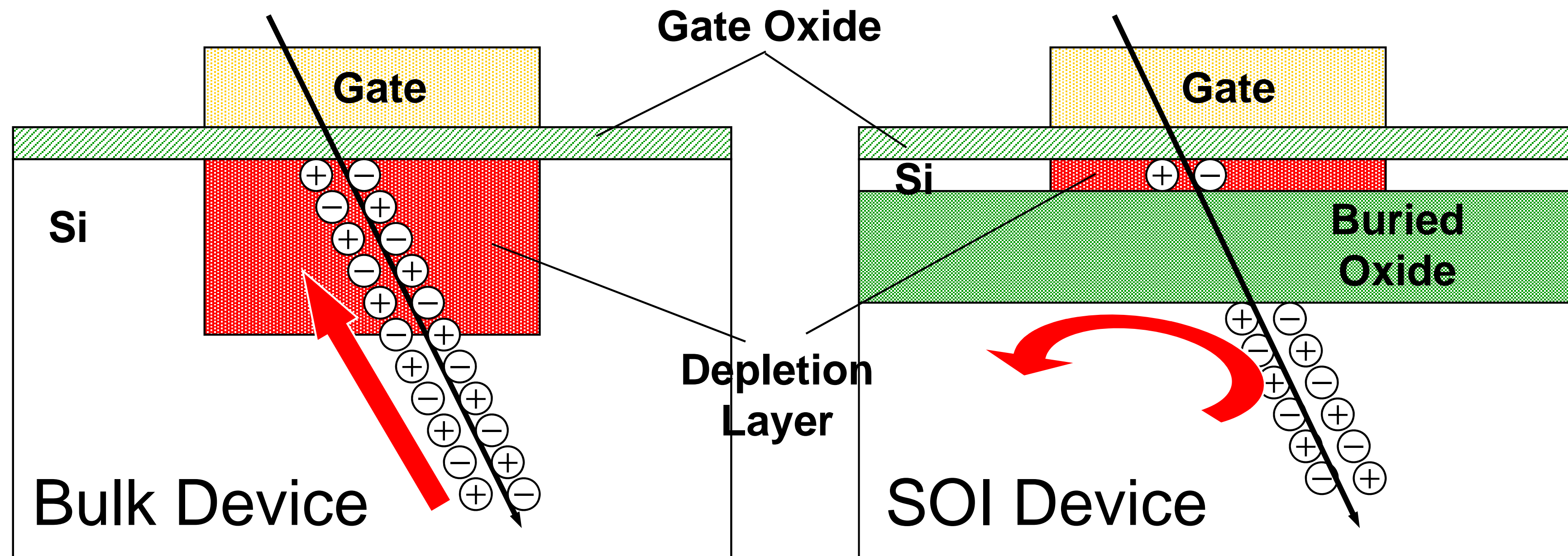
with BPW=0V



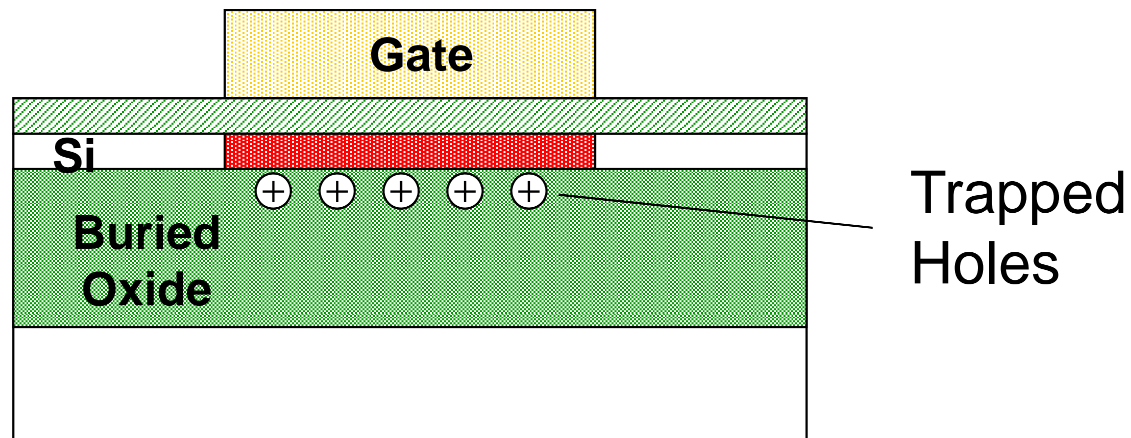
Back gate effect is suppressed by the BPW.

Radiation Tolerance

SOI is Immune to Single Event Effect



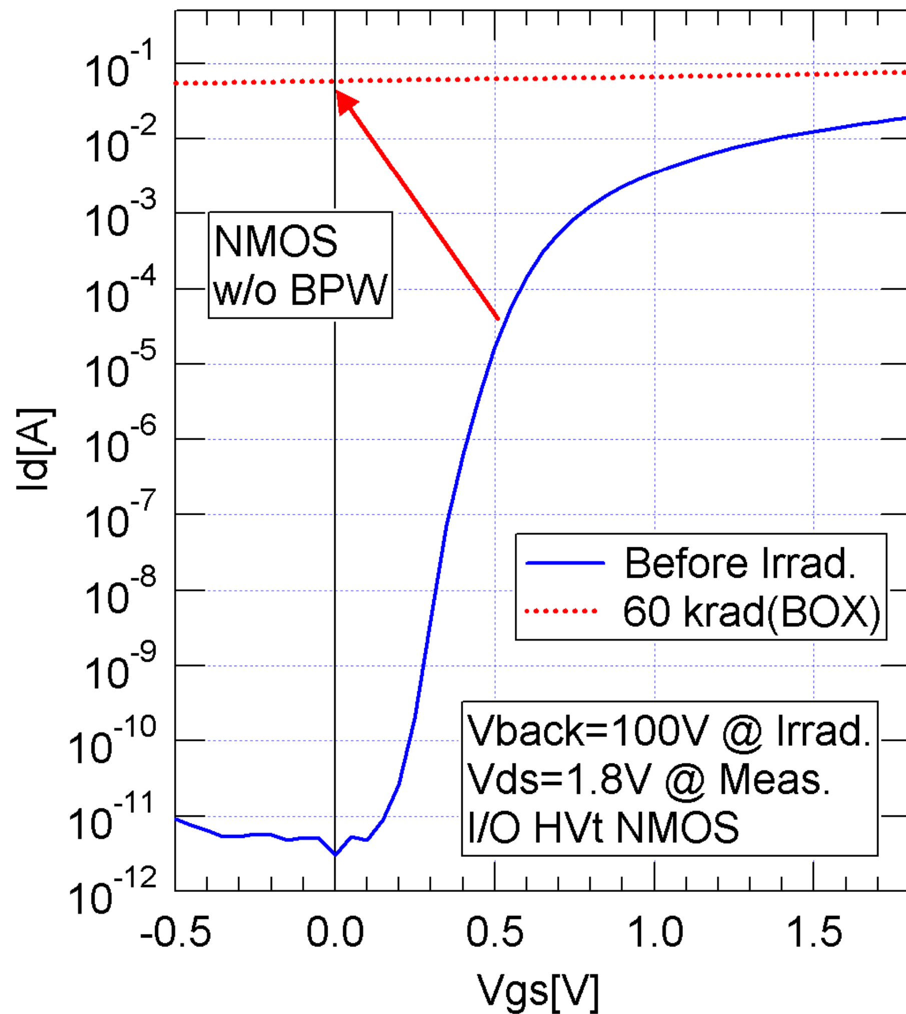
But not necessary strong to Total Ionization Dose due to thick BOX layer

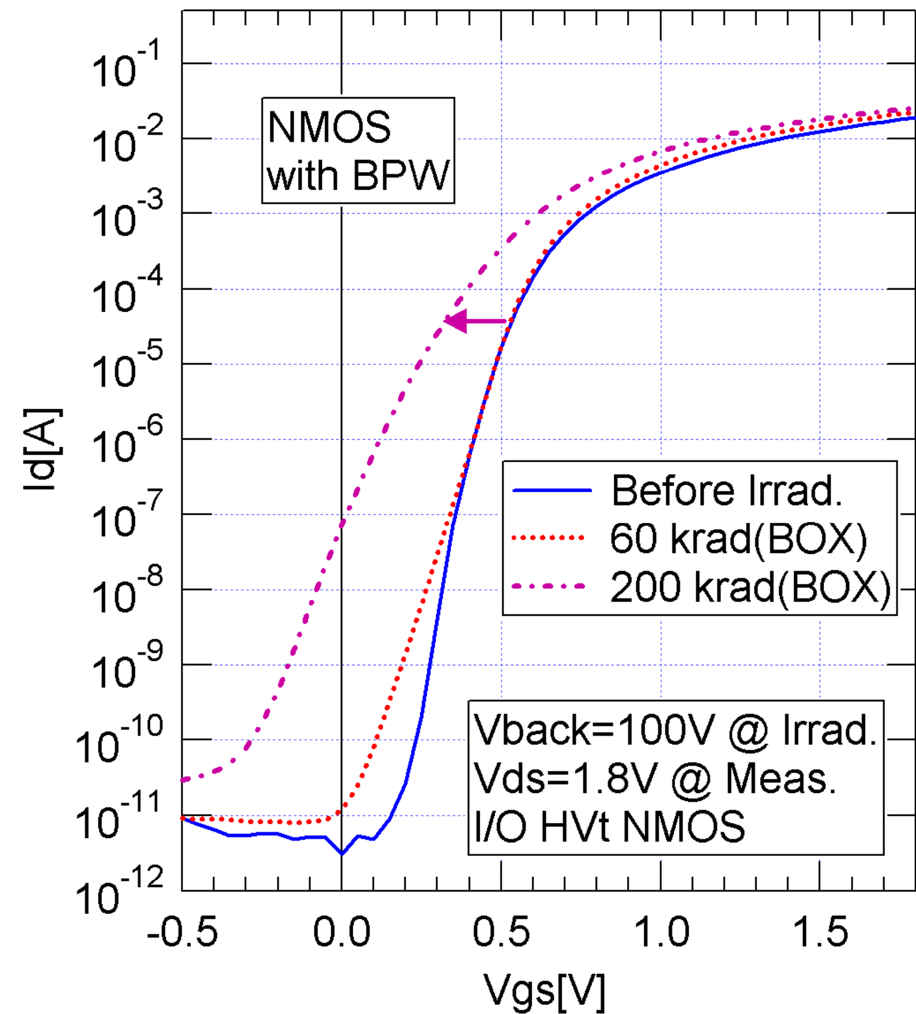


Radiation Tolerance and BPW

By adding the BPW layer, Electric field in the BOX is reduced and possibility of charge recombination will increase. Thus increase radiation tolerance.

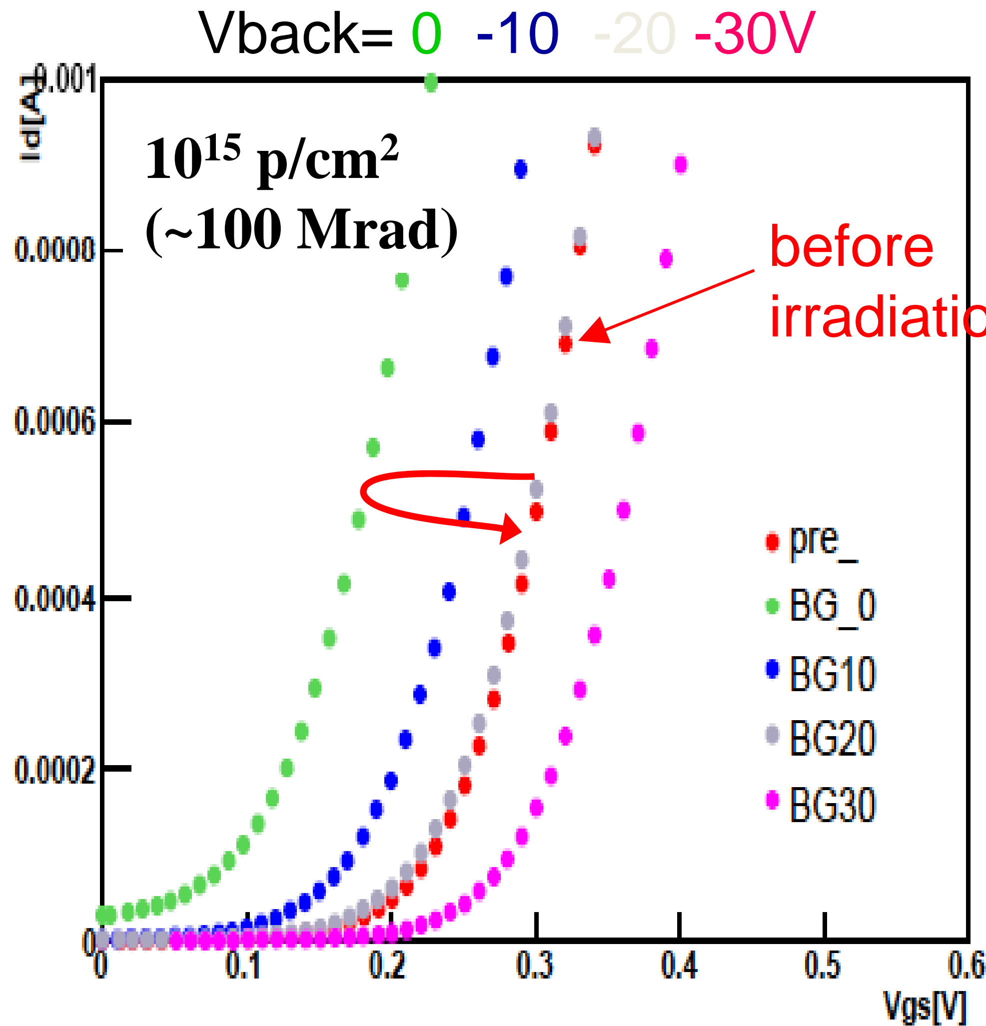
X-ray Irradiation

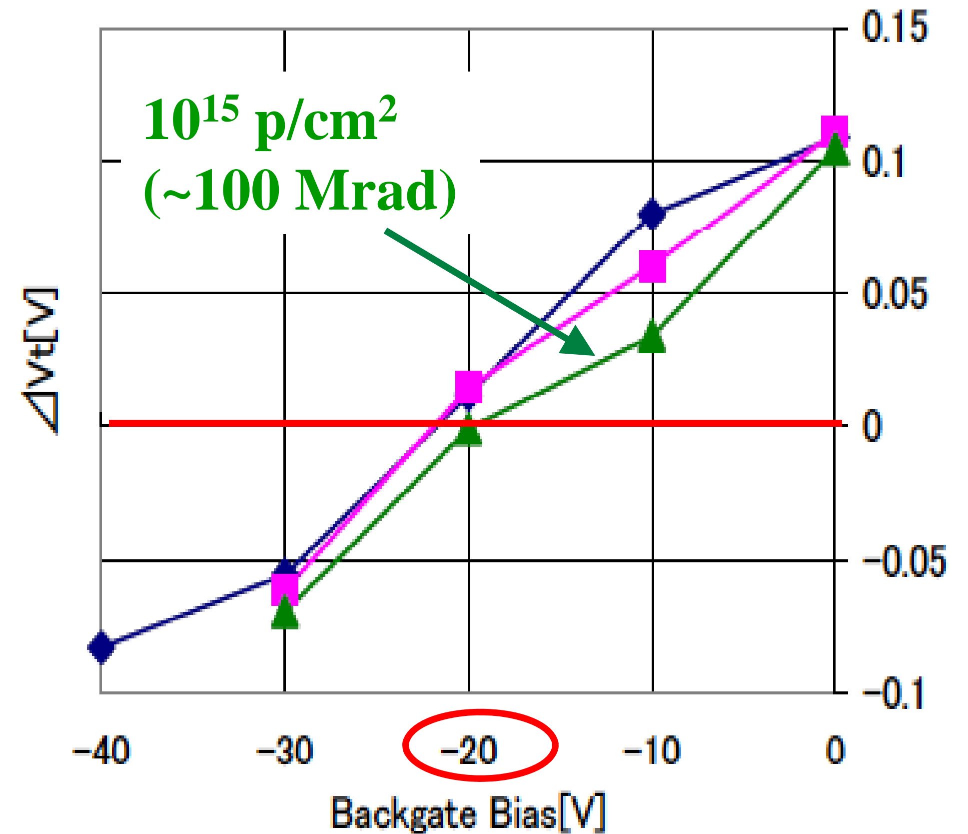




TID(Total Ionization Doze) Damage Compensation

Leak Current and V_{Th} resumes to nearly original value by biasing back side even at 100Mrad.

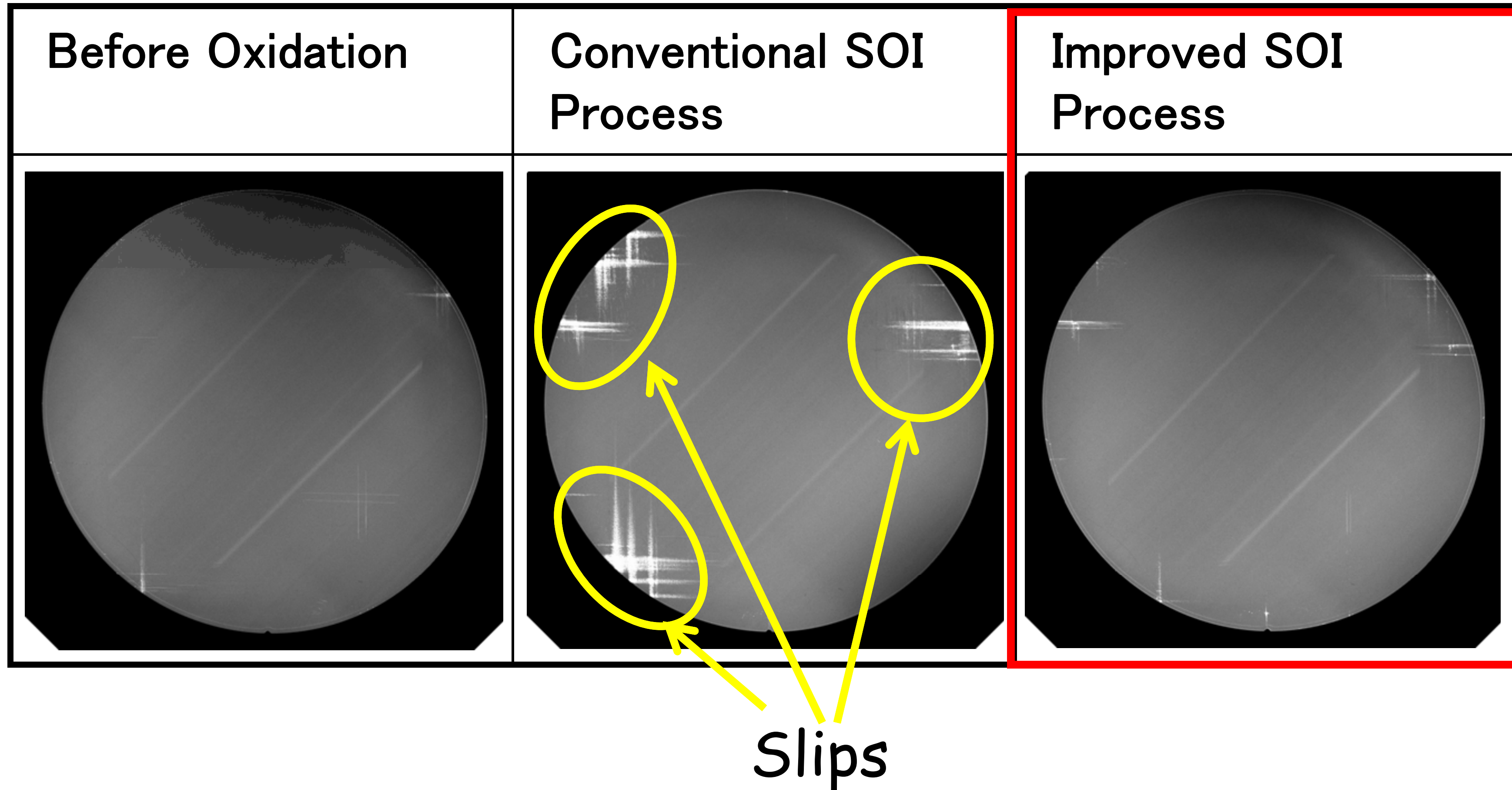




This can be done with nested well or double SOI wafer

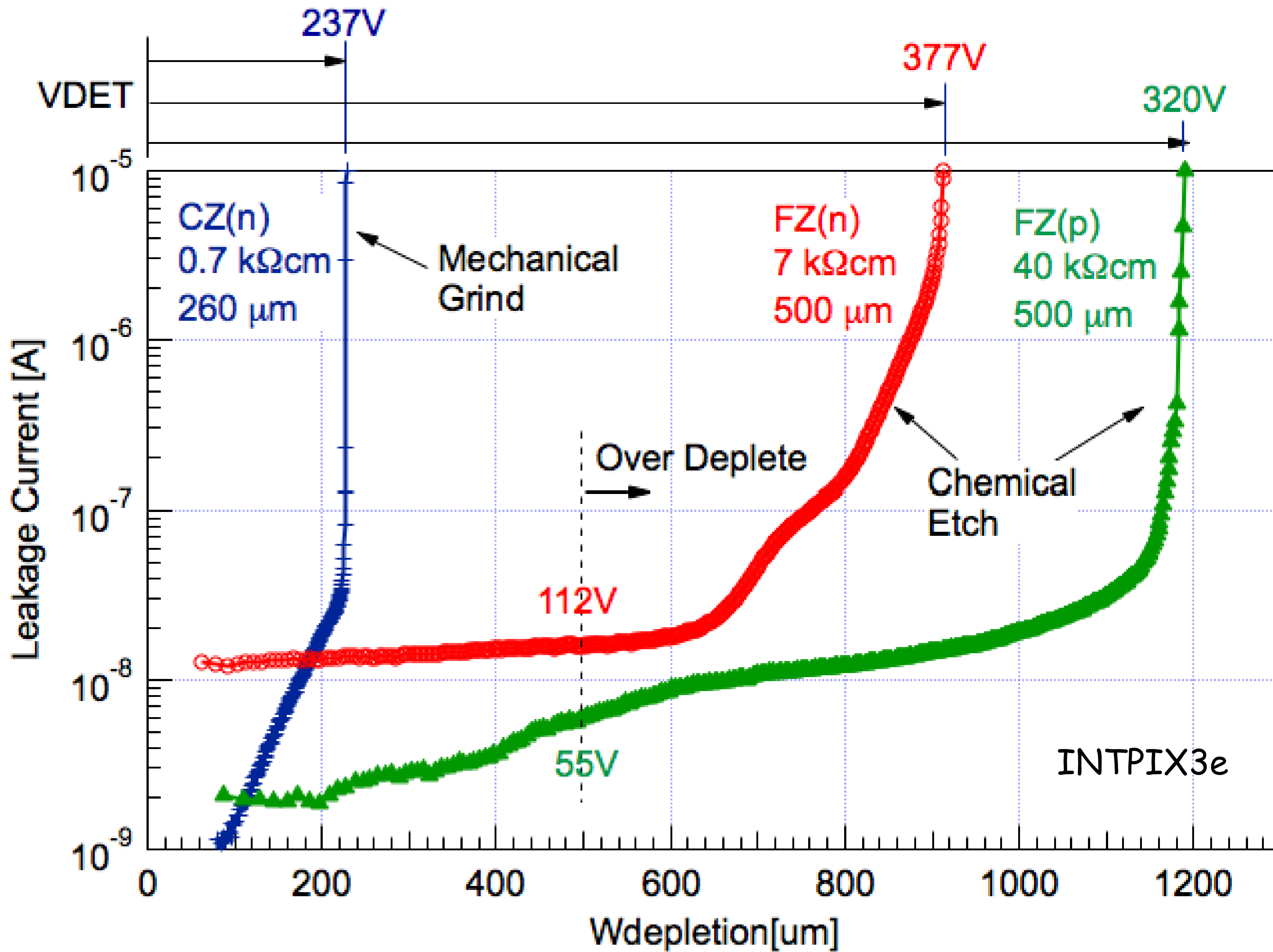
FZ(p and n) SOI Wafer

It was difficult to process 8” FZ-SOI wafer in CMOS process.

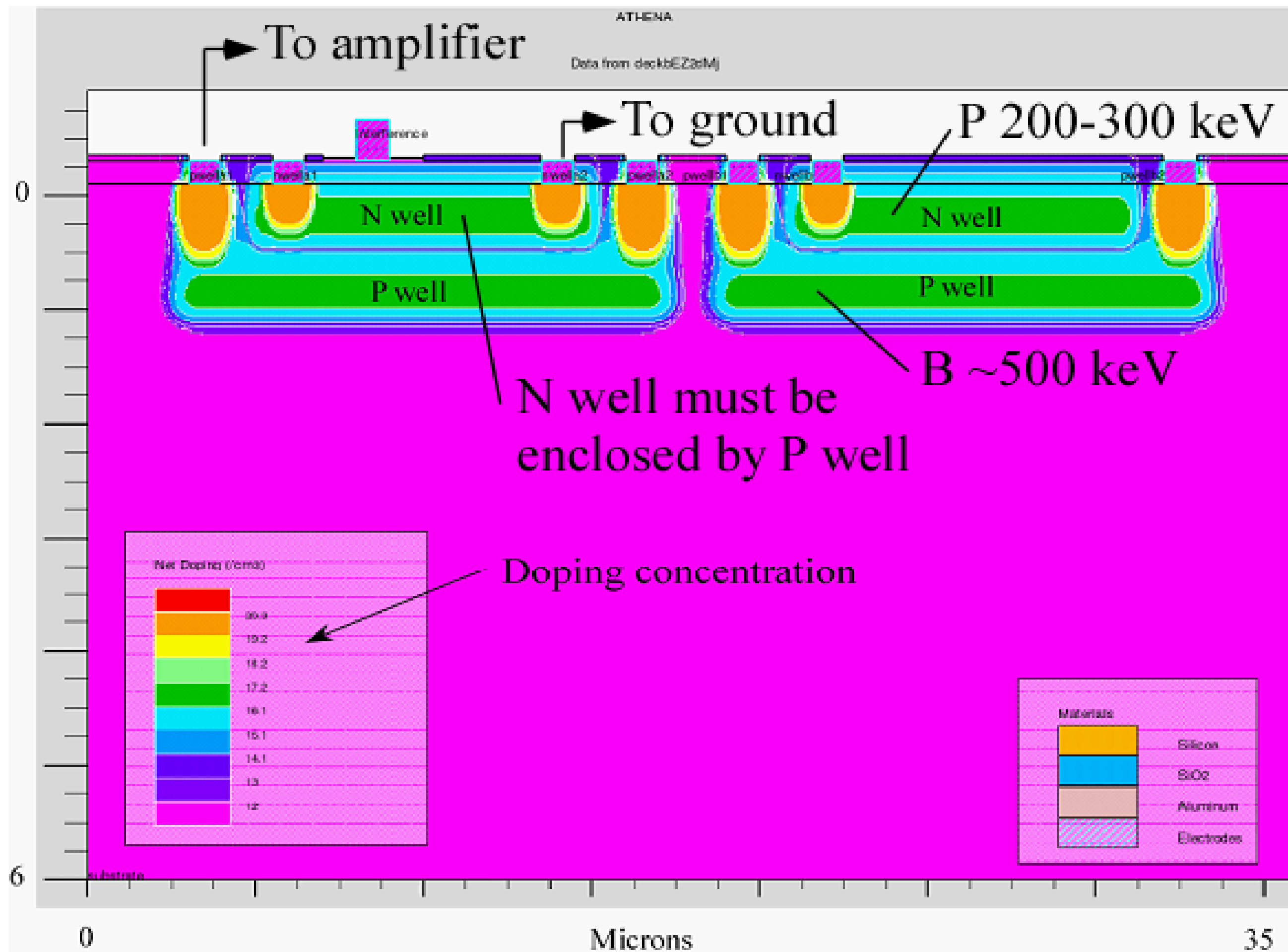


We optimized the process parameters, and succeeded to perform the process without creating many slips.

Wafer type and Leakage Current

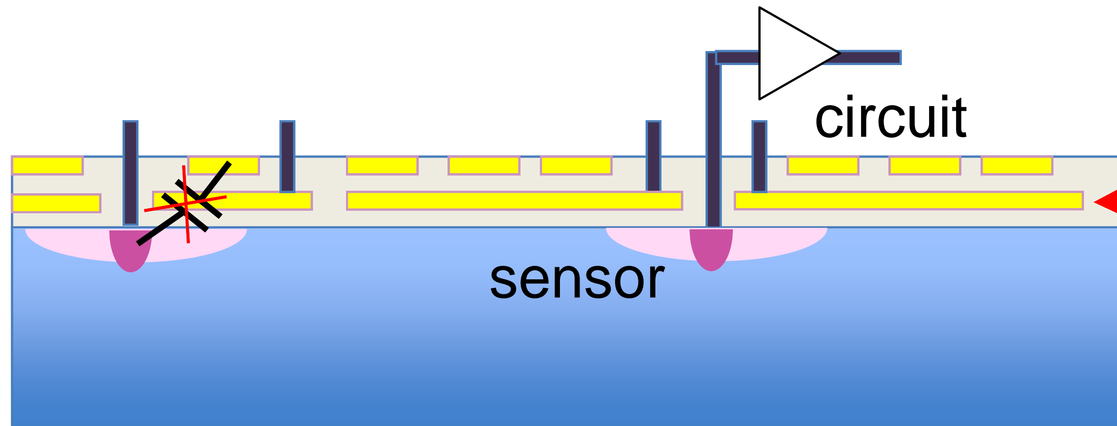


Nested BNW/BPW Structure



- Signal is collected with the deep Buried P-well.
- Back gate and Cross Talk are shielded with the Buried N-well.

Double SOI Layer wafer



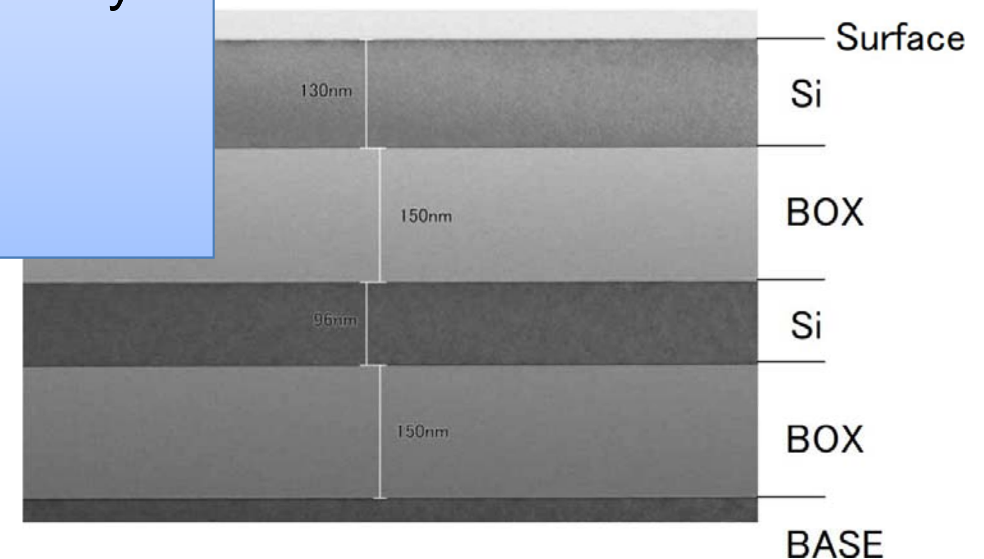
additional conduction layer

Shield sensors from circuit

In addition to the shielding between sensor and electronics,

* oxide trapped hole can be compensated
* able to control Tr threshold voltage block by block
* additional components such as diode, resistors can be implemented.

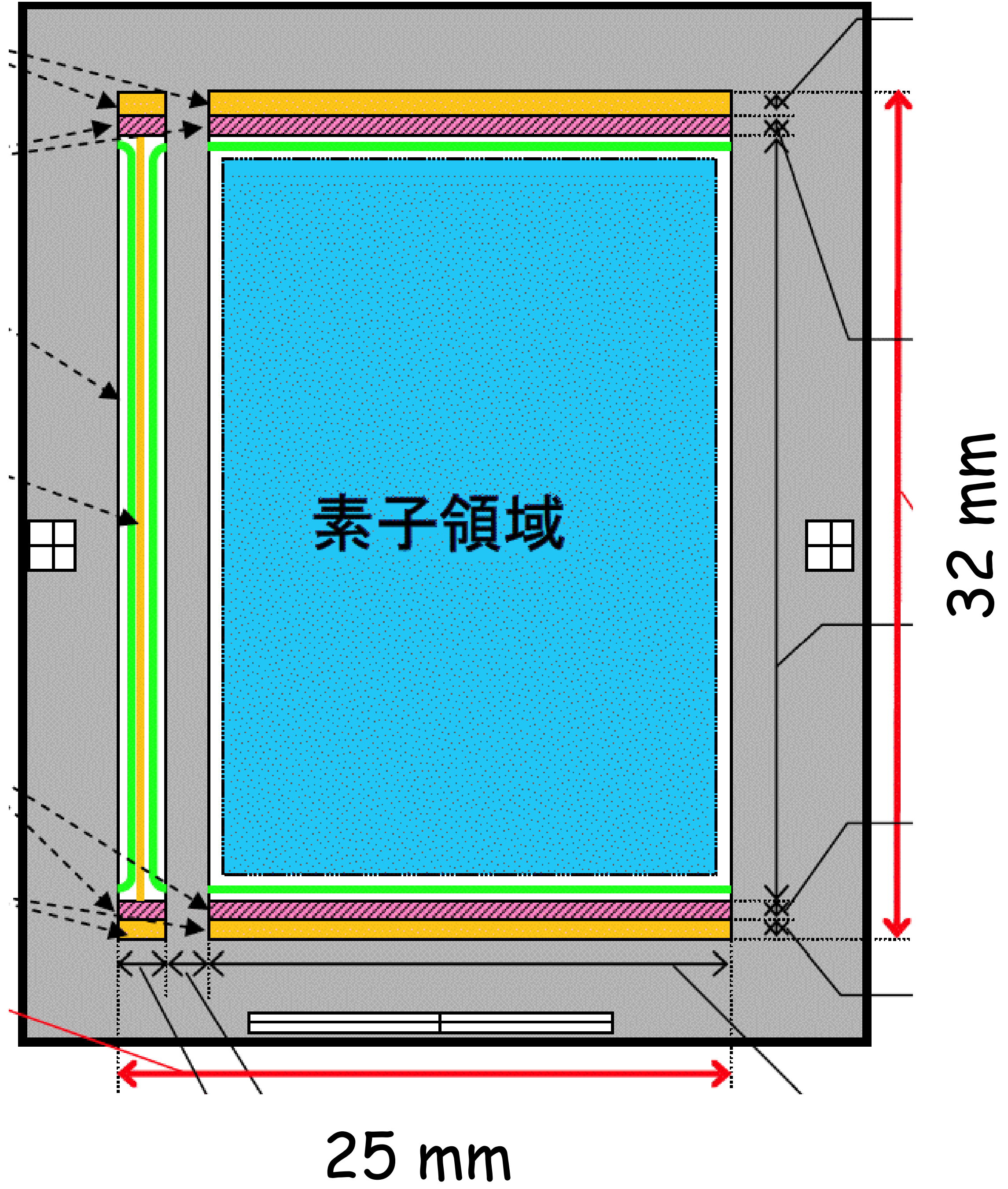
Wafer is ready.
Process study is in progress.



Larger Mask

Present Mask

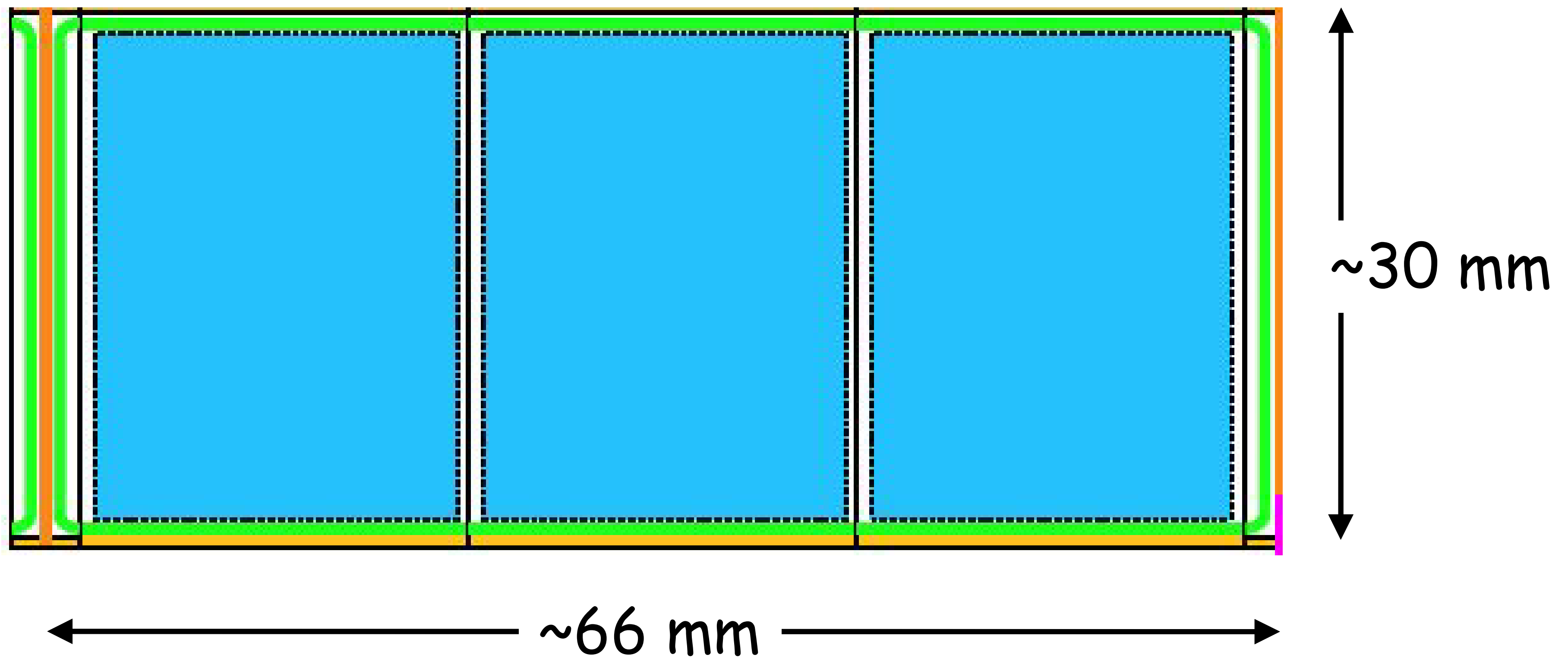
20.8 mm
x
20.8 mm



Larger mask will be used from next MPW run.
→ Larger Sensor & Reduced cost per area.

Stitching

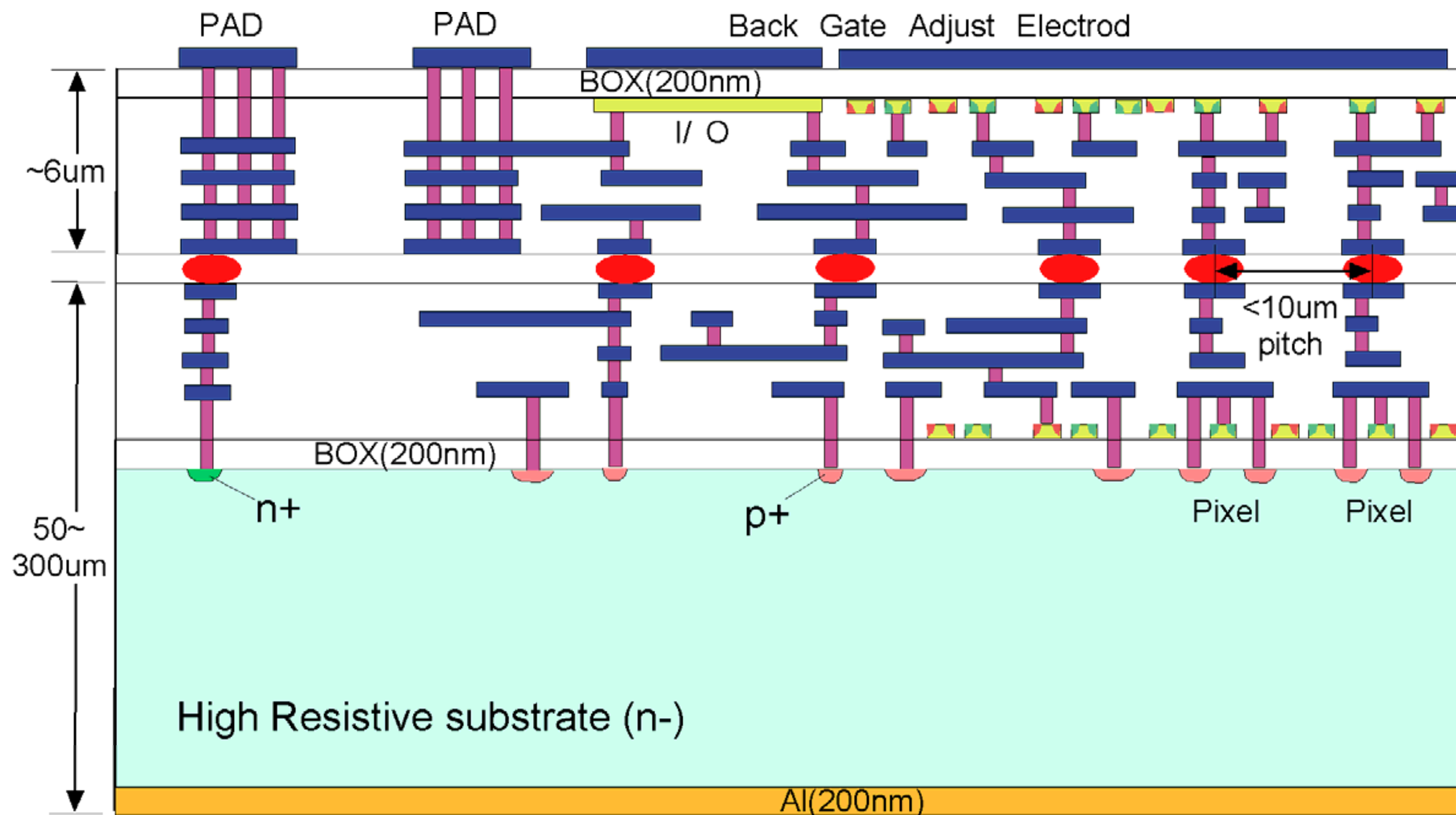
Stitching test is in preparation.



Vertical (3D) Integration

T-micro + OKI Semi
+ KEK/LBNL/Fermilab

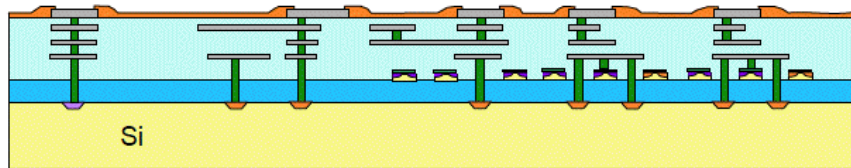
We have submitted 3D test chips on Feb. 2009 and Feb. 2010 to the SOI process. These chips are being bonded with μ-bump technology (~5 um pitch) of T-micro Co (ZyCube).
We had a few technical problems and non-technical issues.

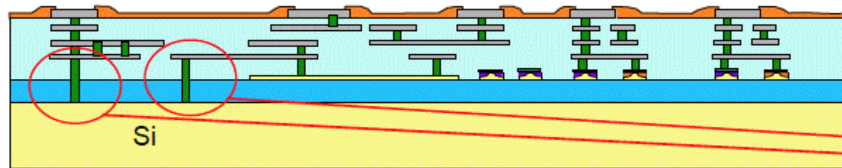


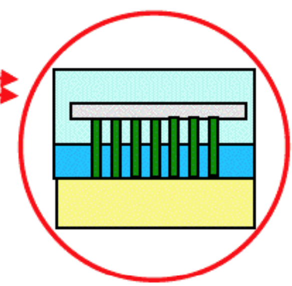
(1) Stack Process Flow (after finishing wafer process)

Lower Chip

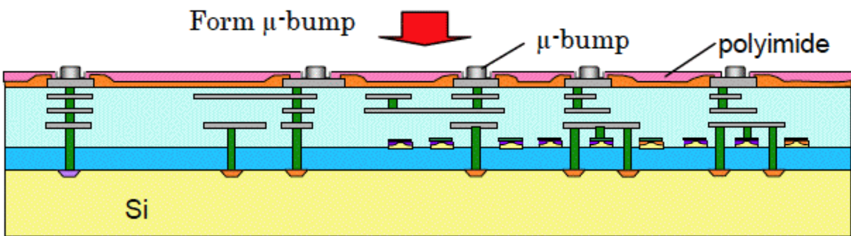
Upper Chip
(Layout must be done with mirror inverted)



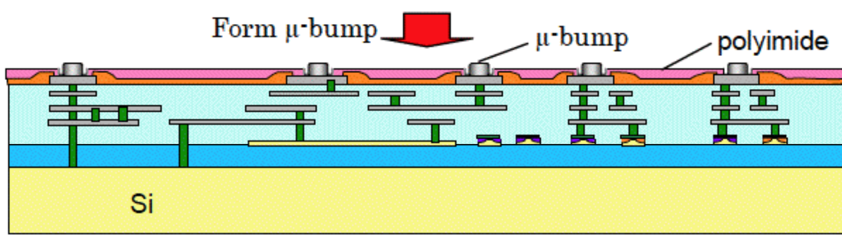




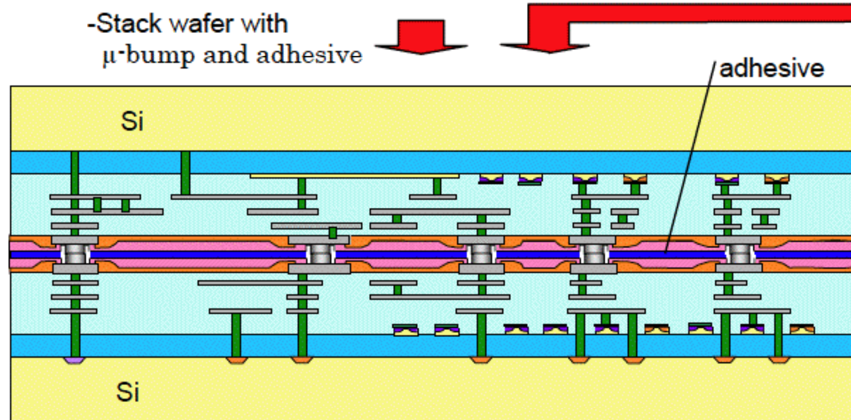
Form µ-bump



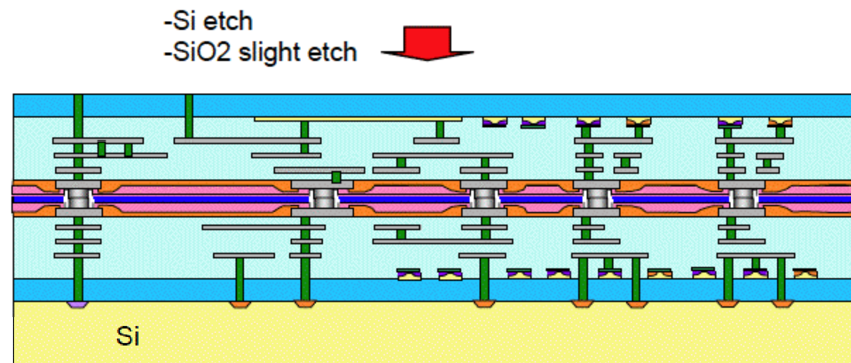
Form µ-bump



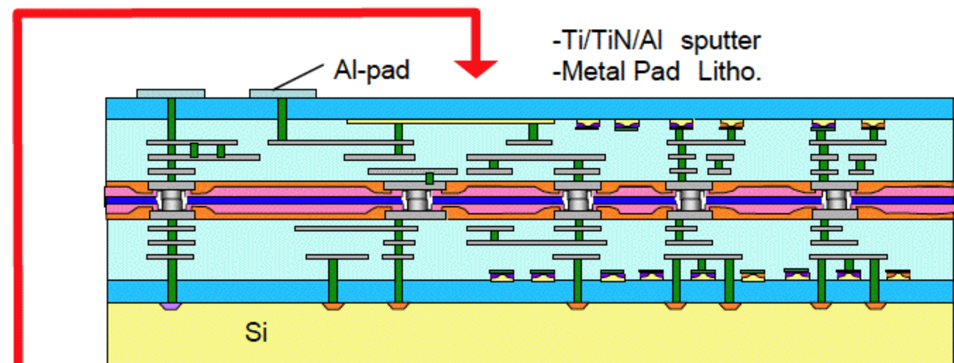
-Stack wafer with
µ-bump and adhesive



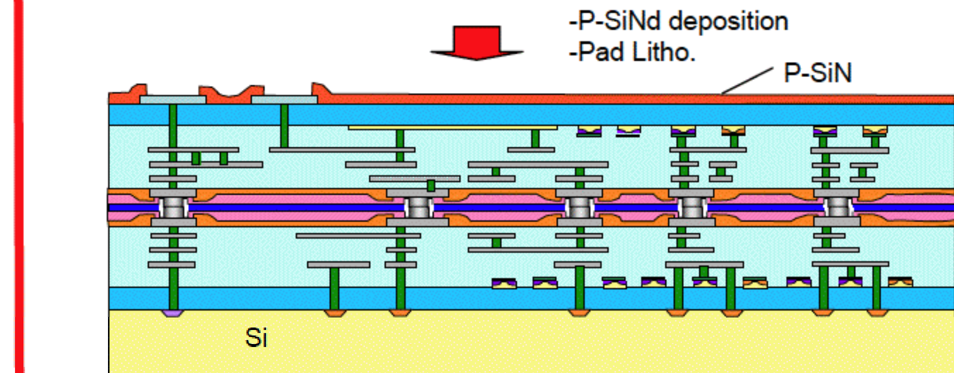
-Si etch
-SiO2 slight etch



-Ti/TiN/Al sputter
-Metal Pad Litho.

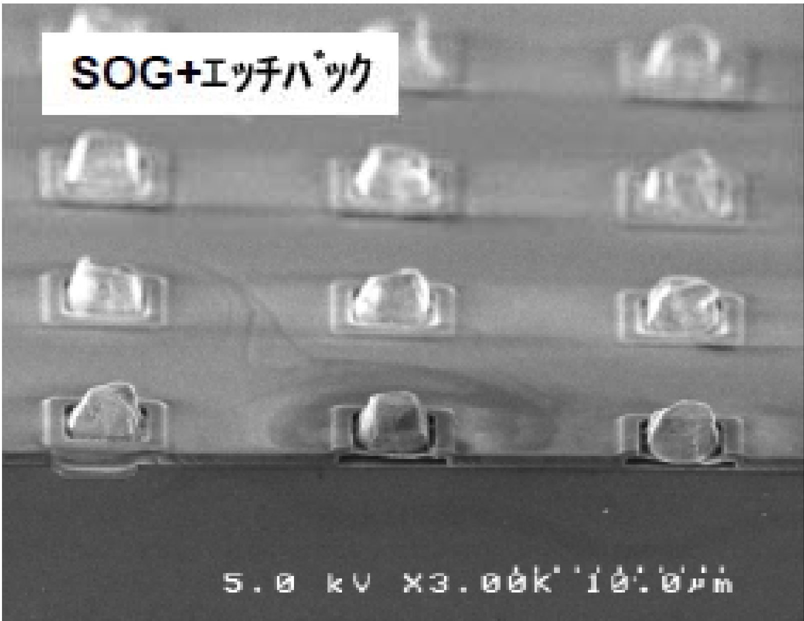


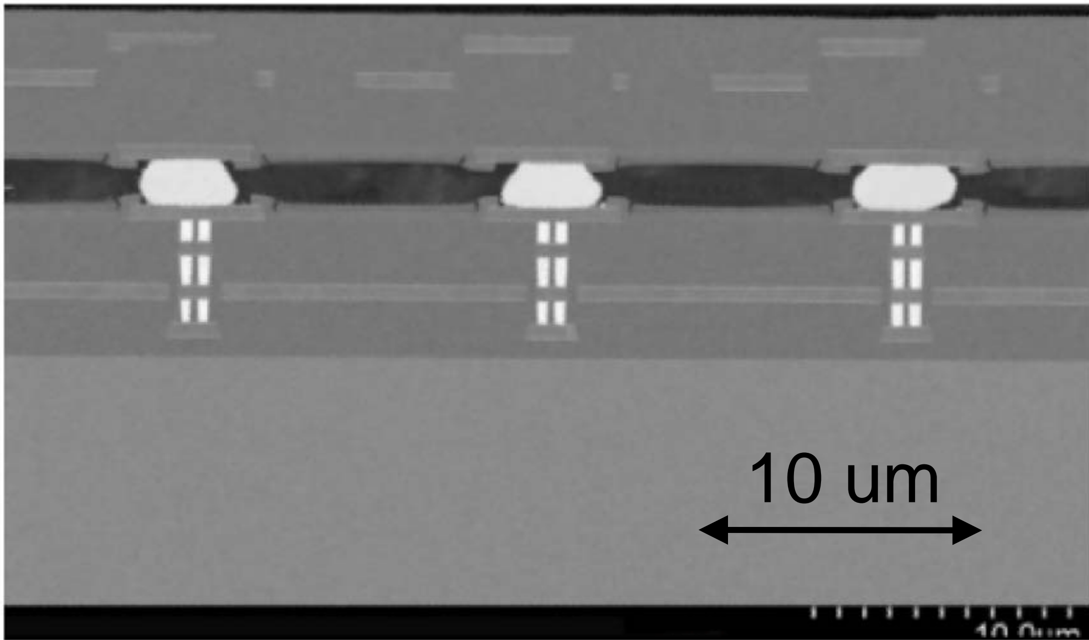
-P-SiNd deposition
-Pad Litho.

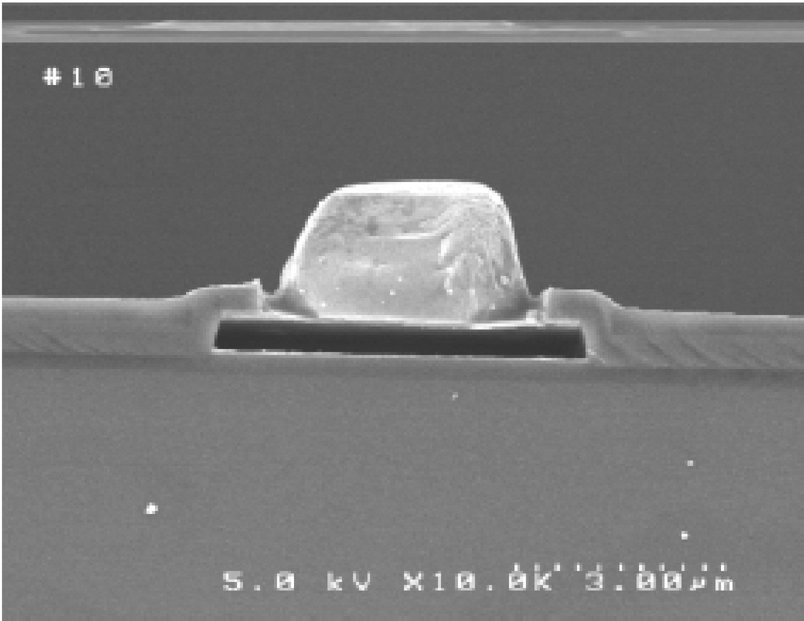


T-Micro

μ-bumps fabrication







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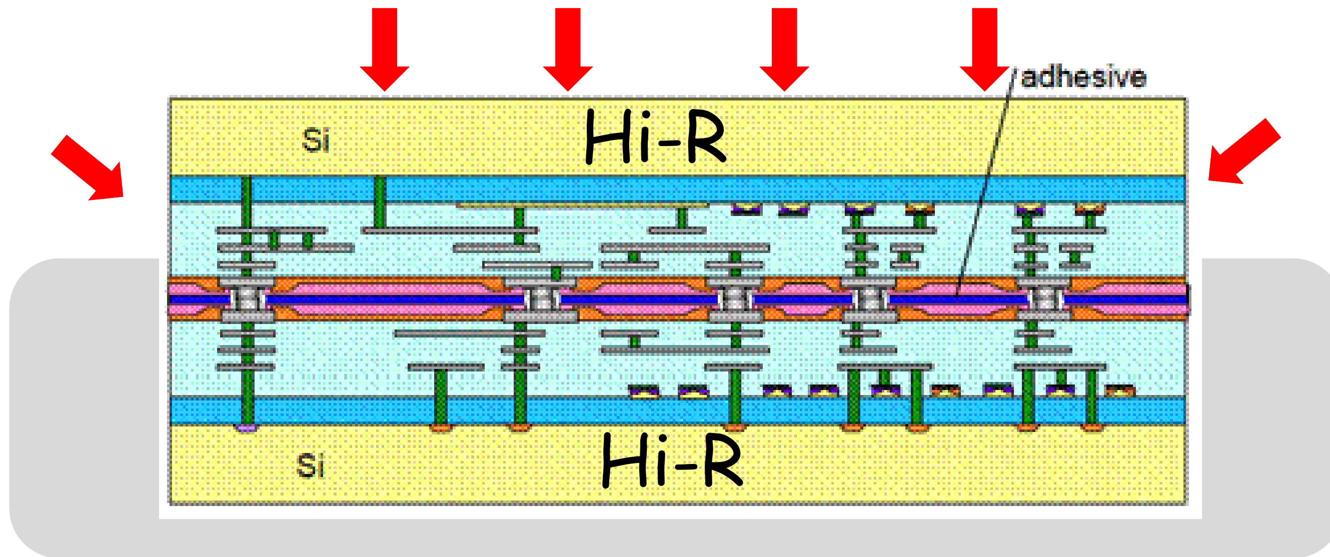
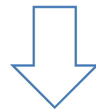
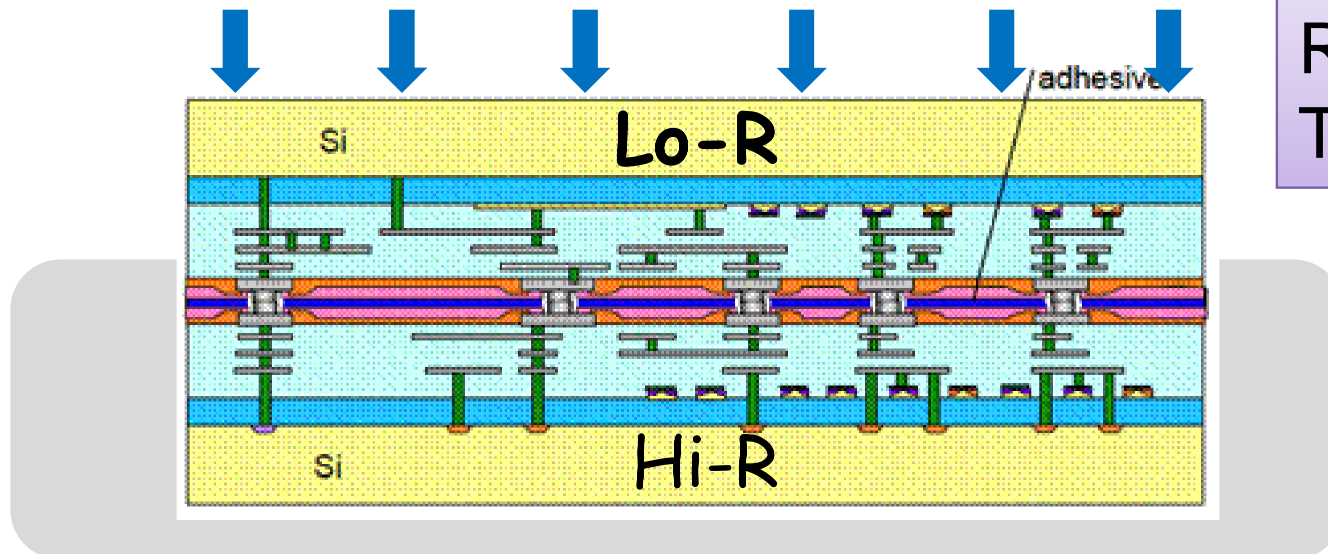
Difficult to Etching

Also Etched from side

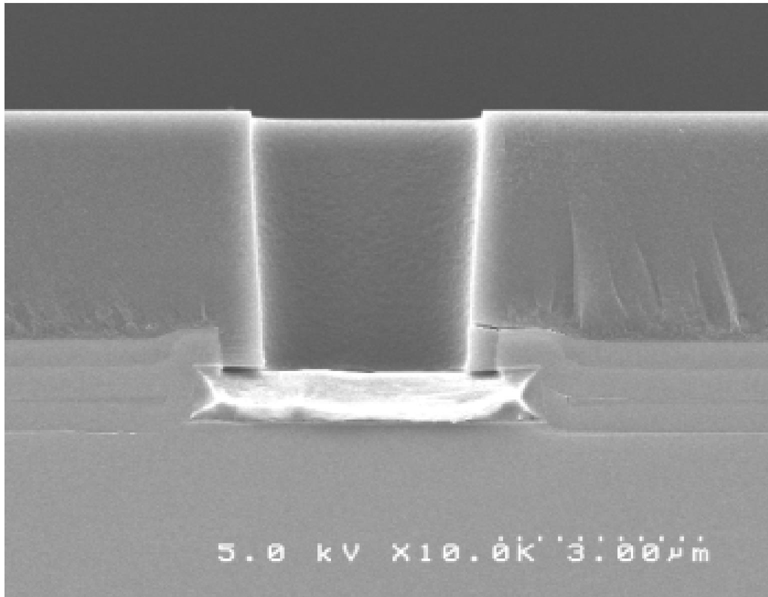




Easy to Etching

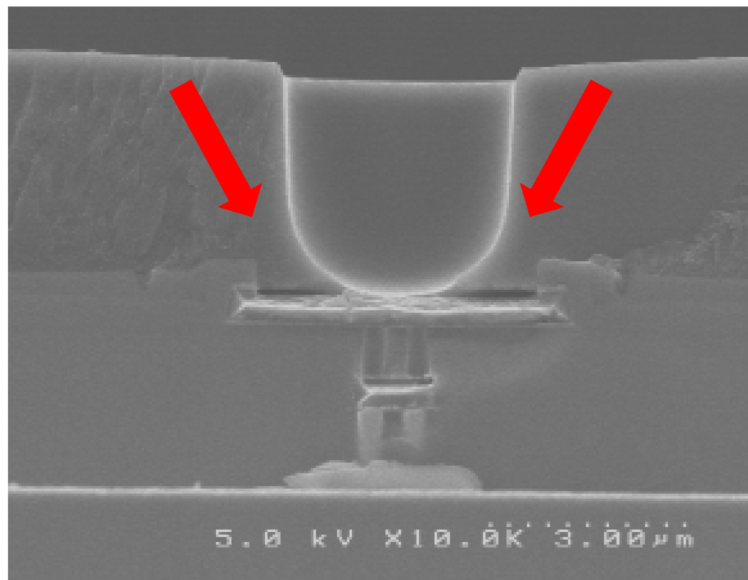


Change Low Resistive Wafer for Top Chip



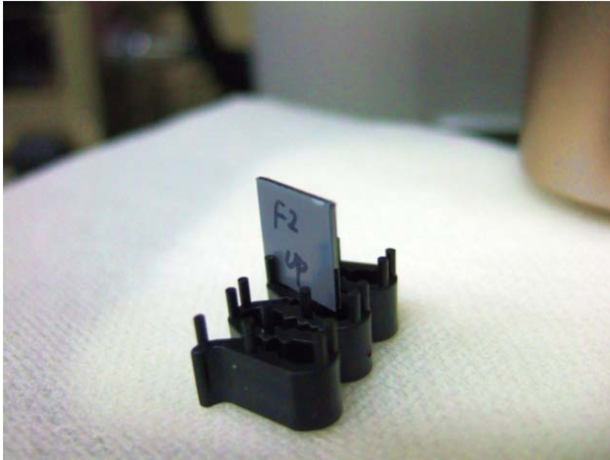
We observed Resist is melting into the μ-bump hole after back grinding.

Back Grinding

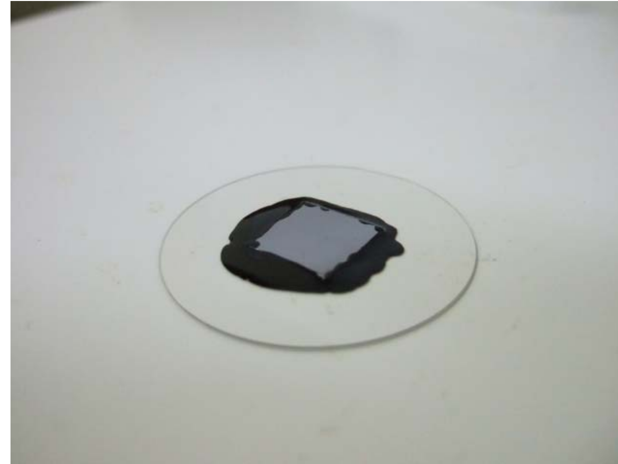


We changed the order, so the back side is grinded before the μ-bump hole formation.

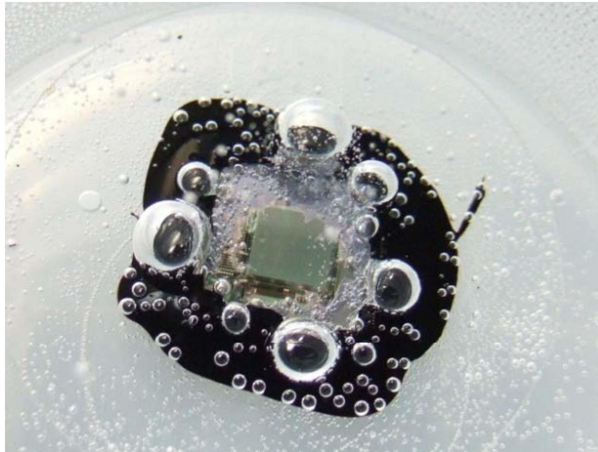
T-Micro



Before adhesive injection


Before Si etching

Si etching


Si etching

After Si etching

Now Back side Al plating is being done

4. Summary

- SOI technology has many good features; low power, large range of operating temperature, low single event effect, vertical integration, ...
- SOI Pixel process becomes more stable and practical to use. Most of the technical problems are solved.
- We have ~twice/year regular MPW runs with increasing no. of users (Next MPW run is Oct. 3rd).
- Many pixel sensors are working and showing good performance.
- The process is still progressing; Higher resistivity, Nested well structure, Double SOI, Larger mask size, Stitching, …
- We welcome new users to the SOI pixel process.