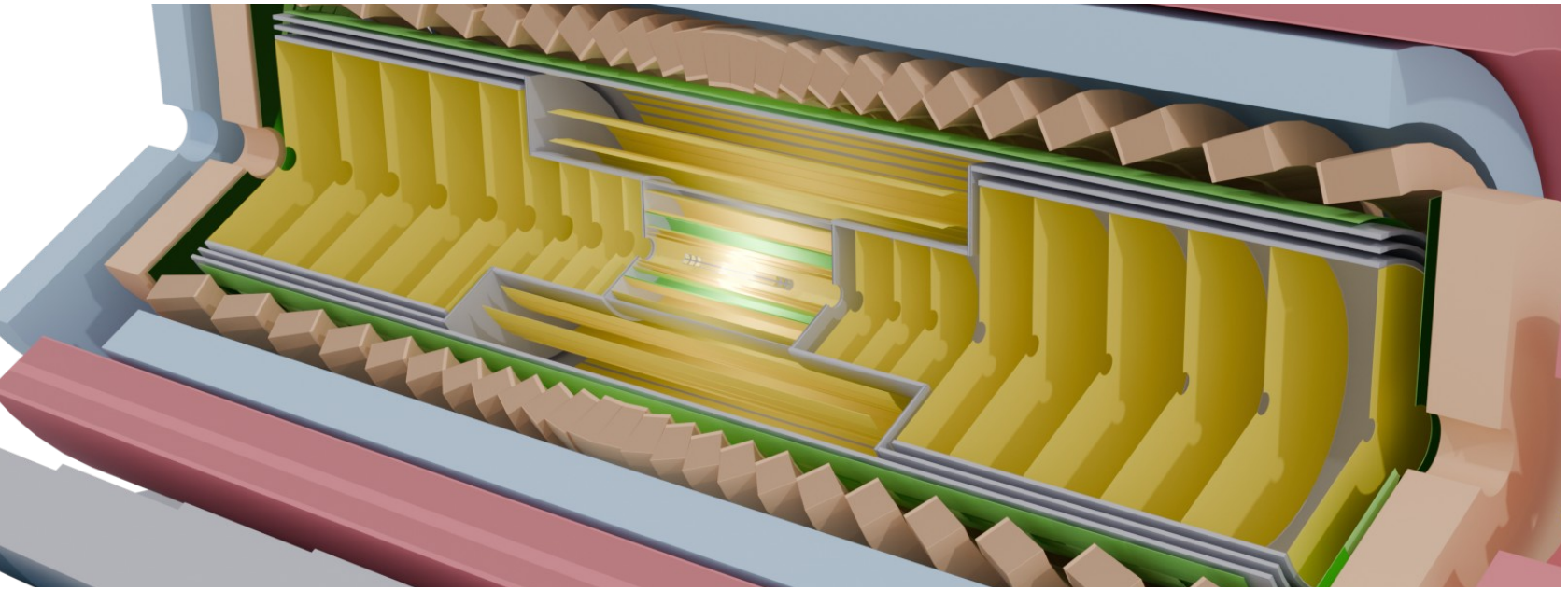
Antonin MAIRE

Wednesday, 09 Oct. 2024 – **ALICE Upgrade Week 2024-10**

https://indico.cern.ch/event/1415726/

Sensor developments for Outer Tracker



DOI:10.5281/zenodo.13894032

Presentation, thanks to Jérôme Baudot, Andrei Dorokhov, Jean Soudier, Frédéric Morel

Outline

A. Analog part, charge collection (pixel grouping)

B. Numeric part, readout (asynchronous strategy)

C. Prospects and project organisation

Based essentially on A. Dorokhov presentation IT/OT/FCT meeting 29 Aug
https://indico.cern.ch/event/1449476/

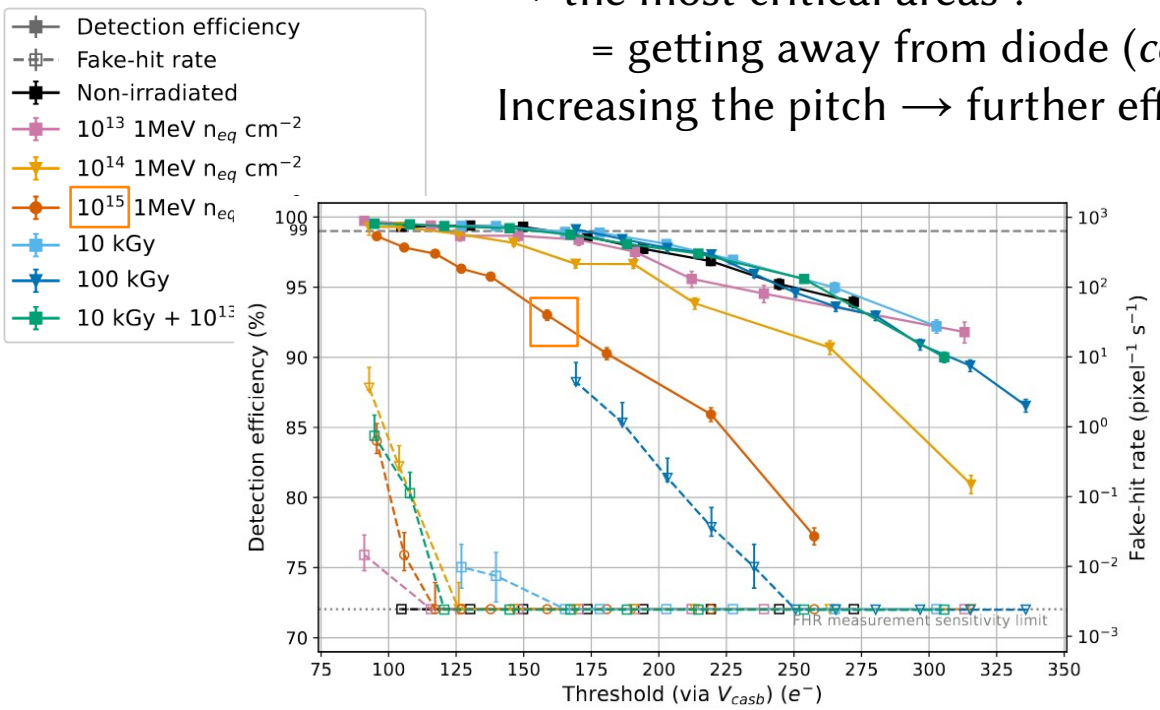
ALICE3 LoI, arXiv:2211.02491
ALICE3 Scoping Document Draft:10248 (LHCC)

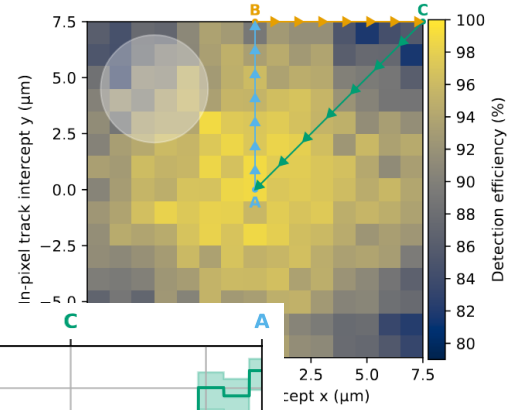
I.1 – Charge collection : a 65nm apparent paradox

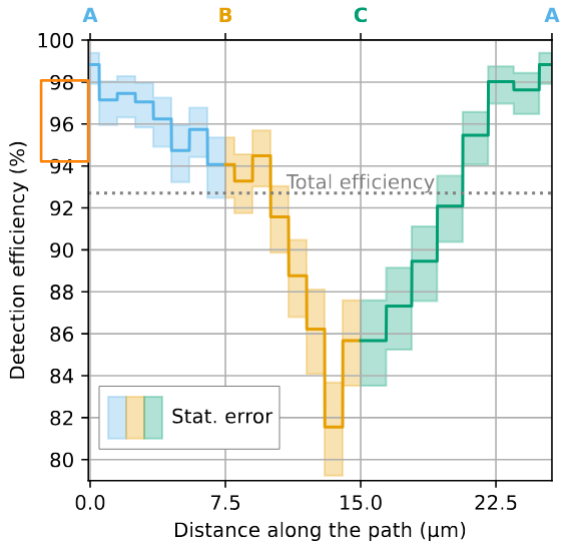
OT spatial resolution ≈ 10 µm
⟶ Spontaneously, calls for a pixel pitch $O[10x\sqrt{12} = 35\ \mu m]$

ITS3 MOSAIX pitch ≈ 22 µm
But : moving to larger pitch (from 22 µm to 35 µm) is <u>not</u> something obvious and easier, in TPSco 65 nm
(uneasiness, to be "confirmed" with APTS chiplets in ER2: "large" pitch = 25, 30, 35, 40, ... 50 µm)

Ex: DPTS chiplet, 15-µm pitch: decrease of efficiency *after irradiation*
⟶ the most critical areas ?
= getting away from diode (*corners*)
Increasing the pitch ⟶ further efficiency decrease







DPTS, arXiv:2212.08621, Figs.16+17

I.2 – Charge collection : to circumvent the large-pitch issue

A. Technology workout:
different doping modifications in order to focus electric field, increasing bias, ...

B. Matrix geometry:
honeycomb structures instead of squared ones
(layout becoming not trivial...)

C. Combination of several smaller pixels into a larger one

Options A and B face some limits for improvement:
Likely not enough to achieve reliable collection for the required pitch...

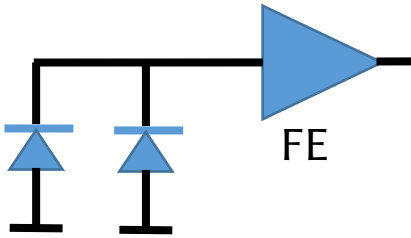
→ explore also option C

I.3 – Charge collection : pixel grouping

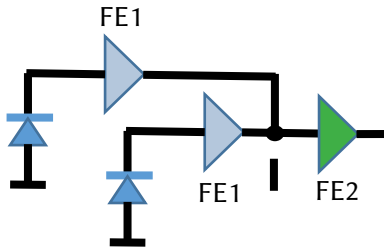
Where to group in the matrix ?

- in digital part ?
  i.e. few small pixels with their *individual* Front-End (FE) circuits, but digitally read as *one*
  → save some bandwidth
  Pb: analogue FE consumption ≠ changed, no hope of power saving thanks to grouping

- in analogue part ?
  ~~A.~~ "Naïvely" connect together several charge collecting nodes:
  power density reduced by number of connected nodes ($1/n$, *i.e.* $\approx ½$ in practice)
  Pb: Signal/Noise quick degradation with n, due to input capacitance increase (limited number of nodes ~2),



  B. To reduce S/N degradation, use a 2-stage front-end: FE_1 and FE_2
  → Pre-amplify signals with FE_1 and sum up potentially more nodes ($n=4$),
  the pixel power becomes sum of $[n.FE_1 + FE_2]$,
  so if consumption of FE ≈ $FE_1 + FE_2$,
  we may also gain some fraction of power density: $FE_1 + FE_2/n < FE$



Specific R&D required:
FE circuit ≠ just combination of $FE_1 + FE_2$, both (FE_1 and FE_2) will differ from FE
small prototypes already tested in 180 nm TJ; however, target = 65 nm

II.1 – Readout architectures : synchronous vs. asynchronous

1. Synchronous, based on priority encoder
(ex. ALPIDE, MIMOSIS, MOSS, MOSAIX = ITS2, CBM, ITS3 ...)

- G. Aglieri Rinella, *The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System*
VCI 2016
10.1016/j.nima.2016.05.016

- F. Morel, *The MIMOSIS pixel sensor*,
TIPP2021
Indico.cern.ch:981823

- P. Vicente Leitao *et al.*, *Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade*
TWEPP2022
10.1088/1748-0221/18/01/C01044.

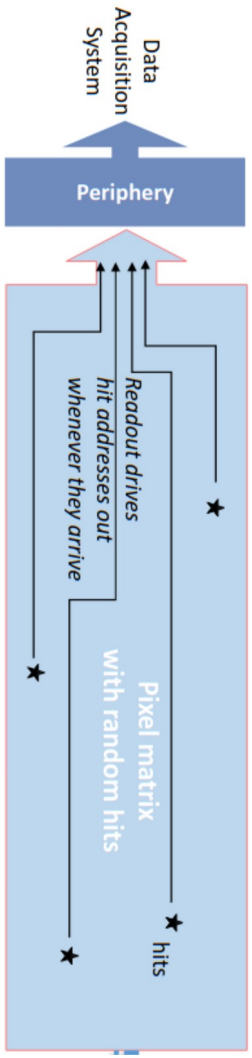
2. Asynchronous, based on Asynchronous Fixed-Priority Tree Arbiter (= SPARC chiplet in ER2)

- W. Uhring *et al*, *Design and Characterization of an Asynchronous Fixed Priority Tree Arbiter for SPAD Array Readout.*
Sensors 2021, 21, 3949.
https://doi.org/10.3390/s21123949

- J. Soudier,
Design of asynchronous ASIC for CMOS pixel sensor readout
18th Trento Workshop on Advanced Silicon Radiation Detectors, 2023
Indico.cern.ch:1223972

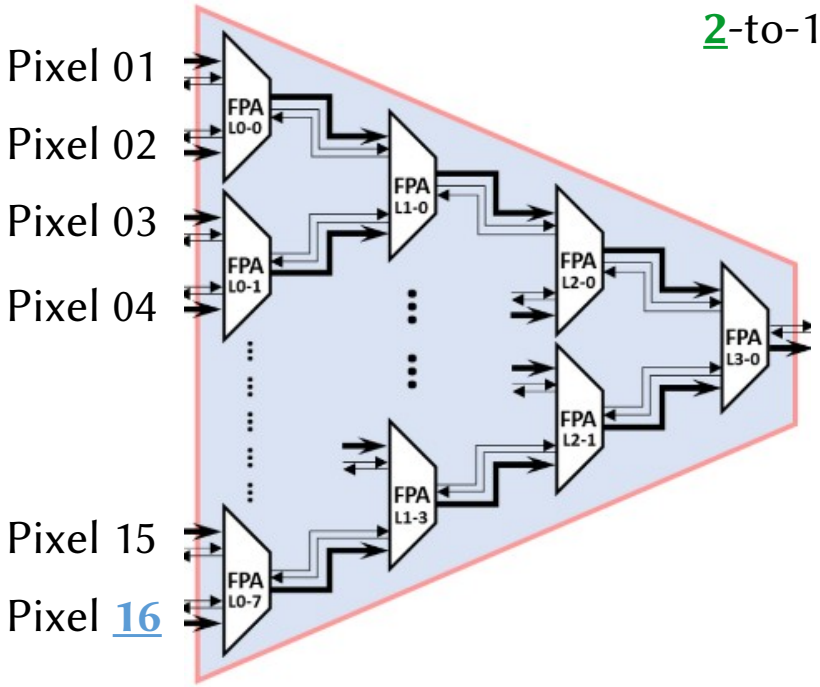
II.2 – Readout arch. : logic principle, cascading of arbiters

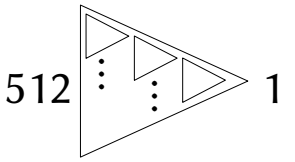
J. Soudier, TREDI23, Indico.cern.ch:1223972



Example 1

4 Levels of
2-to-1 Fixed-Priority Arbiters
(7+4+2+1 = 14 FPA in total)





Example 2

Controller size, Cs = stages of reduction
such that : (Nb of pixels) $^{1/Cs}$ = f, with f reduction factor "f to 1"
Ex : Hyp. : N_{pixels} = 512, Cs = 3, f = 8
→ 1 column of 512 pixels readout by 3 levels of "8-to-1" arbiters,
i.e. [73 = 64 L_0 + 8 L_1 +1 L_2 FPA] to be implemented in the tree

II.3 – Readout arch. : asynchronous readout performances

Results from *post*-layout simulation

Hyp. :
1. single double-column layout, in TPSCo 65nm
2. for various pitches (18-30 µm)
3. for various arbiter size (2:1 to 1024:1)
4. fed with ITS2 simulated hits bank (‹ cluster size › ≈ 4 pixels)
5. hit rate from 1 to 200 MHz/cm^2, assuming 25-ns collision period

Controller	1 MHz/cm²			200 MHz/cm²		
size	mean time	99.9% time	digital power	mean time	99.9% time	digital power
2:1	20 ns	64 ns	3 mW/cm²	22 ns	65 ns	9 mW/cm²
512:1	15 ns	63 ns	1 mW/cm²	17 ns	> 100 ns	5 mW/cm²

Focus on 24-µm pitch results in this table *(NB: no time-walk simulated so far !)*

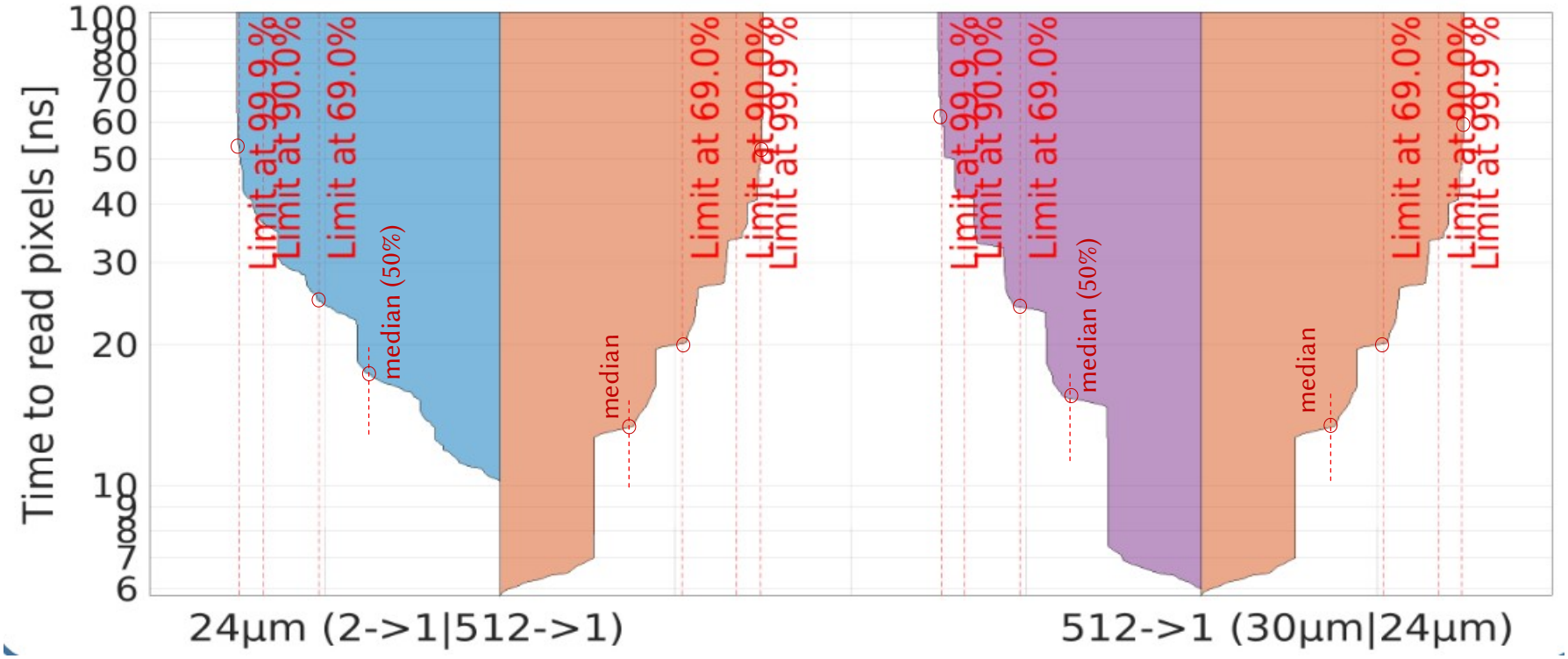
J. Soudier, Pisa2024, poster + NIM-A proceedings

II.3 – Readout arch. : asynchronous readout performances

Readout time performance

Hyp. : Matrix stimulated with random hits (with physical shape), at *100 MHz/cm²*

Beware *no time-walk simulated here !*



J. Soudier, Pisa2024, poster + NIM-A proceedings

II.4 – Readout arch. : asynchronous readout proposal for OT

OT requirements

- Wide range of hit rate 0.1-200 MHz/cm²
(Exceeds ML/OL needs but match generic R&D)

- Compatible with σ_t = 25-100 ns
for timestamping

- Fits within expected pixel pitch 25-50 µm

- Adds only few mW/cm²

- Design matching digital flow

- To be implemented in TPSCo 65 nm

Asynchronous FPA features :

Readout speed:
- Mean time per pixel around 20 ns at 100 MHz/cm²
- 99,9% of pixels read within 100ns
- Rates close to 5.10^9 particles/cm²/s, accessible

Power consumption associated to readout:
- still below 10 mW/cm² for 200 MHz/cm²
- consumption ≈ simply linear per hit
(asynchronous behaviour :
lower hit rate ↔ lower power)

Time stamping:
- Possibility to timestamp hit down to 2 ns,
assuming:
  - Fast clock only at periphery
  (no clock distribution over the matrix)
  - Time-walk correction

J. Soudier, Pisa2024, poster + NIM-A proceedings

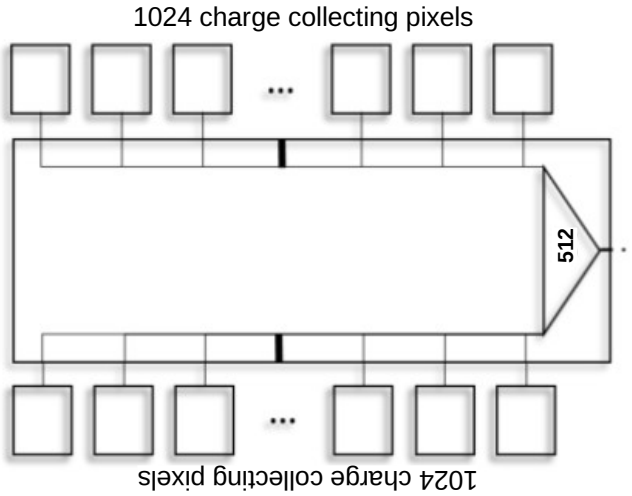
III.1 – Proposal for OT : implementation of async. readout

A. **Demonstrator** = SPARC chiplet
(IPHC Strasbourg + IRFU Saclay)

Chiplet planned for TPSCo 65nm in ER2 (early 2025)
pixel FE : reuse of MOSAIX (provided by ITS3/CERN)
Pixel size: 24.1x16.0 µm²
4 arbiter-size variants: • 2:1 (bandwidth optimised), • 4:1, • 16:1, • 64:1 (≈ less area consumed)

B. Proposal for **OT sensor** = this asynchronous FPA as in-matrix readout

Hypotheses:
- double-column readout strategy
- time stamping, at the end of column only (periphery)
- Sensor size [row = 3.2 cm] x [column =2.5 cm] (≈ reticle size)
  - → 2 column x1024 charge collection pixels of 24-µm pitch
    i.e. 2048-pixel blocks
  - → 1360 columns = 680 double-columns to cover ~32 mm
    (full sensor width)
- with grouping of 4 pixels at the Front-End
  i.e. 2048/4 = 512 individual 4-pixel domains to be red out
- Single arbiter, arbiter-size 512:1
  (alternative : possible cascade *N*:1 with *N*≠512, still for double-column readout)



III.2 – Proposal for OT : loop on power, back of the enveloppe

Jérôme Baudot

Hypothesis : 680 double-columns and 2048 pixels per double-column

- Front-end (analogue + mixed):
  - Without grouping : assumption of 100 nA/pixel ⟶ 22 mW/cm²
    (*NB*: 100 nA is conservative assumption / time walk)
  - With grouping: benefit depends on power balance between FE_1 & FE_2
    If 50/50 ⟶ 14 mW/cm²
    If 80/20 ⟶ 19 mW/cm²

- Read-out:
  1 to 5 mW/cm², depending on hit-rate (1 MHz/cm² [ML+OT-like] ... to 100 MHz/cm² [VD-like])

Conclusion

Range **15 to 25 mW/cm²** seems reachable, driven by Front-end design

Note : these numbers are incomplete, = only for the matrix!

⟶ No (DAC, digital logic, output drivers, ...) in there

Hopefully, still enough to stay within the specifications (≤ 20-40 mW/cm²)

III.3 – Proposal for OT : sensor ingredients missing

Periphery / End of column will further need :

- Arbiter between columns
- Serializer to output (with trigger logic?)
- Smart daisy-chaining between sensors
- DAC, analogue biasing, slow control

Side constraint :
care to minimize non-sensitive area (O[1 mm] width for the periphery)

⟶ To be further discussed (synergies, common conventions with VD...)
⟶ Extra contributions needed to complete the picture

IV.1 – OT sensor project : organisation

- *Pillar 1 :* **Front-end**

  Basis : 180nm experience on staged Front-End
  IPHC: Andrei Dorokhov + part of another designer

  Already under discussion within ALICE : Germany (Heidelberg, ...)

- *Pillar 2 :* **Matrix read-out**

  Basis: SPARC chiplet on asynchronous readout
  IPHC: new Master student arriving in 2025 + part of 65nm digital team

  under discussion within ALICE: Germany

  Interest from other French groups under discussion (DRD3/DRD7 / + non-ALICE3 members)

- *Pillar 3 to N :* **To be planned...**

  - Overall steering of the project
  - Design of other components of the sensor : powering, control, periphery & integration...

IV.2 – OT sensor project: HR context, (ALICE$_3$ on a HEP map)

- EIC / EPIC tracker
- ALICE2 ITS3
- ALICE3 **Vertex Detector**
  - ALICE3 Middle Layers (if stitched and bent)
  - **ALICE3 Middle Layers** (default opt°)
- **ALICE3 Outer Tracker**

- FCCe$^+$e$^-$ **Vertexer**
- FCCe$^+$e$^-$ tracker ?

indico.cern.ch/category/5225/
See 2024-07 wkshop FCCee vtxer
indico.cern.ch:1417976

- Belle II **tracking** upgrades

?

- LHCb Mighty Tracker
- LHCb **Upstr. Tracker**

ECFA European Committee for Future Accelerators
ecfa.web.cern.ch
⟶ ECFA Roadmap = FCCee, a strong priority
…

⟶ ECFA Detector Panel
DRD Panels, Detector R&D
indico.cern.ch/category/6805

- DRD1 Development of Gaseous Detectors
- DRD2 Liquid Detectors
- DRD3 Solid State Detectors — **DRD3.1** = MAPS
- DRD4 Photon Detectors and Particle ID
- DRD5 Quantum and Emerging Technologies
- DRD6 Calorimetry
- DRD7 Electronic Systems — **DRD7.6a** = *access to technologies*

DRD3 *Collaboration* week (17-21 June 24)
117 contributions
indico.cern.ch:1402825

IV.3 – OT sensor project : 1st submission of OT prototype, 2026

OT sensor prototype :

Baseline proposal ≈**25-µm** pitch with **binary** pixel (few versions of FE with/wo **grouping**)
+ **asynchronous** read-out, *O*[**100 ns**] time binning

- 1st alternative:
  baseline with some digitisation of pixel output (ToT) ?
  & aggressive timing (time-walk correction)
- 2nd alternative :
  baseline front-end with different read-out architectures (synchronous **vs** asynch.) ?
- incl. several splits ⟶ **modified process** to optimise tolerance to NIEL fluence

Possible size for prototype:
For pitch ≈ 24 µm and one full functional region (for demonstrator only)
≈ 128 columns (*i.e.* enough columns) x 1024 rows (*i.e. already final* column length) ~ **0.3 x 2.4 cm²**

Consider designing full reticule-size sensor for simulation purpose :
Even if 1 sub-region only will be actually submitted ⟶ anticipation to full size with simulations,
allows for early corrections of possible issues in final sensor
(e.g. matrix power-grid, blocs in periphery, ...)

Appendix

II.2 – Readout arch. : performance comparison for 512 pixels

Firing every 512 pixel in 1 column to evaluate bandwidth, as function of controller size

Controller size, Cs = stages of reduction such that : $512^{1/Cs} = f$, with f reduction factor "f to 1"
Ex : $Cs = 3$, $f = 8 \longrightarrow$ 3 levels of "8 to 1"