# Time of flight sensors R&D

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# The framework

| | Inner TOF | Outer TOF | Forward TOF |
|---|---|---|---|
| Radius (m) | 0.19 | 0.85 | 0.15–1.5 |
| $z$ range (m) | −0.62–0.62 | −2.79–2.79 | 4.05 |
| Surface ($m^2$) | 1.5 | 30 | 14 |
| Granularity ($mm^2$) | $1 \times 1$ | $5 \times 5$ | $1 \times 1$ to $5 \times 5$ |
| Hit rate ($kHz/cm^2$) | 74 | 4 | 122 |
| NIEL (1 MeV $n_{eq}/cm^2$) / month | $1.3 \times 10^{11}$ | $6.2 \times 10^9$ | $2.1 \times 10^{11}$ |
| TID (rad) / month | $4 \times 10^3$ | $2 \times 10^2$ | $6.6 \times 10^3$ |
| Material budget ($\%X_0$) | 1–3 | 1–3 | 1–3 |
| Power density ($mW/cm^2$) | 50 | 50 | 50 |
| Time resolution (ps) | 20 | 20 | 20 |

**Table 11:** TOF specifications.

- **Low Gain Avalanche Diodes (LGADs) readout by dedicated front-end chips have become a workhorse for high resolution silicon timing detectors for charged particles**
- **Typical resolution is 50 ps and can be improved with thinner sensors.**
- **ALICE3 TOF combines large area, coarse pixel sizes and moderate event rate: perfect case for monolithic CMOS sensors with gain…which are not yet "off the shelf"!**
- **Approach:**
  - **Study the timing performance of conventional LGADs with reduced active thickness**
  - **Develop CMOS sensors with internal gain**

# Thinned LGAD: some results

Regular Article

Check for updates

## Beam test results of 25 and 35 $\mu$m thick FBK ultra-fast silicon detectors

F. Carnesecchi[1,a] (iD), S. Strazzi[2,b], A. Alici[2], R. Arcidiacono[4,6], G. Borghi[7,9], M. Boscardin[7,9], N. Cartiglia[4],
M. Centis Vignali[7,9], D. Cavazza[3], G. -F. Dalla Betta[8,9], S. Durando[5], M. Ferrero[4], F. Ficorella[7,9], O. Hammad Ali[7,9],
M. Mandurrino[4], A. Margotti[3], L. Menzio[4,5], R. Nania[3], L. Pancheri[8,9], G. Paternoster[7,9], G. Scioli[2], F. Siviero[4],
V. Sola[4,5], M. Tornago[4,5], G. Vignola[2]

|        | Voltage applied | Gain     | Time resolution |
|--------|-----------------|----------|-----------------|
| FBK25  | 120 V           | $57 \pm 4$ | $(25 \pm 3)$ ps |
| FBK35  | 240 V           | $49 \pm 5$ | $(22 \pm 2)$ ps |
| HPK50  | 245 V           | $61 \pm 3$ | $(34 \pm 3)$ ps |

# CMOS LGADs: the approach

- Try to exploit available **opportunities** and optimise **resources**

- Add gain layers and process splits to the already funded **ARCADIA mask-set**

- Optimise sensor performance by changing only relevant parameters (**short loops**)

- Be fully compatible with a (very) standard **CMOS process**

- First iteration

  timing, but
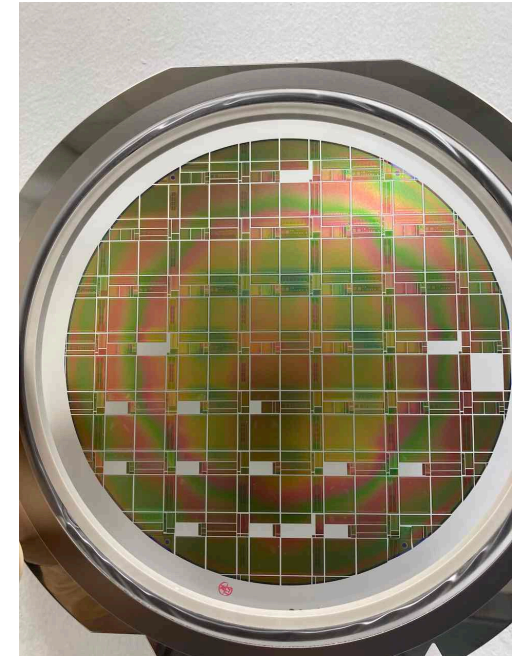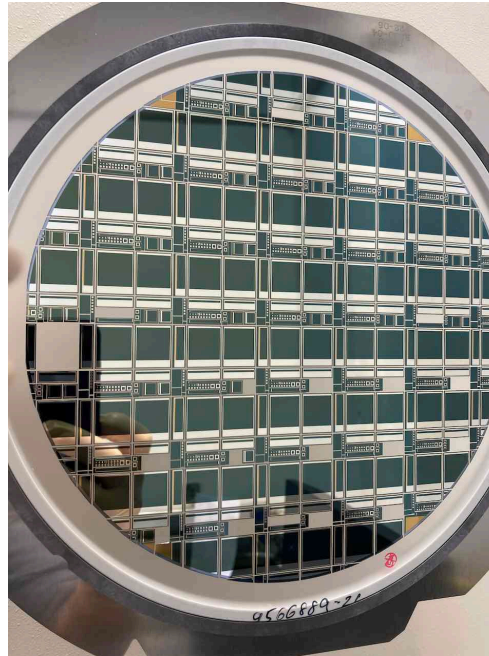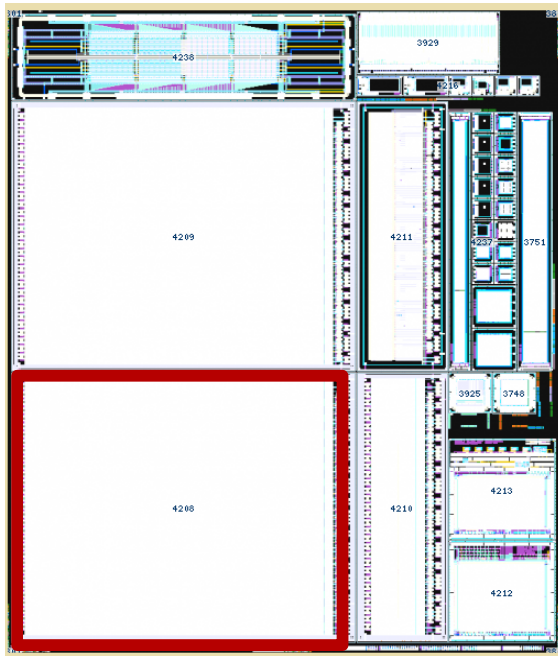
# CMOS LGADs: the concept

- **Addition of a <span style="color:red">simple gain</span> layer and patterned <span style="color:red">termination structures</span>**
- **The deep-pwell separates the pixels and host the front-end electronics**
- **HV on the top: <span style="color:red">AC coupling</span> to the front-end**
- **Both <span style="color:red">active</span> and passive test structures**



ARCADIA pad sensor
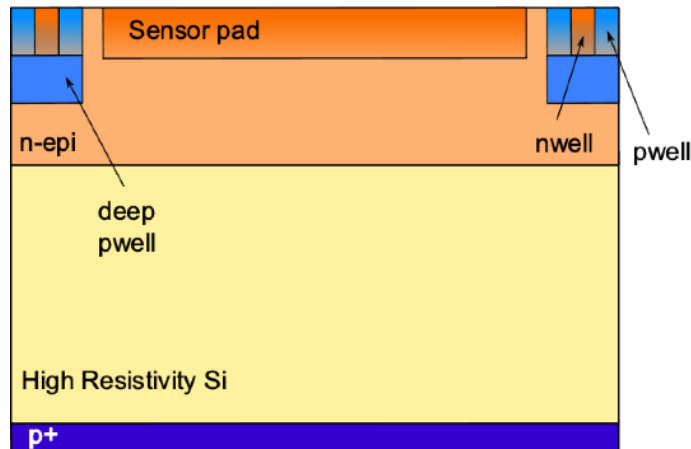
ARCADIA pad sensor with gain

# CMS LGADs: some details
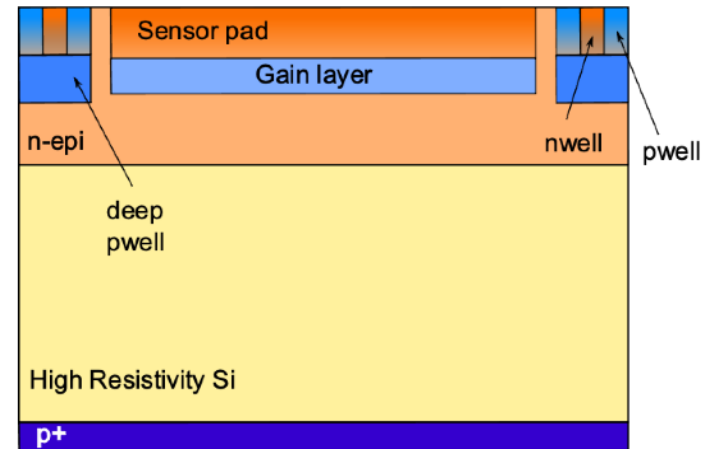
## Test devices: junction termination
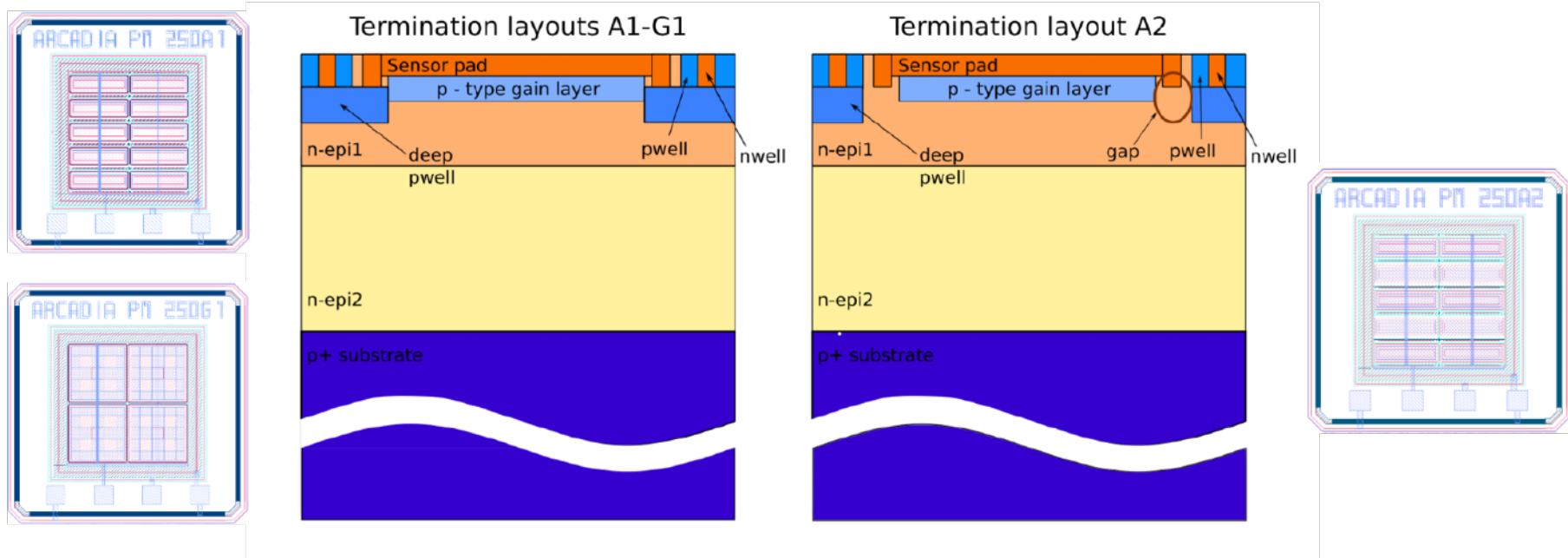


deep pwell below the junction termination: electrons generated below the deep pwell reach the gain layer

Termination directly facing the active region: electrons generated below termination can be collected without gain

# CMOS LGADs: passive test structures

- **Probe station testing**
- **External preamp**
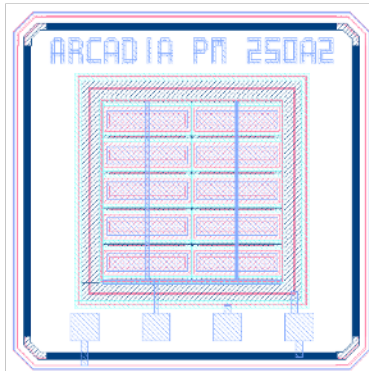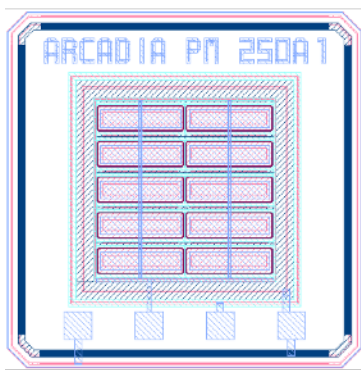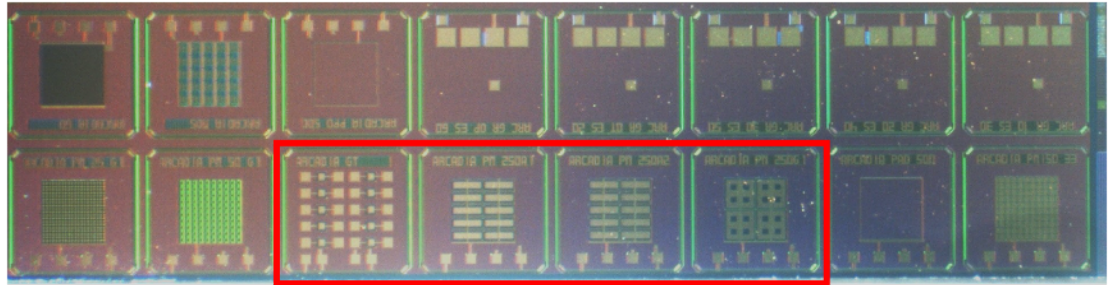




A1 and A2: Rectangular passive pads active area 250μm x 70μm (same geometry as in active pixel array)
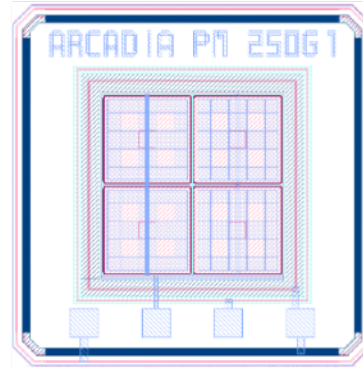
Square passive pads with large fill factor: 250μm x 250μm
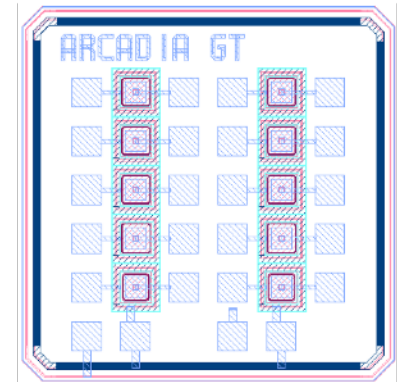
Test pads with variations of Guard Ring geometry

# We have gain!
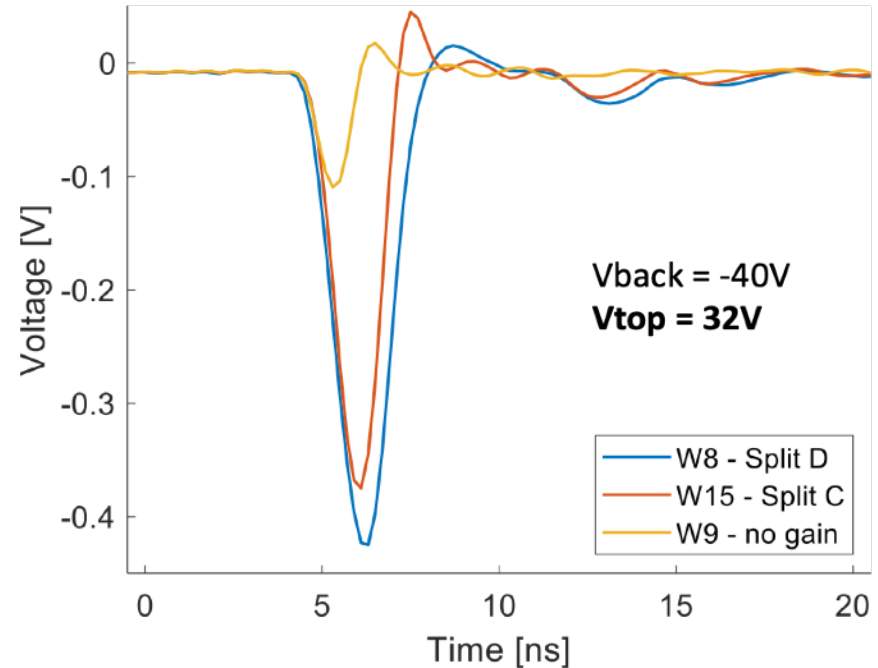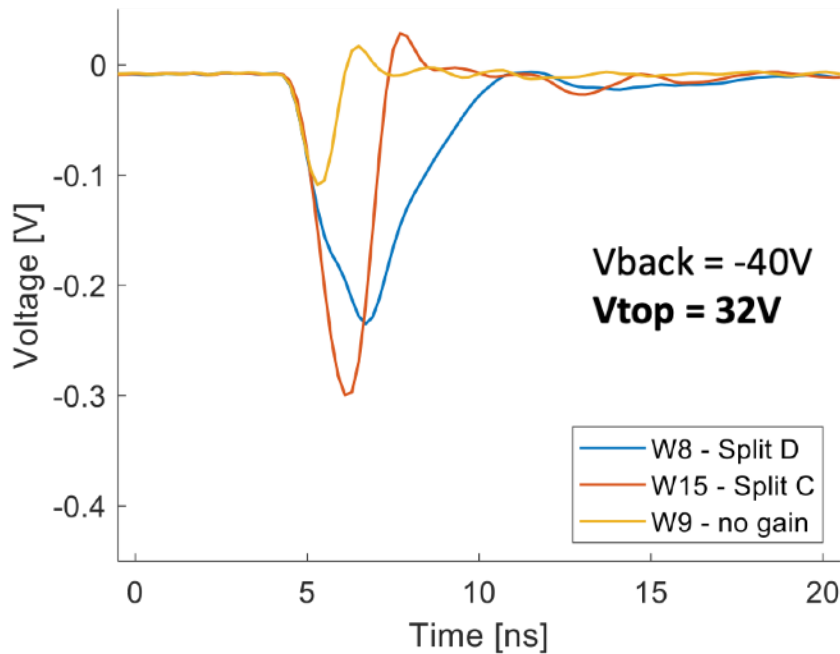
Jacopo Endrizzi

- **In first short loop gain was 2.5x: gain layer to be optimised**
- **So far between 5 and 15, depending on the split**
- **Much better matching with simulations**

# We have gain!

## Quasi-static characterization: A2 gain with NIR LED illumination

- In **device A2** the high-field region expands laterally with voltage: onset of gain at larger Voltage.
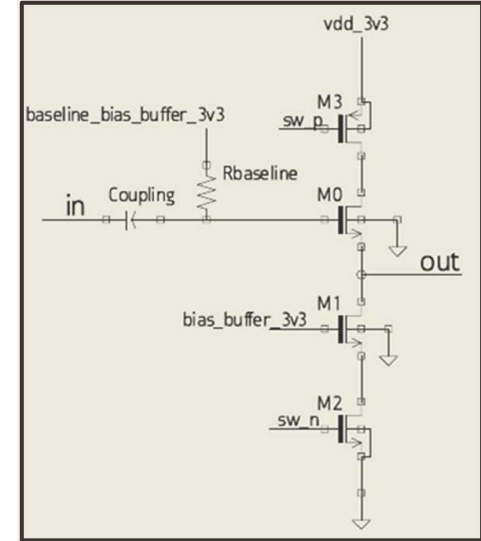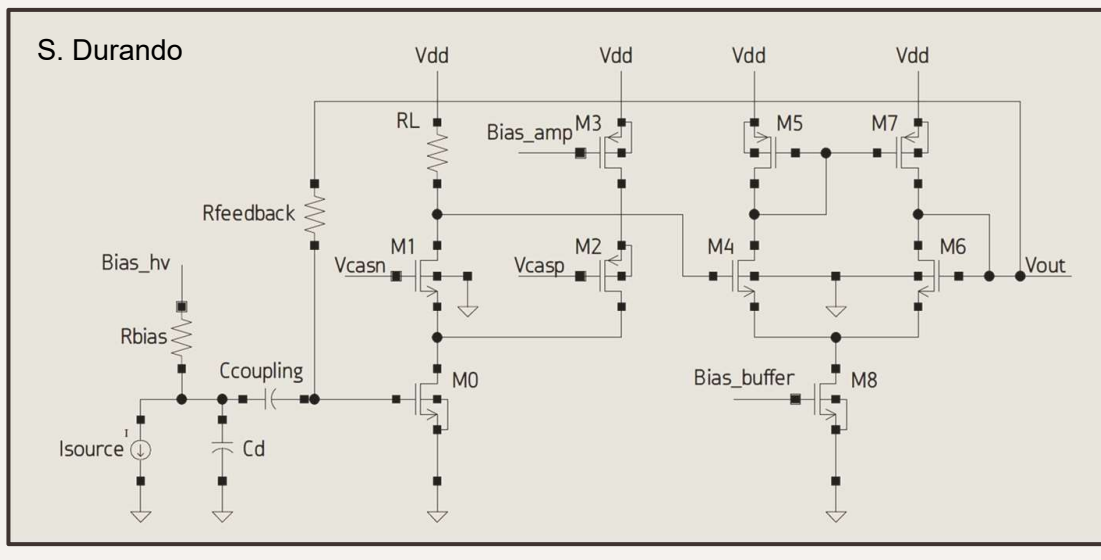- High voltage: 55 – 60V → Gain is similar to central value

9
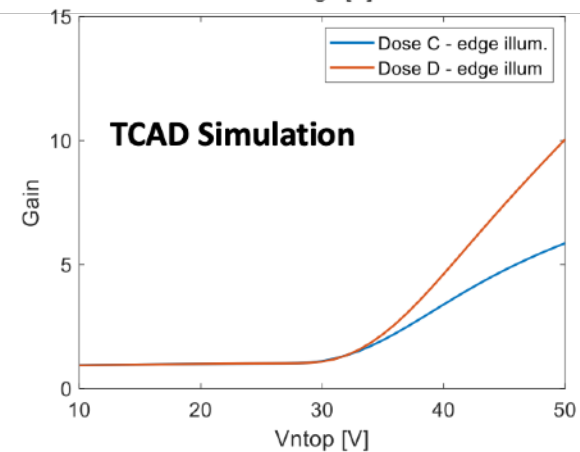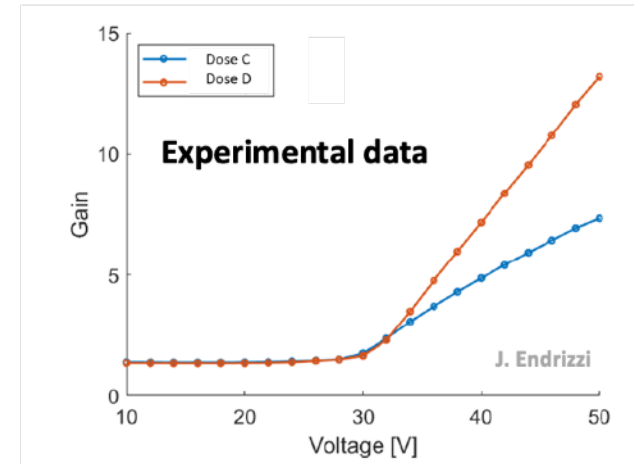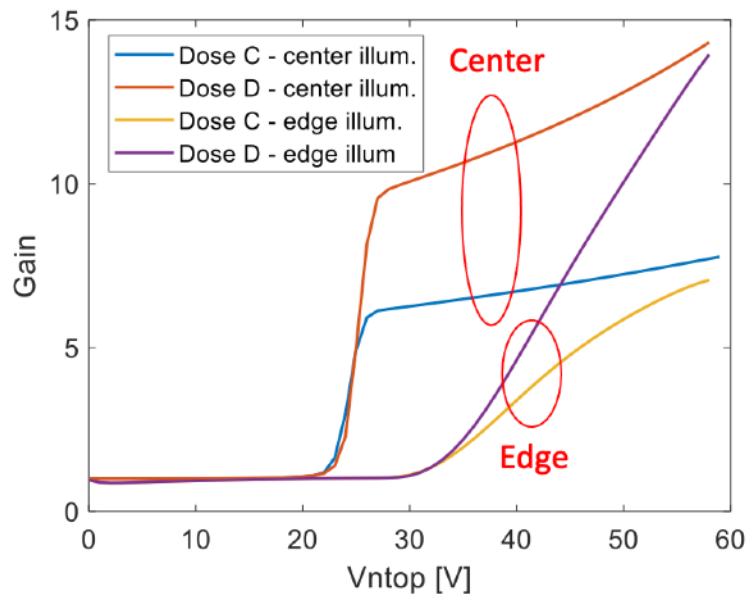
# The effect of the top voltage
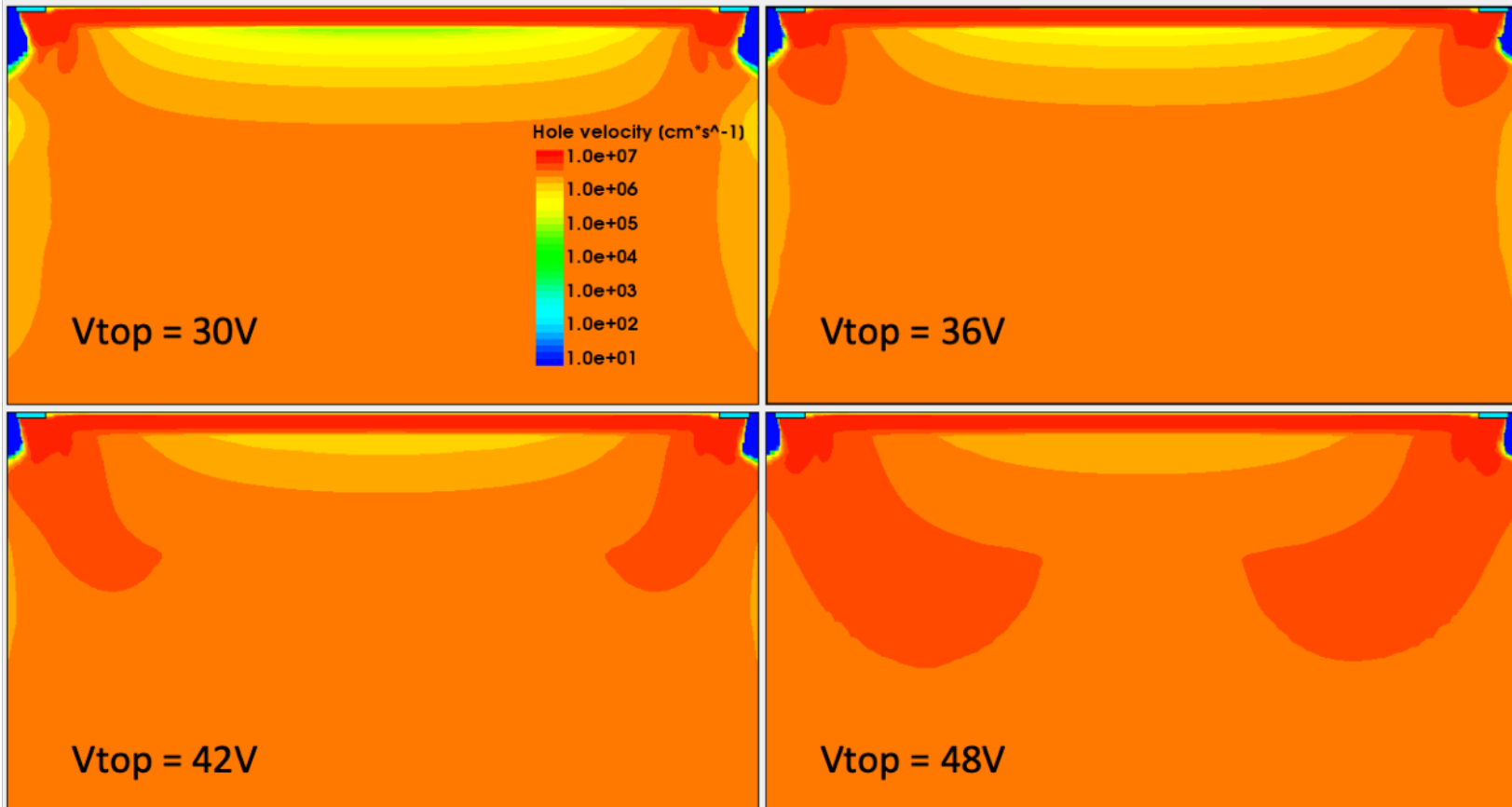
# CMOS LGADs with front-end: first concept
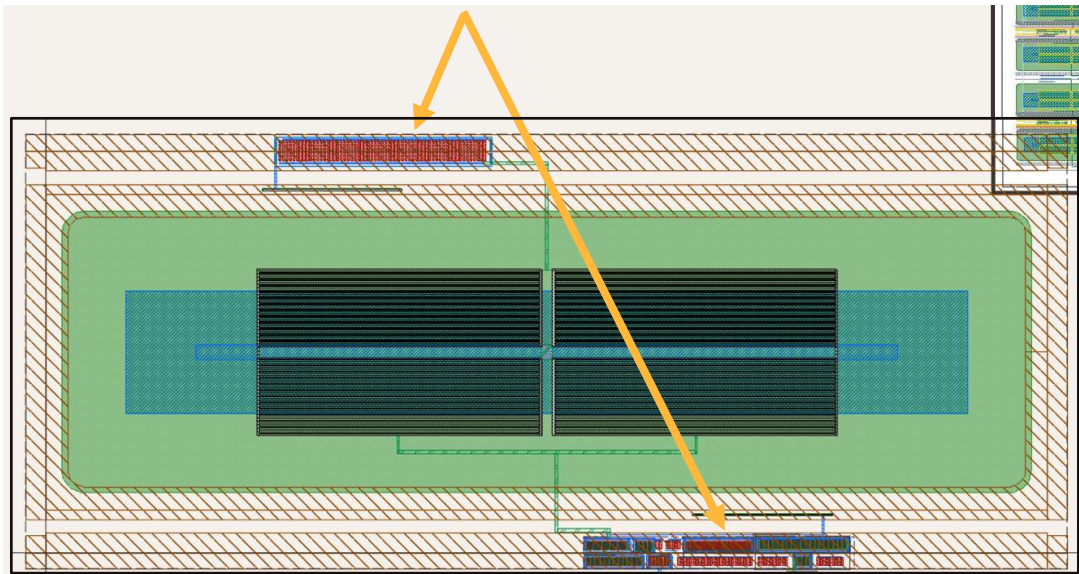


- **Front-end included in the pixel**
- **Similar to FE for standard LGAD**
- **Limit on RX coverage to be relaxed in dedicated runs**

# CMOS LGADs with front-end: ASIC

## First results on monolithic CMOS detector with internal gain

U. Follo [iD],[a,b,*] G. Gioachin [iD],[a,c,*] C. Ferrero [iD],[a,b] M. Mandurrino [iD],[a] M. Bregant [iD],[d]
S. Bufalino [iD],[a,c] F. Carnesecchi [iD],[e] D. Cavazza,[f] M. Colocci [iD],[f,g] T. Corradino [iD],[h,i,1]
M. Da Rocha Rolo [iD],[a] G. Di Nicolantonio,[j] S. Durando [iD],[a,b] G. Margutti [iD],[j] M. Mignone [iD],[a]
R. Nania [iD],[f] L. Pancheri [iD],[h,i] A. Rivetti [iD],[a] B. Sabiu [iD],[f,g] G.G.A. de Souza [iD],[d]
S. Strazzi [iD][f,g] and R. Wheadon [iD][a]
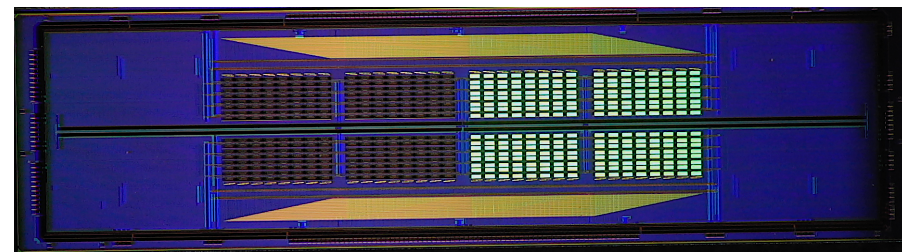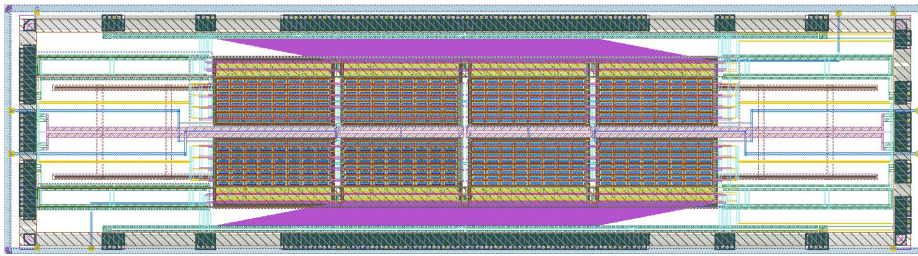
# CMOS LGADs with front-end: results from first short loop
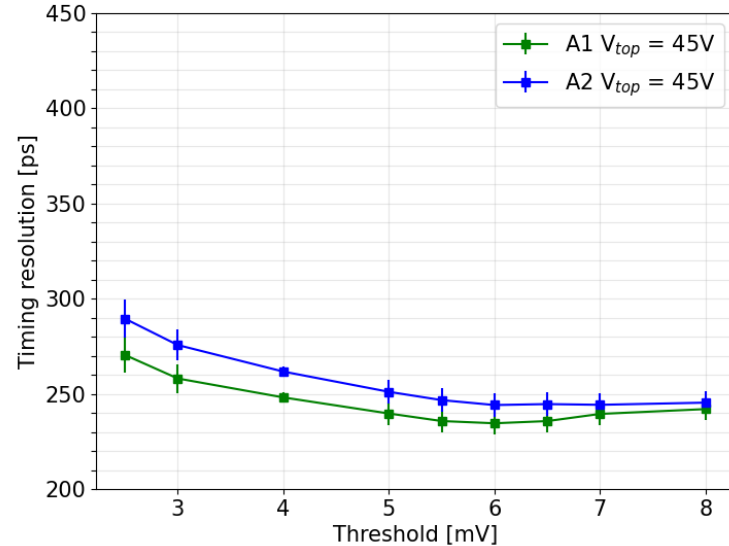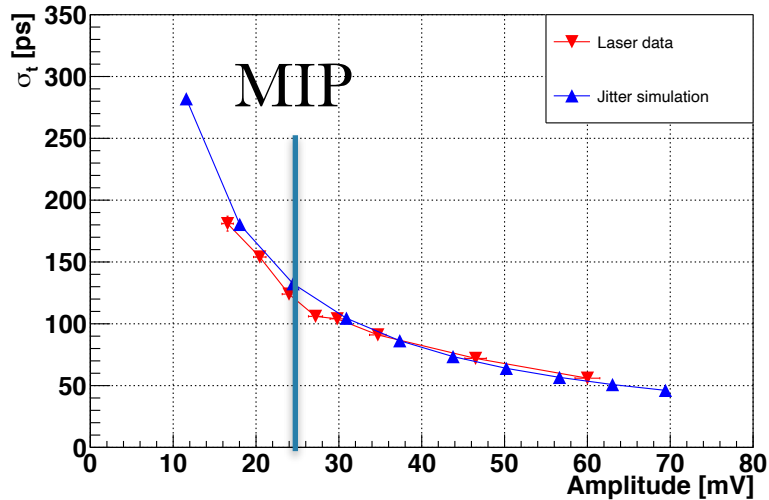


- **Gain: 2.5x**
- **Estimated jitter for 1 MIP with laser: 130 ps**
- **Obtained resolution in beam test with nominal parameters significantly worse: sensor-related effect**

# CMOS LGADs: matching simulation and measurements



ALICE 3 Days -- Umberto Follo - Giulia Gioachin                                    16
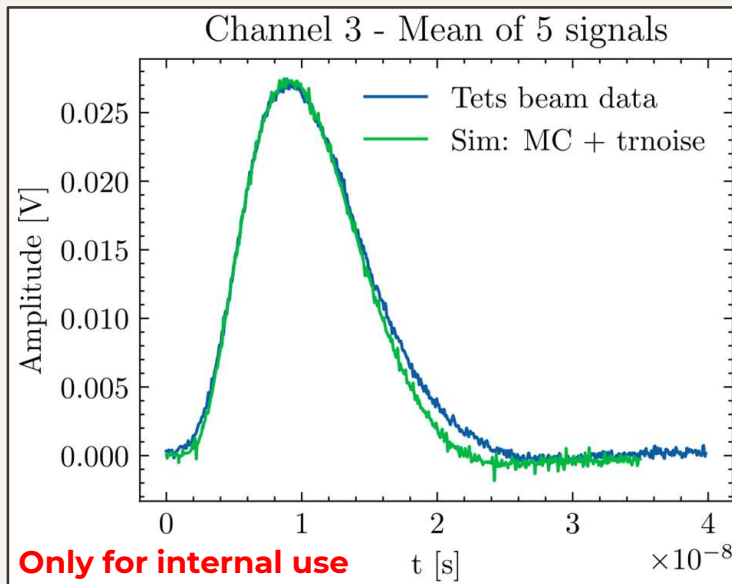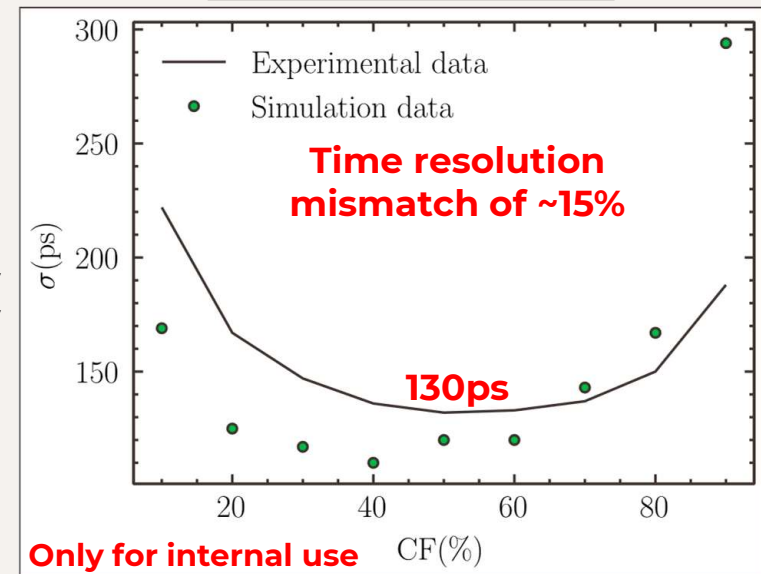
14    • **Different set of experimental parameters to match simulated results**

# CMOS LGADs: FIB



**Backside current lowered of 2 order of magnitude**
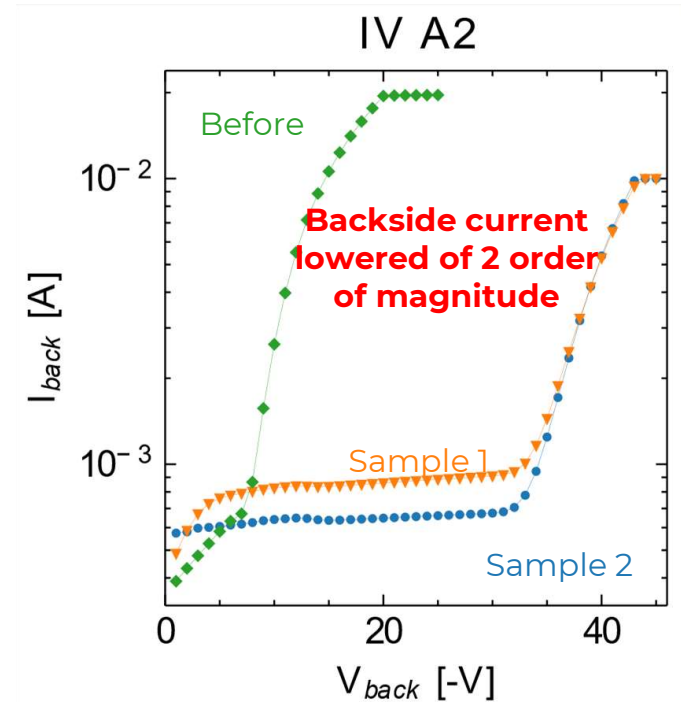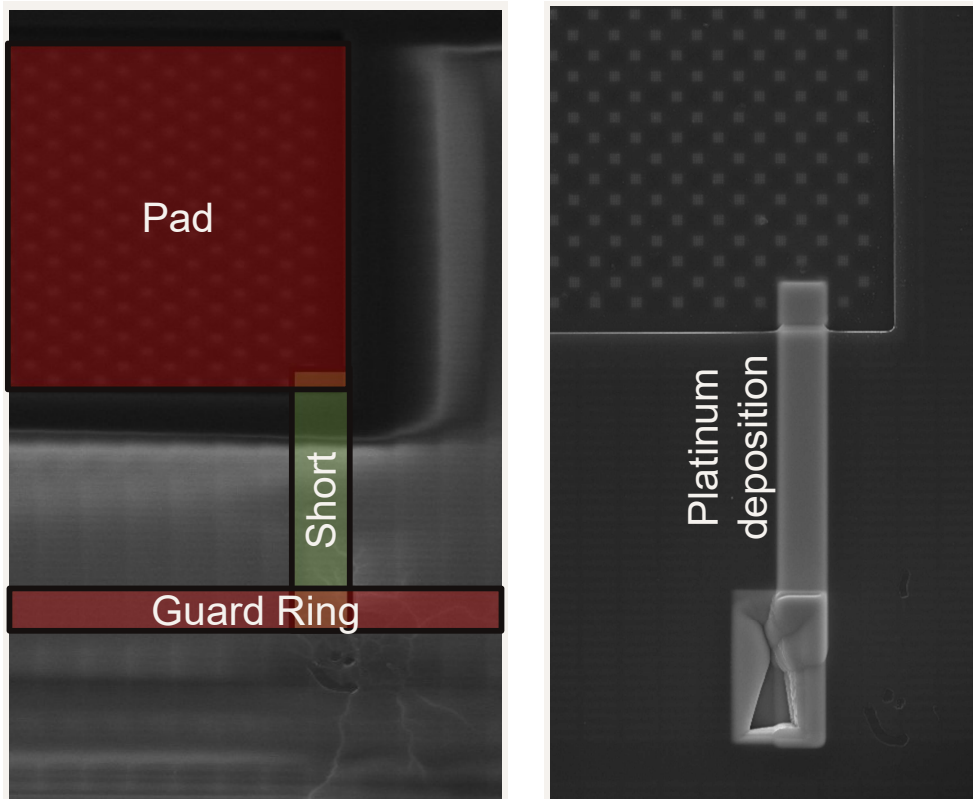
- **Backside current reduced by two order of magnitudes with FIB**
- **FiB done at National Institute for Metrology Research (INRiM) in Torino**

# CMOS LGADs with front-end: new short loop with higher gain

## Fe55 – New production

First estimation of **gain** using a non collimated radiation source of Fe55

Fist gain estimation



Vtop = 60V
Vback = -25V

Amplitude distribution in response to Fe55

Preliminary results

Vtop = 60V
Vback = -25V

Preliminary results
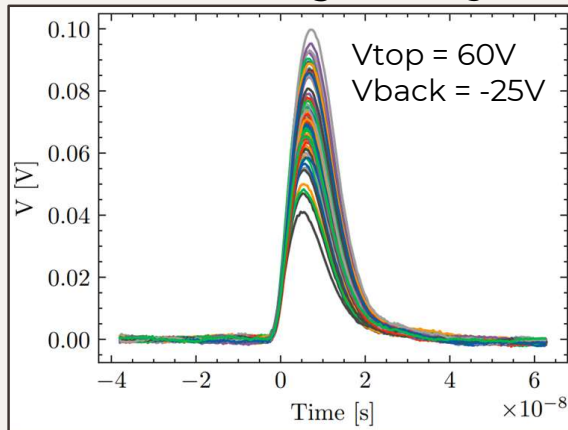
| | Energy (keV) | Relative probability |
|---|---|---|
| $X_K$ | | |
| $K\alpha_2$ | 5,88772 | 51 |
| $K\alpha_1$ | 5,89881 | 100 |
| $K\beta_1$ | 6,49051 | 20,5 |
| $K\beta_5''$ | 6,5354 | |

Superposition of $K_\alpha$ and $K_\beta$
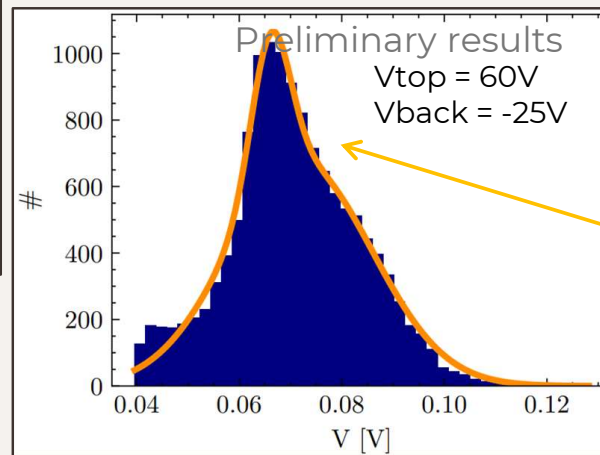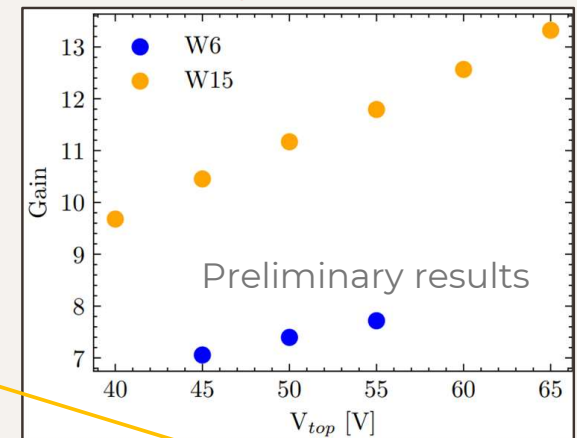
$$Gain = \frac{Peak\ [V/e]}{Electronics_{gain}[V/e]}$$

From electronics simulations matched with data

ALICE 3 Days  --  Umberto Follo - Giulia Gioachin

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https://indico.cern.ch/event/1415726/contributions/6144014/attachments/2942873/5170961/
Presentazione_Upgradeweek.pdf - U. Follo.

16

Mean signal MPV

Vtop = 55V
Vback = -25V



Time resolution vs CFD
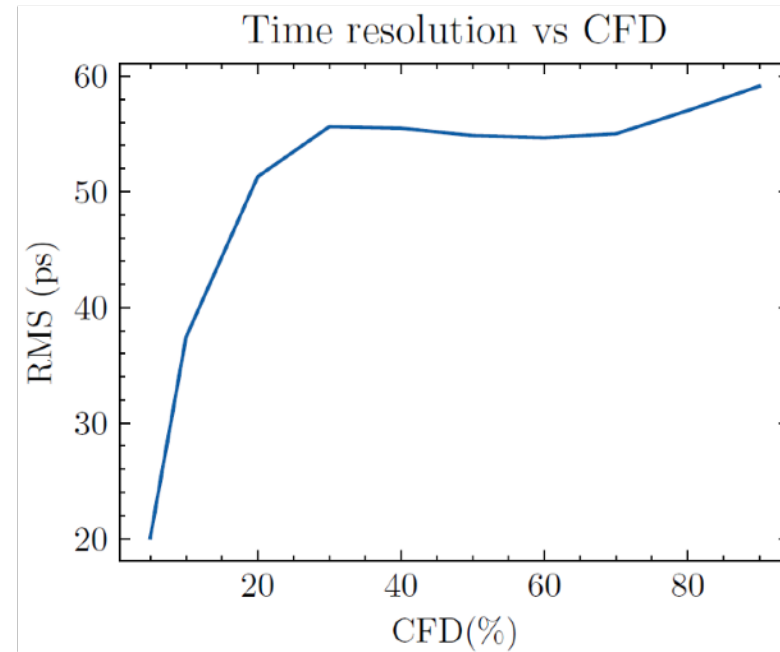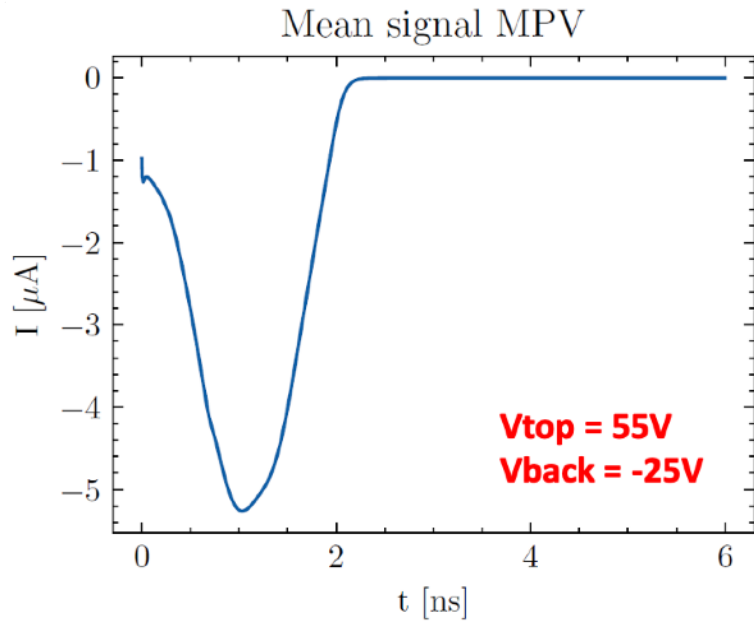
- **Beware of border effect!**

# …and in the next short loops?
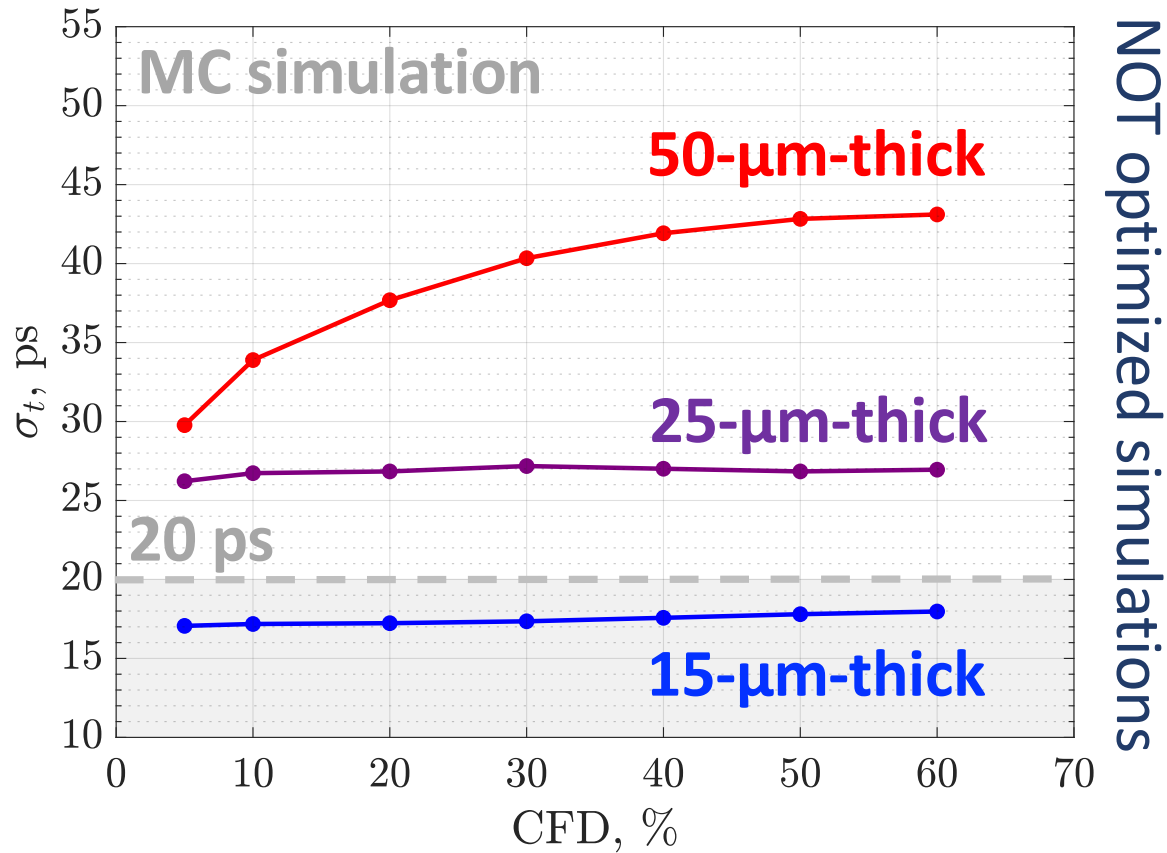


- **Beware of border effect!**

# Back to May 23…
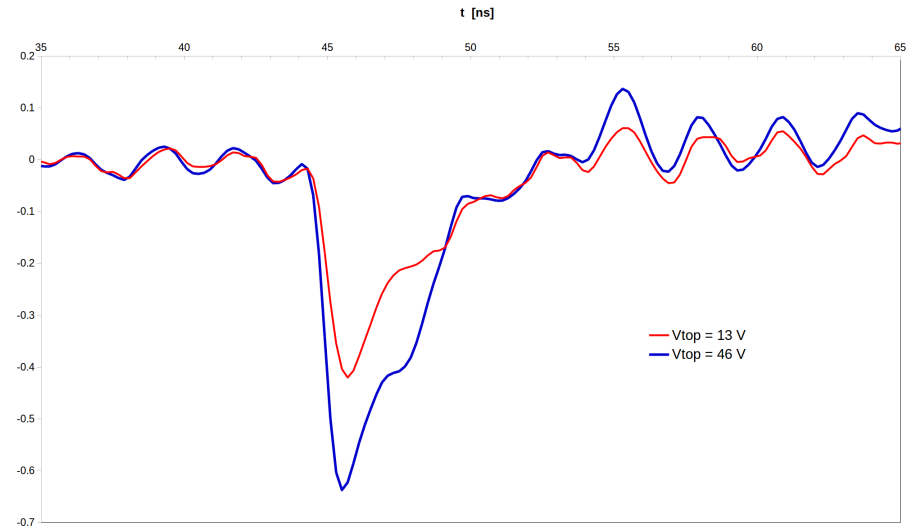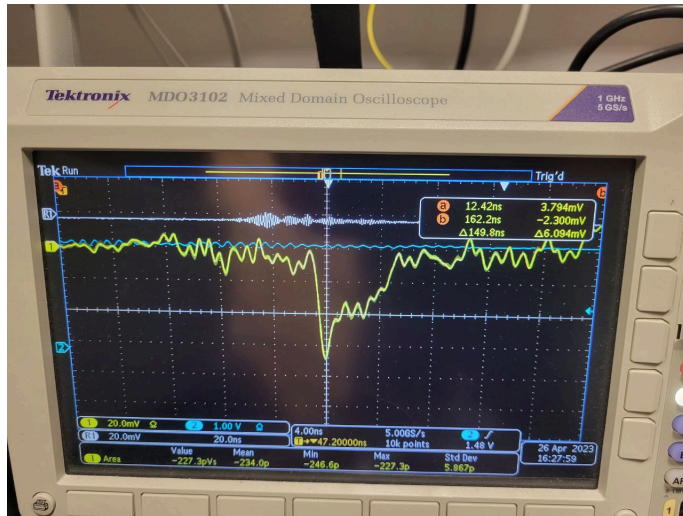




- $V_{top}$ = 40 V
- $V_{back}$ = 160 V
- $V_{Ngr}$ = 8 V
- $f_{laser}$ = 100 Hz
- Signal Amplitude = 120 $\mu A$

- L. Pancheri, S. Durando

- Signals acquired with 1 structure:
  Wafer 5 - 250 A1 (W5_250_A1A2_A1)
    - **Rising time** $\simeq$ 1 ÷ 1.5 **ns**
    - **Signal duration** $\simeq$ 6 **ns**
    - **Increasing $V_{top}$ the signal amplitude increases**

- **First delivered structure are the 200 um thick option: worse set for timing!**

- **50 um thick structure expected soon**

# Next steps

- We have CMOS sensors with embedded front-end and gain

- A very **good progress** in a relatively **short time**

- Test beam (October 24) and simulations activities to match **measurements** and **simulations**

- One short loop with thin active area (first or second quarter 2025) to further improve the **time resolution** by using **thinner** active substrate

- Full sensor optimisation and ultimate time resolution can **not** be **achieved** without a **full set of dedicated masks**

- This will be the **last short loop** which makes sense with the **ARCADIA** mask-set

- After that we need to move to **dedicated engineering run**

# Next engineering runs: ER1
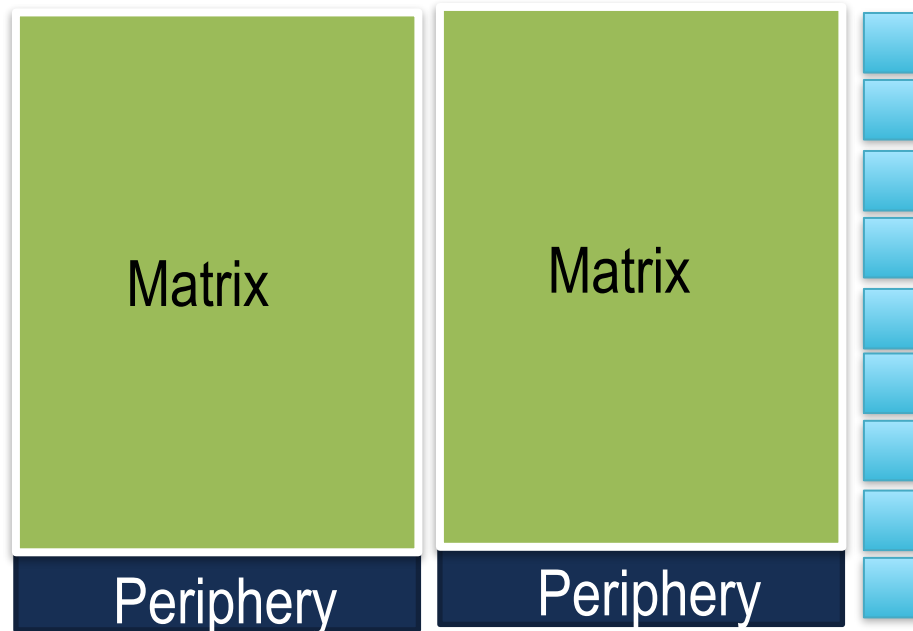


- **Larger test chips contains all what is needed in the final version (including testability:-))**
- **Unit must be uniformly repeatable in view of the final sensor**
- **Pixel size defined to optimise timing**
- **Keep the matrix as simple as possibile and the periphery versatile**
- **Large chips can accommodate a reasonable (2-3) number of different flavours**

# Next engineering runs: ER2
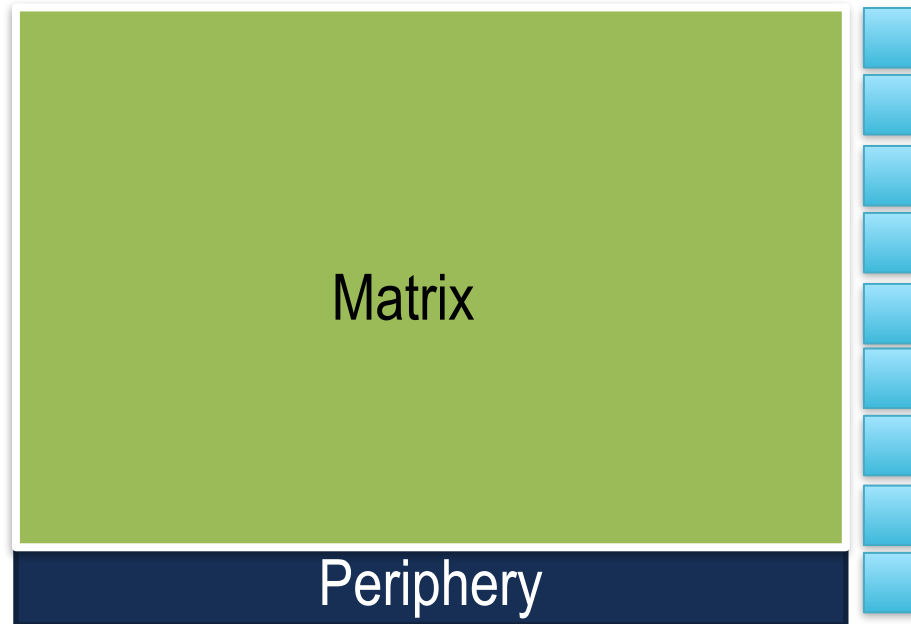


- **Final, <span style="color:red">full-reticle</span> sensor design**

- **Only one sensor and electronics option**

- **Assembled with mostly already silicon proven blocks**

- **<span style="color:red">Pre-production</span> run**

# Next engineering runs: ER3



- **It might not be needed, but HAS TO BE IN THE BUDGET!**
- **Things could be also fixed in "short-loops"**
- **Stitching?**

# Stitching?

https://cerebras.ai/product-chip/



- **24 cm x 24 cm, 2,7 Trilions transistors, stiched processor for AI in 7 nm…**

- **Cost is accordingly…**

# Outlook

- We **have** CMOS LGADs with **gain!**

- Development done at very **low-cost so far…**

- …but there is a **minimum threshold** you can not go below!

- Next imminent steps: beam test, simulation tuning, final short loop

- In the next months: consolidate design, mechanics/integration, read-out teams…i.e. the full project!

- The less is done, but let's be optimistic and carry on!