Perspectives for a RICH front-end based on the ALCOR architecture and possible synergies with other experiments

ALICE Upgrade Week, Krakow, 09/10/2024

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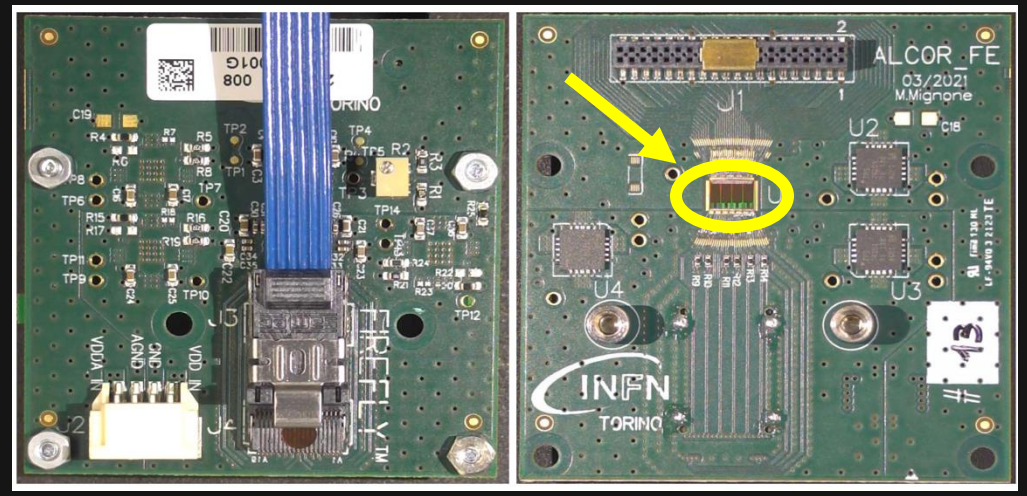
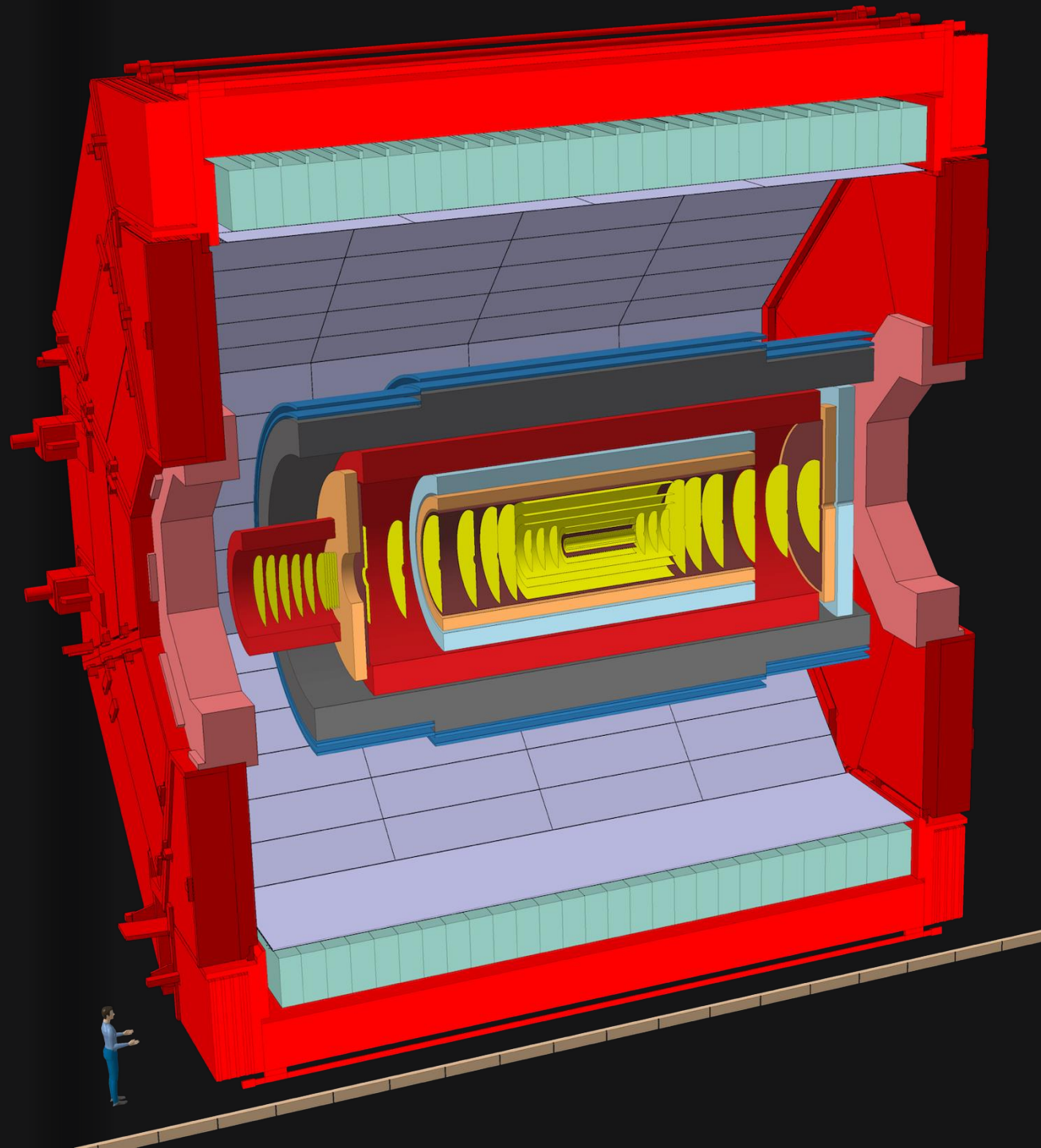


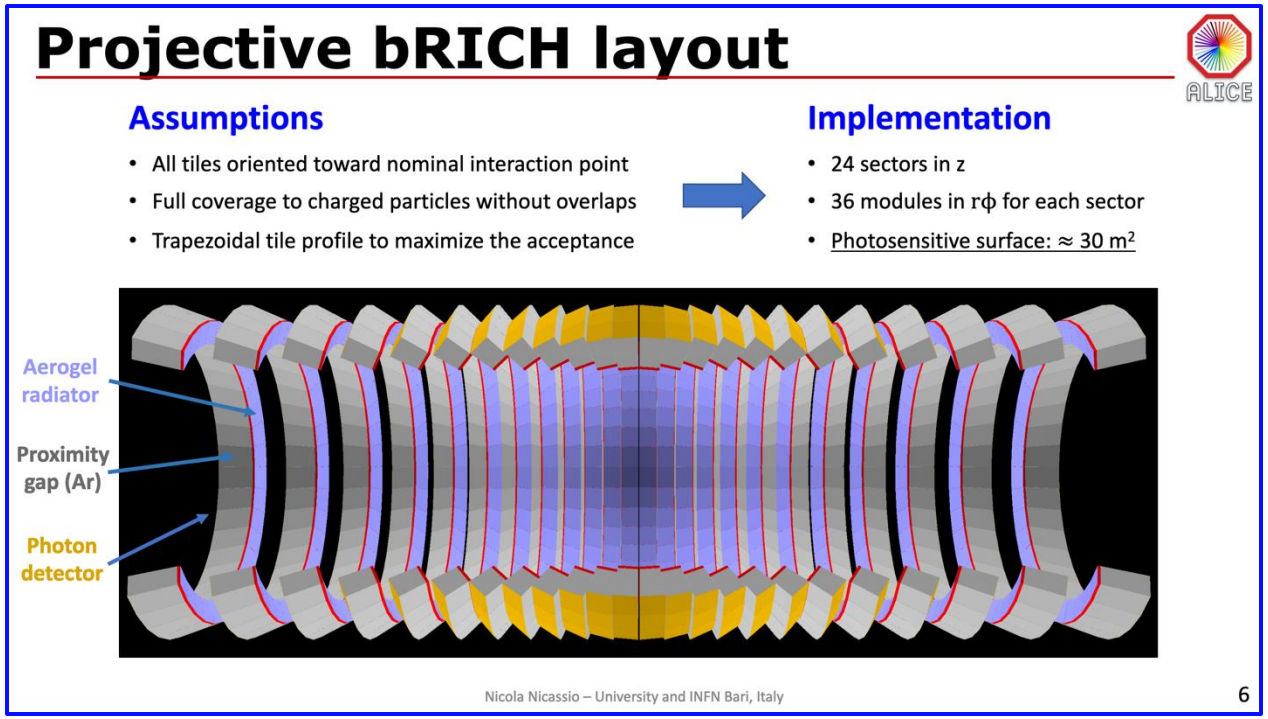


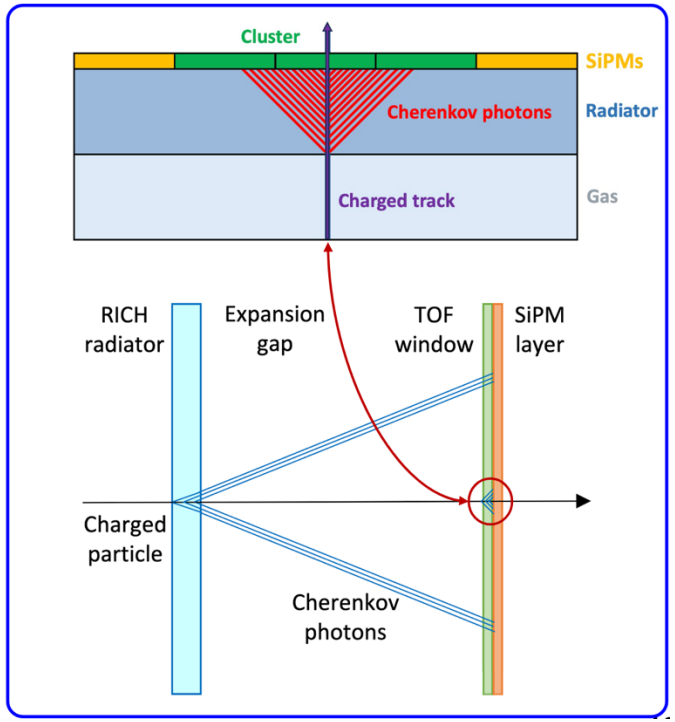
A SiPM-based RICH for Alice 3

The bRICH detector for Alice-3 has the goal to extend the charged particles identification capabilities beyond the limits of the ToF detector:

- p/e in the p range 0.5 – 2.0 GeV/c
- K/p in the p range 2.0 – 10.0 GeV/c
- p/K in the p range 4.0 – 16.0 GeV/c

A design based on an aerogel radiation coupled with SiPM sensors is currently being investigated.



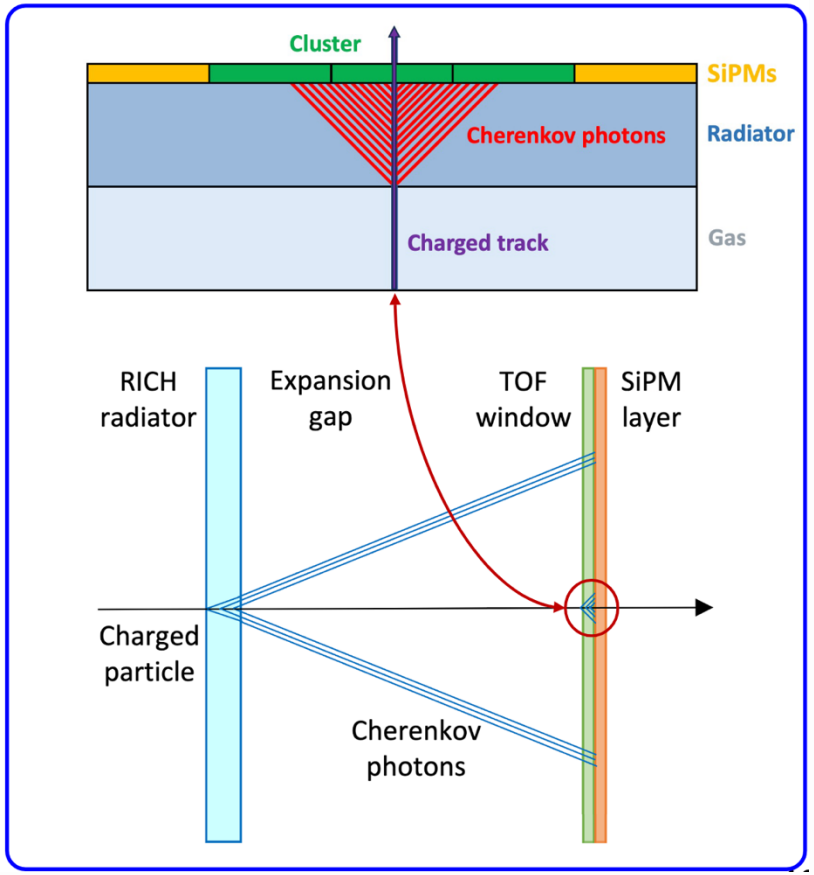


- **24 sensors x 36 modules**
- **Sensor area** ~30.7 m²
- **Total #channels** ~ 7M
- **Radiator:** areogel, lattice of SiO2 grains filled with trapped air
- **Size** L ~ 2 cm, n = 1.03
- **Expansion gap** L ~ 25 cm
- **SiPM size** 2x2 mm²
- **PDE @450 nm** > 40 % (ref. HPK 13360-3050CS)
- **Large acceptance:** |η| < 4

From **"A novel SiPM-based aerogel RICH detector for the future ALICE 3 apparatus at LHC"** – **Nicola Nicassio** (University and INFN Bari) for the ALICE Collaboration INFN2024 , February 26-28, 2024

Requirements for the Readout Electronics

- **Environment with very-high potential pile-up of dark counts because of the radiation damage of the SiPM**
  ➔ Very short acquisition gate required, ~ **1 ns**, in order to reduce the dead time and the bandwidth occupation due to the dark counts.
  Only one bunch of piled-up photons in each gate.
- **ToA with resolution ≲ 50 ps RMS**
- Thermal Dissipation under 500 mW / cm^2
- It is important to discriminate very low photon-count (1-3) events from higher photon-count events (> 5-6)
- Modularity fitting the mechanical constraints
- Modularity fitting the bandwidth constraints of the **lpGBT transceiver**



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Requirements for the Readout Electronics

The SiPM array of the bRICH should be capable of detecting two different signals, discriminating between each other:

- **Single-photon** or low-photon-count hits due to the interaction of the incoming particle with the **RICH radiator**
- **High-photon-count** (> 5) clusters due to the interaction of the charged particle with the **radiation layer installed in close proximity** of the sensor.

These second hits allow to locate the center of the Cherenkov light rings, thus simplifying considerably the reconstruction process.

Clustered photons: more than 5 photoelectrons in the same SiPM device.

Mainly single photons impinging on each SiPM device in the Cherenkov projected ring.

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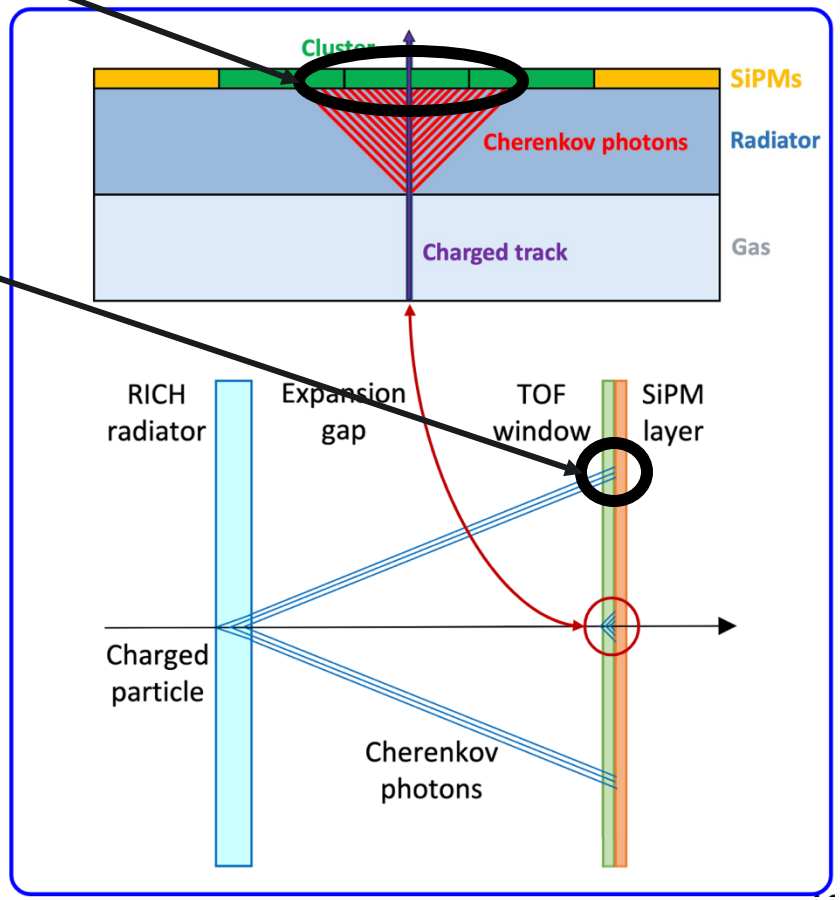
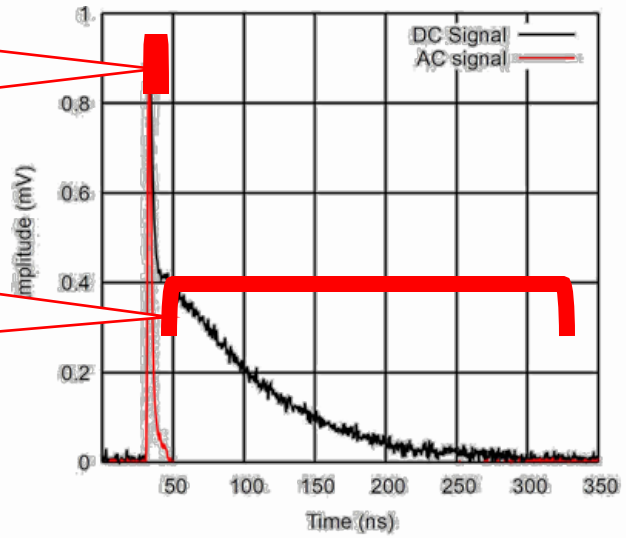


1 ns integration gate with high-gain, integral limited to the peak

Very high probability of dark, piled-up pulses in this region!



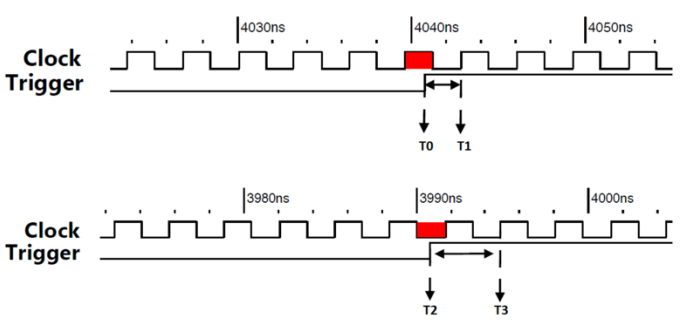
In-Pixel Signal Processing

Time-of-Arrival

The Time-of-Arrival information of each photon is crucial, since it is used to cluster the photons related to the same event, thus discriminating the signal from the background of dark counts.

The Time-of-Arrival is obtained from the timing discriminator embedded in each pixel of the readout ASIC, using a Time-to-Digital converter.

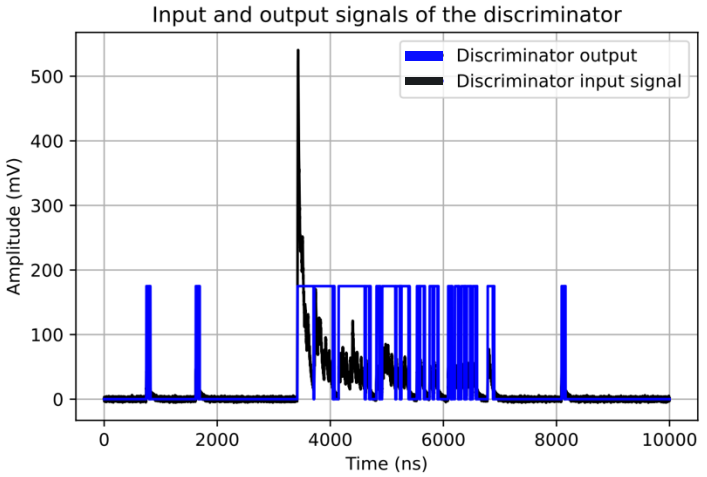
The Time-to-Digital converter interpolates the synchronous coarse counter triggered by the clock, therefore it measures the time interval between the discriminator output and the following edge of the clock.

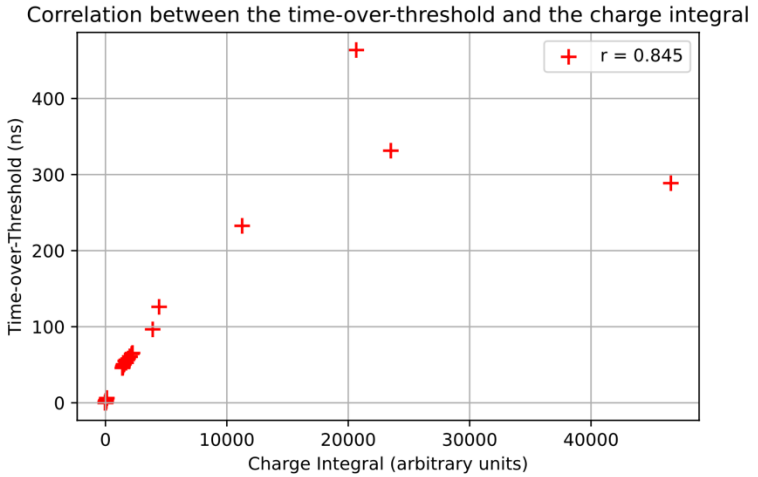


Cherenkov Ring / Central cluster discrimination

Photons emitted from the primary aerogel radiator, in a single event, travel through the expansion gap hitting different SiPM pixels of the sensor.
On the contrary, the photons produced in the interaction with the radiator directly coupled to the sensor provide information on the charged particle track position.

This information cannot be extracted using the Time-over-Threshold or the charge integration of the whole SiPM discharge pulse because of the very high probability of getting pile-up with a dark count event.

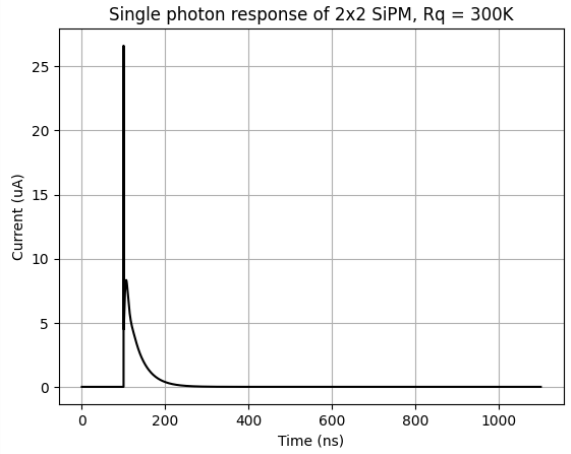




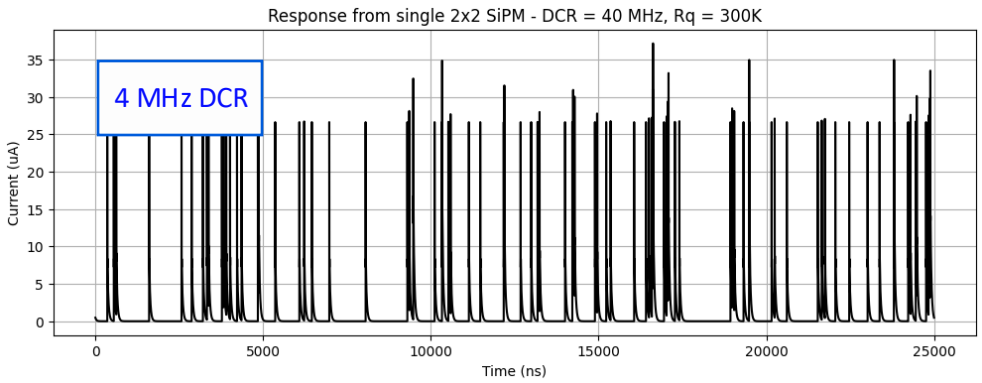
Dark Count Rate: SiPM and Bandwidth Limitations

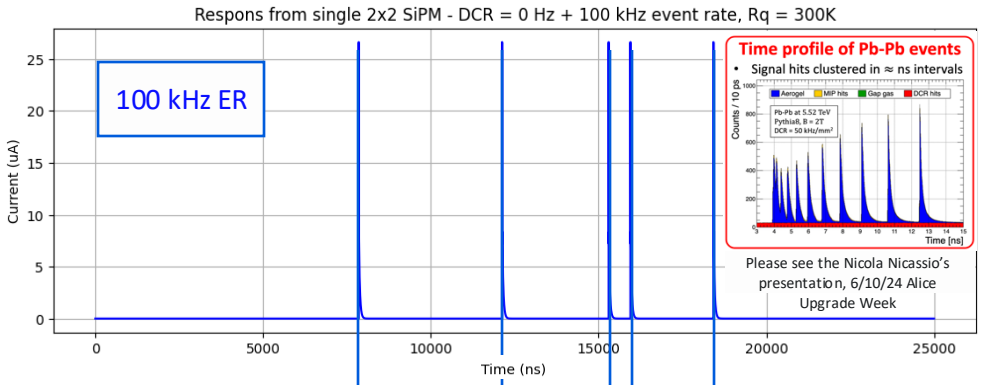
Some simple simulations considering the current output waveform from the SiPM sensor, a **DCR of 4 MHz** and an **event rate of 100 kHz / pixel** show that even considering an infinite bandwidth of the input stage of the readout ASIC, the intrinsic pulse width of the detector is sufficient to introduce pile-up effects of the Cherenkov light pulses with the dark count pulses.

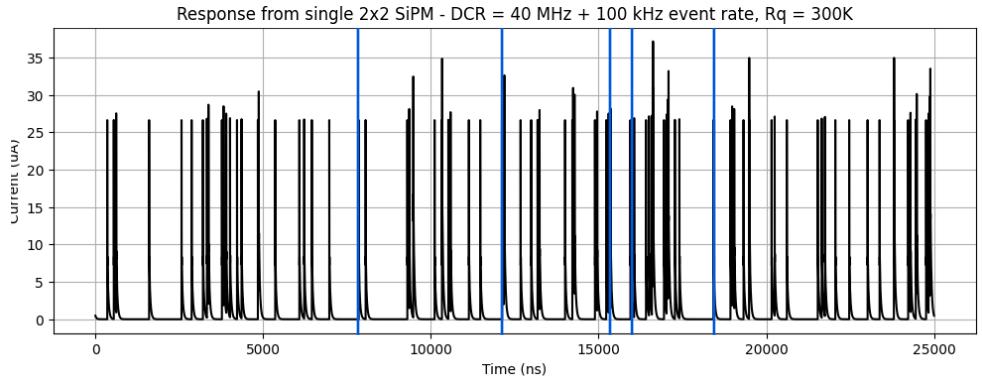
This effect cannot be mitigated by simply introducing an arbitrary short VETO gate on the output of the discriminator. It is an intrinsic limitation of the detector technology.



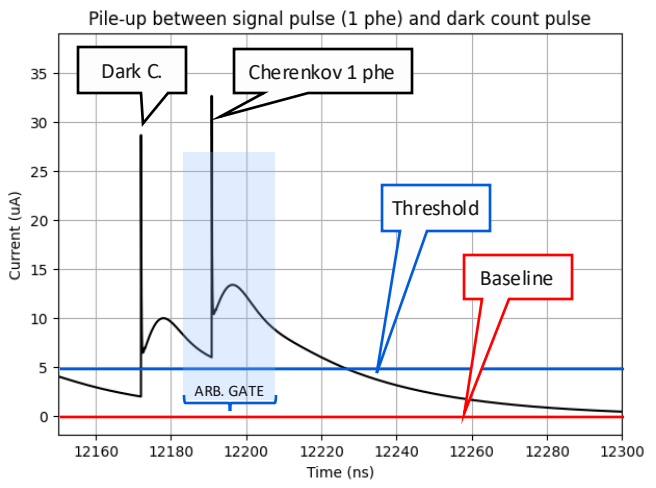
Current detector response, hard-limit with ideal electronics having infinite bandwidth.

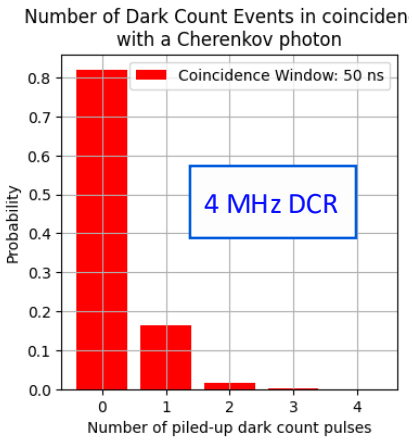


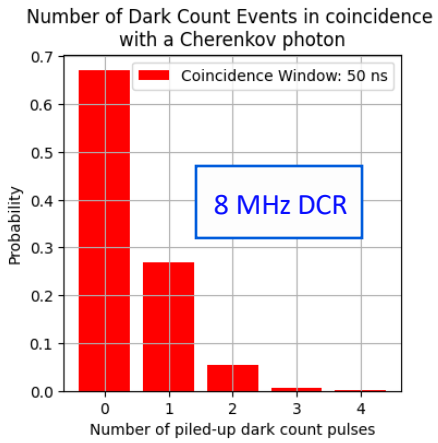




Pile-up with DCR at the detector-response level







Channel Modularity: Data Rate

28x e-Links
@320 Mbps
Single Data Rate

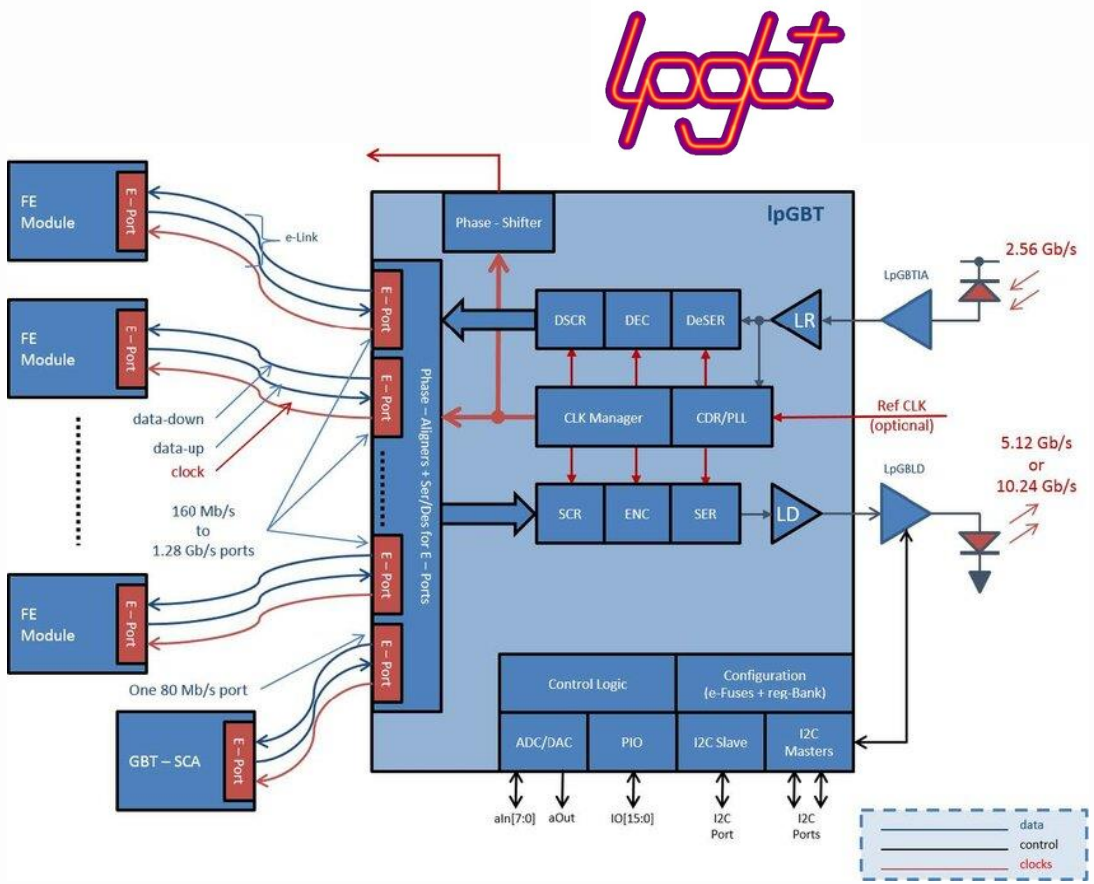
28-columns
chip with 32 px/col:
~10 Mbps/pixel

~156 events/s
for each pixel

Considering a Dark Count Rate (DCR) of 4 MHz, with a 25 ns bunch-crossing period, at the limit, **the pixel requires a 1 ns gate.**

The channel modularity is not only constrained by the mechanical integration, but also by the high-bandwidth requirements due to the high dark count rate. A system with a 320 Mbps LVDS data transceiver for each column, tailored to fit the lpGBT data transceiver requirements, can process up to 156 events/s per pixel.

- **5.12Gbps / FEC5**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (112bit)**: From lpGBT e-links.
  - **FEC (10bit)**: Can correct up to 5 consecutives errors.
- **5.12Gbps / FEC12**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (98bit)**: From lpGBT e-links (2bit unconnected).
  - **FEC (24bit)**: Can correct up to 5 consecutives errors.
- **10.24Gbps / FEC5**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (230bit)**: From lpGBT e-links (6bit unconnected).
  - **FEC (20bit)**: Can correct up to 5 consecutives errors.
- **10.24Gbps / FEC12**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (202bit)**: From lpGBT e-links (10bit unconnected).
  - **FEC (48bit)**: Can correct up to 5 consecutives errors.



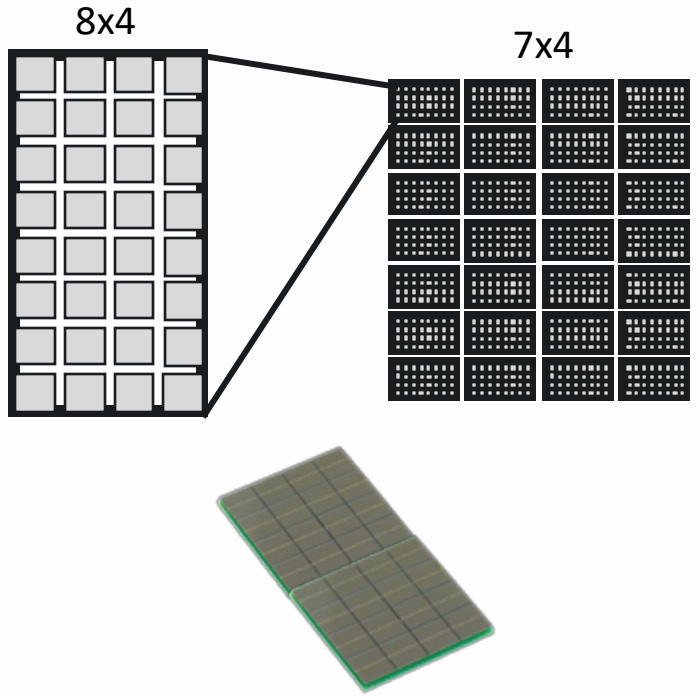
https://cds.cern.ch/record/2809058/files/lpGBT_manual.pdf

Channel Modularity: Sensor Integration

Mechanical Integration:

A convenient design could be based on modules of 896 channels each one:

- The **readout ASIC** has **28 columns with 32 pixels** each one
- Each **SiPM matrix has 8x4 devices**.
- On each module, represented by a 6x6 cm^2 PCB, **7x4 SiPM matrices** are installed, covering an area of **6.4 x 5.6 cm^2**
- **20x20 mm^2** are occupied by the readout ASIC, **9x9 mm^2** are dedicated to the lpGBT



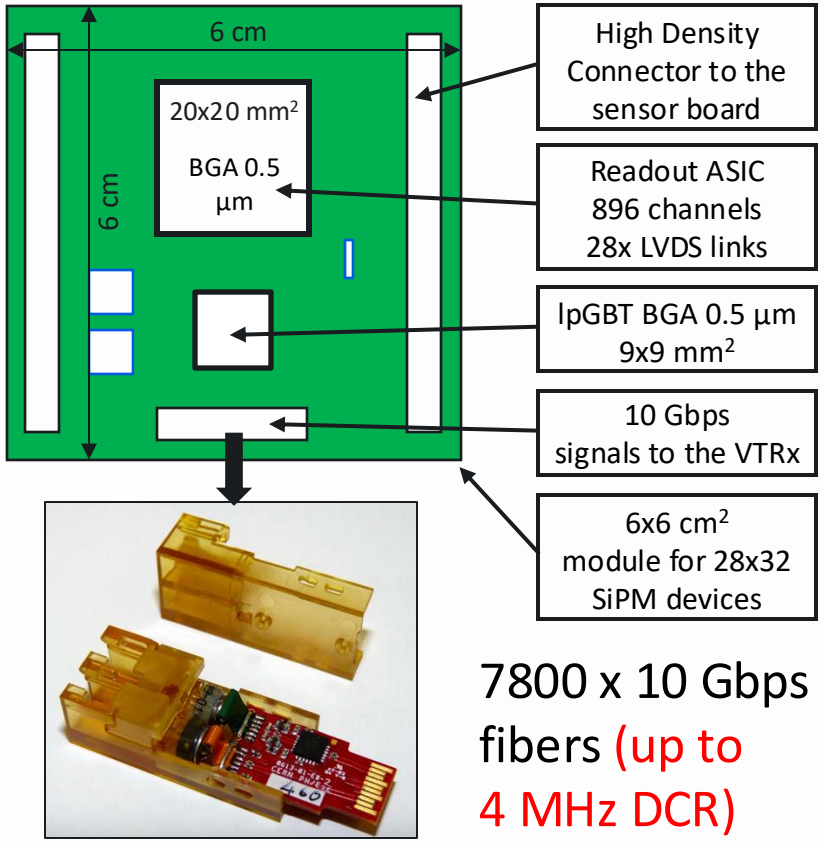
Power density:

- Each channel has a power consumption lower of 10 mW
- Less than 10 W per chip + 0.5 mW for the lpGBT
- Less than 15 W/board, reaching a **power density lower than 400 mW/cm^2** that can be managed using a standard cooling system.

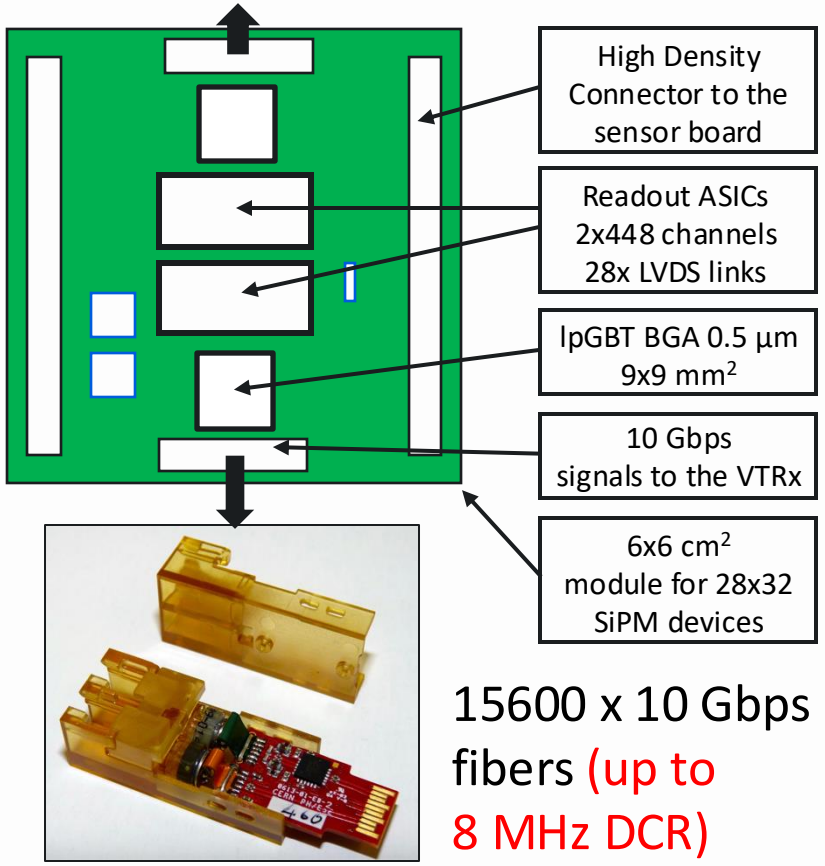
For about 7.000.000 channels [30 m^2], **7800 lpGBTs** are required with annexed optical transceivers and dedicated fibers.
The use of WDM techniques can reduce the number of fibers for the same bandwidth.

Channel Modularity: Higher BW Options

Higher bandwidth solutions are required if the dark count rate is above 4 MHz.
They consist of more readout ASICs with shorter columns in order to increase the available bandwidth for each pixel. The number of lpGBTs is doubled but the complexity grows very fast.
This approach is limited by the cost, by the power density and by the complexity of the PCB design.



7800 x 10 Gbps fibers (up to 4 MHz DCR)



15600 x 10 Gbps fibers (up to 8 MHz DCR)

4xASICs
4xlpGBT
on 2 sides

31200 x 10 Gbps fibers (up to 16 MHz DCR)

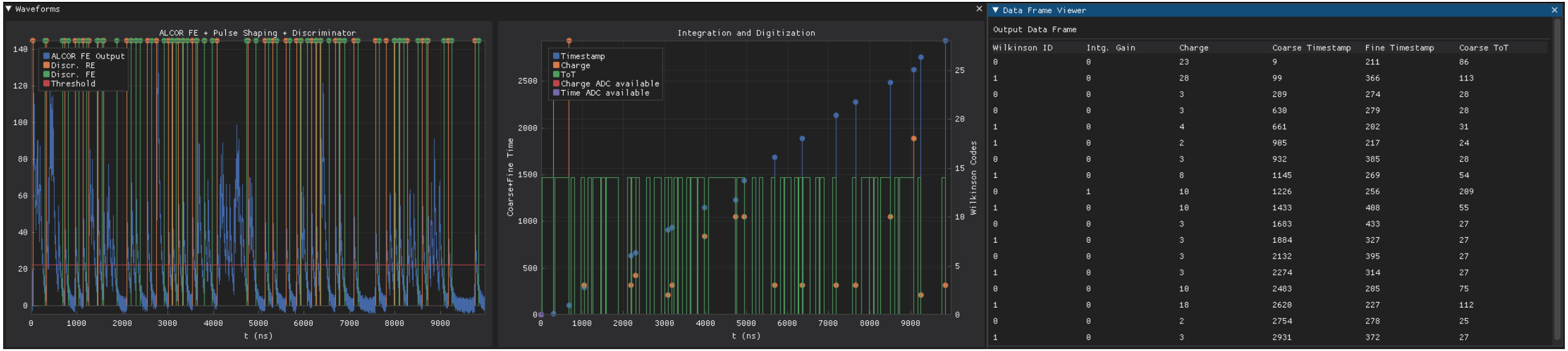
The System is Bandwidth and Sensor limited

An event rate of 156 kHz for each pixel can be easily managed by a variety of different pixel architectures

- With enough derandomization buffers (4), even a pixel based on 8-bit Wilkinson data converters (average conversion time $2^{Nbit-1} / f_{clk}$) can withstand this event rate.

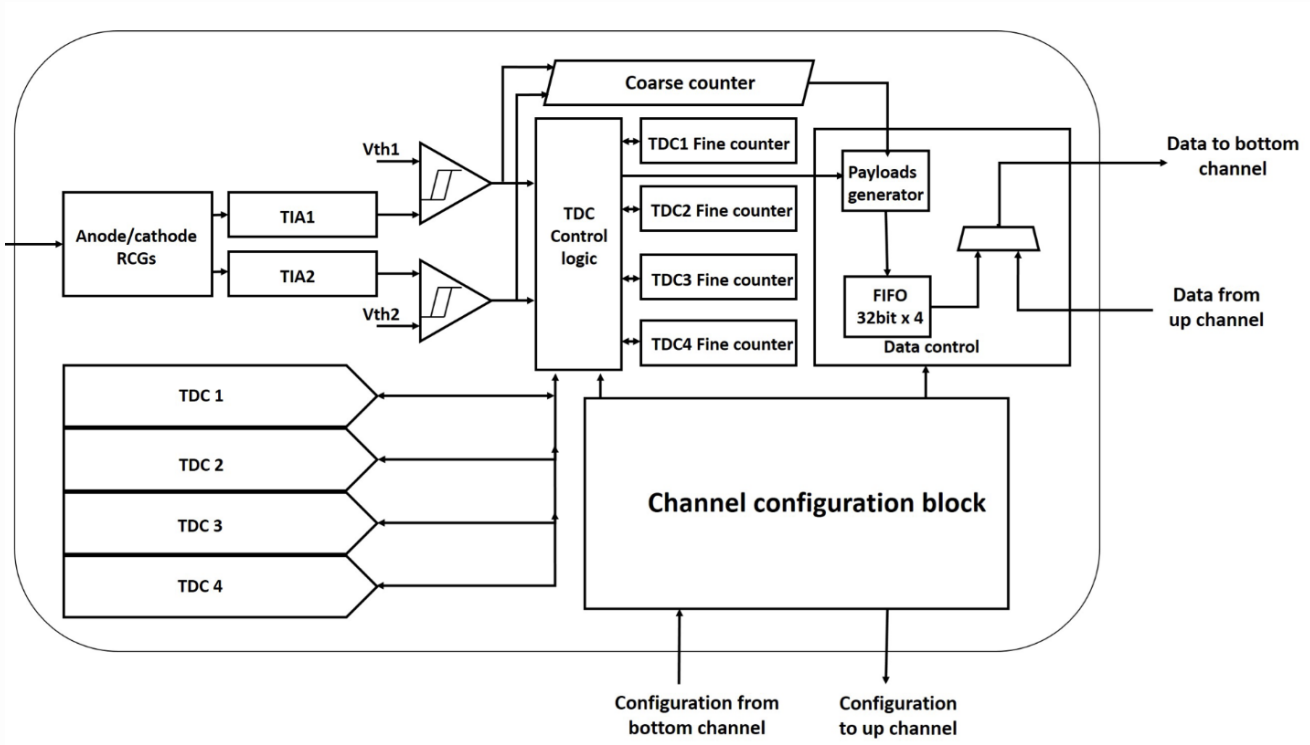
As an example, in the picture below 4 MHz of dark count events + 156 kHz Cherenkov light events are processed by the GRAIN ASIC pixel architecture, evolution of the ALCOR ASIC architecture.

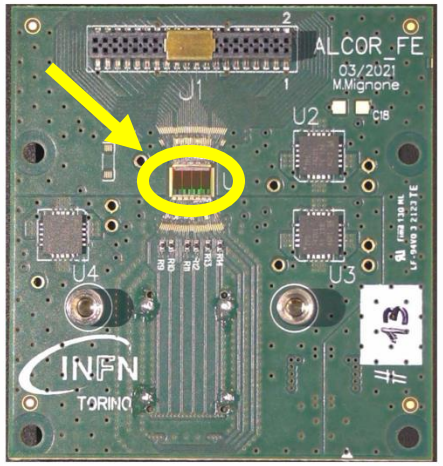
The system is primarily bandwidth-limited, then limited by the thermal, mechanical and package/PCB integration constraints.
When the DCR increases above 5-10 MHz, the probability of dark counts and signal pile-up at the detector response level is not negligible!

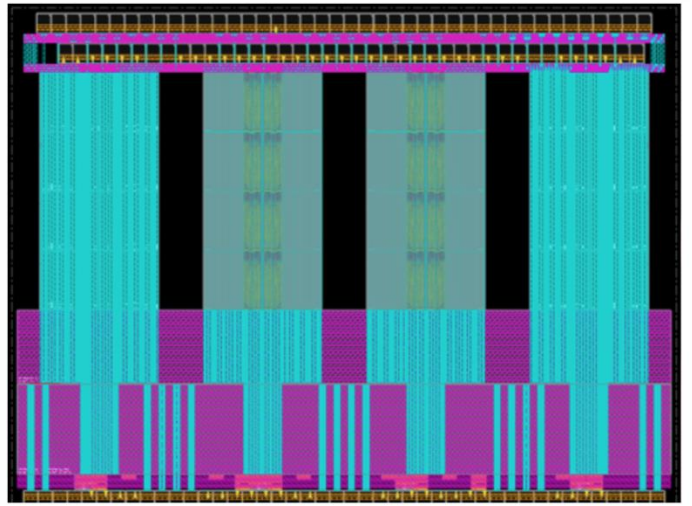


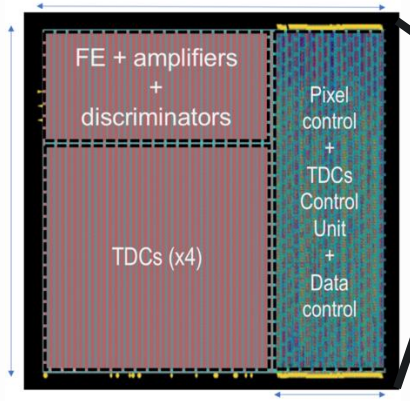
The ALCOR ASIC by the INFN-Torino VLSI Group

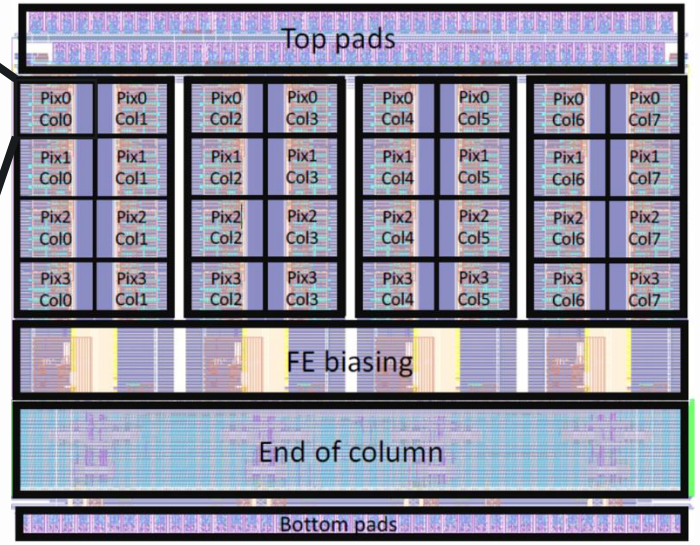
- Original chip (ALCOR32) developed in the framework of R&D for cryogenic readout of SiPM (Darkside collaboration)
- Short turn-around time thank to the re-use of several IPs (TDC, readout logic) already silicon proven
- Serves as the basis for the design of front-end ASICs for EPIC and DUNE
- Cost-effective 110 nm CMOS technology











Ongoing developments of SiPM Readout ASICs

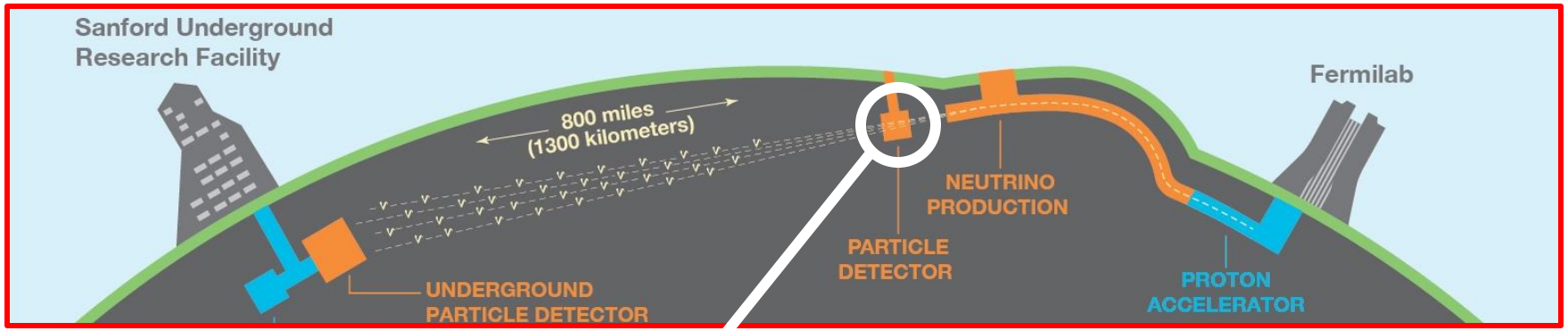
Ongoing developments started from the silicon-proven architecture of the ALCOR x32 channel SiPM readout ASIC:

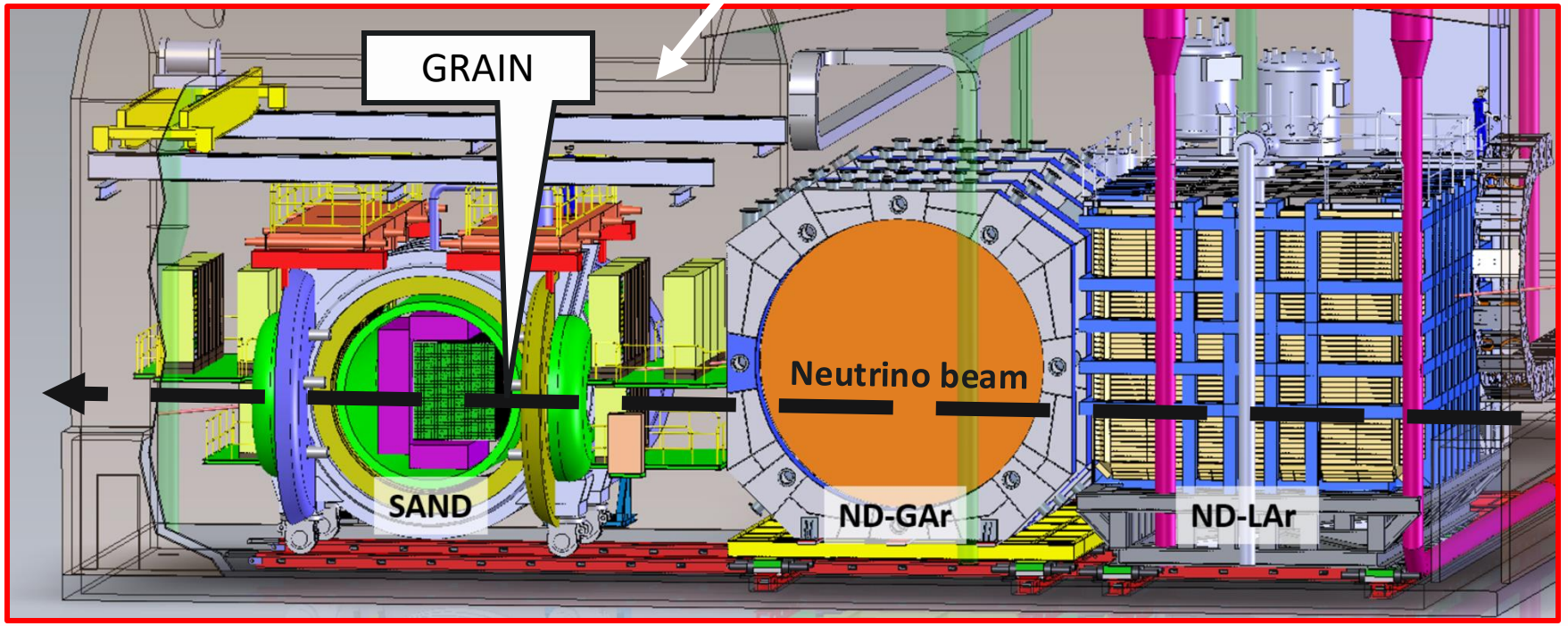
Feature	ASIC for EIC dRICH	ASIC for GRAIN at DUNE
Channel modularity	64 pixels (8 columns)	1024 pixels (32 columns)
Measurements	ToA, ToT	ToA, ToT, Charge Integral
VETO Signal	YES – Global, external	YES – Global, internally generated or ext.
Time-of-Arrival resolution RMS	≈ 150 ps with C_{IN} = 100 pF	≈ 50 ps (target)
Time-over-Threshold resolution RMS	≈ 1 ns	≈ 1 ns
Charge integration response	N.A.	Bilinear (2 gain values) + peak sensitive
Charge integral resolution	N.A.	9 bit: 10 codes / phe; 3 codes / phe
Charge integral dynamic range	N.A.	[1 – 25 phe] ; [25 – 150 phe]
Power density	10 mW / channel [AVG]	10 mW / channel [AVG]
Silicon die size	4.95 x 3.78 mm^2	≈ 20 x 20 mm^2
Operating Temperature	300 K	77 K – 300 K
Number of LVDS Tranceivers	8 (one for each column)	32 (one for each column)
LVDS Transceiver Speed	320 Mbps SDR or 640 Mbps DDR	320 Mbps SDR
Clock Frequency	310 -325 MHz	310 – 325 MHz
Power gating mode in low duty cycle	No	Yes

The SiPM Readout ASIC for GRAIN at DUNE

DUNE is a novel long-baseline accelerator neutrino experiment under construction in the USA, consisting of two detectors located 1300 km apart. **The Near Detector complex is located at Fermilab**, downstream the neutrino beamline, while the **far detector is hosted underground in the Sanford Facility in South Dakota**.
The GRAIN detector is a cryogenic LAr active target located inside the SAND apparatus at the Near Detector.

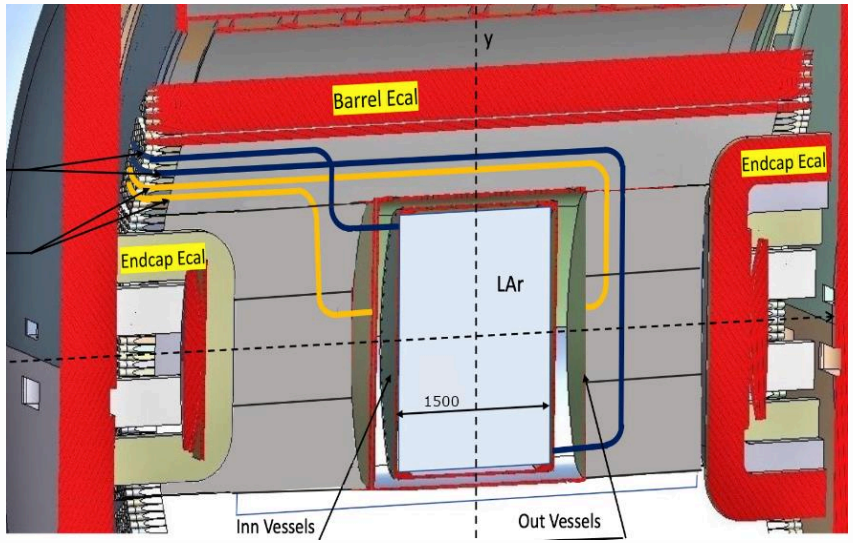
GRAIN is able to perform not only timing measurement and calorimetric charge measurement, but thanks to an optical focusing system, it can perform **track imaging** thus reconstructing the interactions of the secondary charged particles produced by the primary neutrino interaction.

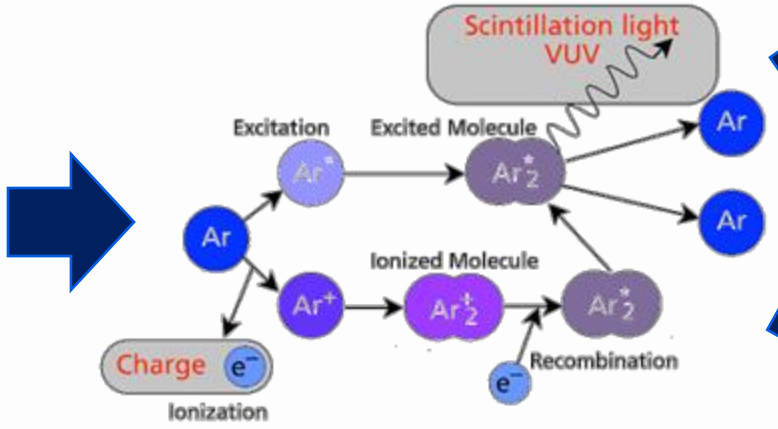


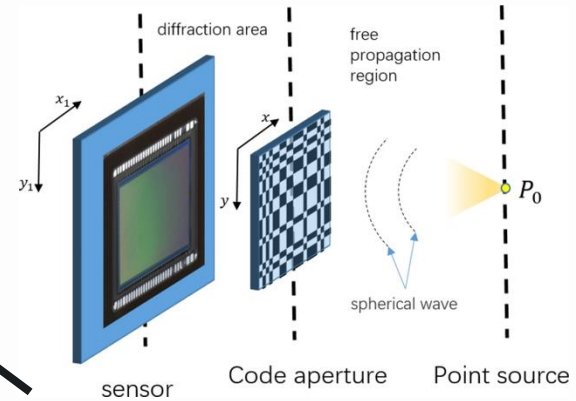


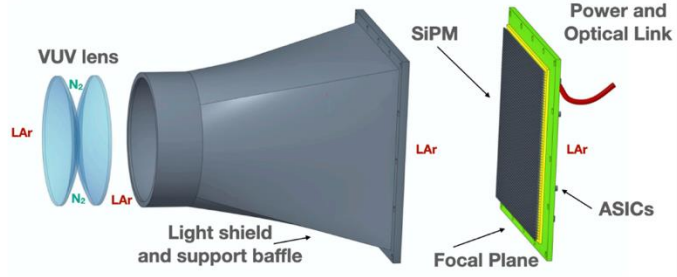
The SiPM Readout ASIC for GRAIN at DUNE

The liquid Argon active target is a **cryogenic vessel containing 1 ton of liquid Argon at 77 K.**
Ionizing charged particles are produced by weak interactions of the neutrino beam with the target.
The scintillation process of the liquid Argon **emits in the spectral region of VUV**, as a consequence of the decomposition of an Ar^*_2 excimer molecule.
INFN-Genova and INFN-Bologna are currently investigating two different techniques for focusing the VUV scintillation light: an approach based on **coded-masks** that maximize the active volume and a **solution based on N_2 lenses**, that reduces the photon absorption. **The scintillation light is focused on 32x32 SiPM pixel matrices.**







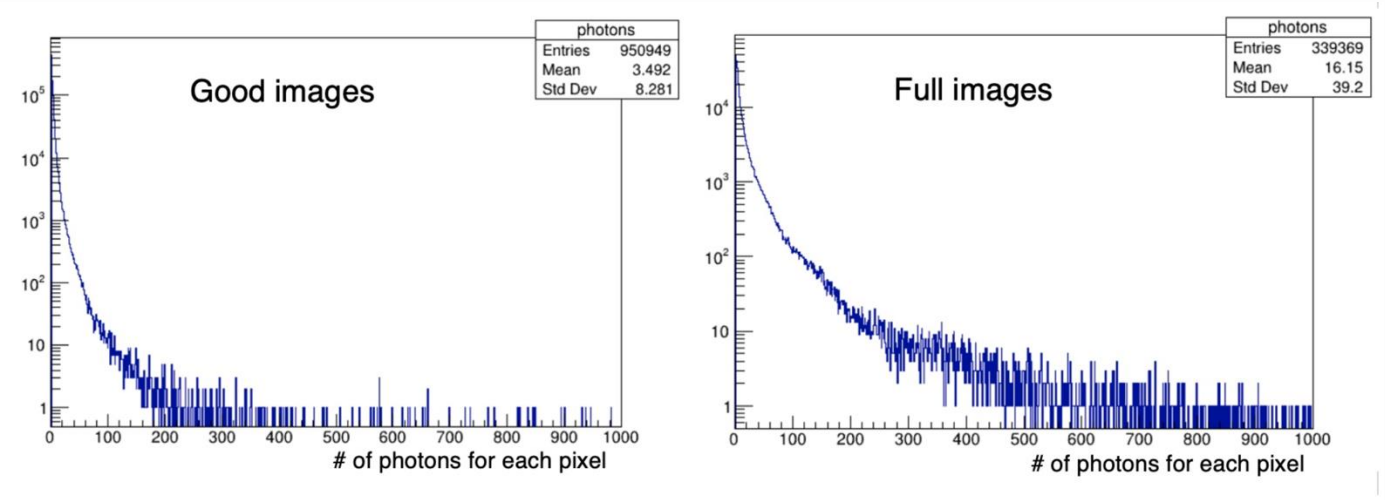


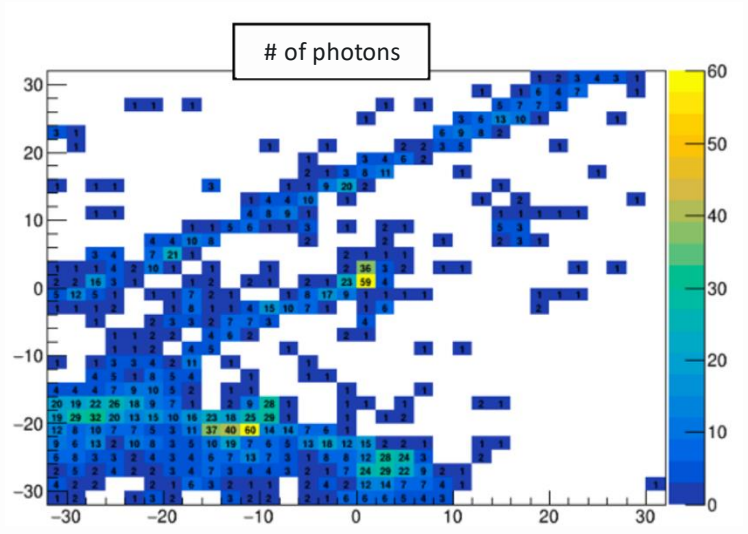
[1] Araujo, Gabriela Rodrigues. *Wavelength Shifting and Photon Detection of Scintillation Light from Liquid Argon*. 2019. *DOI.org (Datacite)*, https://doi.org/10.13140/RG.2.2.22656.79360
[2] VICENZI, MATTEO. *A GRAIN of SAND for DUNE: Development of Simulations and Reconstruction Algorithms for the Liquid Argon Target of the SAND Detector in DUNE*. Jan. 2023. *DOI.org (Datacite)*, https://doi.org/10.15167/VICENZI-MATTEO_PHD2023-01-20.

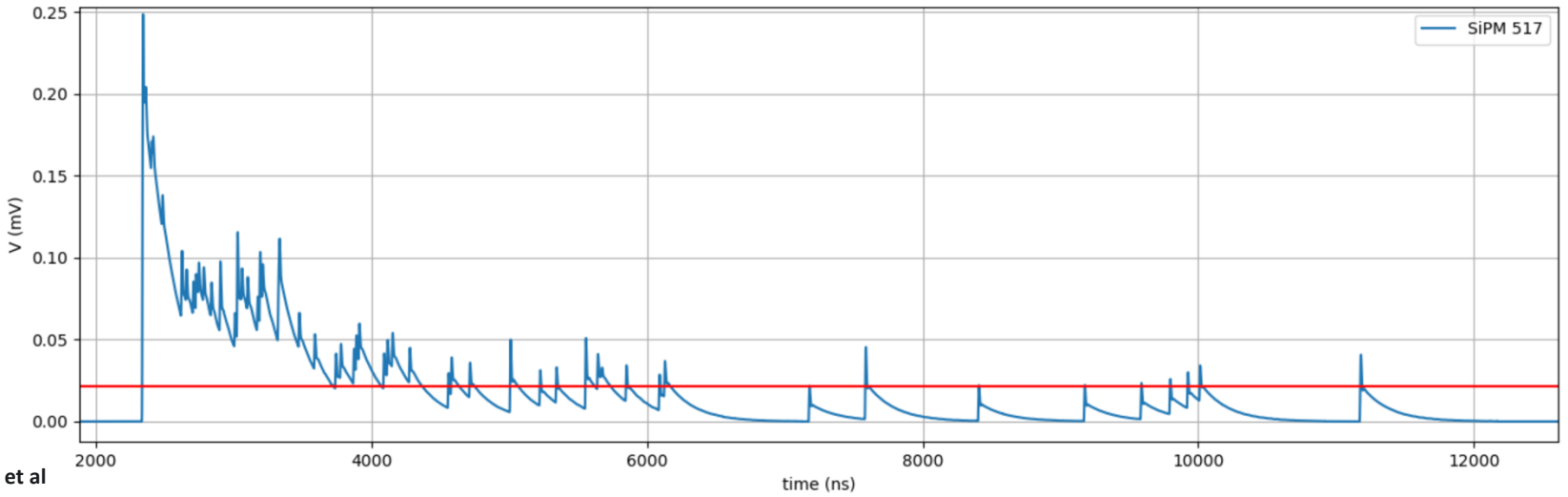
The SiPM Readout ASIC for GRAIN at DUNE

The signal produced by each SiPM has a complex structure, since it contains single photon pulses as well as pulses with a large number of piled-up photons. We are interested in:

- Detecting single photons (threshold = 0.5 phe)
- Timestamping the largest possible amount of events
- Minimizing the amount of charge that is not integrated and digitized.







Plots from "ASIC requirements for GRAIN optical detector readout" – A. Caminata et al

Requirements for the GRAIN ASIC

In such a complex signal, at the output of the TIA it is not possible to estimate the photon number using the Time-over-Threshold method, a charge integrator with single-photon resolution and large dynamic range is needed.

The average TDP needs to be limited to 5 mW / cm^2 to avoid phase transition in the liquid Argon. Very high channel density (1024 channel / chip) and different interfaces are needed.

The event dataframe is expanded from 32 bits to 64 bits in order to transmit also the integrated-charge information consisting of the ADC code and the analog integrator status flags.

It is more robust thanks to the Hamming Forward Error Correction.

Event Word

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32

Column ID	Channel ID	Gain ID	ADC ID	Charge Integral	Time-over-Threshold Counter
5-bit	5-bit	2-bit	2-bit	9-bit	9-bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Time Coarse Counter	Time Fine Counter	H.O.	Hamming FEC
15-bit	9-bit	1-bit	7-bit

Status Word

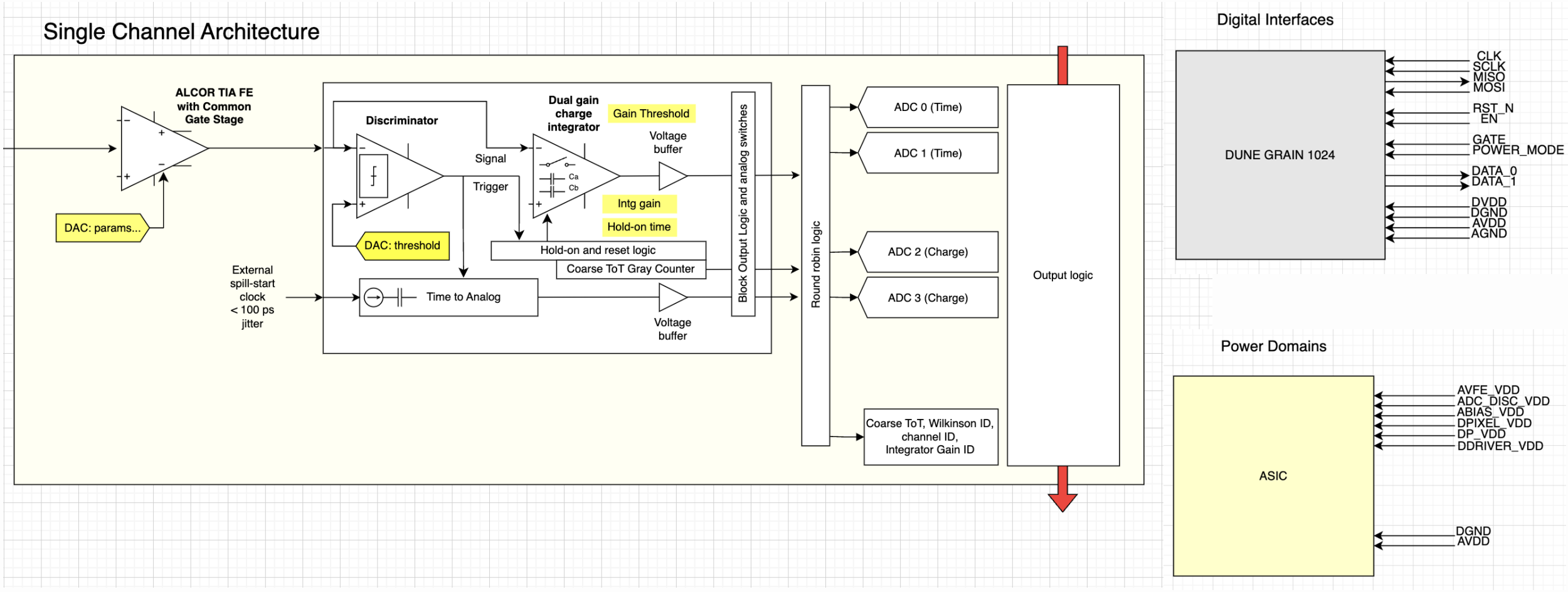
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Column ID	Channel ID	Lost Events Counter	Hold-on Merged Events Counter	SEU Counter	R.O.
5-bit	5-bit	7-bit	10-bit	4-bit	1-bit

Parameter	Value
SiPM Size	2 x 2 mm^2 (140 pF) 3 x 3 mm^2 (500 pF)
# Channels/ASIC	1024
Operating Temperatures	300 K – 77 K
<Power Consumption>	5 W / cm^2 ◊
Duty Cycle	On ≥ 9.6 µs (50 µs) Off ◊◊ < 0.1 s
Measurements:	Q - ToA - ToT
Integrator Dynamic Range	100 PE
RMS_{ToA} (first PE)	100 ÷ 150 ps / 1PE
RMS_{ToT}	≈ ns
Threshold	0.5 x 1PE
SNR	30

Bandwidth: 64b/event, 200 events/spill, >1 s spill+interspill period, ~15 kbps/pixel, ~480 kbps/column, **< 20 Mbps for 1024 pixels**

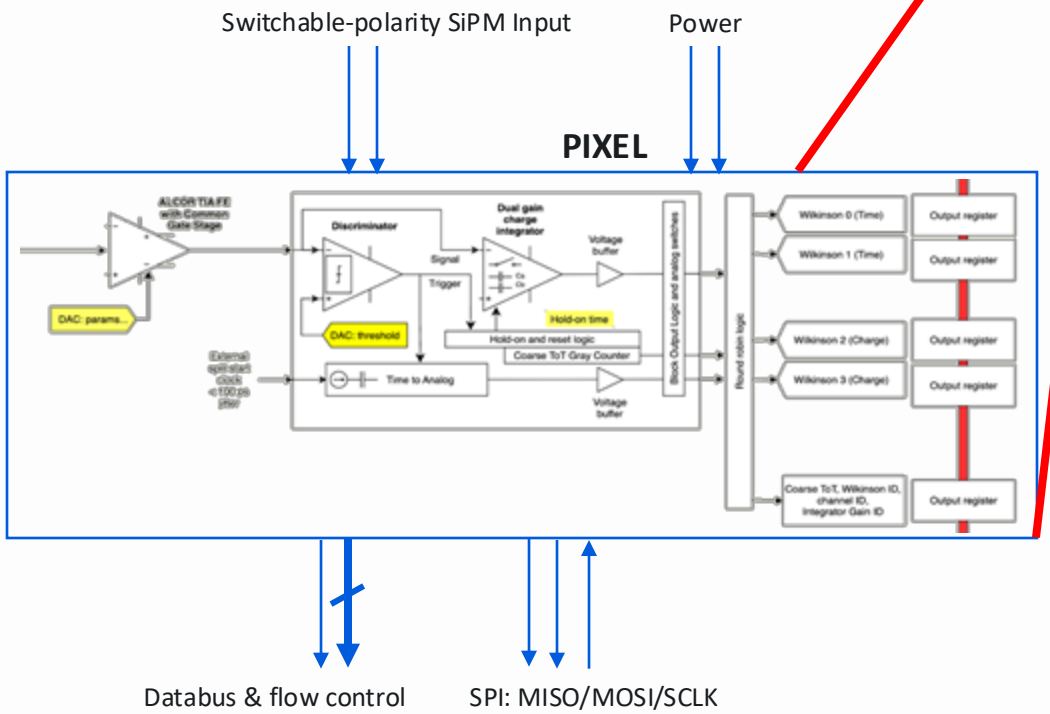
The GRAIN Readout ASIC: New Architecture

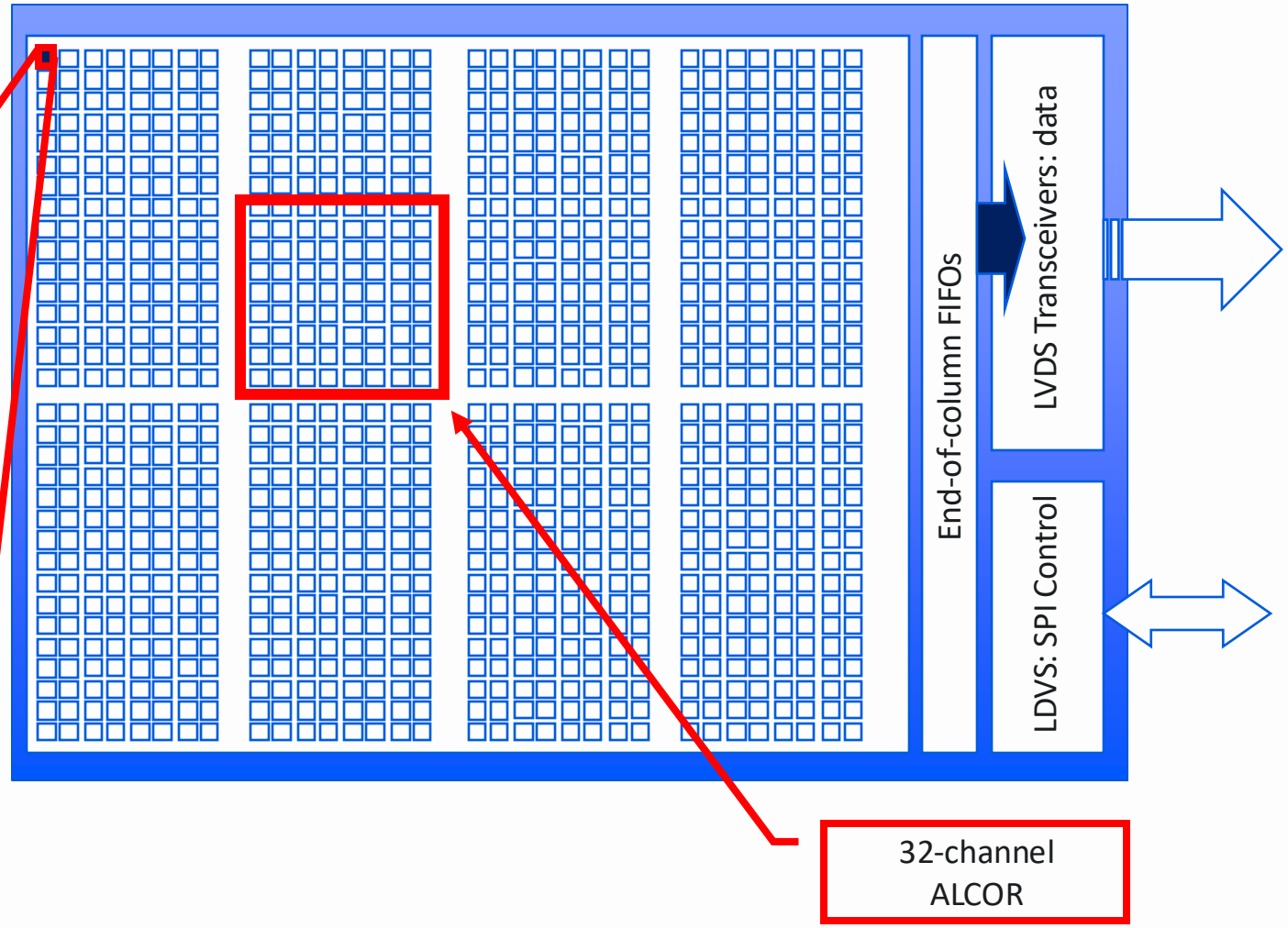


Preliminary!

The GRAIN Readout ASIC: New Architecture

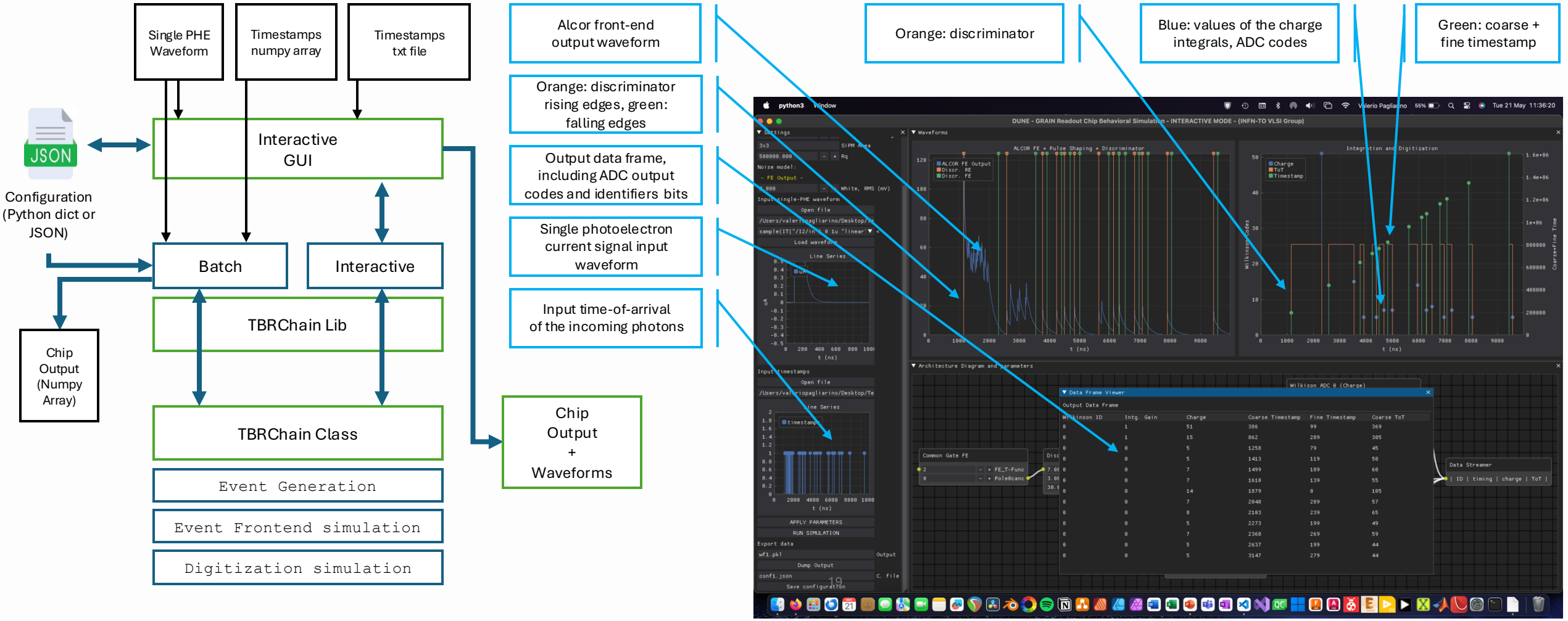
The architecture of the chip includes 1024 mixed-signal pixels capable of event timestamping, charge integration with programmable parameters using a SPI slow control channel.
Each columns is equipped with buffering FIFO memories and the chip has fast LVDS transceivers.





Behavioural Model for Architecture Validation

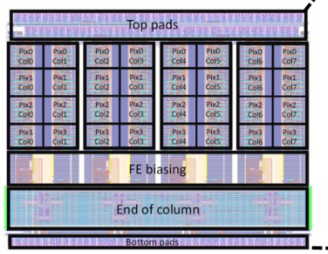
The software can work both in interactive mode with a GUI, or in batch mode for attempting reconstruction of a moderate number of events.



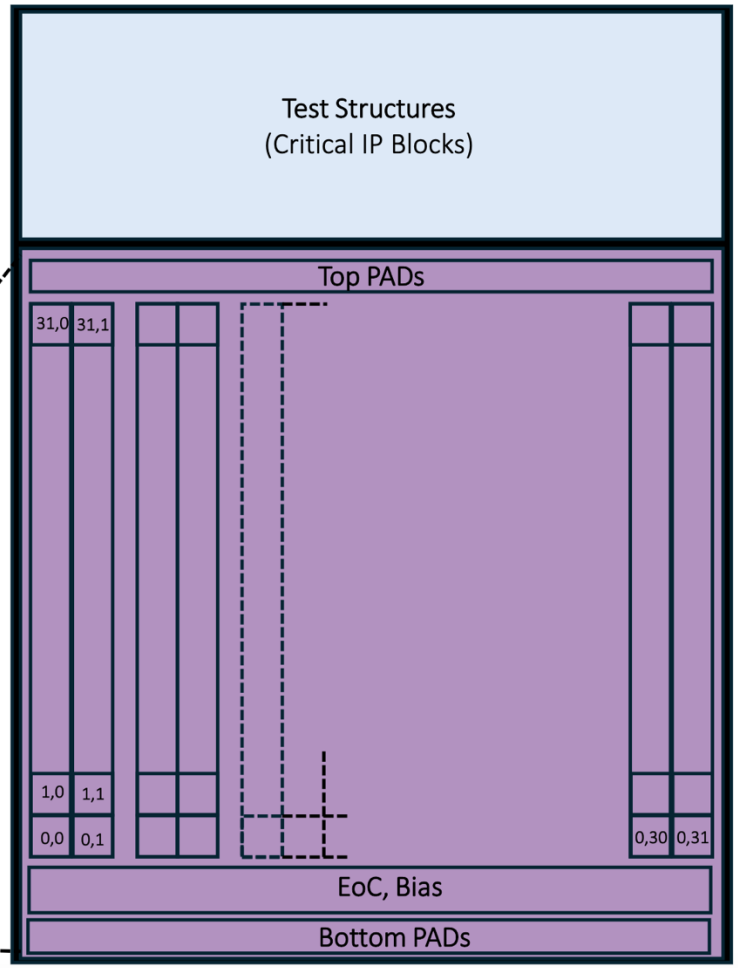
The GRAIN Readout ASIC: Floorplan

Courtesy of Stefano Durando

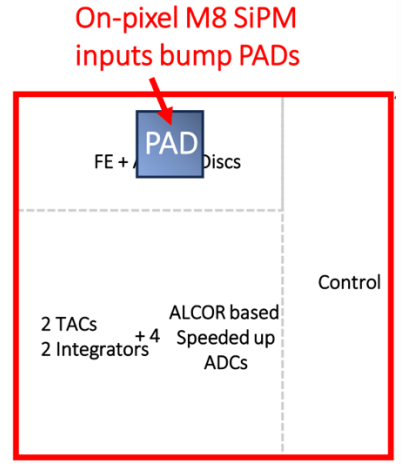
- ALCOR: 32 → GRAIN: 1024 channels = 32 x 32 pixels matrix
- Wafer reticle size : 20.340 mm x 31.840 mm
  - Safe circuit size < 20 mm x 20 mm
  - Hp: pixel channel pitch ≈ 500 µm
    → 32 x 500 µm = 16 mm + EoC, Biasing and PADFrame
- Advanced packaging techniques:
  - ASIC bump bonded to interposer for SiPMs and PCB board connection
    - On pixel PAD for SiPM
    - Inter-column supply and ground PADs to reduce IR drops
- Pin out under discussion:
  - Power Domains
    - 3 Analog + 3 Digital
  - Differential:
    - 1 Clk + 3 SPI
      + 1 trigger +2 Data
  - Single ended
    - 1 Reset + 1 Global_EN
      + 1 Low Power



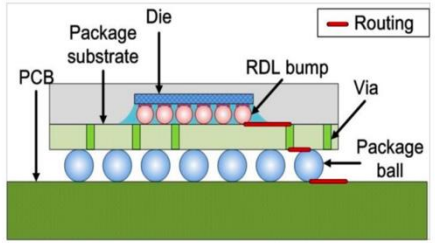
ALCOR v1



GRAIN ASIC



GRAIN ASIC : Pixel Channel

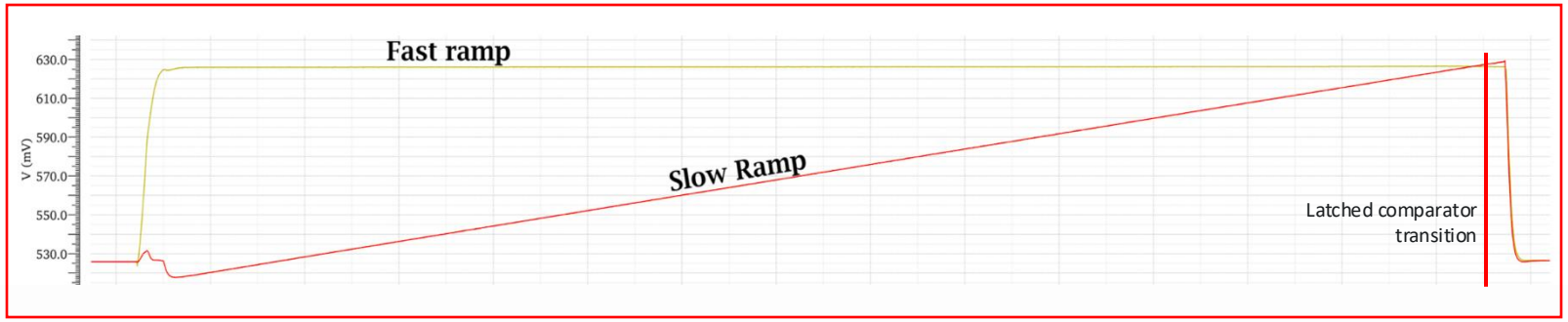


Flip-chip BGA working principle

Hsu, Hsin-Wu & Chen, Meng-Ling & Chen, Hung-Ming & Li, Hung-Chun & Chen, Shi-Hao. (2012). On effective flip-chip routing via pseudo single redistribution layer. 1597-1602. 10.1109/DATE.2012.6176727.

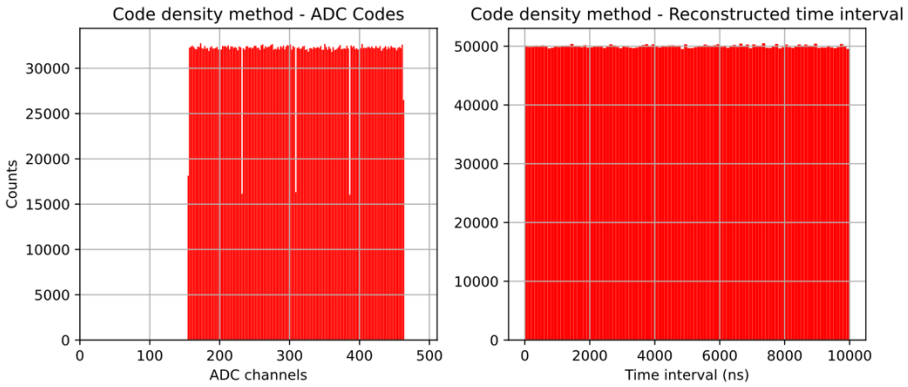
Time Digitization based on TAC + Wilkinson ADC

The Time-to-Digital converter inherited from the ALCOR chip is based on a high-precision current source that is steered to an integration capacitor when triggered by the asyncronous discriminator. The integrated charge is then digitized using a Wilkinson ADC.
The dead-time of the channel depends on the ADC code (up to 2^N with N = #bits, f_{clk} = 320 MHz) that is being digitized and it can be reduced using all the four TDCs in round-robin mode. **The conversion time of the Wilkinson ADC introduces an excessive dead time for the cameras of the GRAIN detector.**



$$T = T_{\text{coarse}} \cdot \frac{1}{f_{clk}} - T_{\text{fine}}$$

$$T_{fine} = \begin{cases} ADC_{fine} \cdot TDC_{time-binning}; & ADC_{fine} < ADC_{cut} \\ (ADC_{fine} - ADC_{cut}) \cdot TDC_{time-binning}; & ADC_{fine} > ADC_{cut} \end{cases}$$



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Event Word

Column ID	Channel ID	TDC ID	Coarse Counter	Fine Counter
3 bits	3 bits	2 bits	15 bits	9 bits

Status Word

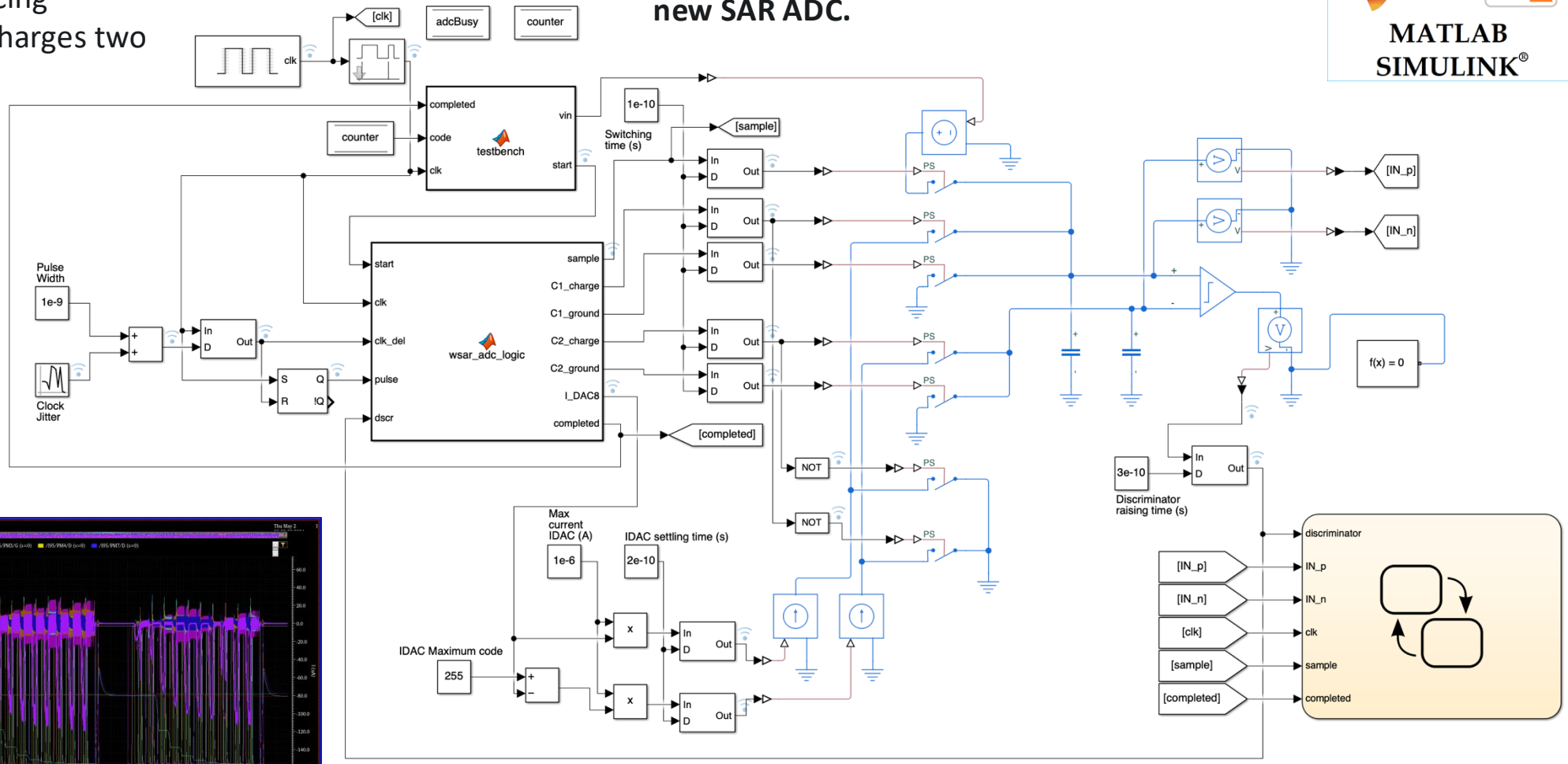
Column ID	Pixel ID	Lost event counter	Lost e.w. counter TDC1	Lost e.w. counter TDC2	Lost e.w. counter TDC3	Lost e.w. counter TDC4	SEU counter
3 bits	3 bits	6 bits	4 bits	4 bits	4 bits	4 bits	4 bits

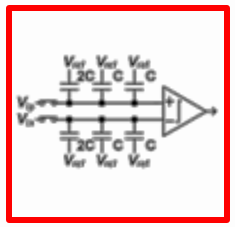
The GRAIN Readout ASIC: Faster ADCs

The new data converters for GRAIN uses a current-steering DAC producing accurate current pulses that charges two switched capacitors.
A the beginning of the conversion C_1 is tied to GND, While C_2 is charged at V_{IN}.
The system can be controlled by a faster SAR logic or by a back-compatible Wilkinson logic.
The current-steering architecture is fast and more silent compared to a switched capacitor SAR ADC.

Behavioral Mixed Signal Model of the new SAR ADC.

MATLAB SIMULINK®

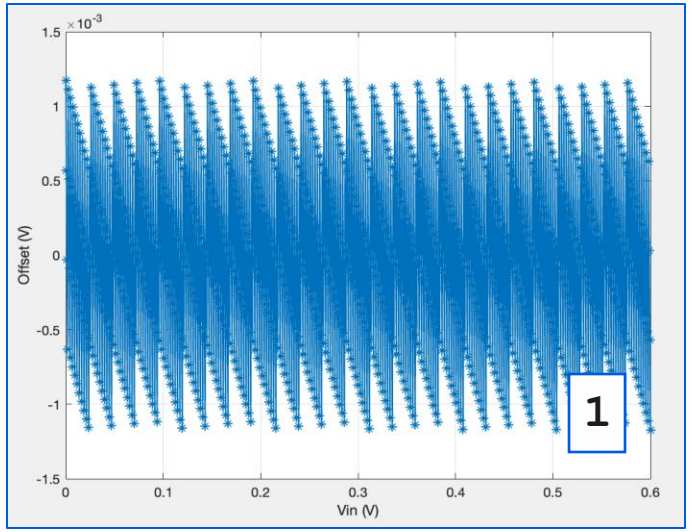


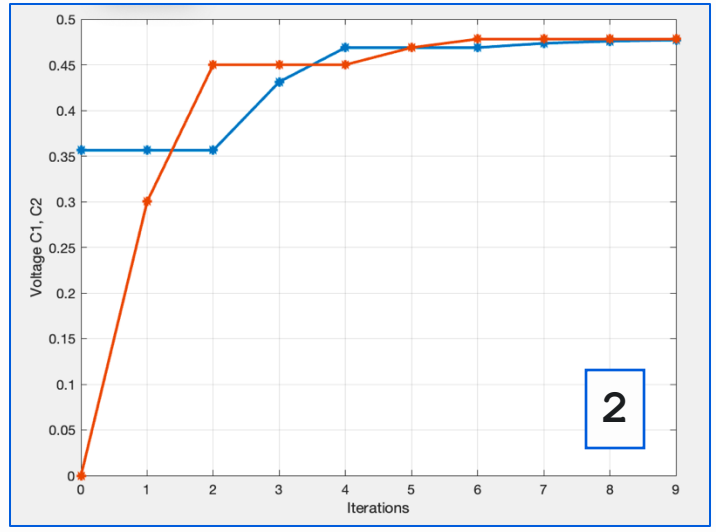


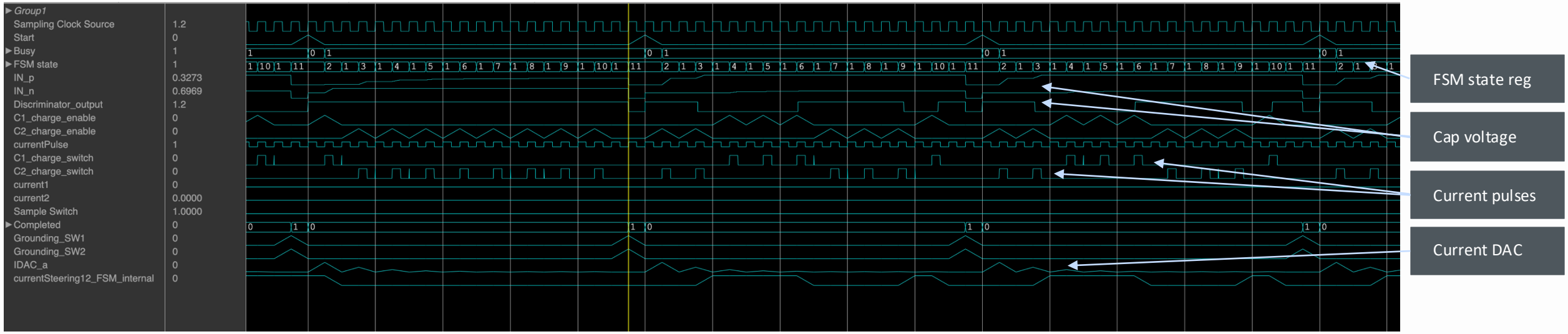
The GRAIN Readout ASIC: Faster ADCs

Results of the system-level simulations:

- [1] **Residuals** obtained converting values uniformly distributed in the dynamic range of the ADC. (Between 0 and 0.5 * Vdd)
- [2] **Example of single data conversion** for Vin = 0.475 V. The voltage across the two capacitors C1 and C2 is plotted against the number of iterations
- [3] **Time-domain simulation** of the digital control signals and of the analog voltages across the capacitors during conversion.







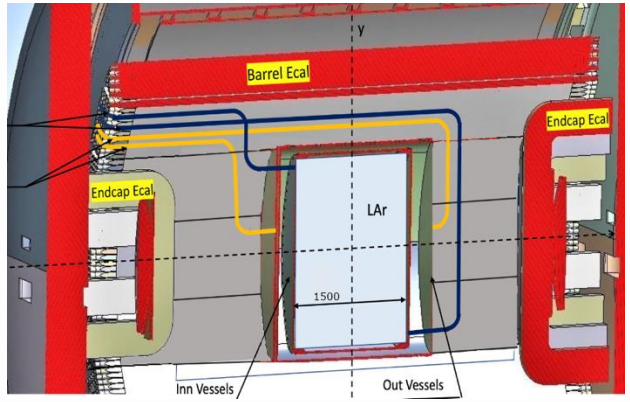
A synergic development of the ASIC for GRAIN & bRICH

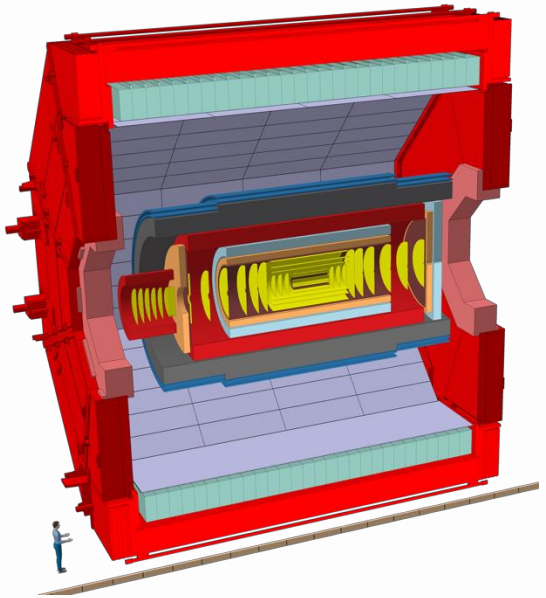
Even though the signal structure is very different in the Alice bRICH and in the GRAIN detector (very different duty cycle, dark count rate and bandwidth) after a careful examination it emerges that the modifications needed to adapt the GRAIN ASIC to the bRICH are limited:

- **Additional global-VETO signal**, with stochastic and deterministic jitter smaller than 100 ps and duration in the order of 1 ns.
- **Additional charge integration high-gain mode for performing photon counting by integrating only the peak** of the SiPM discharge signal
- **One LVDS transceiver for each column** operating at 320 MHz single data rate, instead of one per chip.

The set of features that will not be exploited by the bRICH is limited as well:

- **Power gating** for reducing the power consumption during the cryogenic operation
- **Integration of the whole SiPM discharge pulse** with bilinear response
- **Two 32-pixel columns unused**, that can be disabled via the slow control interface to reduce the power consumption



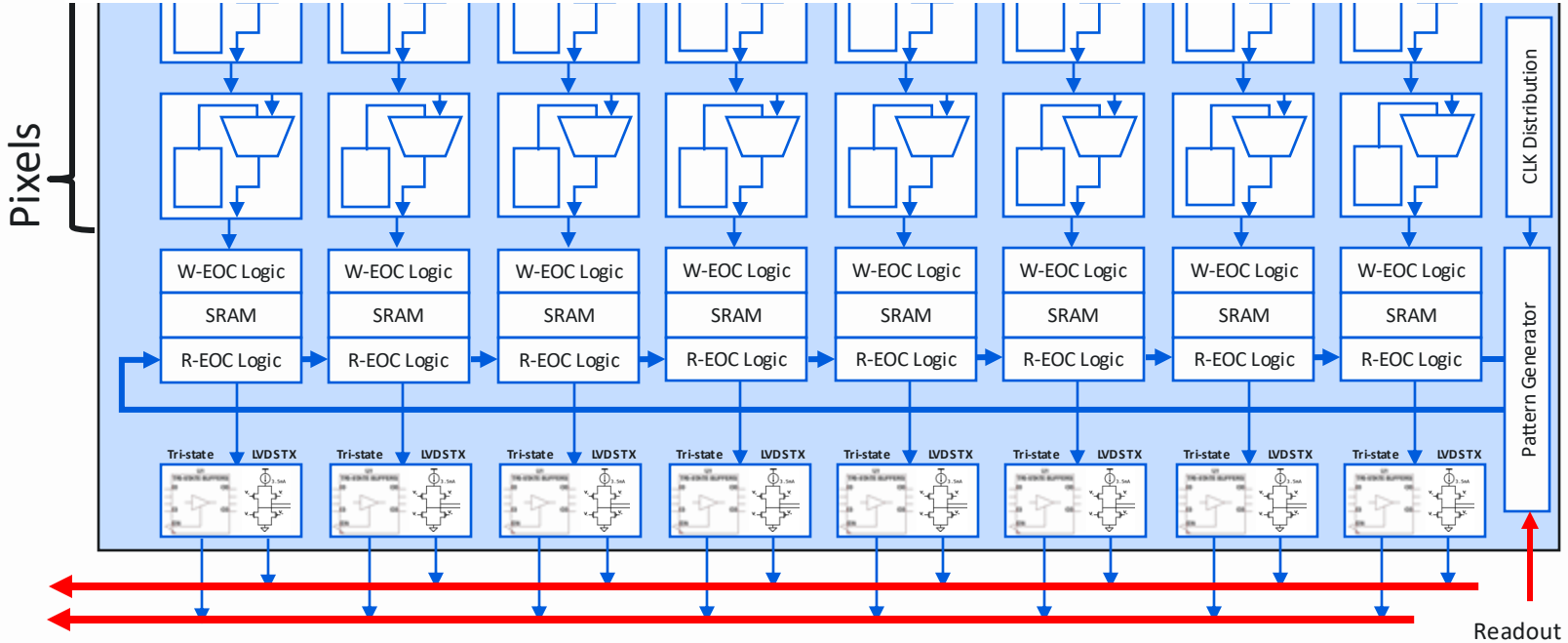


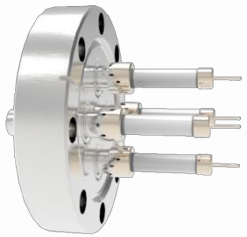
A synergic development of the ASIC for GRAIN & bRICH

Tri-state LVDS Transceivers

Because of the high dark count rate per pixel (about 4 MHz at the end-of-life of the detector) the bRICH readout ASIC requires a relatively high data transmission bandwidth.
On the contrary, in the GRAIN detector at DUNE the number of LVDS lines should be strongly limited because of the complexity of the flanges installed for crossing the cryostat walls.

These two constraints can be satisfied simultaneously by implementing tri-state LVDS transceivers that can operate with programmable time-division multiplexing of the access to LVDS link.





In the GRAIN detector the number of LVDS feedthrough in the cryostat must be limited!

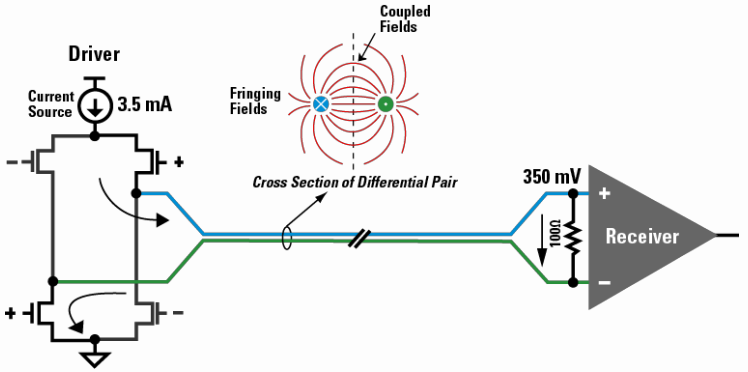
- Very high cost of high-speed connectors
- Load for cryocoolers

Alice bRICH

GRAIN-DUNE

Link aggregation:

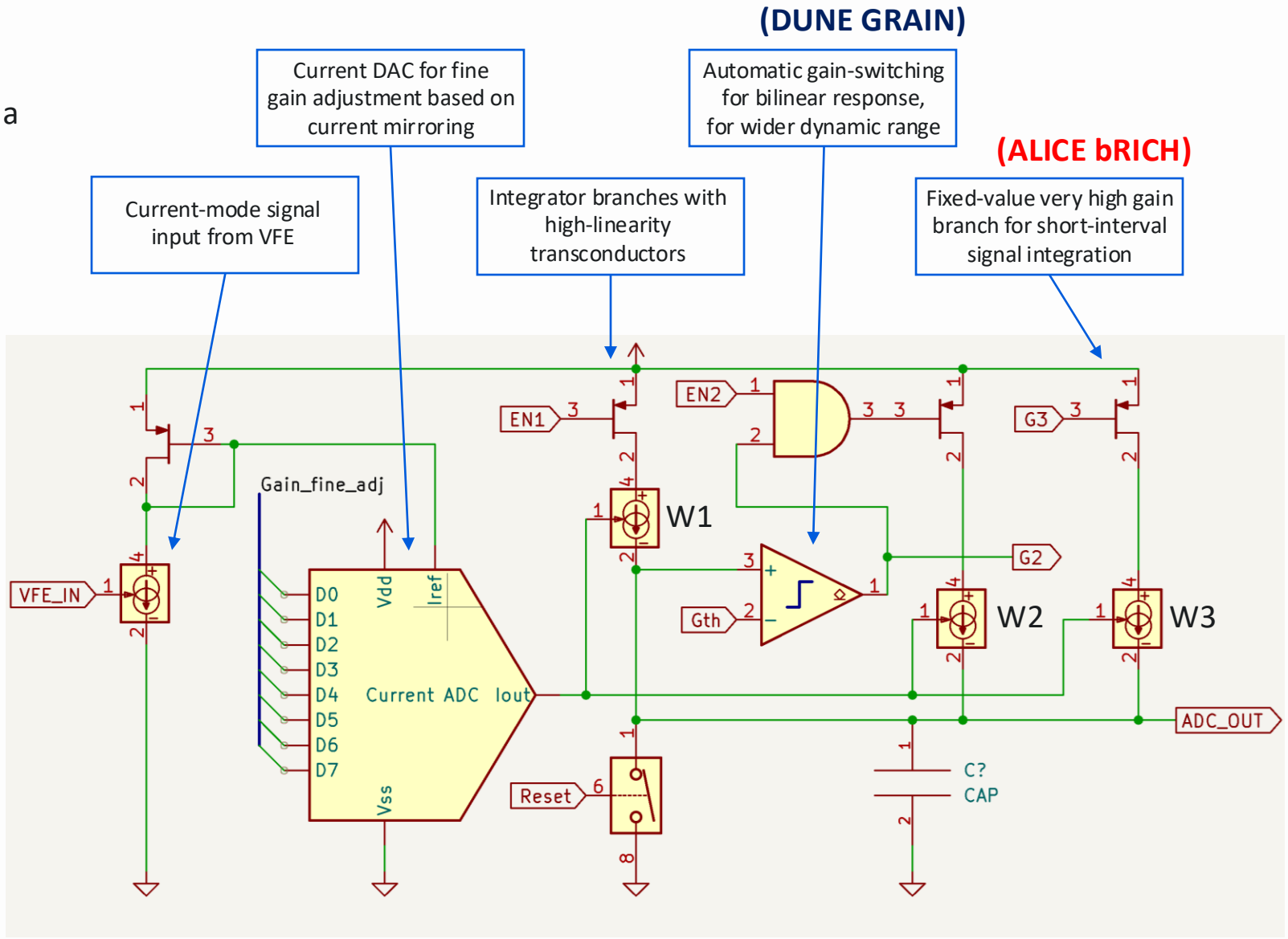
- MAX: 28 LVDS channels: 320 Mbps / column (28 c)
- MIN: 1 LVDS channel: 10 Mbps / column (32 c)



Charge Integration

The GRAIN ASIC features a charge integration with a current-mode input coming from the regulated common-gate very frontend stage.

- After being adjusted by a programmable DAC based on current mirrors for precisely tune the gain, the signal is integrated on a capacitor charged by an array of transconductors.
- When the voltage across the capacitor increases above an adjustable threshold, some transconductors are disabled in order to reduce the gain following a bi-linear response, thus widening the dynamic range.
- In the ALICE-3 bRICH these features are not exploited, instead, a fixed branch is used witch a much higher gain, in order to match the ADC input dynamic range, with a very fast integration gate.

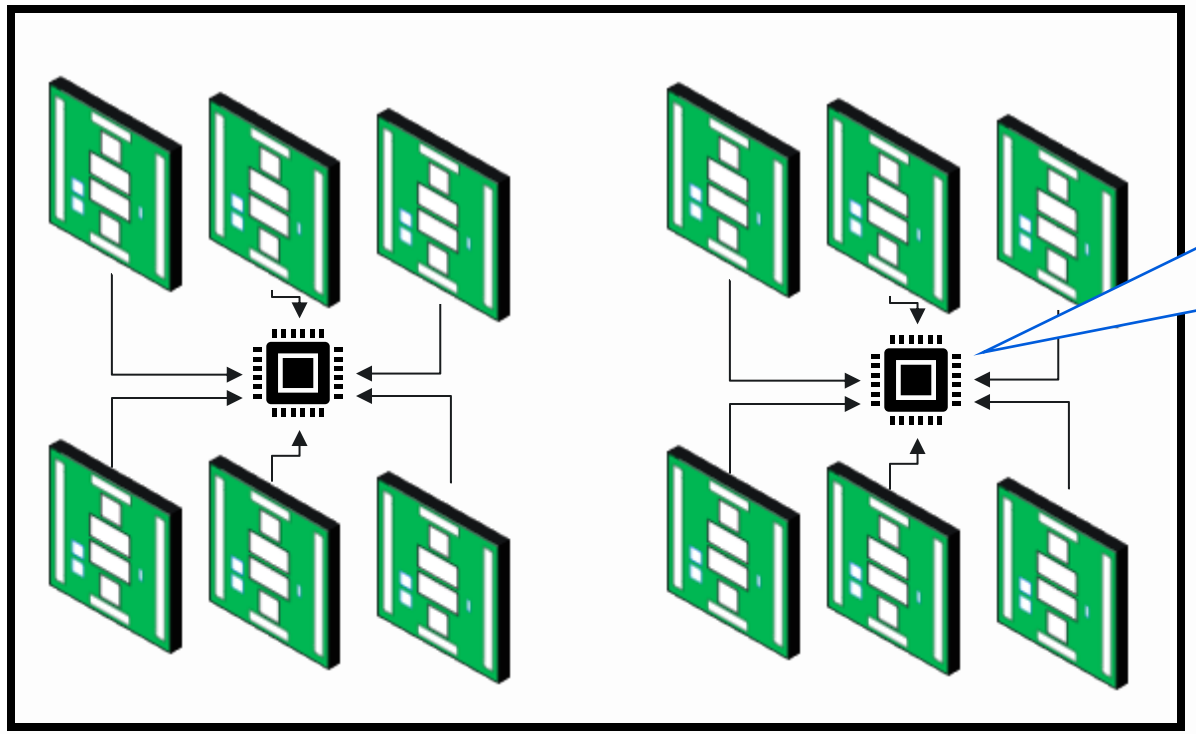


Alternatives Approaches for high DCR: selective readout

An alternative solution is to introduce an additional ASIC between the lpGBT transmission links and the readout ASIC, with the role of clustering the time-of-arrival measurements, discriminating the dark count an forwarding to the counting room only the meaningful data. This introduces an additional cost and it is difficult to optimize the modularity of this data concentrator in order to avoid an additional communication bus between data concentrators, considering the distribution of the rings of Cherenkov light. In alternative, a distributed ToA histogram can be computed and then the RX link of the lpGBT can be used to request a selective readout to the ASICs. In this case the complexity and the latency increase considerably, therefore much larger on-chip SRAMs are needed.

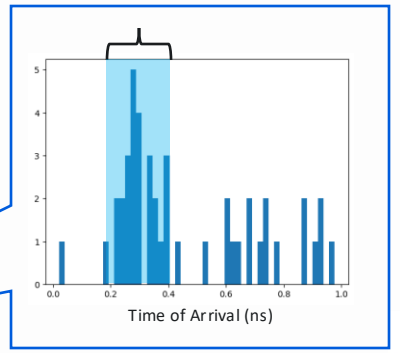
Dedicated data-concentrator ASIC for selective readout

Additional high-bandwidth ASIC required, difficult to find a modularity that allows the clustering of the timestamps without inter-chip communication.

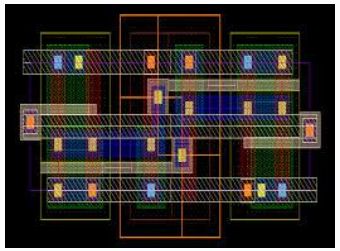


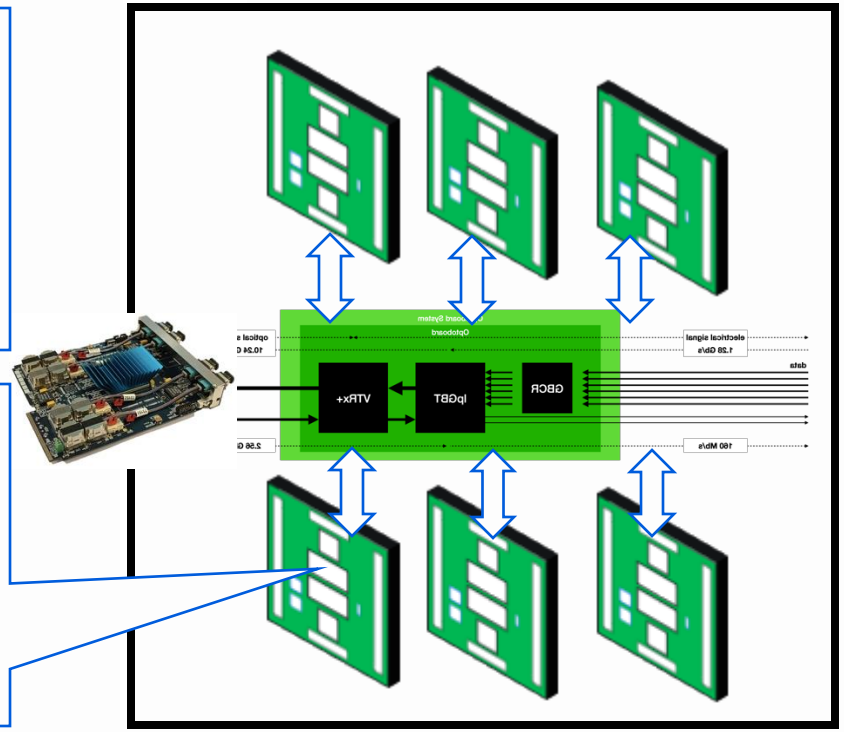
Clustering and then selective readout requested through the lpGBT RX channel

Very large amount of SRAM memory needed inside the ASIC for buffering the events



On-chip SRAM





Conclusions

The Alice-3 bRICH is a challenging system because the very high DCR of the SiPMs, requiring up to 7 – 10 Tbit/s of readout bandwidth from the detector to the counting room. The system is bandwidth-limited and, ultimately, limited by the response time of the sensors.

The shaping time, signal processing time and data conversion time of the pixels inside the readout ASIC with proper derandomization buffers and VETO gates can withstand the event rate.

The 1024-channel ASIC currently being designed in Torino for the GRAIN detector at DUNE, with relatively small modifications, can therefore fit the application if the DCR estimation of 4 MHz is realistic.
The synergy could represent a great opportunity for reducing the cost, reducing the development risks and increasing the chip functionalities and performance, as a consequence of the additional resources.