ALICE 3 RICH FEE preliminary module concept

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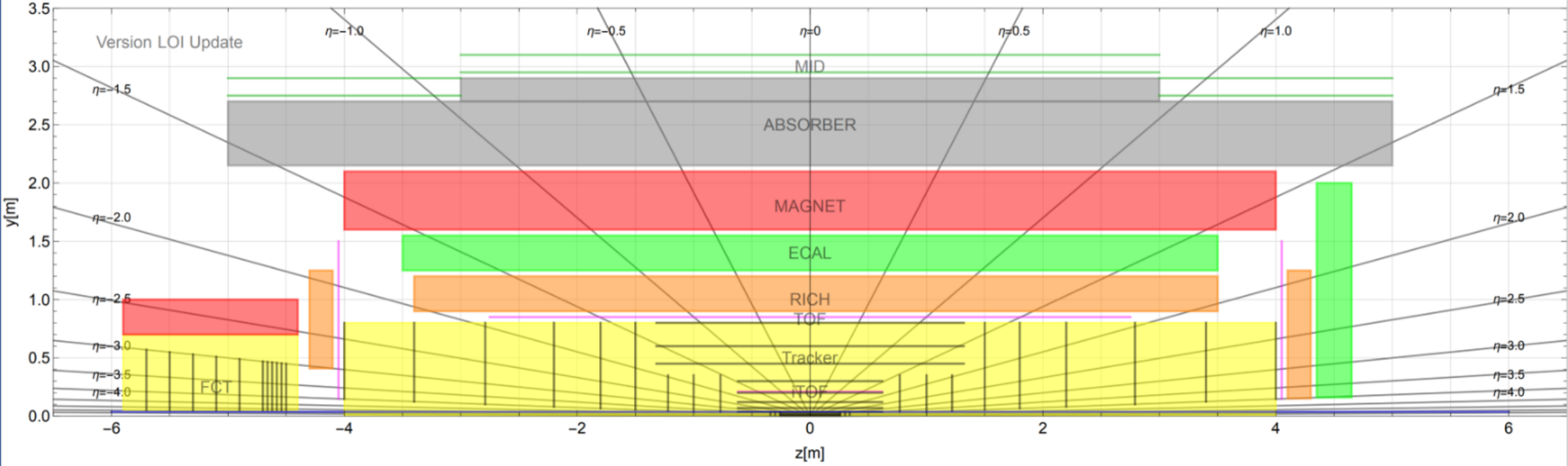
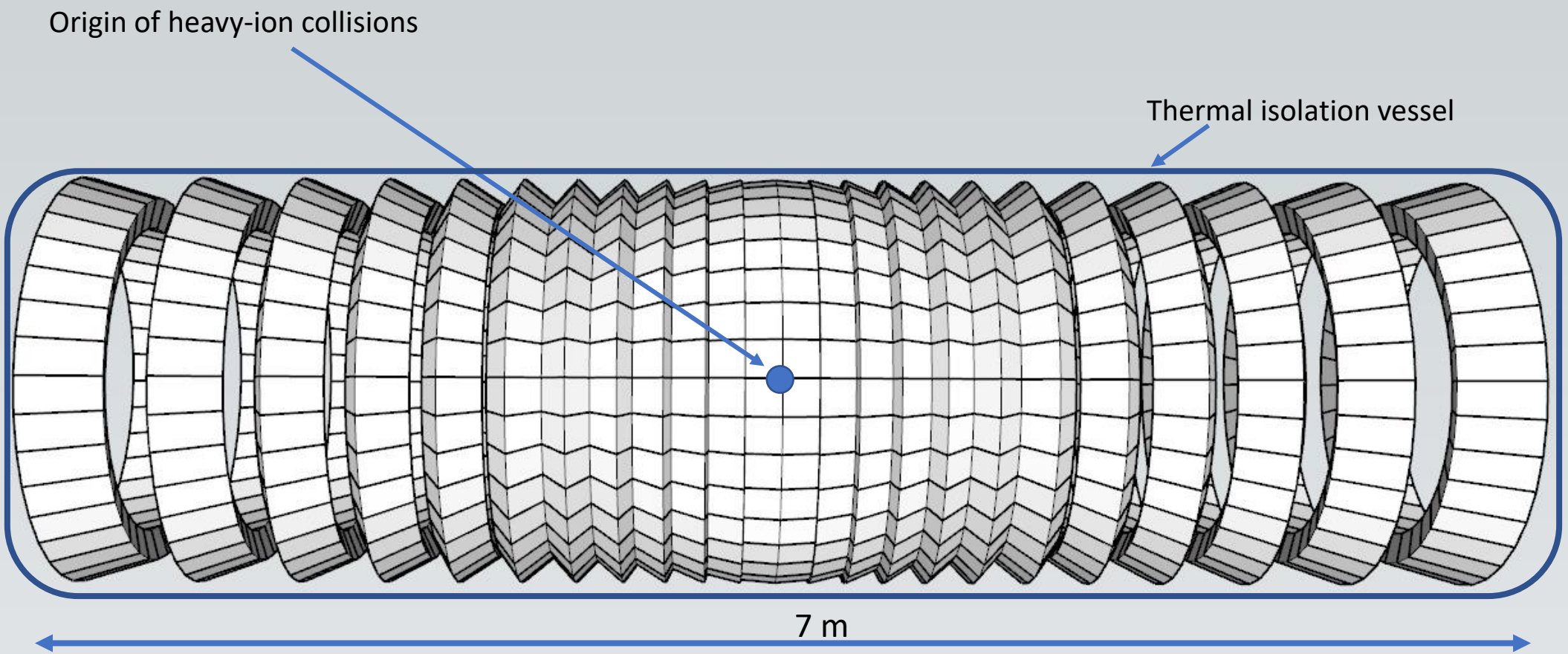
On behalf of the ALICE-3 RICH Group

ALICE current system layout dimensions



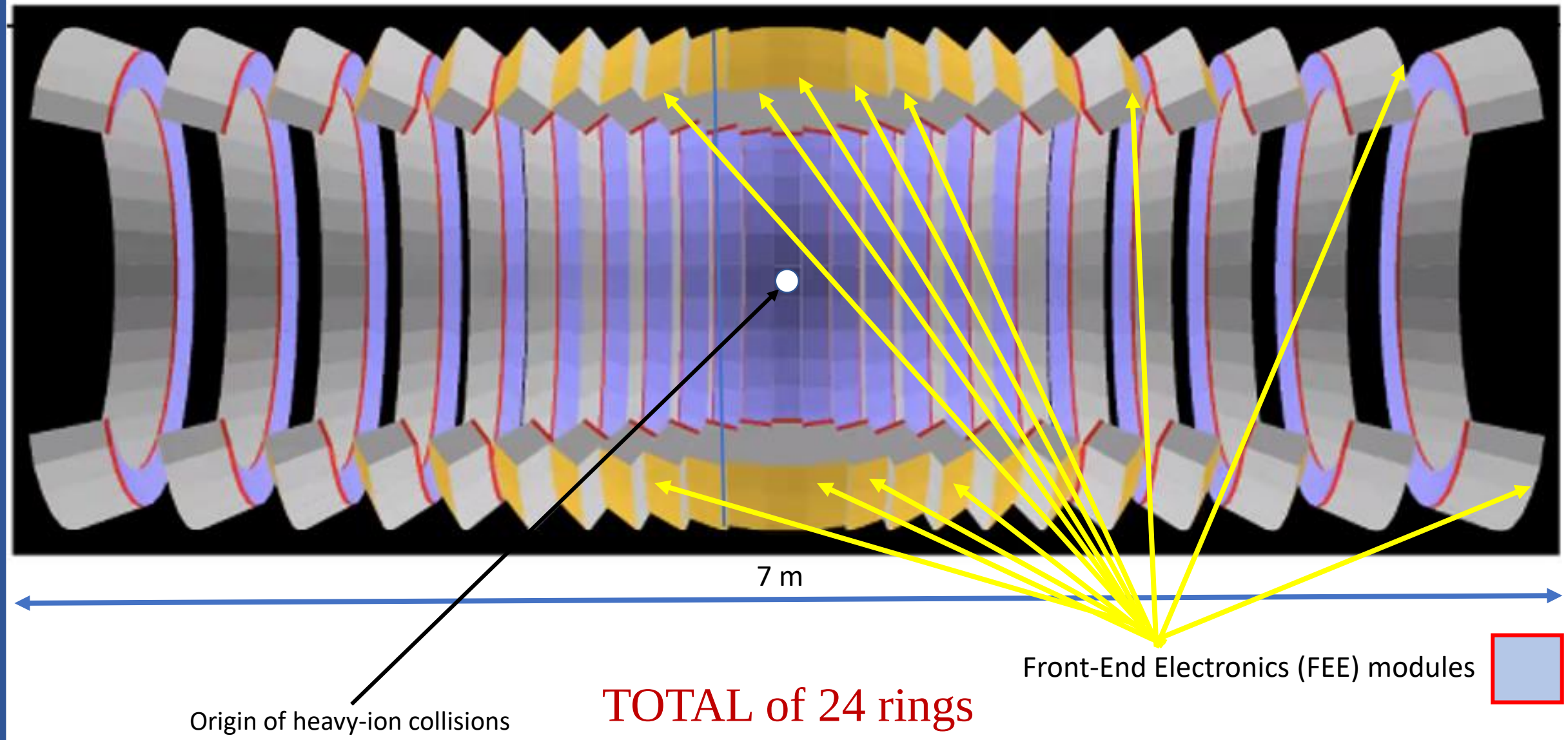
RICH barrel



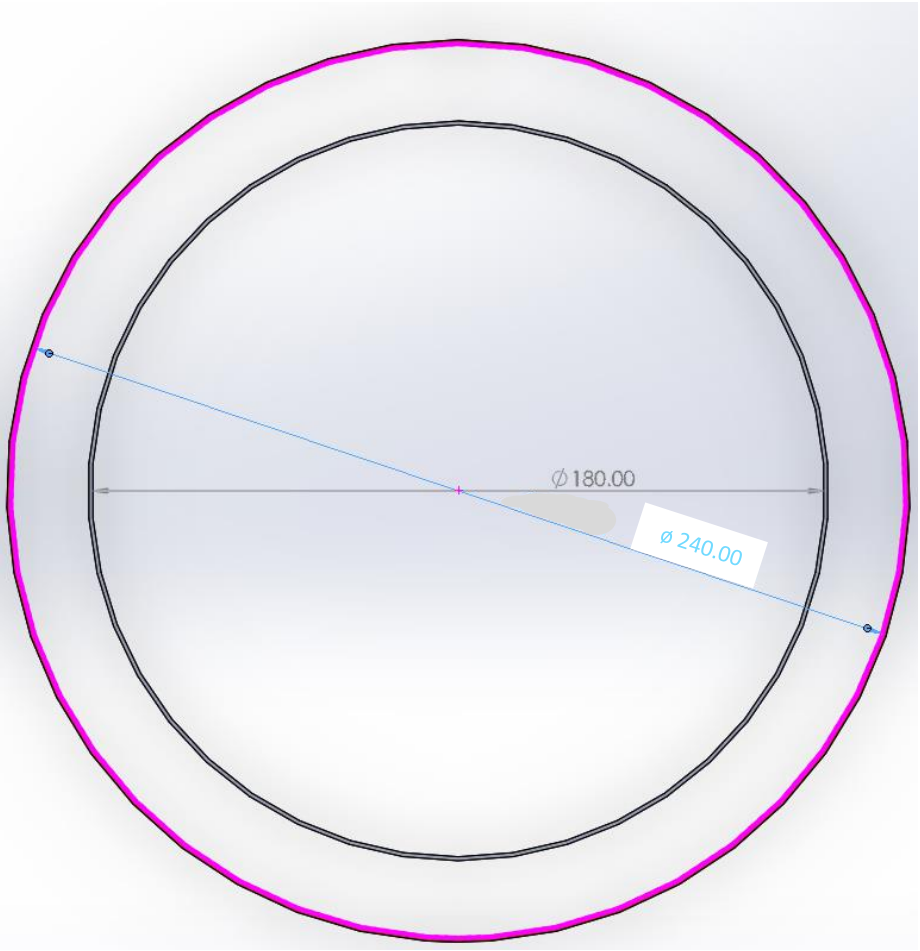
TOTAL of 24 rings: each with 36 segments (with dimensions of 15 x 20 cm^2 perpendicular to the particle beam)

The first approach for front-end electronics proposed is modular, 4-side tileable, forming FEE “super-modules”, placed on and completely filling each of the 36 segments (with an approx. area of 15 x 20 cm^2) per ring, each placed perpendicularly to the origin of heavy-ion collisions.

RICH proposed system layout

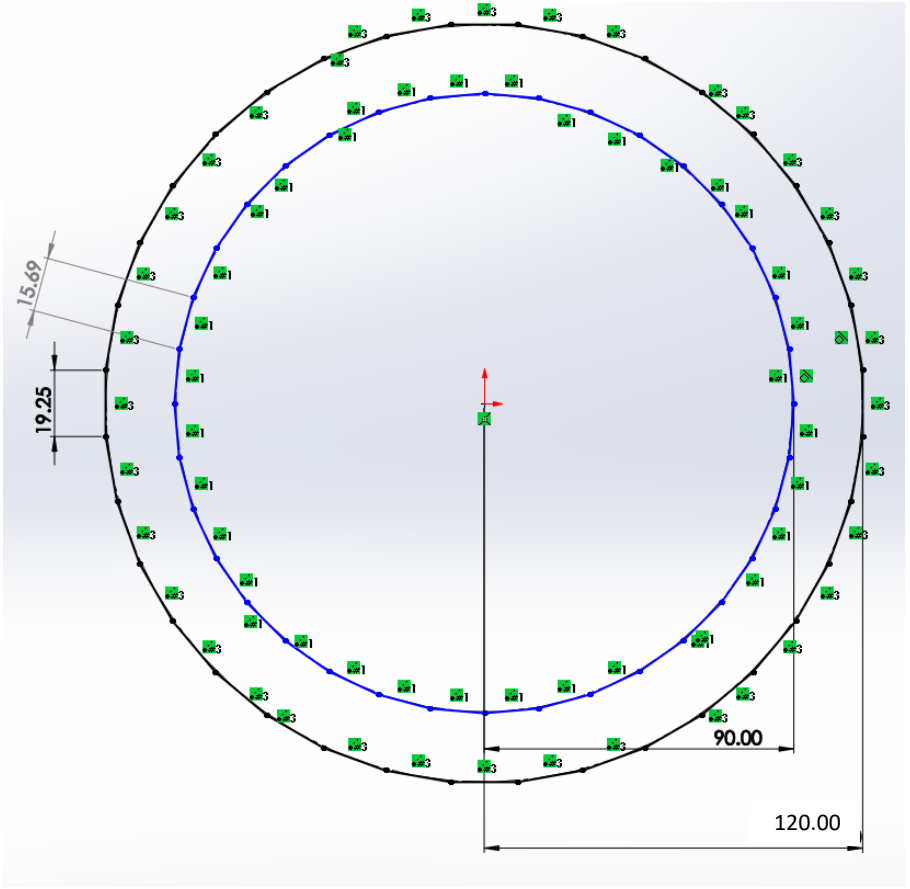


RICH Space Dimensions

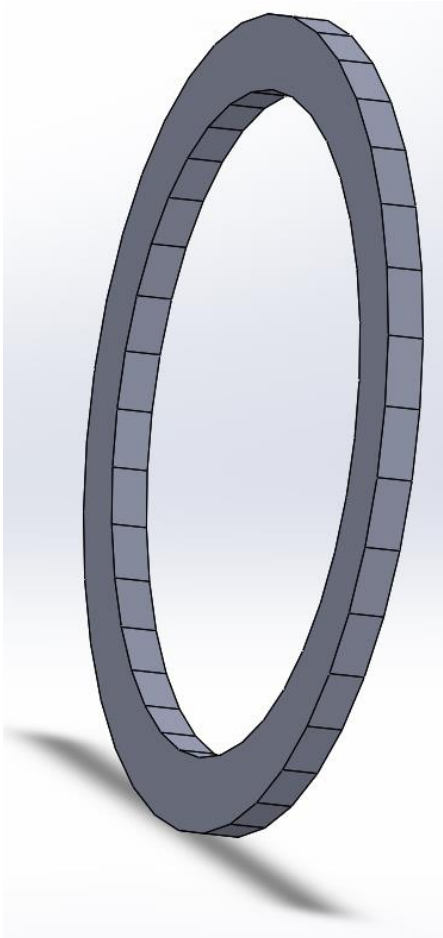


Barrel dimensions: Radius 90 cm to 120 cm
Space in between: 30cm

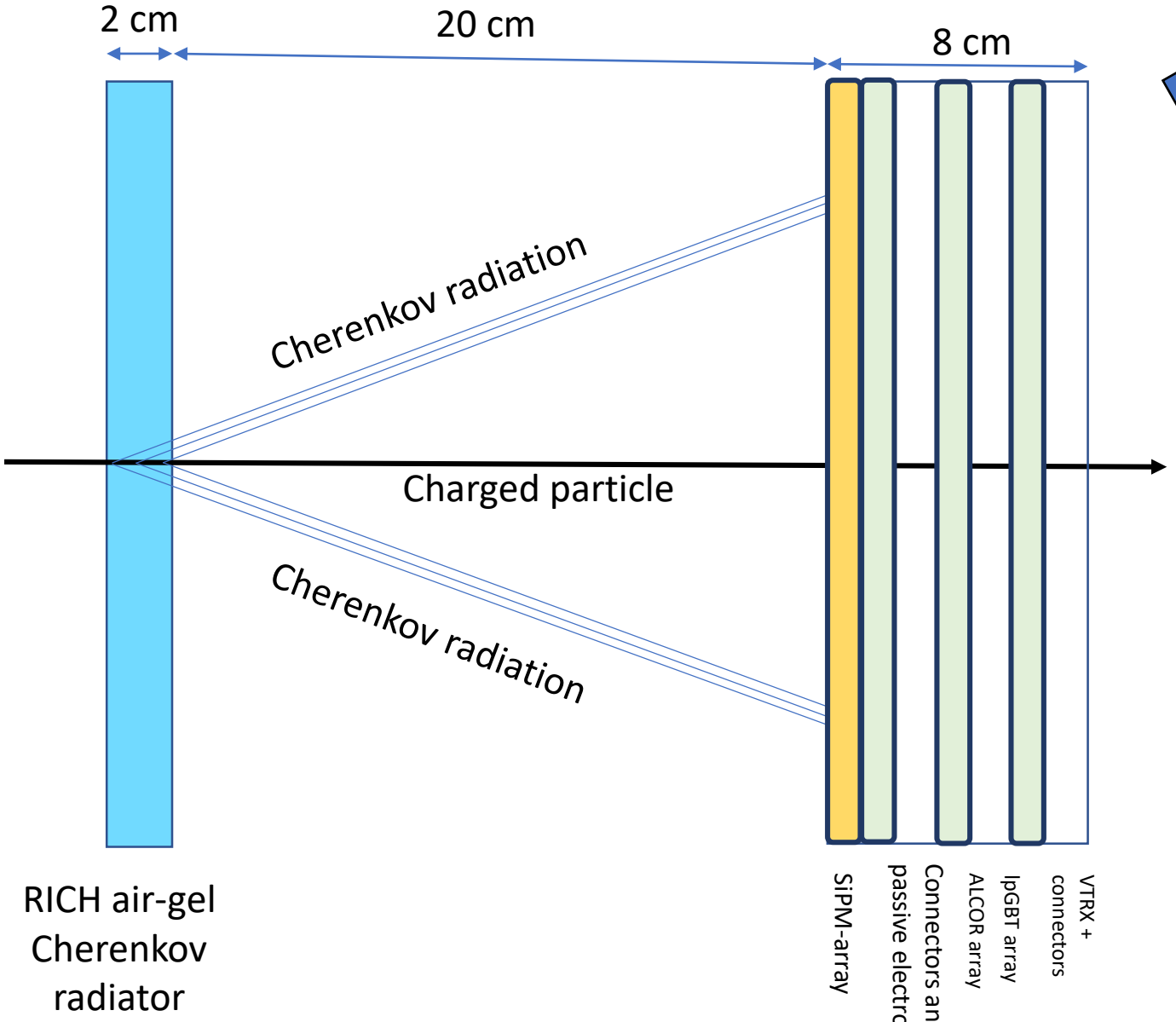
Ring 0

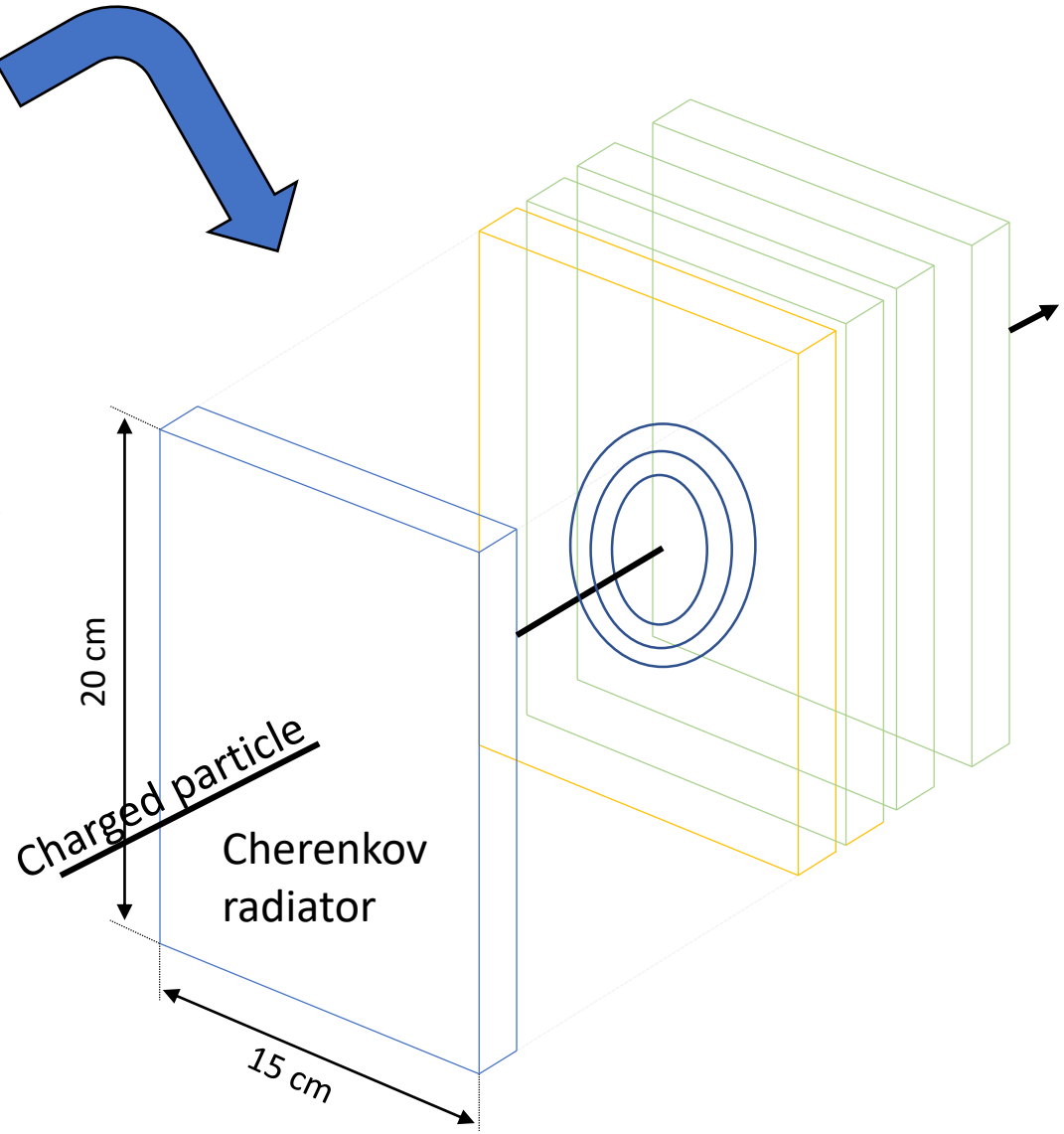


The ring consists of 36 segments
Goal dimension specification for the 36 segments (super-modules) per ring: 15 x 20 cm^2

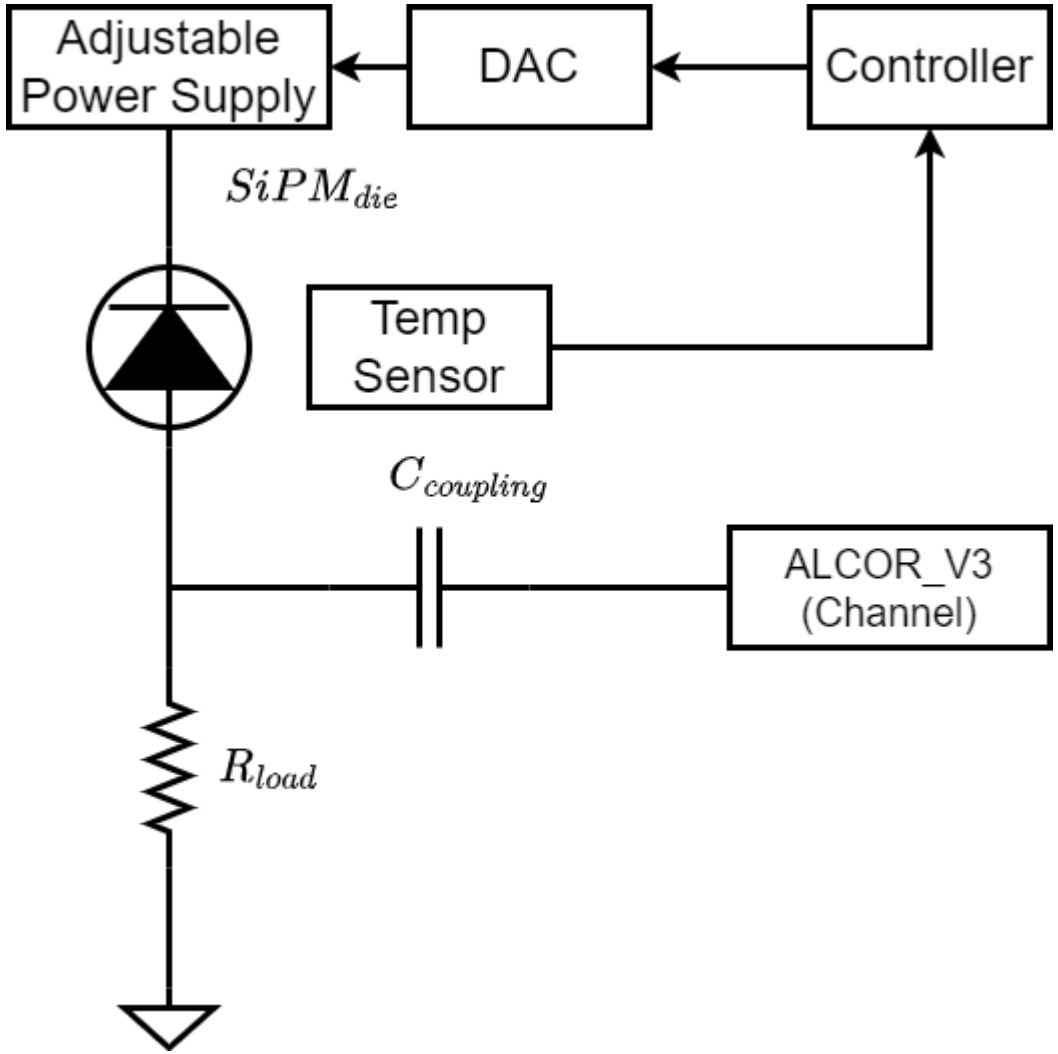


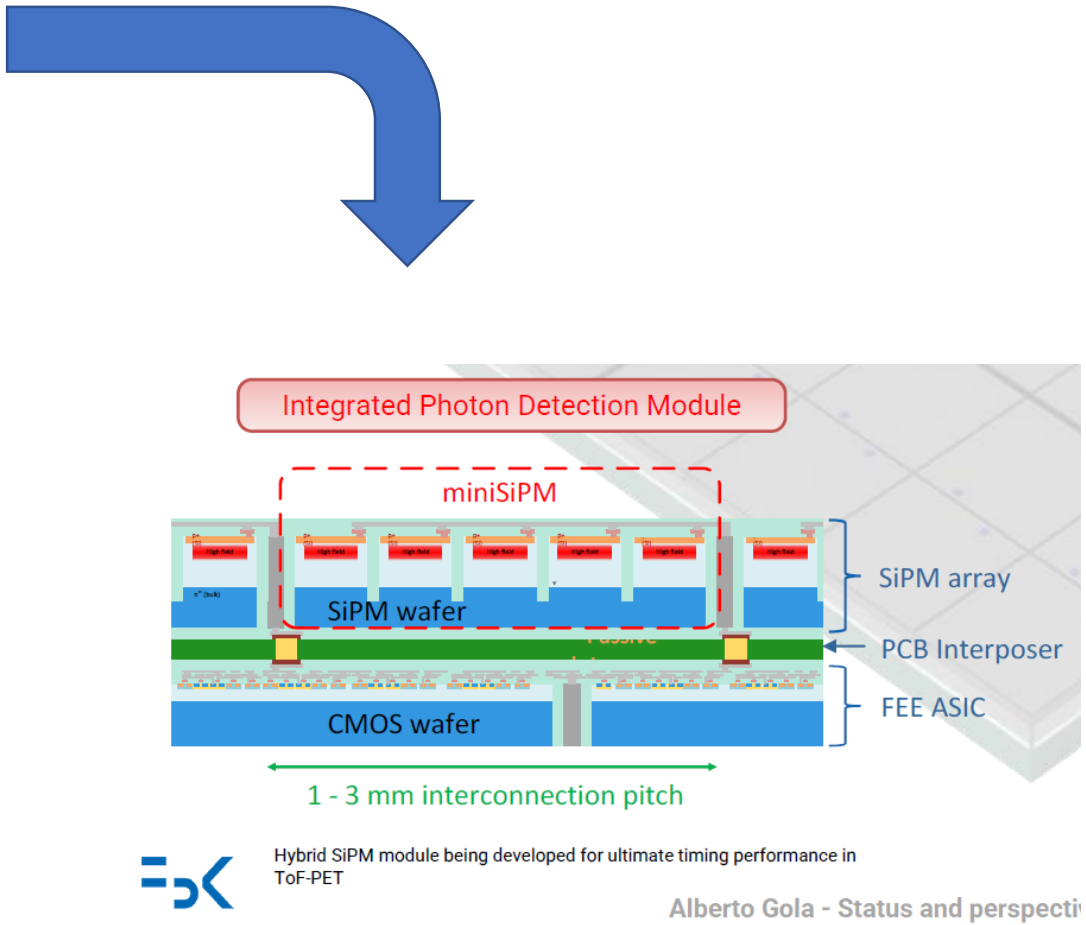
RICH FEE Functional Diagram





ALICE-3 RICH FEE: SiPM array





Source: Alberto Gola, “Status and perspectives of SiPMs at FBK”, CERN, 2023

Fig. 2: SiPM die and ALCOR V3 general connection with temperature sensor.

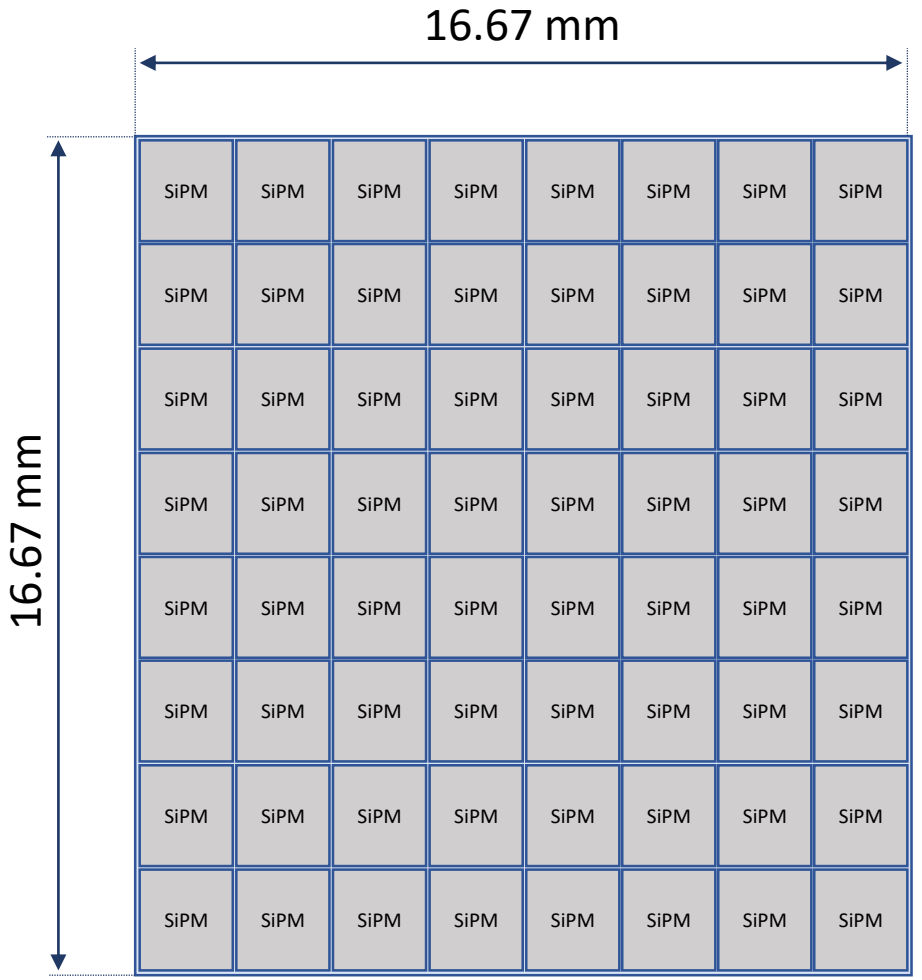
ALICE-3 RICH FEE: Preliminary Assembly Proposal

The proposed modular assembly includes:

- a **SiPM-tile**, which comprises an array of 8 x 8 SiPMs → **64 SiPM channels**
- a **SiPM-module**, constituted by 3 x 3 SiPM-tiles → **576 SiPM channels**
- a SiPM **super-module** made up of 3 x 4 SiPM-modules → **6,912 SiPM channels**

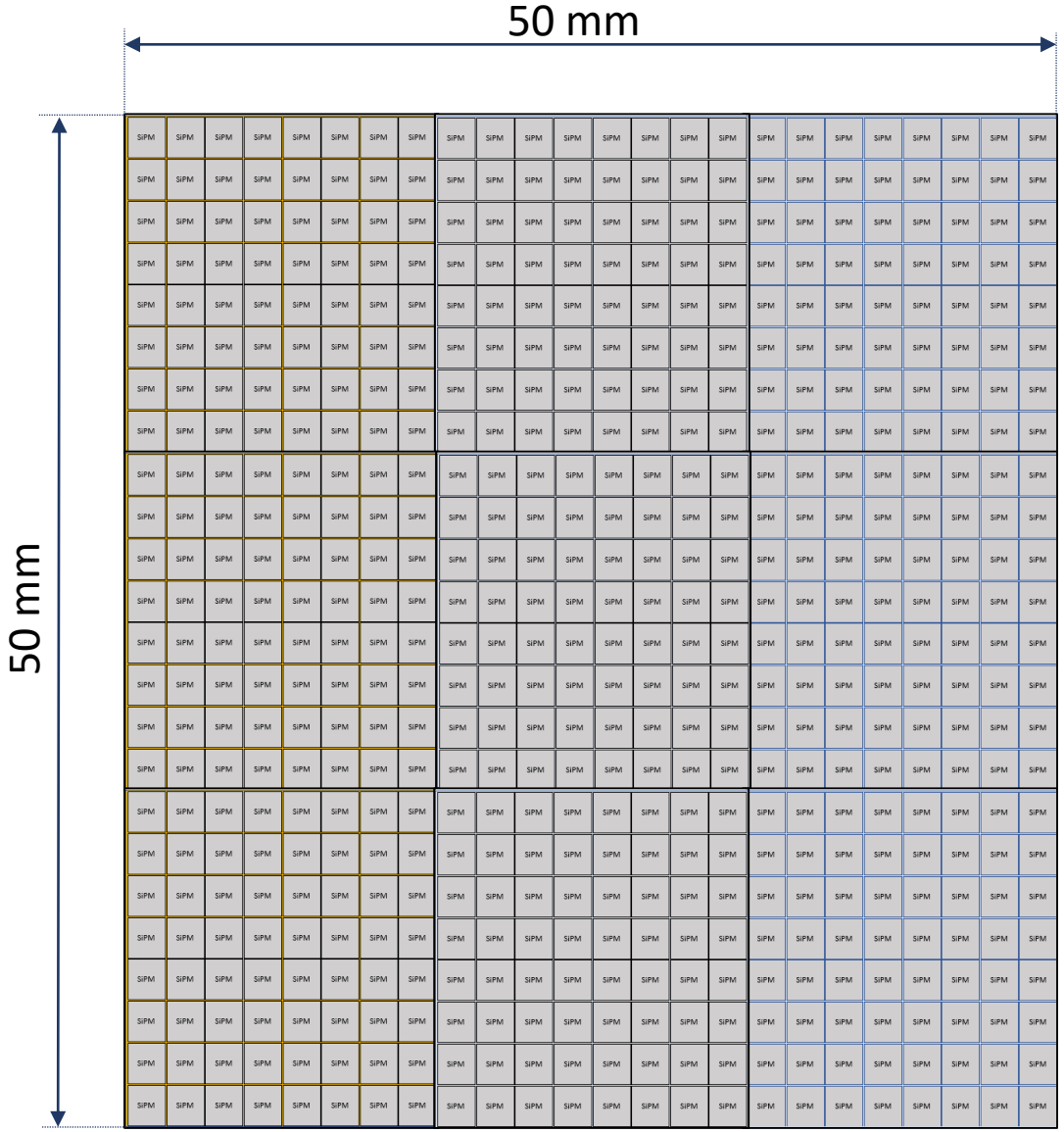
SiPM Super-module size must be equal area of each of the 36 segments of a RICH mechanical ring → 15 x 20 cm^2

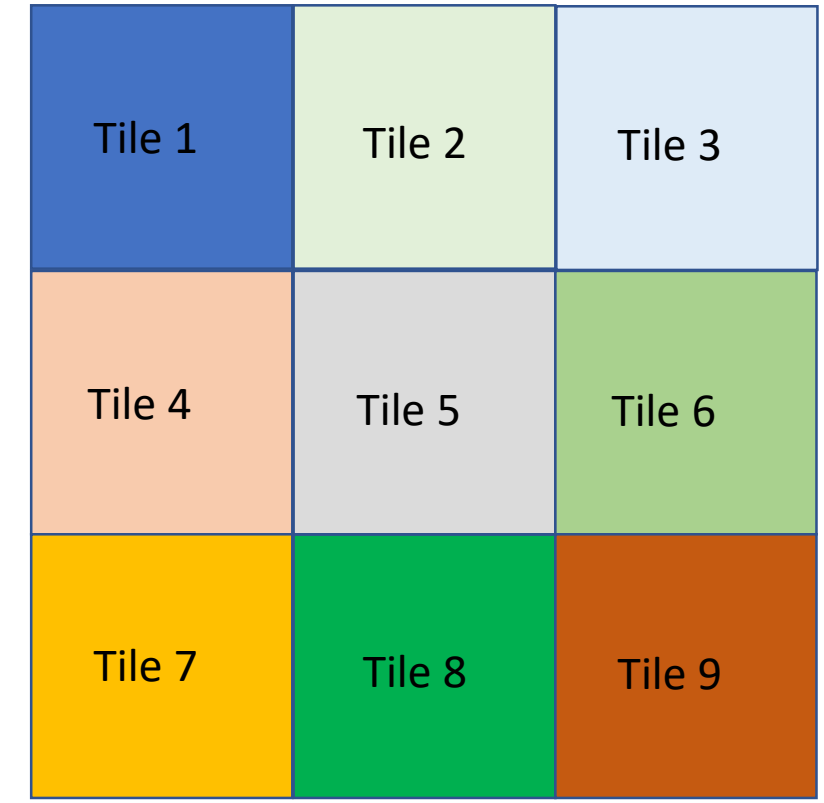
SiPM pitch ≤ 2.083 x 2.083 mm^2



SiPM Tile → 64 SiPM channels

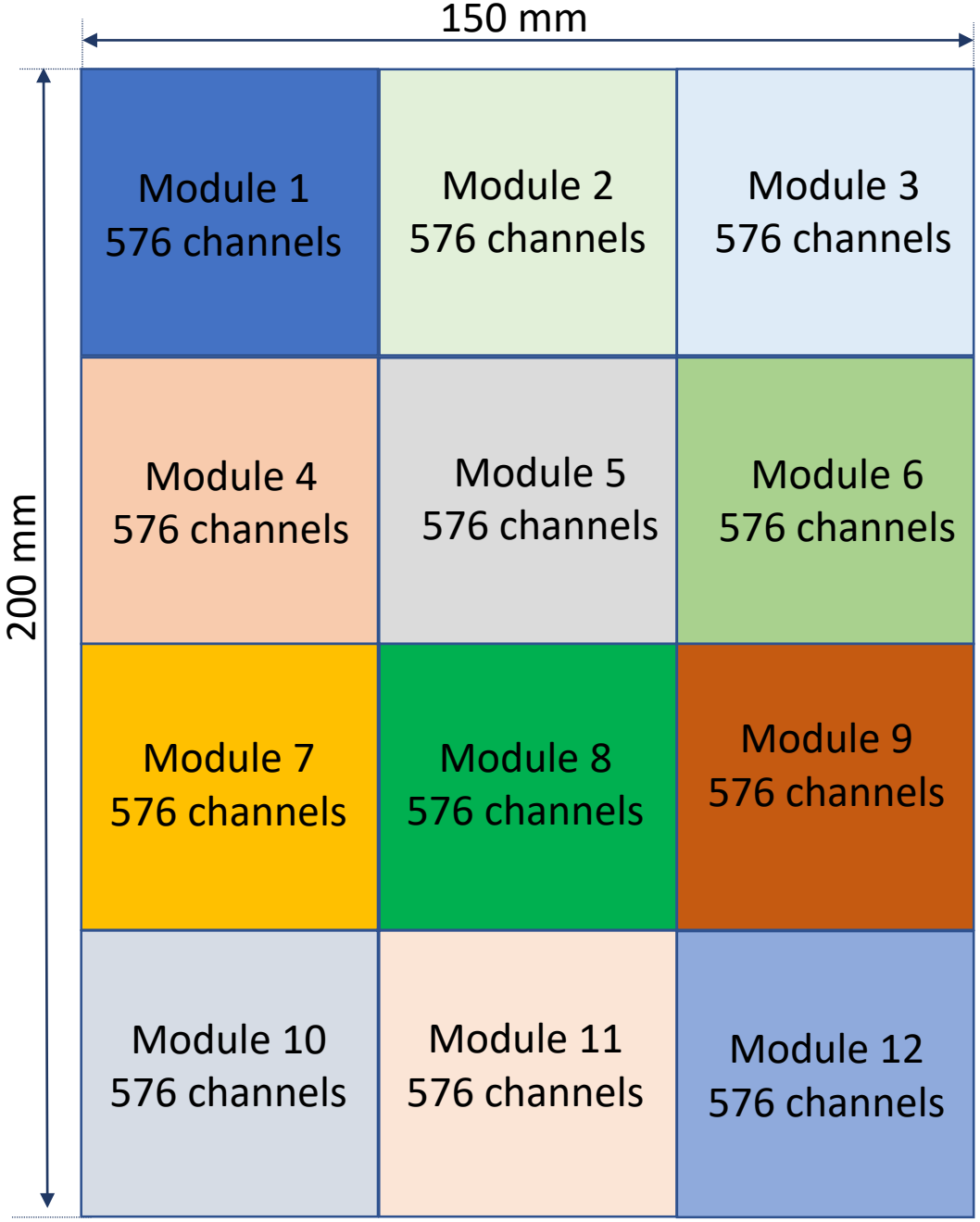
ALICE-3 RICH FEE: Preliminary Assembly Proposal





SiPM-module, constituted by 3 x 3 SiPM-tiles → **576 SiPM channels**

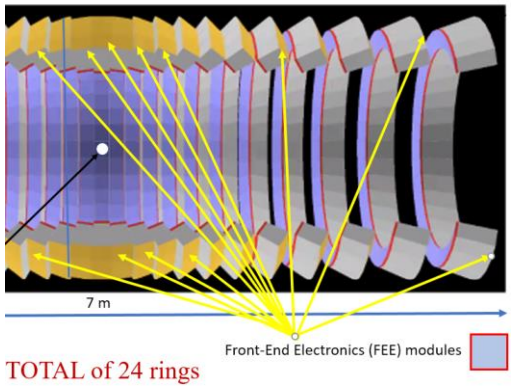
ALICE-3 RICH FEE: Preliminary Assembly Proposal



Challenges:

1. The mandatory solution size requirement is 20 cm x 15 cm.
2. The maximum thickness of the solution is 30 mm.
3. The solutions must operate in a cryogenic environment of -40° C.
4. The solutions must operate in a high-radiation environment.
5. We have only preliminary information on the ALCOR specs.

SiPM super-module, constituted by 3 x 4 SiPM modules
→ 12 x 576 = **6,912 SiPM channels**



Disclaimer: the total number my slightly change by fine tuning the pitch of the sensors.

ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on ALCOR ASICs

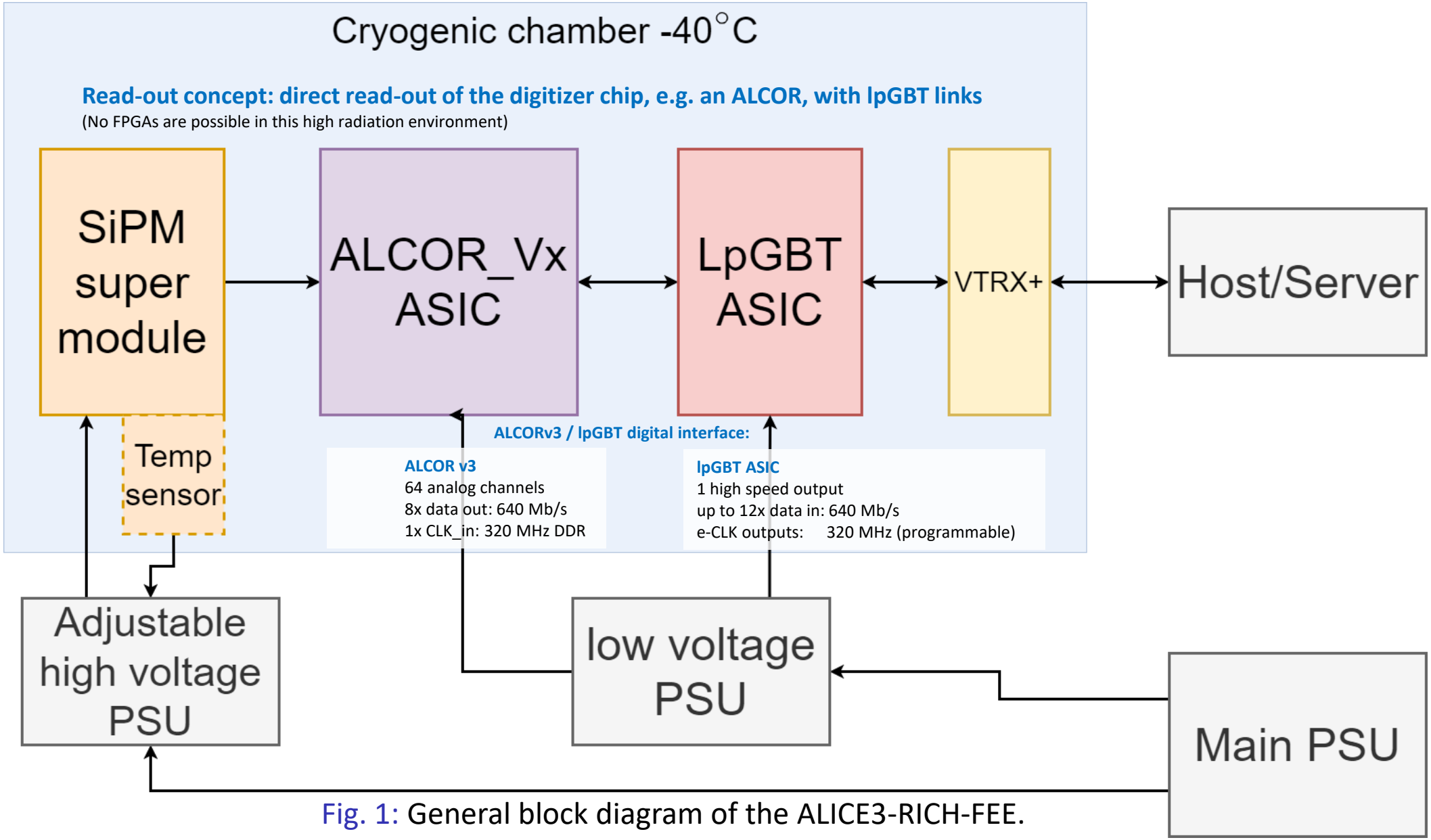


Fig. 1: General block diagram of the ALICE3-RICH-FEE.

ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on ALCOR ASICs

Ongoing developments started from the silicon-proven architecture of the ALCOR x32 channel SiPM readout ASIC:

Feature	ASIC for EIC dRICH	ASIC for GRAIN at DUNE
Channel modularity	64 pixels (8 columns)	1024 pixels (32 columns)
Measurements	ToA, ToT	ToA, ToT, Charge Integral
VETO Signal	YES – Global, external	YES – Global, internally generated or ext.
Time-of-Arrival resolution RMS	≈ 150 ps with C_{IN} = 100 pF	≈ 50 ps (target)
Time-over-Threshold resolution RMS	≈ 1 ns	≈ 1 ns
Charge integration response	N.A.	Bilinear (2 gain values) + peak sensitive
Charge integral resolution	N.A.	9 bit: 10 codes / phe; 3 codes / phe
Charge integral dynamic range	N.A.	[1 – 25 phe] ; [25 – 150 phe]
Power density	10 mW / channel [AVG]	10 mW / channel [AVG]
Silicon die size	4.95 x 3.78 mm²	≈ 20 x 20 mm²
Operating Temperature	300 K	77 K – 300 K
Number of LVDS Tranceivers	8 (one for each column)	32 (one for each column)
LVDS Transceiver Speed	320 Mbps SDR or 640 Mbps DDR	320 Mbps SDR
Clock Frequency	310 -325 MHz	310 – 325 MHz
Power gating mode in low duty cycle	No	Yes

See Valerio Pagliarino's presentation „Perspectives for a RICH front-end based on the ALCOR architecture and possible synergies with other experiments"
5th ALICE UPGRADE WEEK in Kraków (7-11 October 2024): Overview · Indico (cern.ch)

ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on ALCOR ASICs

We have investigated the following read-out schemes based on different present and future ALCOR ASICs:

Existing:

- 32-ch ALCOR_v2: not considered

Existing:

- 64-ch ALCOR_v3 with 320 Mb/s data lines
- 64-ch ALCOR_v3 with 640 Mb/s data lines

In development:

- 1024-ch ALCOR with 320 Mb/s data lines
- 1024-ch ALCOR with 320 Mb/s data lines

- Using of additional ECON-D ASICs for ZS and data aggregation

ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on ALCOR ASICs

Study No.1: Read-out scheme based on

ALCOR_v3 with 640 Mb/s data lines

ALICE-3 RICH FEE: Preliminary Read-out Concept based on the **ALCOR_v3** ASIC

How many FEE components do we need?

In a supermodule…

- We have 6 912 SiPMs in a Suermodule…
- ALCOR_v3 has 64 analog input channels
- → *108 ALCOR_v3 ASIC is needed in a Supermodule*
- 1 ALCOR_v3 has 8 digital output lines running at 640 Mb/s.
- Using the lpGBT in 10.24 Gb/s & FEC12 configuration, 12 input e-links are available at 640 Mb/s speed in an lpGBT ASIC to read out the ALCOR(s).
- → *72 lpGBT ASICs are required in a Supemodule*
- A VTRX+ optical transceiver module has 4 TX and 1 RX lines
- → *18 VTRX+ modules are need in a Supermodule*

Total number of FE components foreseen…

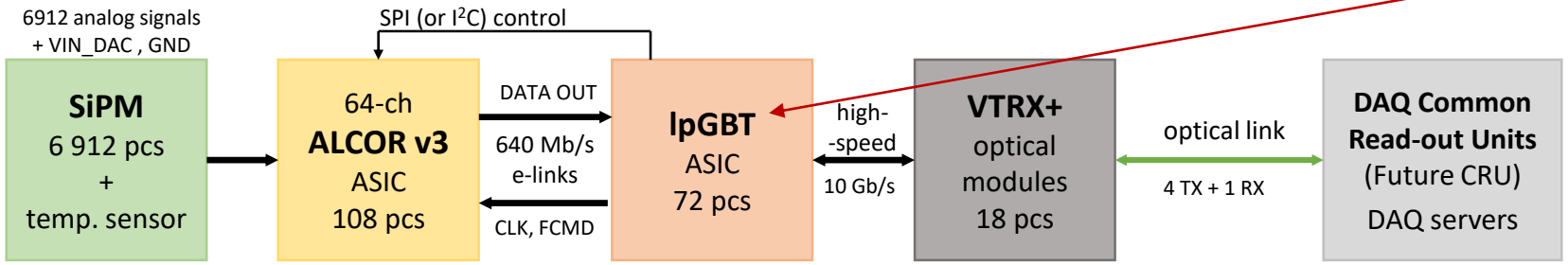
- We have 24 rings and 36 sectors, so we have 864 Supermodules
- Components needed:
  - ALCOR_v3: 864 x 108 = 93 312 pcs
  - lpGBT ASIC: 864 x 72 = 62 208 pcs
  - VTRX+ module: 864 x 18 = 15 552 pcs

Huge numbers of components, very high interconnection density → challenging implementation

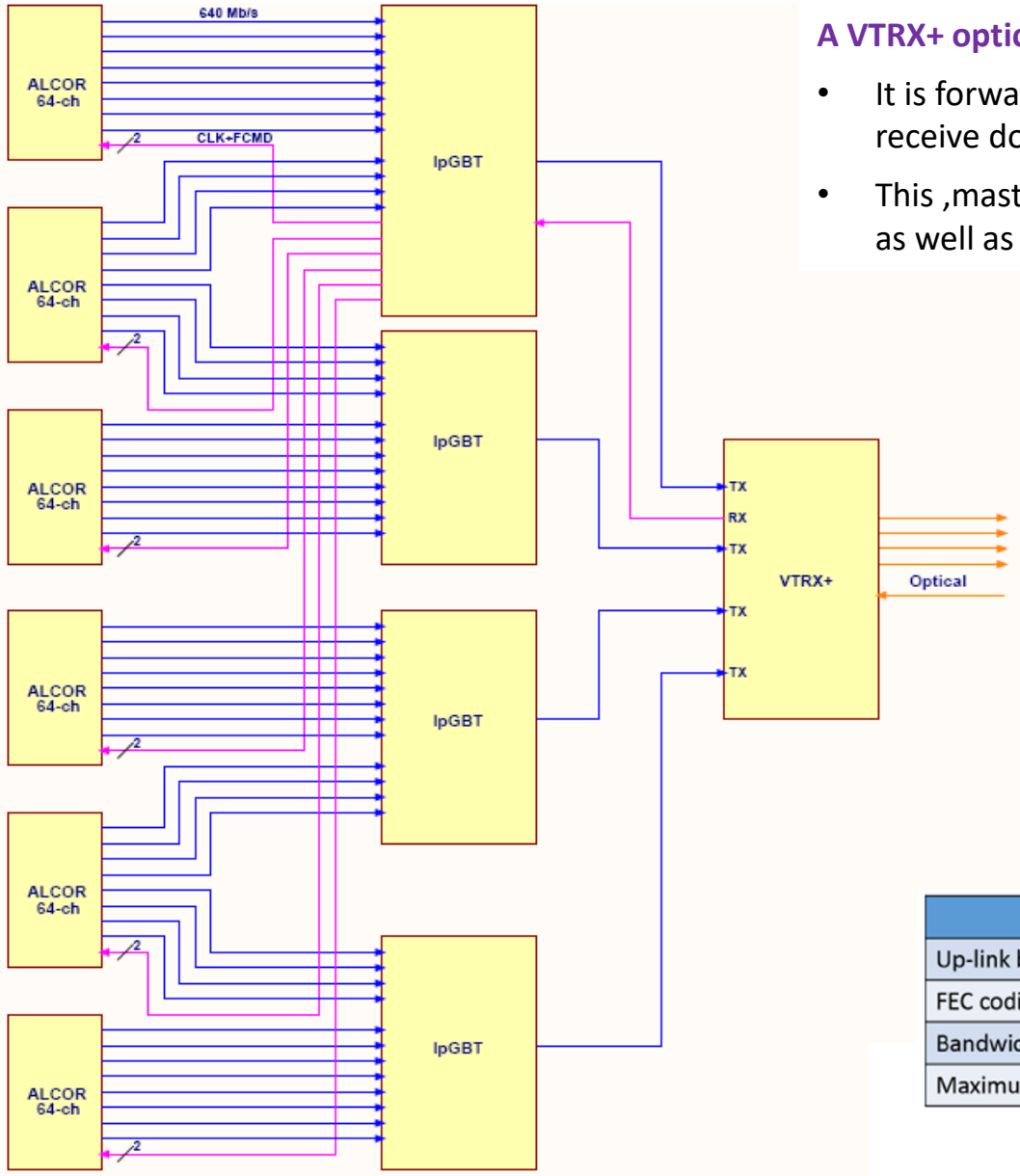
1. Let's see if it is possible… (next slides)

2. RICH is very much interested in new versions of ALCOR (or else) to reduce the initial number of data lines

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6



ALICE-3 RICH FEE: Read-out, Fast and Slow Control Segmentation (ALCOR_v3)



A VTRX+ optical module can handle 4 uplinks and 1 downlink

- It is forwarded electrically to 1 lpGBT only → only 1 of the 4 lpGBT ASICs connected can receive downstream data.
- This ‚master' lpGBT ASIC has to do the Fast Control and configuration of the 6 ALCORs, as well as the Slow Control of that segment of the FEE.

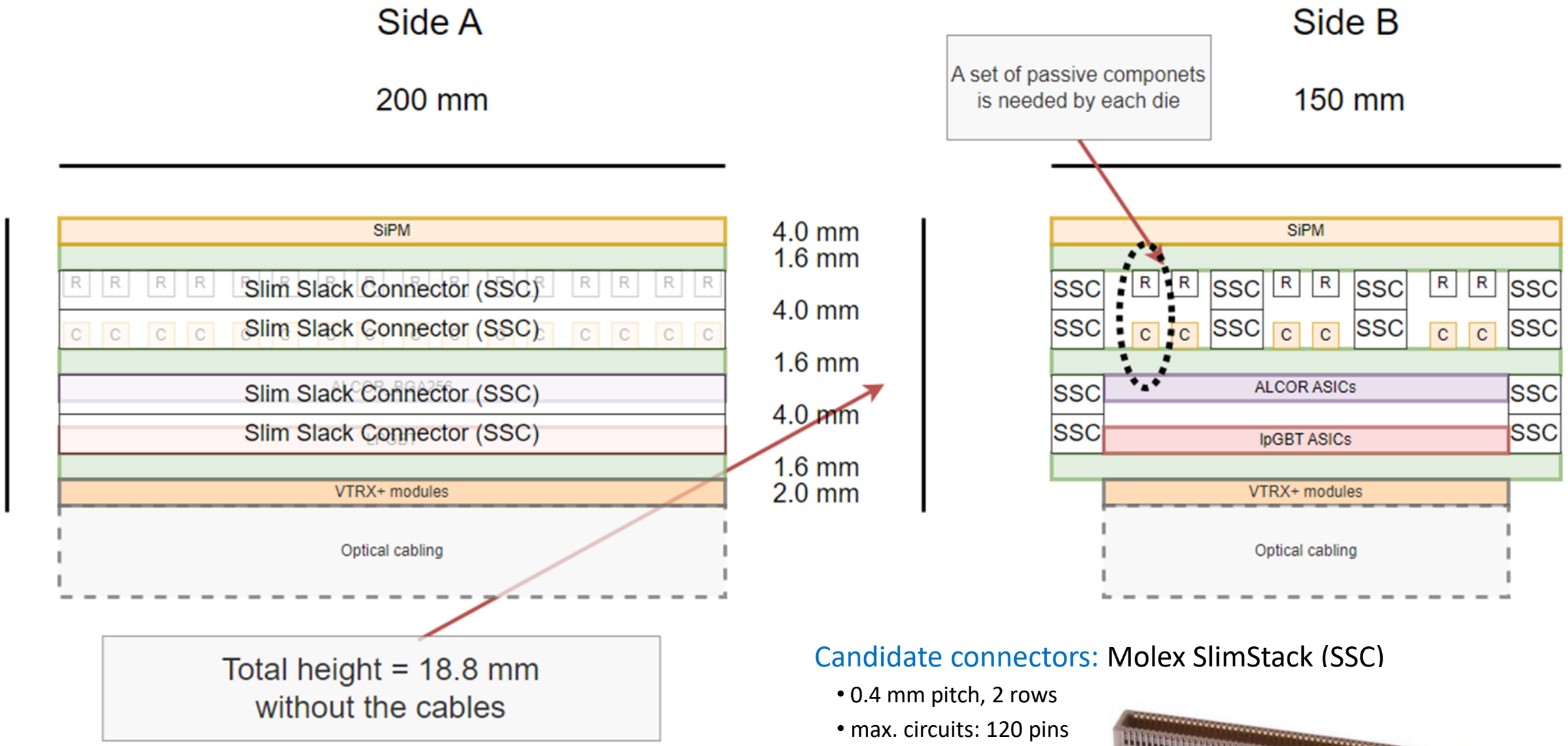
What is behind 1 downlink?

1x	VTRX+ module (4x TX, 1x RX)
4x	lpGBT ASIC (1x ‚master' + 3x ‚slave')
6x	64-ch ALCOR_v3 front-end ASIC
384	SiPMs (analog channles)

This is the possible level of granularity for the fast-control and slow-control of the FEE.

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

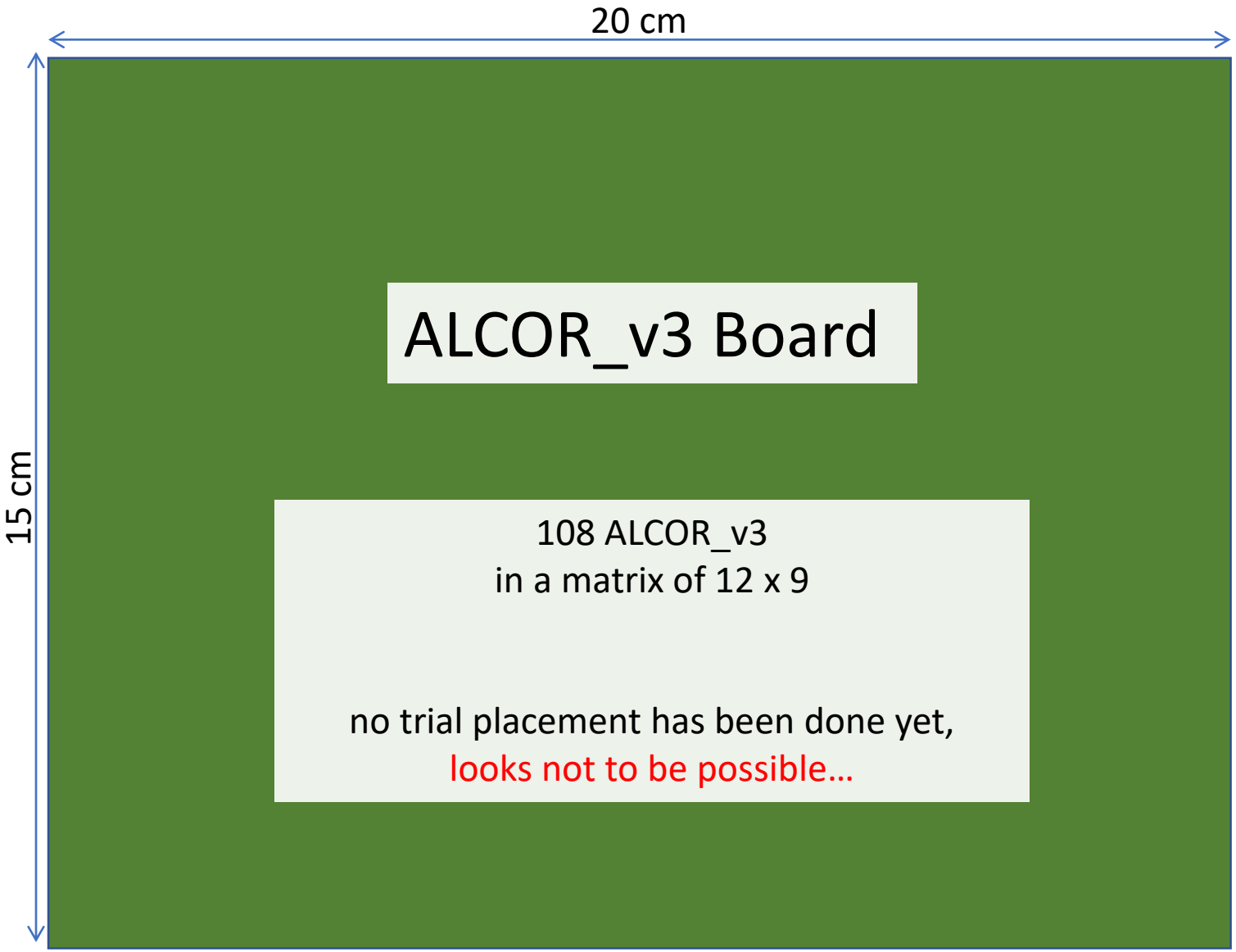
ALICE-3 RICH FEE: Stack of PCBs with board-to-board connectors



Candidate connectors: Molex SlimStack (SSC)

- 0.4 mm pitch, 2 rows
- max. circuits: 120 pins
- stacking height: 4 mm
- mating cycles: ~ 30

ALICE-3 RICH FEE: ALCOR_v3 with 640 Mb/s data lines



108 x ALCOR_v3 /board

ALCORs can be placed, but...

- **Connectors: 28x 120 pin, 0.4 mm**
  e.g. Molex SlimStack Connector (SSC)

  No. of connector pins needed between the SiPM PCB and the ALCOR PCB:
  - signals: ~ 6 912 !
  - GND: many! (up to thousands to avoid xtalk)
  - LV: hundreds!

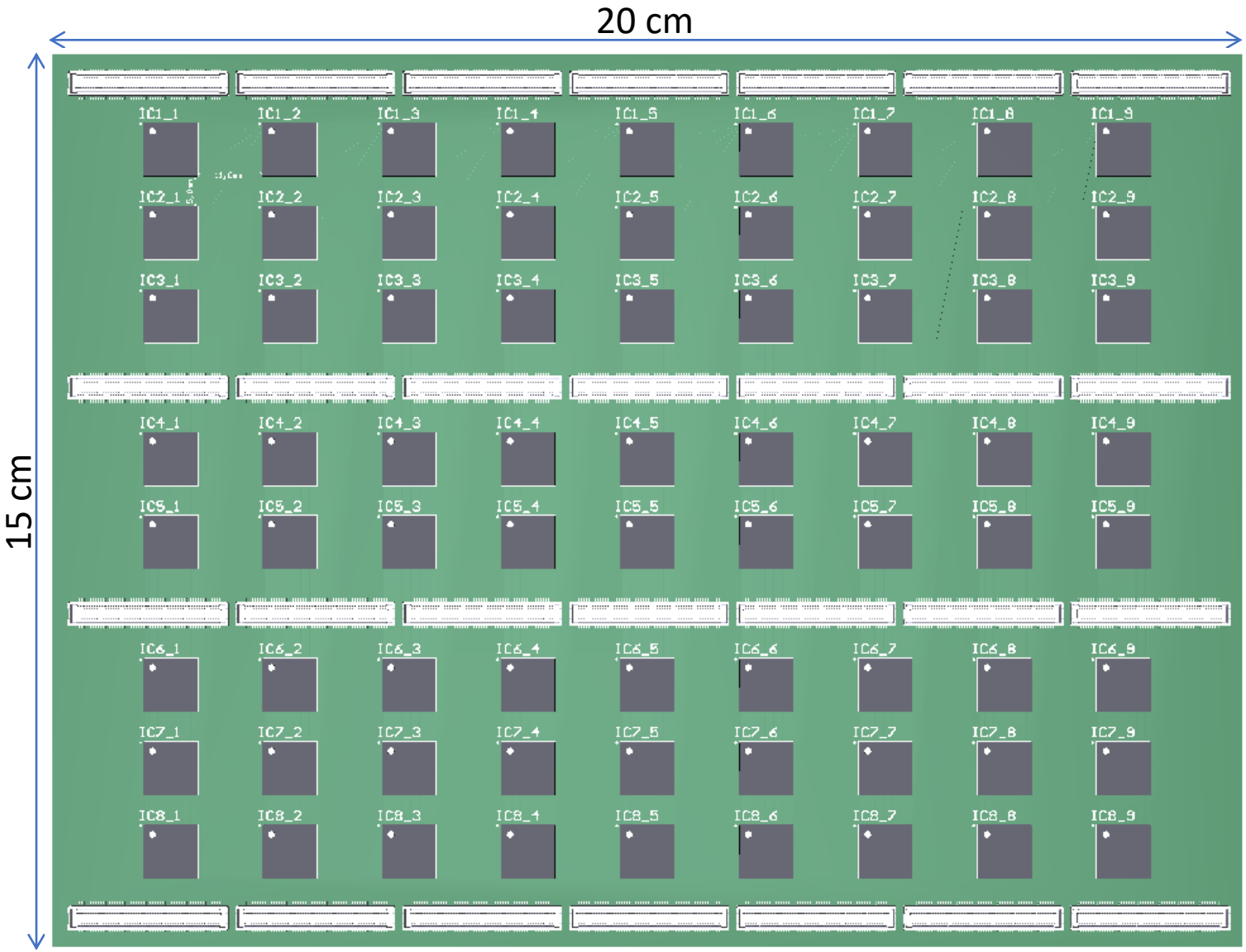
  No. of connector pins available: ~ 6 720
  (issue no.1 - Looks to be a showstopper for this concept...)

- **No. of outgoing e-Links:** 108 x 8 = **864**

- **Power dissipation on this side**
  P_{ALCOR} = 108x 64x 12 mW = **84 W /board**, max

Is it routable?
Maybe... further study is needed if concept is not dropped. Cross-talk, noise, etc.

ALICE-3 RICH FEE: ALCOR_v3 with 640 Mb/s data lines



TOP side

72x lpGBT ASICs /board

Components can be placed, but:

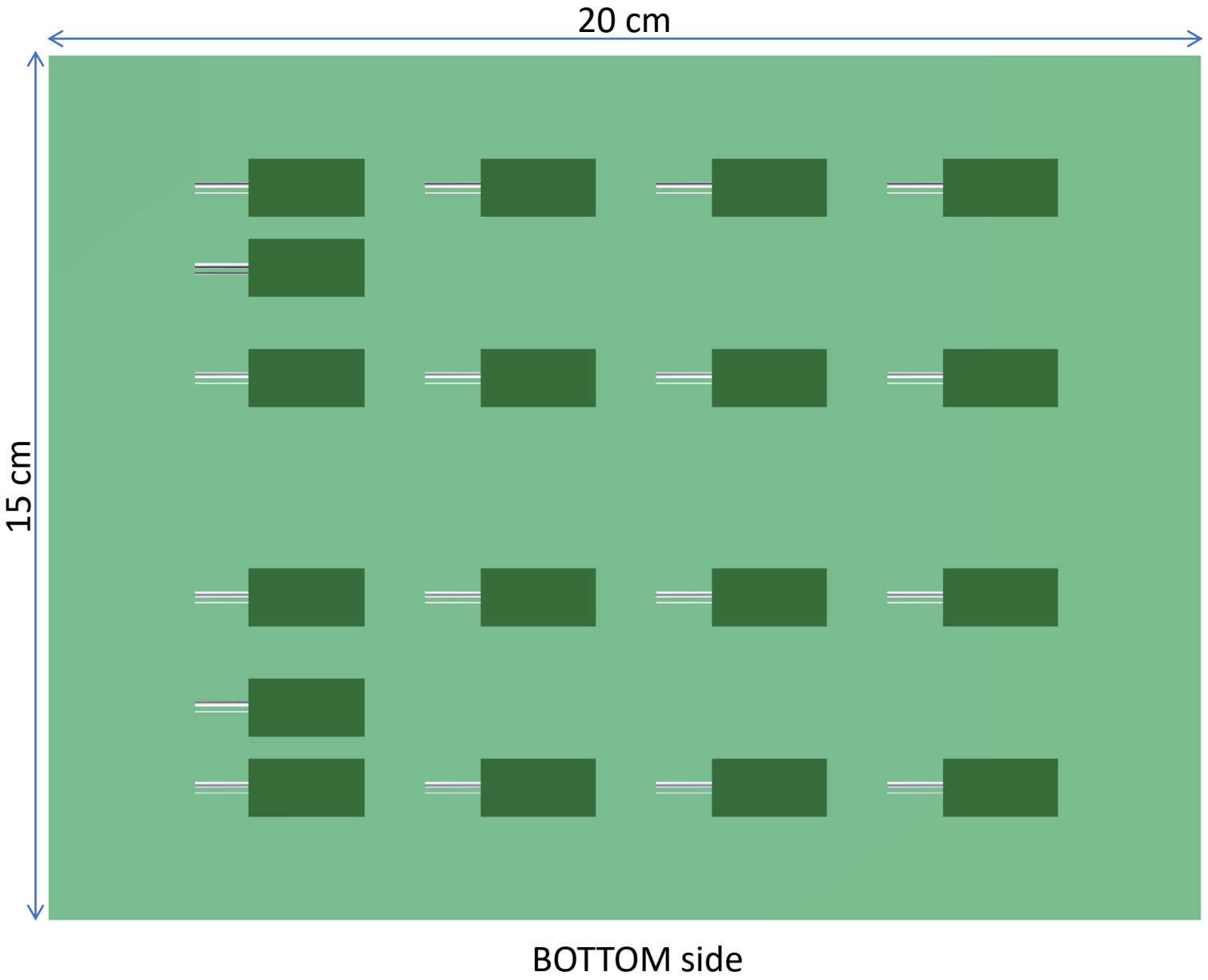
- **No. of eLinks from the ALCOR board: ~ 864**
- **No. of connector pins needed** between the ALCOR PCB and the lpGBT & VTRX+ PCB:
  - signals + GND: 3x 864 = **2 592 pins**
  - LV delivery: hundreds (see later)

  No. of connector pins available: ~ 3 360

- **Power dissipation on this side**
  P_{lpGBT} = 72x 0.5 W, max = 36 W /board, max

Is it routable?
Maybe on 16 layers... further study is needed if concept is not dropped.

ALICE-3 RICH FEE: ALCOR_v3 with 640 Mb/s data lines



18x VTRX+ modules /board

w/ long pigtail cables (up to 4 m!)

Components can be placed

- **10 Gb/s high-speed lines (90x) go to the other side via carefully designed diff. vias**
- **Power dissipation on this side**
  P_{tot} = 18x 0.24 W, max = 4.3 W /board, max.

* * *

I_{LV} (lpGBT, 72 pcs) = **30 A, max** **@1.2V**
(24 A, typ @1.2V)

I_{LV} (VTRX+, 18 pcs) = 1.6 A @ 2.5V
= 0.5 A @ 1.2V

P (lpGBT+VTRX+)$_{tot,\ max}$ = 36+4.3 W = **41 W /board**

T amb: -40 °C

ALICE-3 RICH FEE: LV Supply and Power Dissipation (ALCOR_v3_640 Mb/s)

LV Current Supply

Current consumption of the FEE components in each Supermodule…

I_{LV} (ALCOR_v3, 108 pcs)	10..12 mW /ch (ALCOR_v3)	
	= 70 A, max	@1.2V
I_{LV} (lpGBT, 72 pcs)	= 30 A, max	@1.2V
I_{LV} (VTRX+, 18 pcs)	= 1.6 A	@ 2.5V
	= 0.5 A	@ 1.2V

The total 1.2V current consumption of each Supermodule sums up to ~ 100 A

- thick cables need space... no option
- Local DC/DC conversion is a must
- additional *power board* in the PCB stack will be needed
- a single rad-hard „bPOL48V" DC/DC converter has an
  - $I_{out, max}$ = ~ 10..15 A (w/ propoer cooling)
- We would need a ***very high number of*** **DC/DC converters** in each Supermodule... **(Issue No. 2a)**
- high density board-to-board connectors (e.g. this SlimStack connectors) can deliver 0.3..0.5A /pin → an additional hundreds of pins are needed for LV delivery **(Issue No. 2b)**
- the even distribution of the current on hundreds of connector pins on multiple connectors can not be guaranteed...

This looks to be a showstopper with the present ALCOR_v3 ASIC and direct lpGBT read-out.

Power dissipation /cooling

Dissipation of the FEE components in a Supermodule…

P (ALCOR_v3, 108 pcs)	= 84 W, max
P (lpGBT, 72 pcs)	= 36 W, max (see previous slides)
P (VTRX+, 18 pcs)	= 4.6 W, max (see previous slides)

120..130 W /Supermodule

* * *

In this scheme the *total dissipation* of the FEE compnents in the cryogenic vessel (I.e. all 864 Supermodules, 24 rings x 36 segments)

125 W x 864 = **110 kW**, max.

Cooling down the cryogenic vessel to -40 °C while heating it with 110 kW is a challange, if feasible.

To be further evaluated... but the large FEE dissipation can also be a showstopper for this scenario with the ALCOR_v3.

ALICE-3 RICH FEE: ASICs need and Cost estimations

FEE Components Cost (estimations)

ASIC components need:

• ALCOR_v3:	864 x 108	= 93 312 pcs	? CHF/ea	= ?
• lpGBT ASIC:	864 x 72	= 62 208 pcs	25 CHF /ea	= 1.56 MCHF
• VTRX+ module:	864 x 18	= 15 552 pcs	140 CHF /ea	= 2.18 MCHF
• DC/DC:	864 x ?			

Connectors

• Molex SSC	864 x 60	= 50k+ pcs	< 2 CHF & 50K	= < 0.1 MCHF

PCB (bare)

• est.	864 x 4	= 3 500 pcs	~ 300 CHF /ea	= ~ 1 MCHF

DAQ /Common Read-out Units (of that time):

lpGBT uplinks: ~ 62 000

CRUs with 48 inputs: ~ 1 300 ... also looks not acceptable...

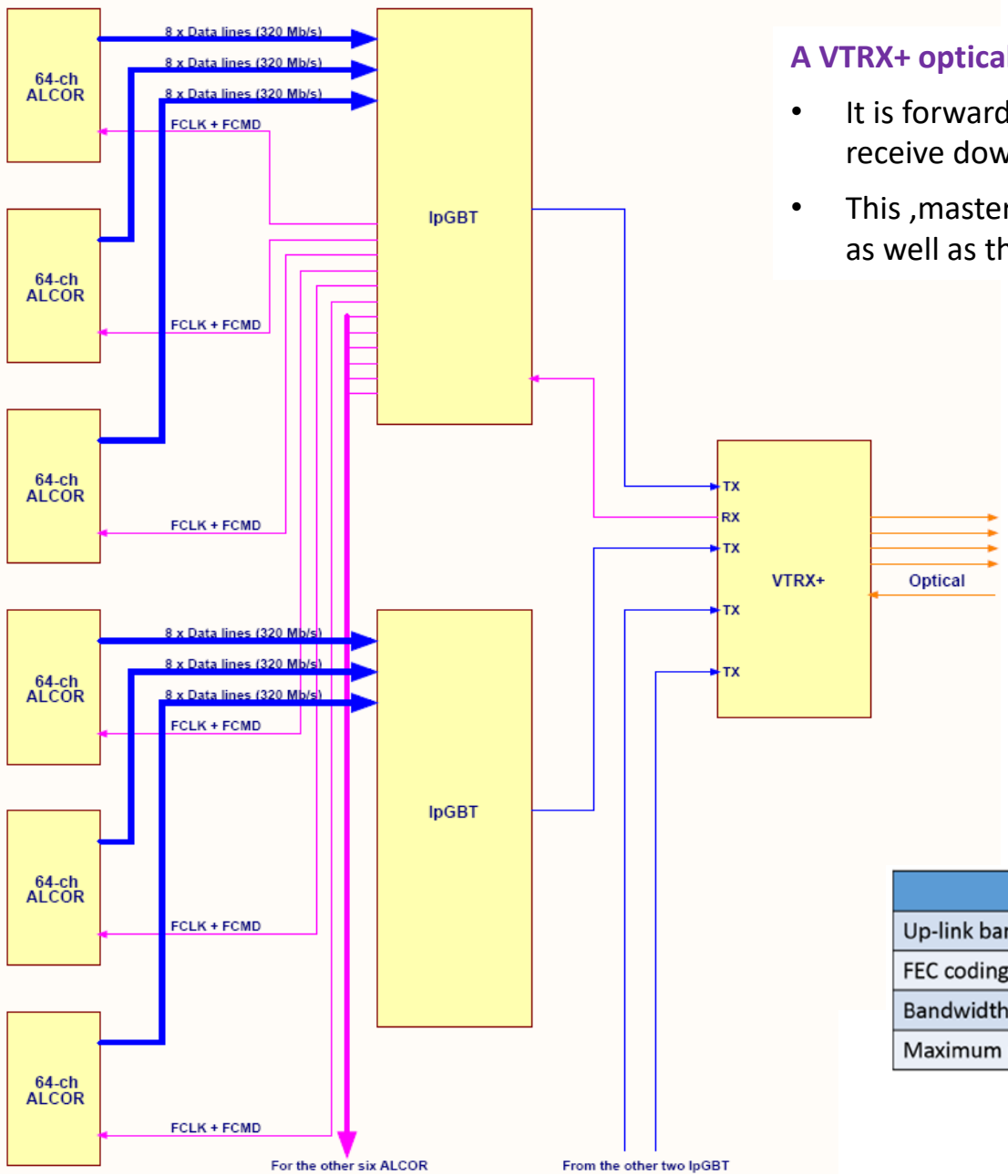
ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on ALCOR ASICs

Study No. 2: Read-out scheme based on

ALCOR_v3 with 320 Mb/s data lines

the same, but the number of lpGBT and VTRX+ components (and CRUs) can be halved...

ALICE-3 RICH FEE: Read-out, Fast and Slow Control Segmentation (ALCOR_v3)



A VTRX+ optical module can handle 4 uplinks and 1 downlink

- It is forwarded electrically to 1 lpGBT only → only 1 of the 4 lpGBT ASICs connected can receive downstream data.
- This ‚master' lpGBT ASIC has to do the Fast Control and configuration of the 6 ALCORs, as well as the Slow Control of that segment of the FEE.

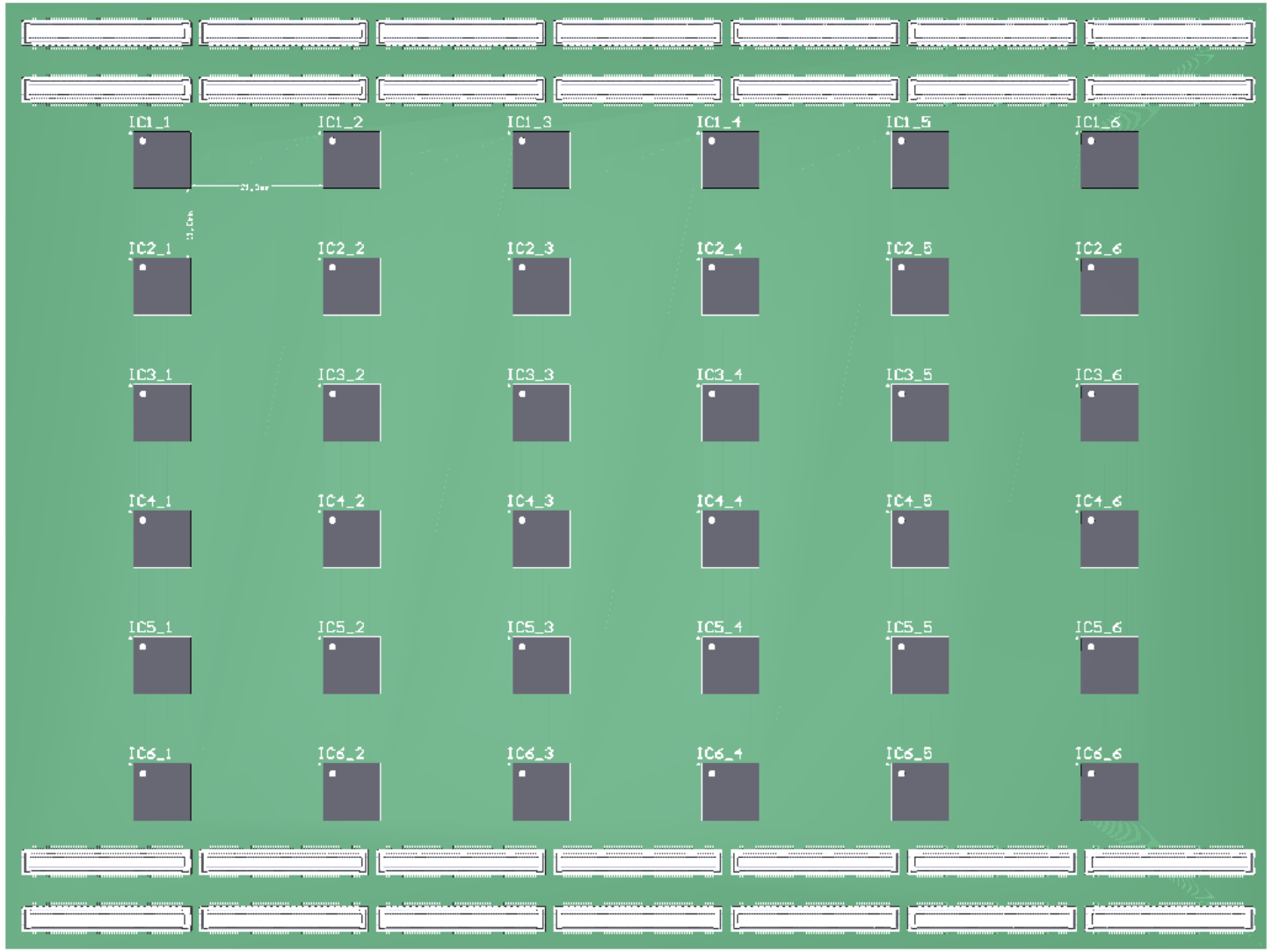
What is behind 1 downlink?

1x	VTRX+ module (4x TX, 1x RX)
4x	lpGBT ASIC (1x ‚master' + 3x ‚slave')
12x	64-ch ALCOR_v3 front-end ASIC
768	SiPMs (analog channles)

This is the possible level of granularity for the fast-control and slow-control of the FEE.

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

ALICE-3 RICH FEE: ALCOR_v3 with 320 Mb/s data lines



TOP side

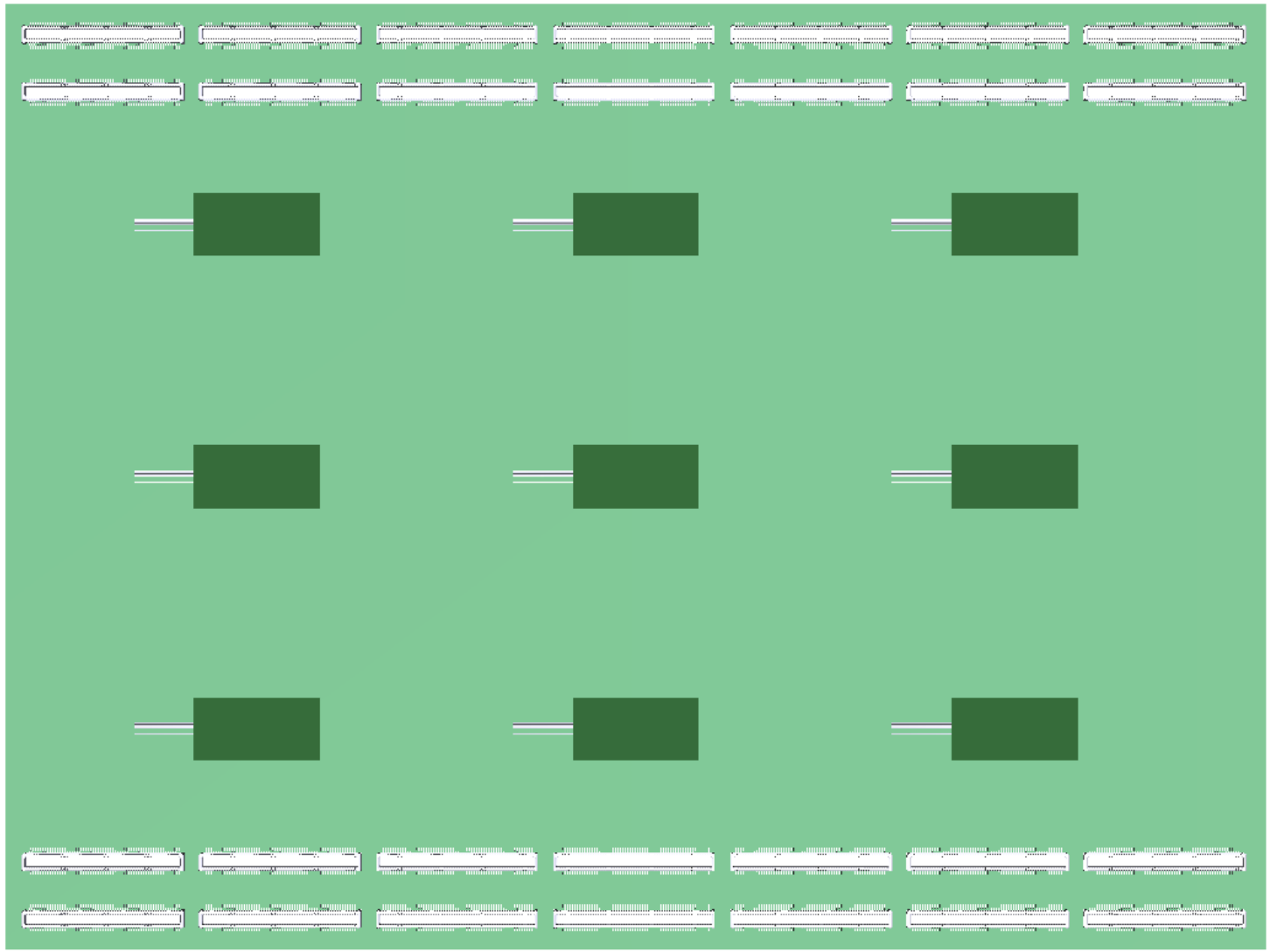
36x lpGBT ASICs /board

- **Components can be placed, but:**
- **No. of eLinks: ~ 540**
- **No. of connector pins needed** between the ALCOR PCB to the lpGBT PCB remains the same:
  - signals: ~ 6 912
  - GND: many (up to thousands)
  - LV hundreds

  No. of connector pins available: 3 360 or 6 720, max, if we double the connectors (issue no.1)
- **Power dissipation on this side:**
  P_{lpGBT} = 36x 0.5 W, max = **18 W /board**, max

Is it routable?
Looks feasible...

ALICE-3 RICH FEE: ALCOR_v3 with 320 Mb/s data lines



BOTTOM side

9x VTRX+ modules /board

w/ long pigtail cables (up to 4 m)

Components can be placed

- **10 Gb/s high-speed lines (45x) go to the other side via carefully designed diff. vias**
- **Power dissipation on this side:**
  P_{tot} (VTRX+) = 9x 0.24 W, max = 2.2 W /board, max.

* * *

I_{LV} (lpGBT, 36 pcs) = **15 A, max** **@1.2V**
(12 A, typ @1.2V)

I_{LV} (VTRX+, 18 pcs) = 0.8 A @ 2.5V
= 0.25 A @ 1.2V

P (lpGBT+VTRX+)$_{tot,\ max}$ = 18+2.2 W = **21 W /board**

T amb: -40 °C

ALICE-3 RICH FEE: LV Supply and Power Dissipation (ALCOR_v3_320 Mb/s)

LV Current Supply

Current consumption of the FEE components in each Supermodule…

I_{LV} (ALCOR_v3, 108 pcs)	10..12 mW /ch (ALCOR_v3)	
	= 70 A, max	@1.2V
I_{LV} (lpGBT, 36 pcs)	= 15 A, max	@1.2V
I_{LV} (VTRX+, 9 pcs)	= 0.8 A	@ 2.5V
	= 0.25 A	@ 1.2V

The total 1.2V current consumption of each Supermodule sums up to ~ 85 A

- Supplying 85 A instead of 100 A /Supermodule is still very demanding if feasible
- We would need a ***very high number of*** **DC/DC converters** in each Supermodule... **(Issue No. 2a)**
- high density board-to-board connectors (e.g. this SlimStack connectors) can deliver 0.3..0.5A /pin → an additional hundreds of pins are needed for LV delivery **(Issue No. 2b)**
- the even distribution of the current on hundreds of connector pins on multiple connectors can not be guaranteed...

The high LV current need dominated by the ALCORs still looks to be a showstopper for this scenario with ALCOR_v3.

Power dissipation /cooling

Dissipation of the FEE components in a Supermodule…

P (ALCOR_v3, 108 pcs)	= 84 W, max
P (lpGBT, 36 pcs)	= 18 W, max (see previous slides)
P (VTRX+, 9 pcs)	= 2.3 W, max (see previous slides)

100..110 W /Supermodule

* * *

In this scheme the *total dissipation* of the FEE compnents in the cryogenic vessel (I.e. all 864 Supermodules, 24 rings x 36 segments)

105 W x 864 = **91 kW**, max.

Cooling down the cryogenic vessel to -40 °C while heating it with 90 kW is still a challange, if feasible. **(Issue No. 3)**

To be further evaluated... but the high dissipation dominated by the ALCORs can still be a showstopper for this scenario with ALCOR_v3.

ALICE-3 RICH FEE: Conclusion with the ALCOR_v3 ASIC

Our conclusion:

For the RICH FEE, the present **64-ch ALCOR_v3** is not a feasible option
(neither with 640 Mb/s nor with 320 Mb/s data lines (e-links))

ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on an 1024-ch ALCOR

Study No. 3: Read-out scheme based on

1024-ch ALCOR with 320 Mb/s data lines

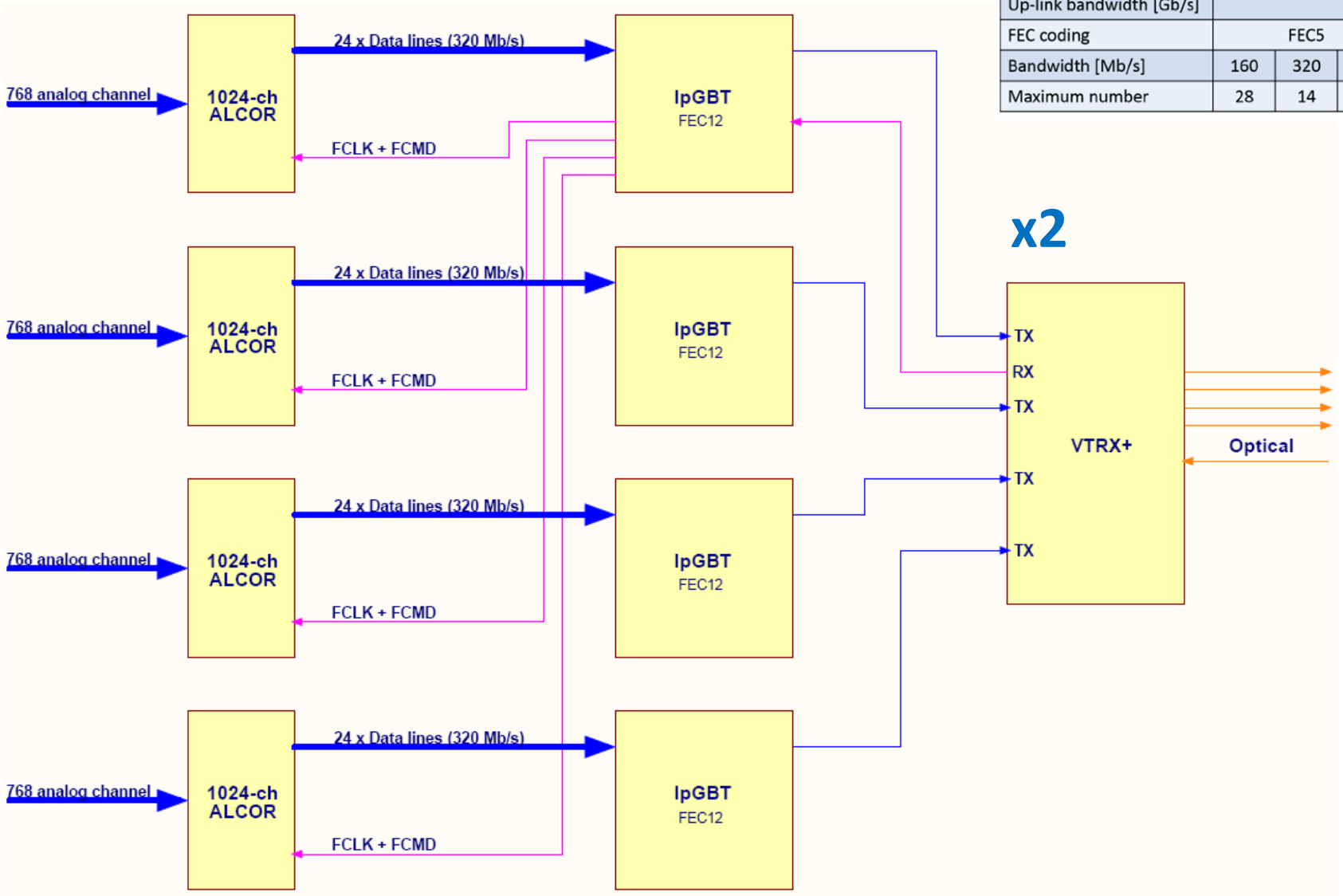
ALICE-3 RICH FEE: Preliminary Read-out Proposal Based on an 1024-ch ALCOR

The new 1024-ch ALCOR

- will have 32 output data lines that correspond to 32 columns with 32 pixels in each column
- Unused columns can be disabled
- Moreover, columns can be multiplexed to a lesser number of output lines, by a factor of powers of two
- With 32 columns, the no. of the output lines can be 32, 16, 8, 4, 2, 1,
  reducing the available bandwith for one column (or one pixel) proportionally

(*for more details see Valerio's presentation*)

ALICE-3 RICH FEE: 1024-ch ALCOR and lpGBT with FEC12



Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

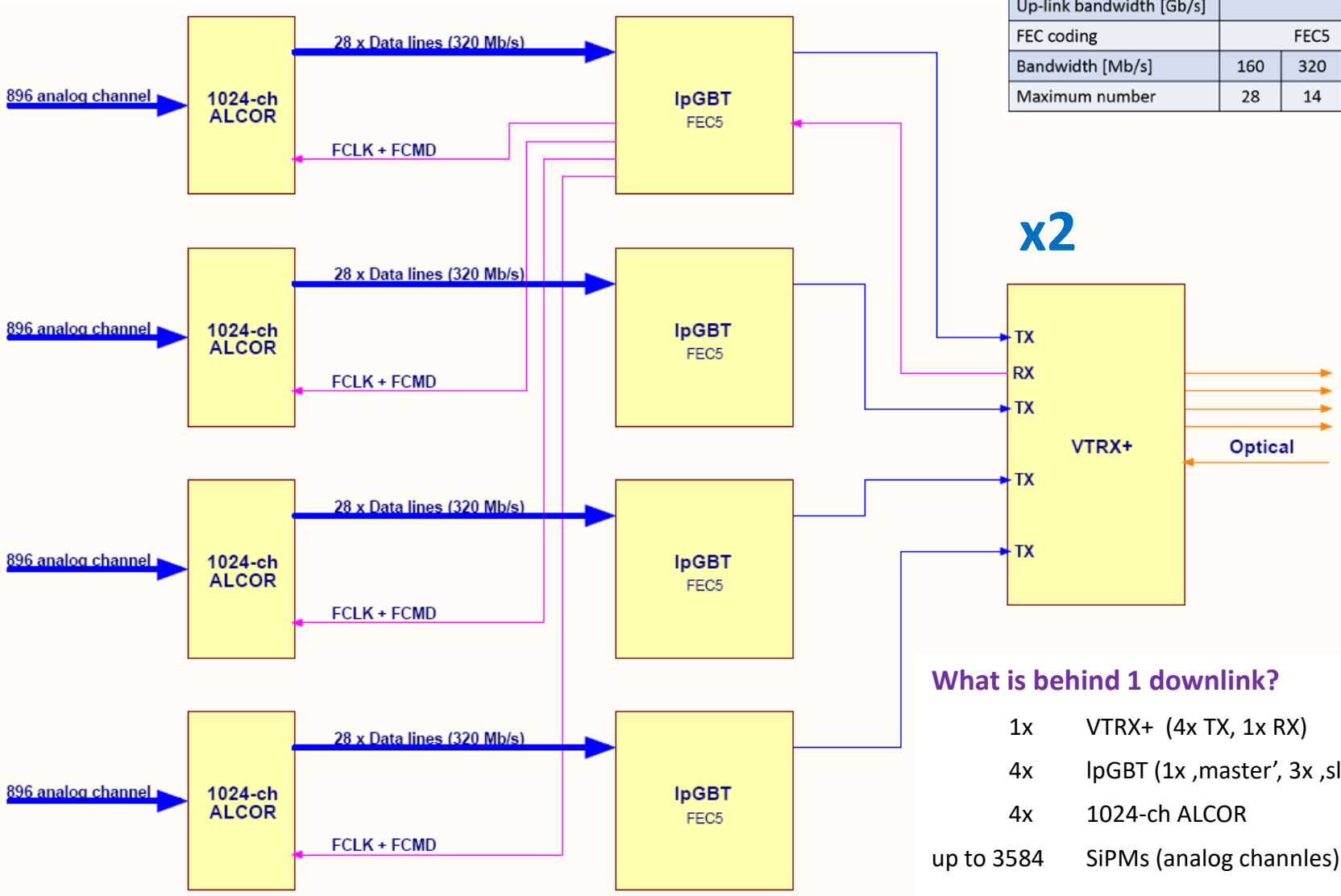
No. of components in a Supemodule:

- With 24 data lines (and no multiplexing) the 1024-ch ALCOR can handle **768 pixels**
- **6 912 pixels** / 768 = **9 ALCOR / Supermodule**
- *Not a nice number* because of the lpGBT/VTRX+ granularity of 4.

  (With *8 ALCORs* and FEC12 we can have **6 144 pixels, max** in a SM **only**)

24 columns of an ALCOR is read out, 8 are disabled

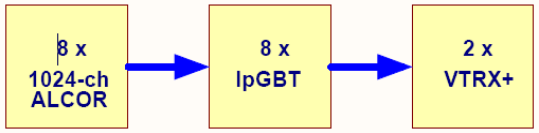
ALICE-3 RICH FEE: 1024-ch ALCOR and lpGBT with FEC5



Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

No. of components in a Supemodule:

- With **28 data lines** (no multiplexing) the 1024-ch ALCOR can handle **896 pixels**
- **6 912 pixels** / 896 = 7.7
  ➔ **8 ALCOR / Supermodule**



- This can be either:
  - 7x 28 lines + 1x 20 lines, or
  - 8x 27 lines
- Reading-out 8 ALCORs, all with 28 data lines (lpGBT FEC5) we can have **7 168 pixels** in a Supermodule

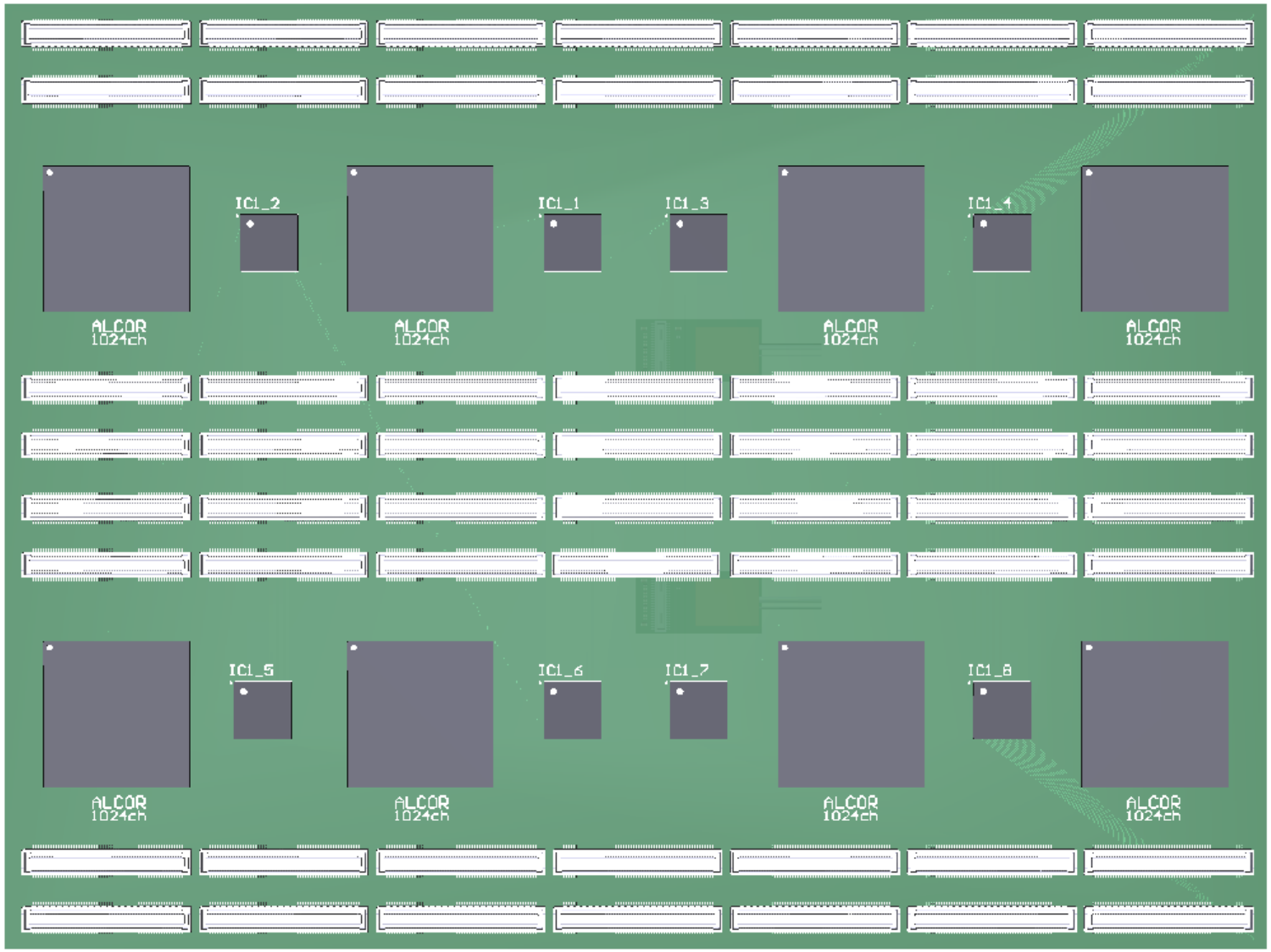
What is behind 1 downlink?

1x	VTRX+ (4x TX, 1x RX)
4x	lpGBT (1x ‚master', 3x ‚slave')
4x	1024-ch ALCOR
up to 3584	SiPMs (analog channles)

28 columns of an ALCOR is read out, 4 are disabled

This is the possible level of granularity for the fast-control and slow-control of the FEE.

ALICE-3 RICH FEE: 1024-ch ALCORs and lpGBTs on the same board



TOP side

8 ALCOR (1024-ch) + 8 lpGBT could be placed on the *same* board

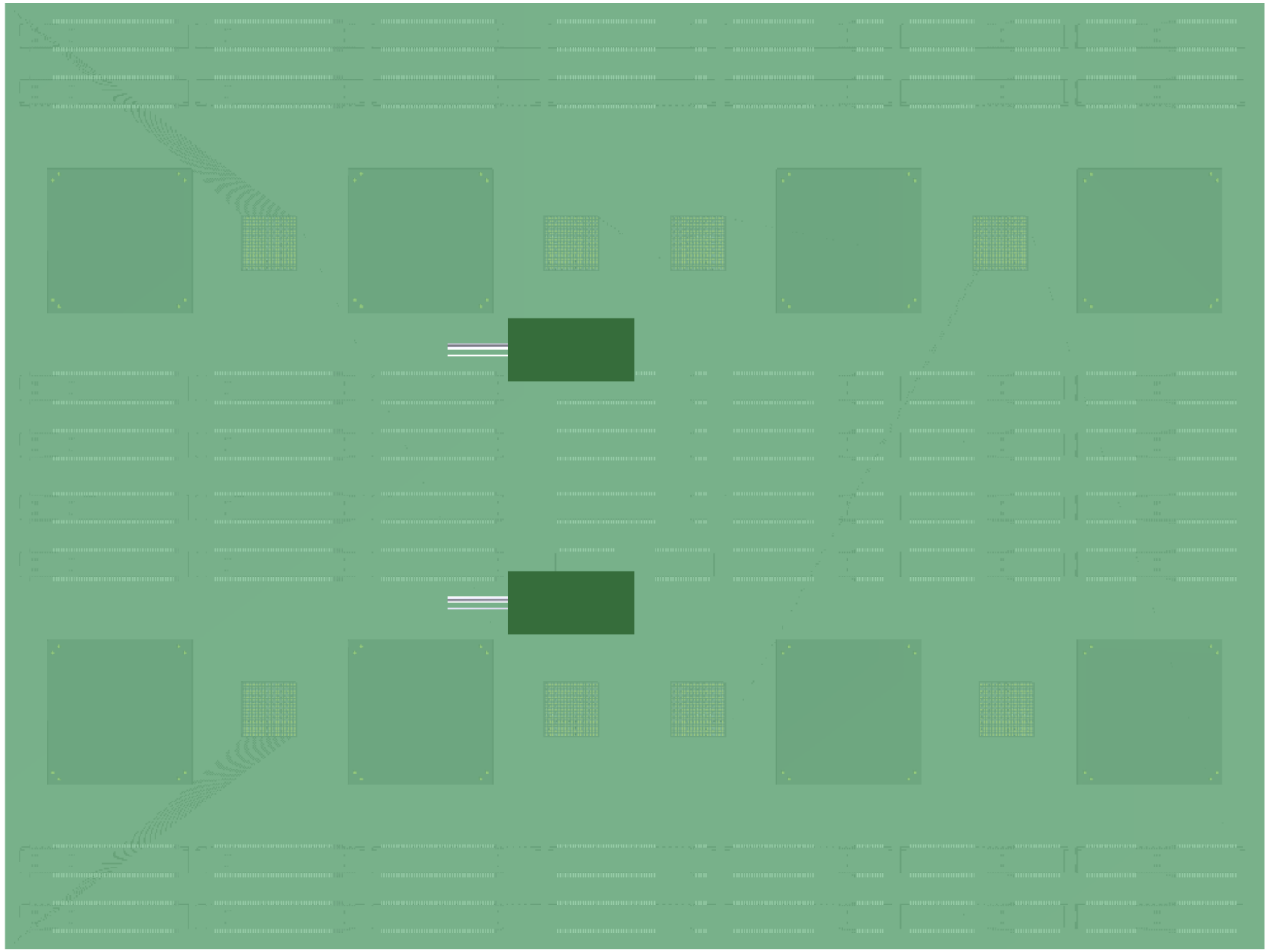
- **Components can be placed, but..**
- **No. of connector pins needed** between the SiPM PCB and the (ALCOR + lpGBT) PCB remains the same:
  - analog signals: ~ 6 912
  - GND: many (up to thousands to avoid xtalk)

Even with doubling the number of connectors the number of the available pins (~ 6 720) is not enough (issue no.1, still a showstopper...)

No. of eLinks: ~ 224 (all PCB-internal)

- **Power dissipation on this side:**
  P_{ALCOR} = 8x 10 W, max = **80 W /board**, max
  P_{lpGBT} = 8x 0.5 W = **4 W /board**, max

ALICE-3 RICH FEE: 1024-ch ALCORs and lpGBTs on the same board



BOTTOM side

2x VTRX+ modules /board

w/ long pigtail cables (up to 4 m)

- **Lot of space** for overlappig cables, service electronics (e.g. including some of the DC/DC converters)
- **10 Gb/s high-speed lines (45x) go to the other side via carefully designed diff. vias**
- **Power dissipation on this side:**
  P_{tot} (VTRX+) = 2x 0.24 W = **0.5 W, max**: negligible

* * *

Current need & dissipation:

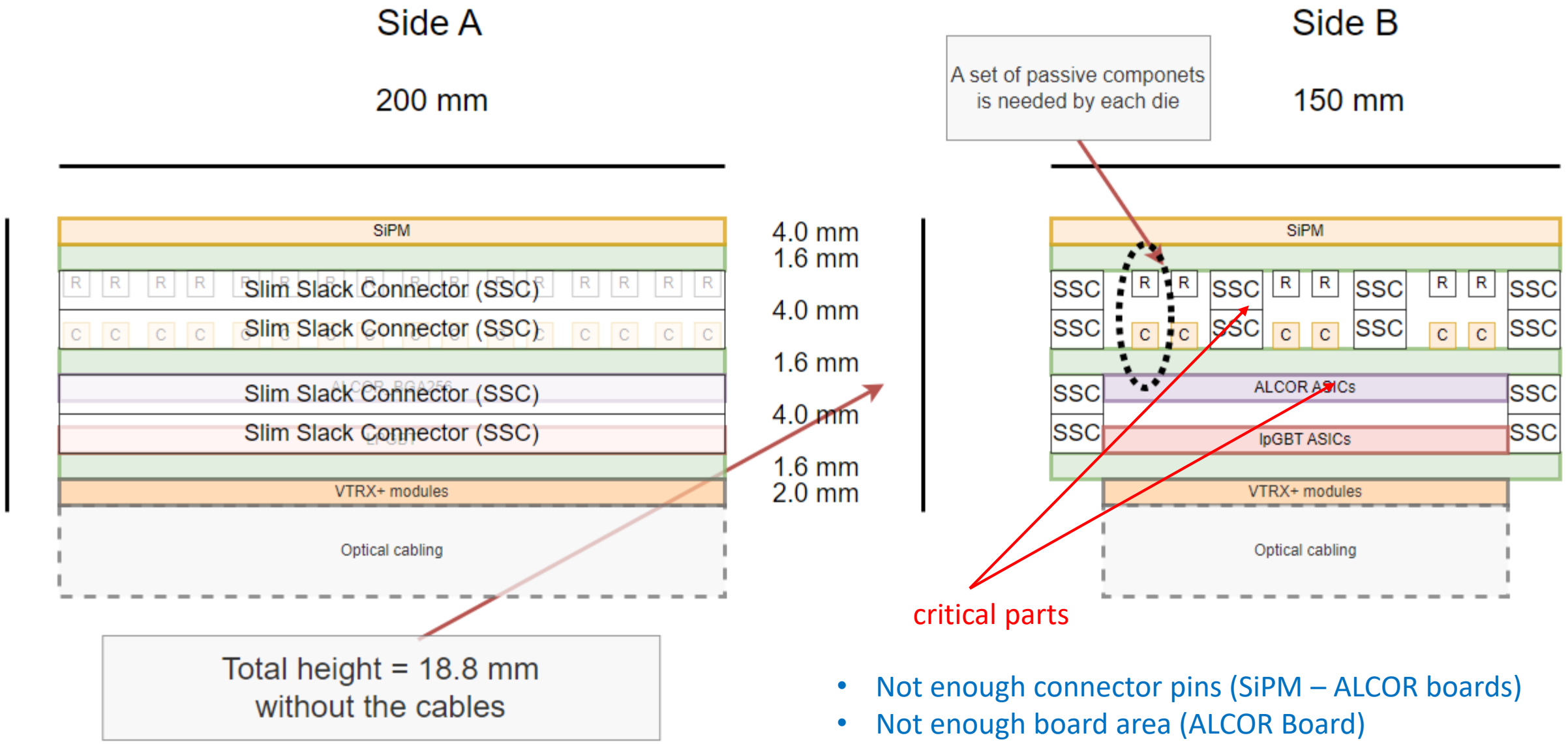
I_{LV} (ALCOR, 8 pcs) = **70 A, max** **@1.2V**

I_{LV} (lpGBT+, 8 pcs) = 3.4 A @ 1.2V

P (lpGBT+VTRX+)$_{tot,\ max}$ = 84 W+4 W = **88 W /board**

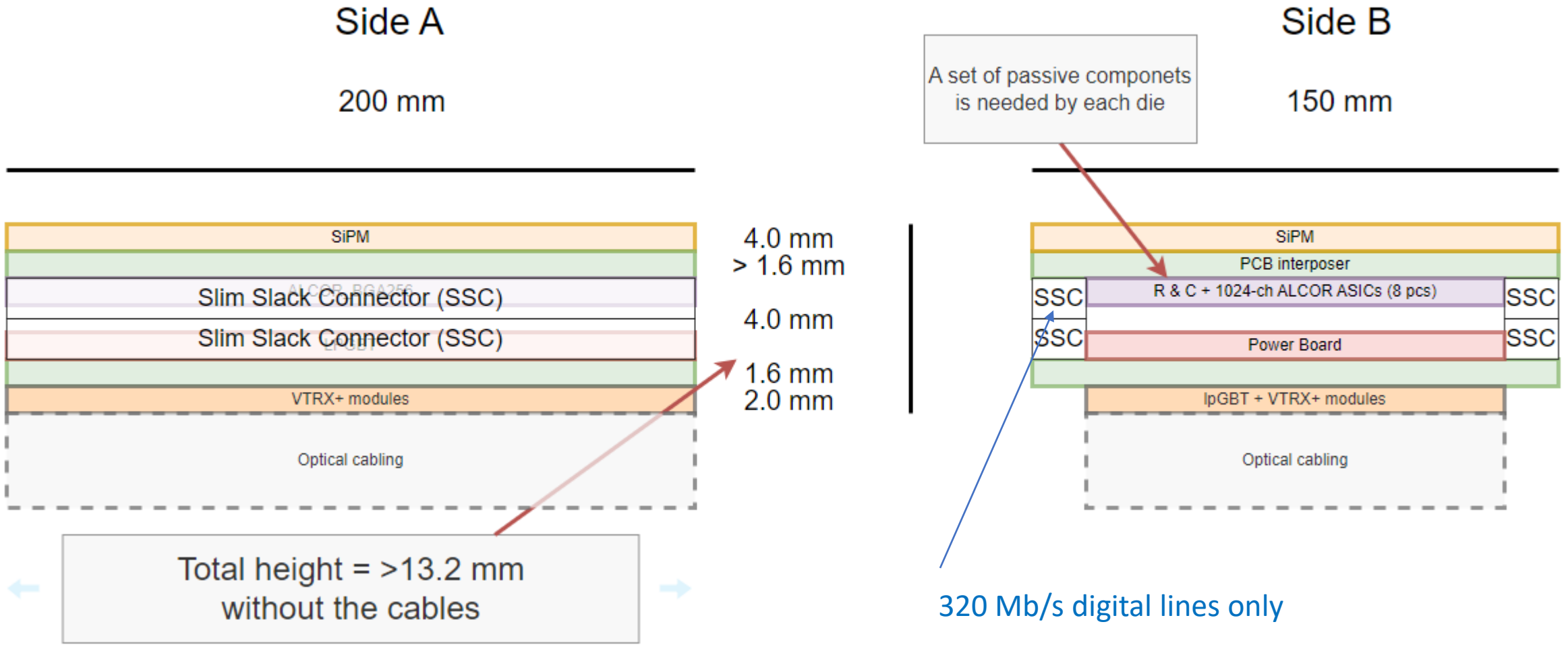
T amb: -40 °C

ALICE-3 RICH FEE: Most critical: the analog board-to-board connections



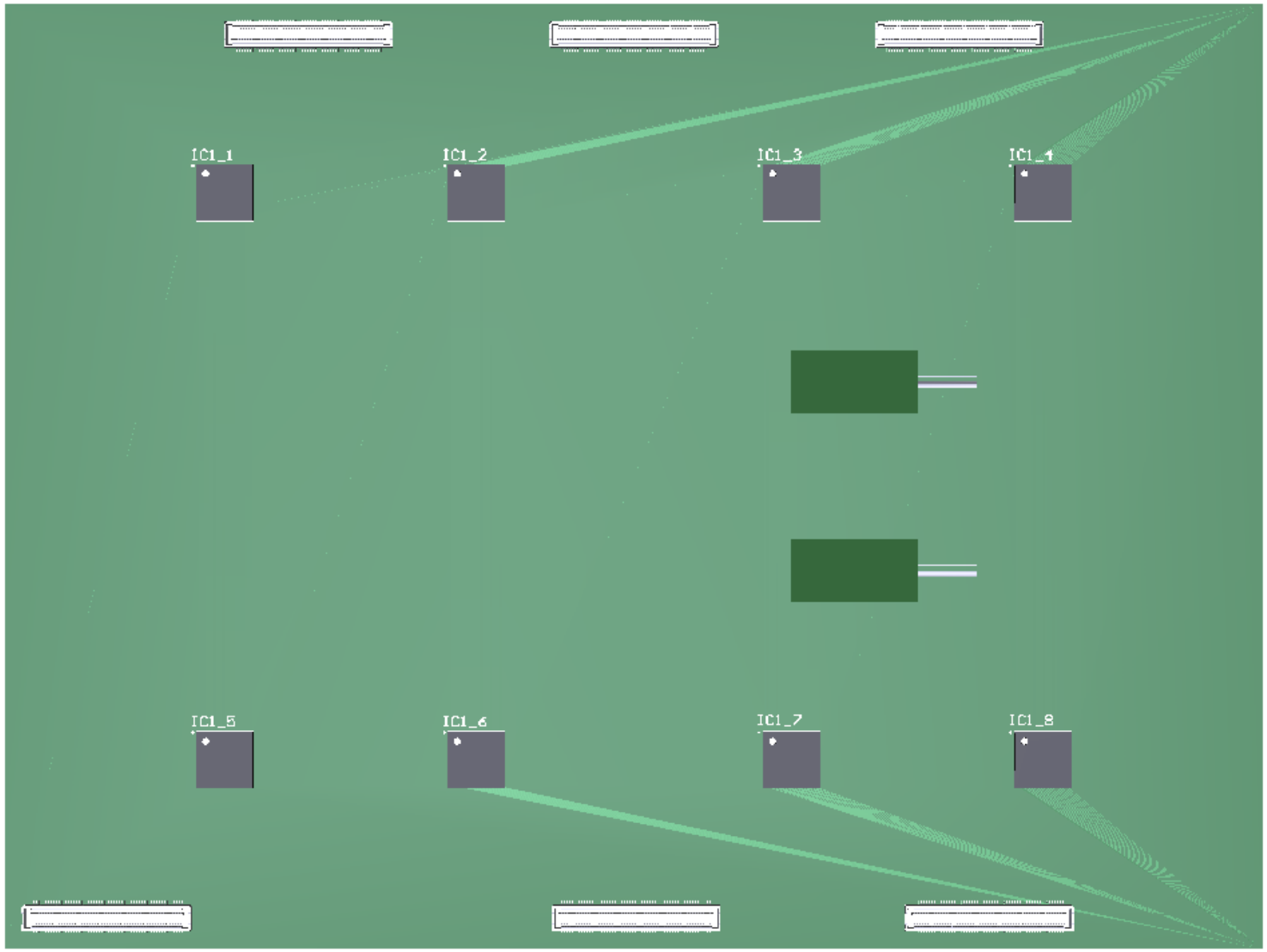
- Not enough connector pins (SiPM – ALCOR boards)
- Not enough board area (ALCOR Board)
- Signal integrity issues (cross-talk, noise)

ALICE-3 RICH FEE: Eliminating the connectors…



ALICE-3 RICH FEE: 1024-ch ALCORs on the bottom of the SIPM board...

The 1024-ch ALCORs moved to the bottom of the SiPM board….



TOP side

8x lpGBT ASICs + 2x VTRX+ /board

- **Components placement is not a problem**
- **Only digital lines (e-Links) go through the connectors.**
- **No. of e-Links coming from the „SiPM+ALCOR" board:** 8x 28 = **224, max.**
- **No. of connector pins needed** between the „SiPM & ALCOR" and the „lpGBT & VTRX+" boards:
  - e-Link signals + GND: 3x 224 = **672**
  - LV for the SiPM+ALCOR board: **hundreds...**
- **No. of connector pins available: up to a few thousands... (see before)**
- **Power dissipation of the „lpGBT & VTRX+" board :**

  $P_{lpGBT} + P_{VTRX+}$ = < **5W /board**

ALICE-3 RICH FEE: LV Supply and Power Dissipation with the 1024-ch ALCOR

LV Current Supply

Current consumption of the FEE components in each Supermodule…

I_{LV} (ALCOR_v3, 8 pcs)	10..12 mW /ch (1024-ch ALCOR)	
	= 70 A, max	@1.2V (remains high!)
I_{LV} (lpGBT, 8 pcs)	= 3.4 A, max	@1.2V
I_{LV} (VTRX+, 2 pcs)	= 0.18 A	@ 2.5V
	= 0.06 A	@ 1.2V

The total 1.2V current consumption of each Supermodule sums up to ~ 75 A

- Supplying 75 A /Supermodule is still very demanding, if feasible
- We would need a ***high number of*** **DC/DC converters (e.g 6, min)** in each Supermodule... **(Issue No. 2a)**
- high density board-to-board connectors (e.g. this SlimStack connectors) can deliver 0.3..0.5A /pin → an additional hundreds of pins are needed for LV delivery **(Issue No. 2b)**
- the even distribution of the current on hundreds of connector pins on multiple connectors can not be guaranteed...

The high LV current need dominated by the ALCORs are still challenging.

Power dissipation /cooling

Dissipation of the FEE components in a Supermodule…

P (1024-ch ALCOR, 8 pcs)	= 84 W, max (remians high!)
P (lpGBT, 8 pcs)	= 4 W, max (see previous slides)
P (VTRX+, 2 pcs)	= 0.5 W, max (see previous slides)

85..90 W /Supermodule

* * *

In this scheme the *total dissipation* of the FEE compnents in the cryogenic vessel (I.e. all 864 Supermodules, 24 rings x 36 segments)

105 W x 864 = **78 kW**, max.

Cooling down the cryogenic vessel to -40 °C while heating it with 78 kW is still a challange, if feasible. **(Issue No. 3)**

To be further evaluated... but the high dissipation dominated by the ALCORs can still be challenging.

But Issue No. 1 (with the connectors) is solved at least, by omitting the connectors between the SiPMs and the ALCORs. (this eliminates >> 7000 signal pins there

ALICE-3 RICH FEE: ASICs need and cost estimations with 1024-ch ALCOR

FEE Components Cost (estimations)

ASIC components need:

• ALCOR_v3:	864 x 8	= 6 912 pcs	? CHF/ea	= ?
• lpGBT ASIC:	864 x 8	= 6 912 pcs	25 CHF /ea	= 173 kCHF
• VTRX+ module:	864 x 2	= 1 728 pcs	140 CHF /ea	= 242 kCHF
• DC/DC:	864 x ?			

Looks much better...

Connectors

• Molex SSC	864 x 14	= 12k+ pcs	< 2.5 CHF & 10K = < 50 kCHF

PCB (bare)

• est.	864 x 4	= 3 500 pcs	~ 300 CHF /ea = ~ 1 MCHF

DAQ /Common Read-out Units (of that time)**:**

lpGBT uplinks: ~ 6 912

CRUs with 48 inputs: ~ 144

... also looks more affordable...

ALICE-3 RICH FEE: Further considerations /1

1. Multiplexing columns of the 1024-ch ALCOR to their digital output lines

- All 32 columns (all 1024 channels) would be available in ALCOR, but only 16, 8, 4, 2, or 1 output data lines would be used depending on the ‚occupancy' of the data channels.
- To make use of this (i.e. to spare with link components) this has to be decided *in advance*, design the PCBs accordingly, then it is frozen... → a safe decision has to be made.
- With 1024 ALCOR channels available, only 7 ALCORs (instead of 8) would be needed in a Supermodule (not a big reduction…)
- The link components (lpGBT and VTRX+ ASICs, CRUs…) could be significantly reduced (by a factor of 2, 4, 8, 16… etc, depending on the multiplexing factor)
  - it can reduce cost, but
  - it does not help in the challenge of LV power supply and dissipation of the FEE that are *technically* the more critical issues

ALICE-3 RICH FEE: Further considerations /2

2. Using a rad-hard data concentrator ASIC (e.g. ECON-D)

- ad-hard ASICs with *e-Link inputs* and *e-Link outputs*
- By *zero suppression* it can reduce data volume and aggregate data of multiple input links to lesser number of output links (before the lpGBTs)
- In ALICE, we will use ECON-D ASICs on the coming FoCal Pads read-out concentrator boards (Run 4), so we will get experience with them
- They can help in reducing the number of the link components (e.g lpGBTs), but they themselves are additional components, designing the FE PCBs will not be easier…

ALICE-3 RICH FEE: PCB Technology Required (Preliminary)

Challange level:

Routing-out of the differential signal pairs of the **0.5 mm pitch BGA** ASICs (lpGBT, 1024-ch ALCOR) is the determining factor in the required PCB technology

The following PCB parameters are foreseen:

layer count

- ~ 16 layers (board thickness is not critical)

track/clearence

- down to 60..70 um

thinnest dielectric layer

- down to 60..70 um

vias/microvias

- microvias: 0.25/0.12 mm (diameter/hole), or smaller...

Potential PCB manufacturers exist:

Exception PCB, Somacis, others...

ALICE-3 RICH FEE: Summary and Take-away Message

The first concept is based on the

- array of 2x2 mm SiPMs
- the („already 2-years old”) ***64-channel ALCOR_v3*** digitizer ASIC,
- direct read-out with rad-hard lpGBT optical links

Newer verisons of ALCOR is foreseen with preliminary specifications

- 1024 input channels
- to be followed up and participate in the requirements specification

The feasibilty study of this concept based on the 1024-ch ALCOR, that consist of

- a conceptual design,
- simulations, and
- trial implememntations

has been started.