Muon ID Electronics: plastic scintillator option

October 10, 2024

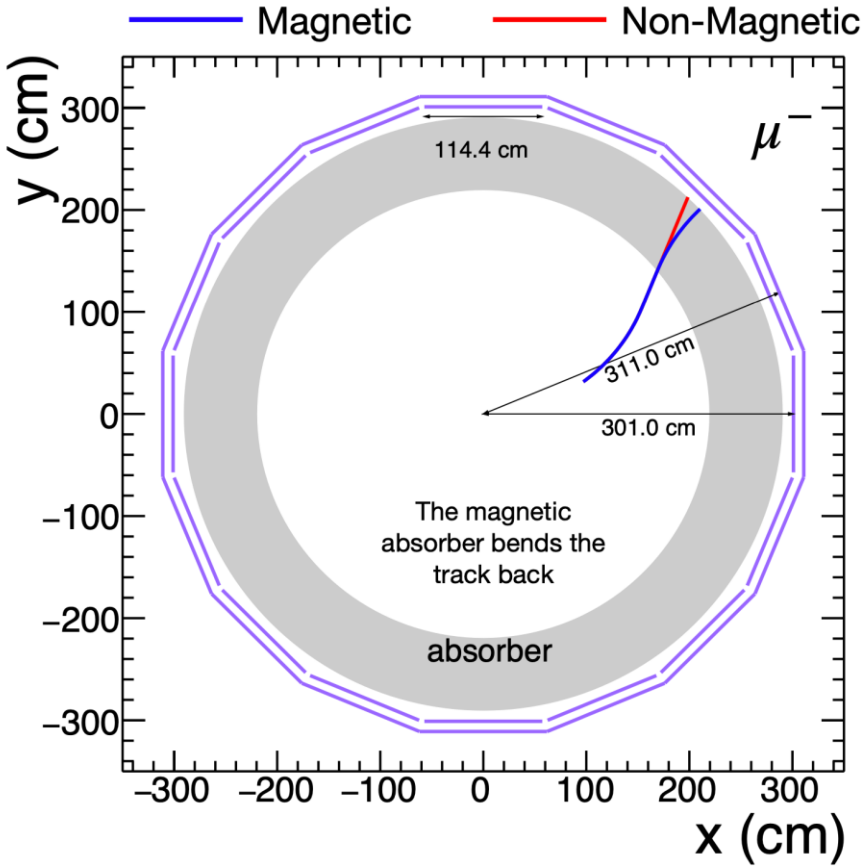
Guillermo Tejeda, for the MID-Mexico electronics group

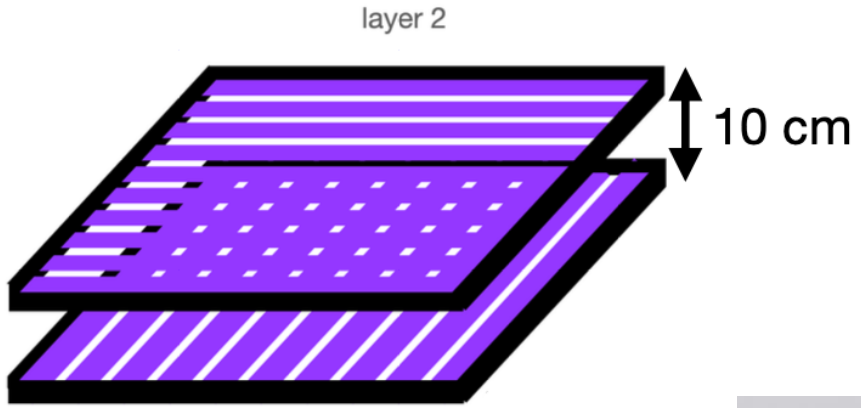
Outline

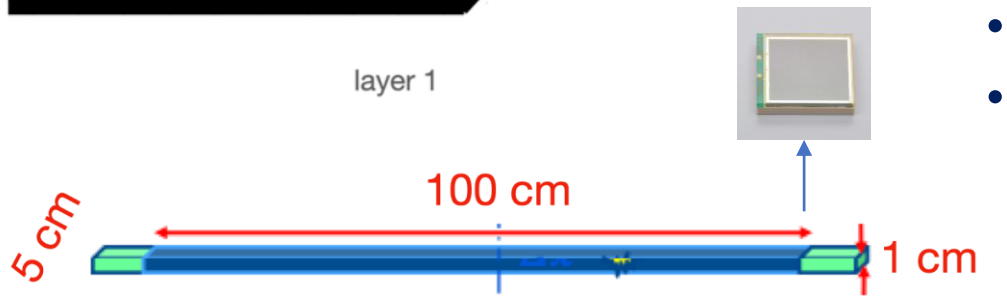
- Introduction
- FEC Design
- Patch Panel Design
- FEC Version 2
- Organization
- Summary

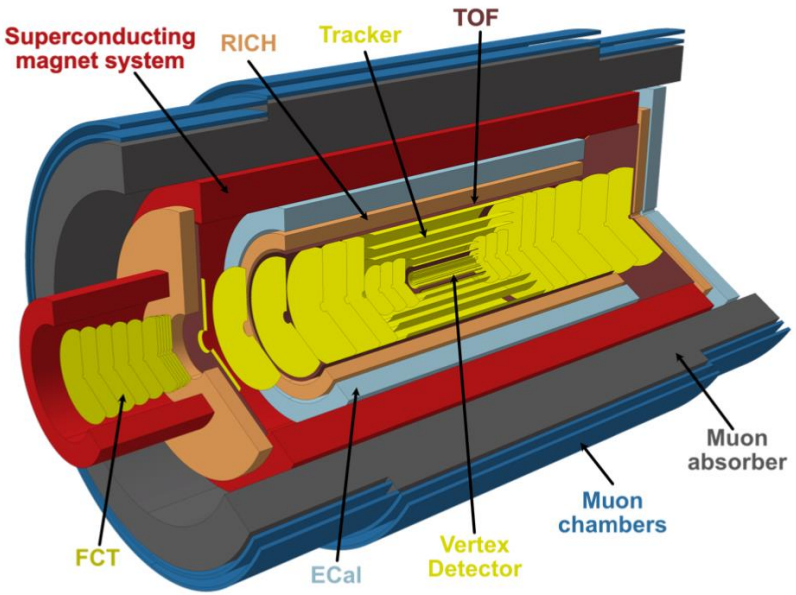
MuonID Detector

Plastic Scintillator Option



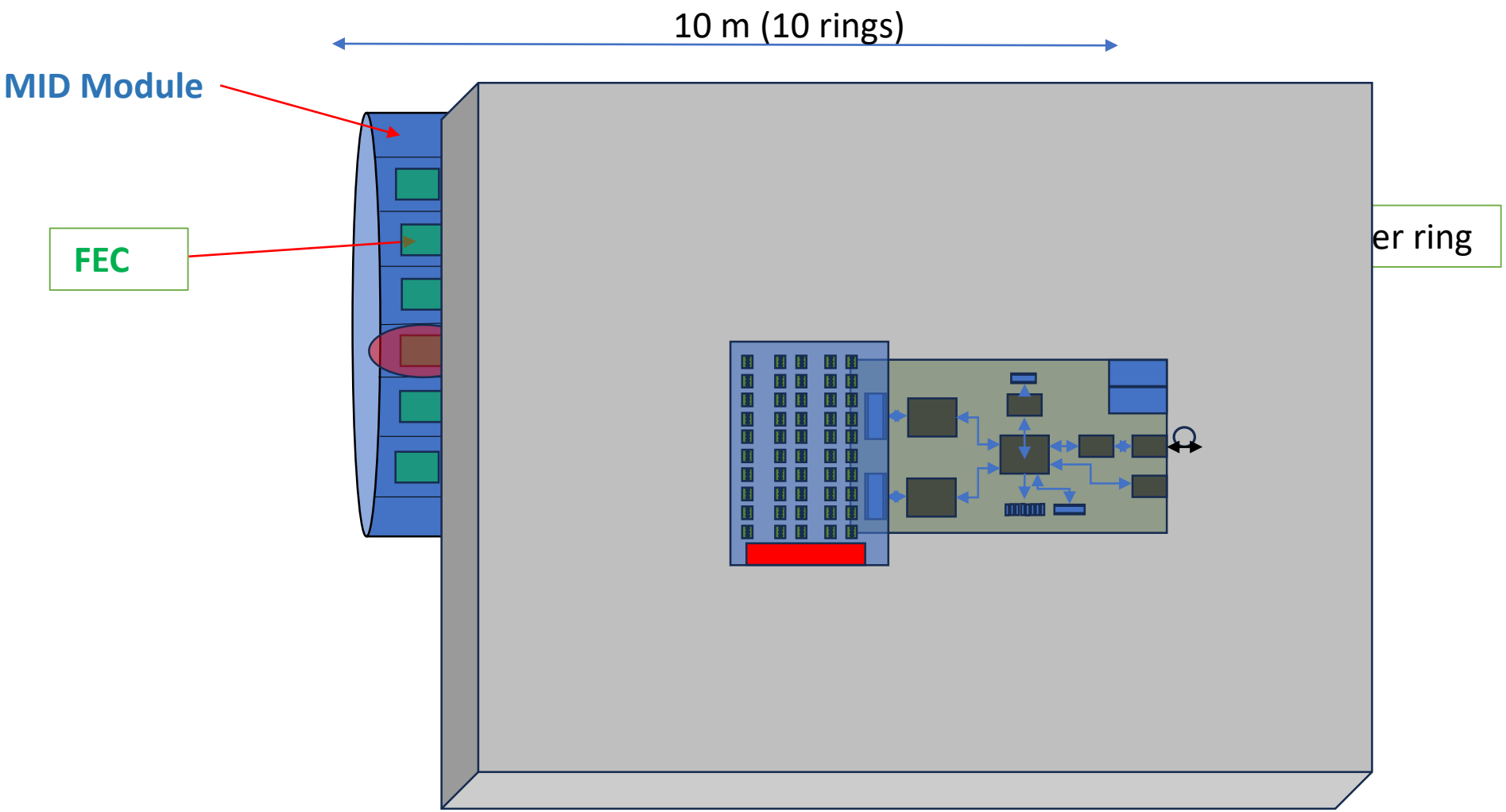






- Assumptions:
  - 10 rings
  - 16 segments per ring
    1 chamber per segment
    40 channels per chamber

Channels Distribution (Option)



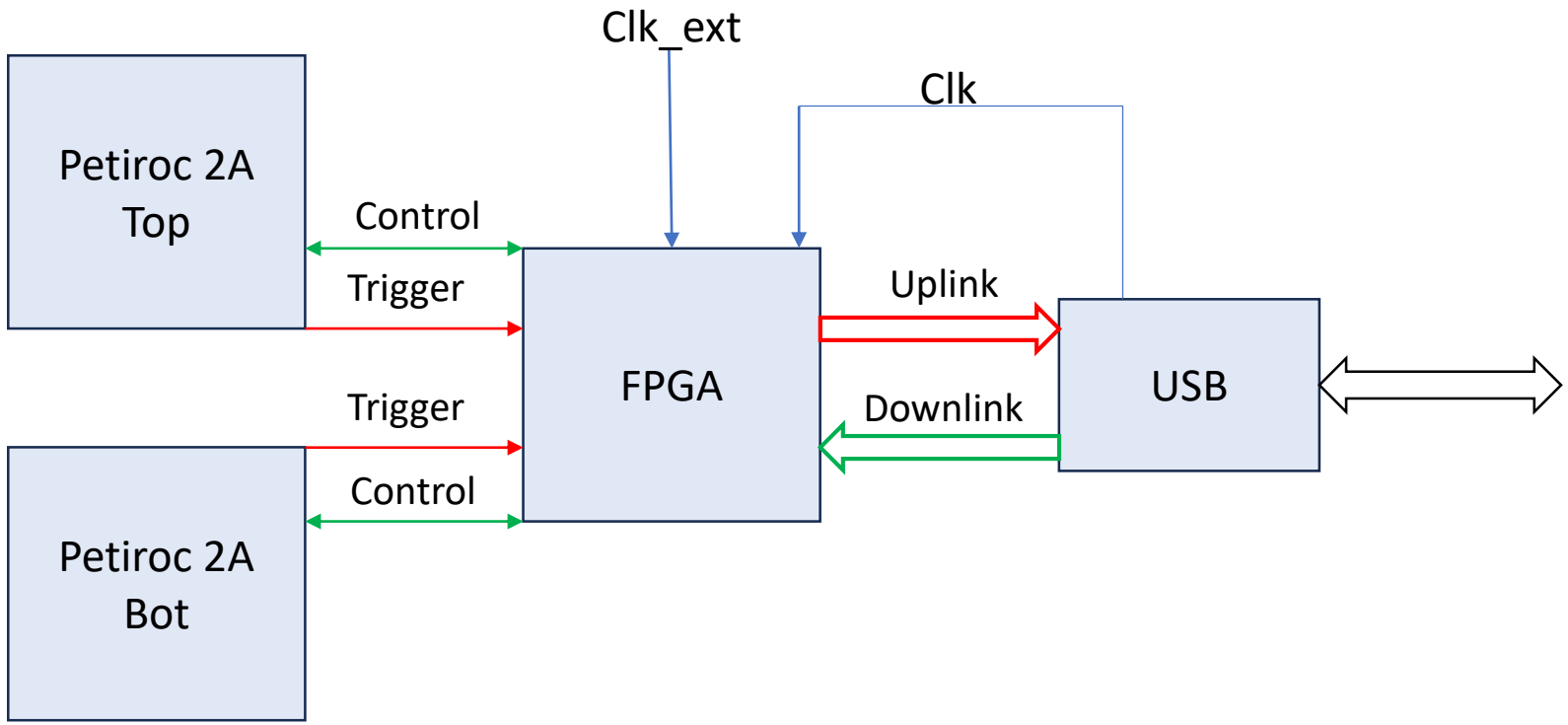
160 FECs in total

40 channels/FEC

Energy & Time measuremnt

Required 160 optical links for all modules

MuonID FEC details



1 FEC/Module 160 (10 spares) FEC in total

2 Erni connectors with 32 ch each

2 ASIC Petiroc 2A

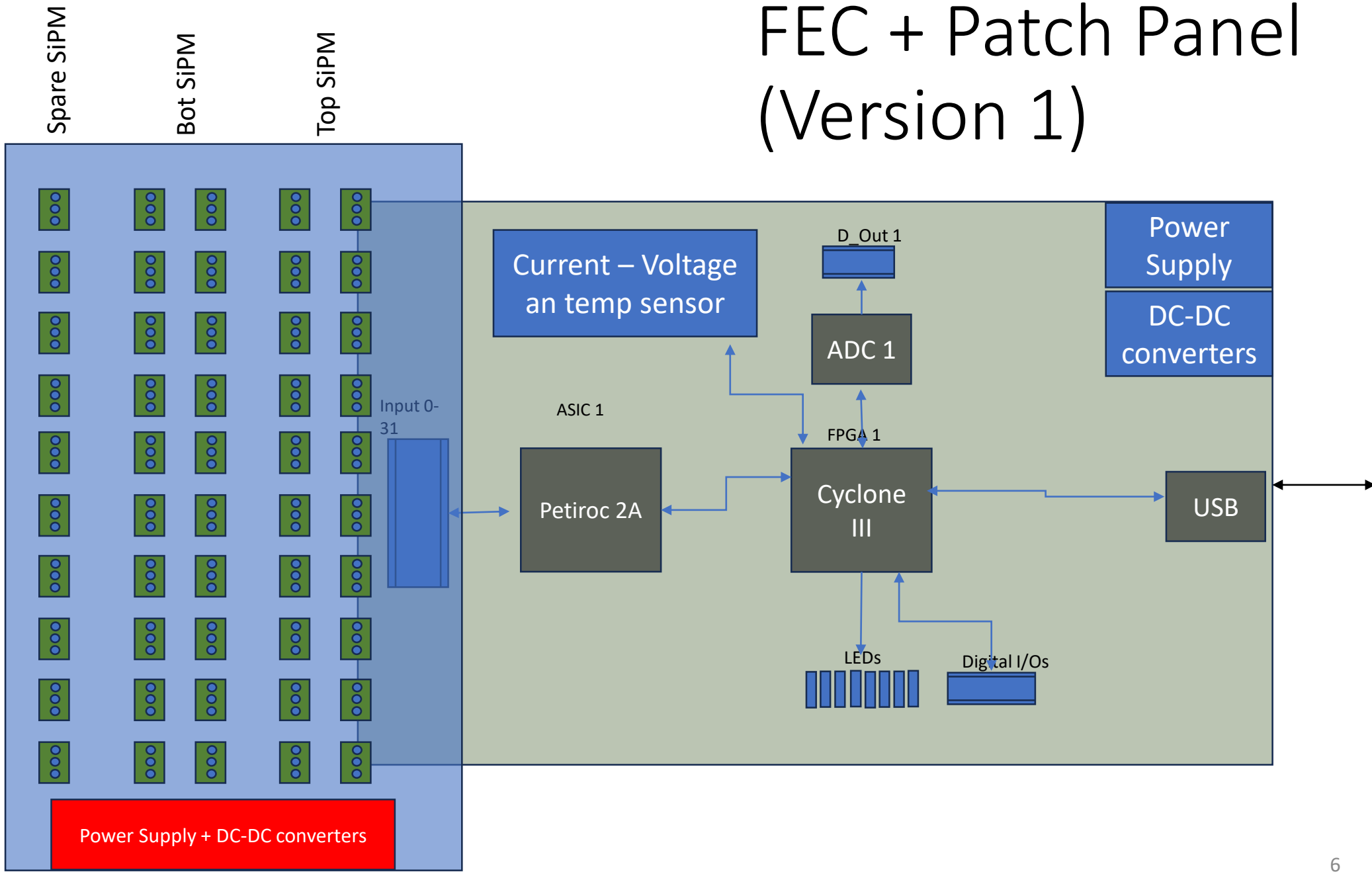
1 FPGA Cyclone V
(non Rad-Hard 5cgtfd5c5f23c7n)

1 LpGBT + VtRx
(for communication and Slow control)

Power supply regulators zone

FEC + Patch Panel (Version 1)

- 1 ASIC Petiroc 2A
- 1 FPGA Cyclone III (non Rad-Hard)
- USB communication and debugging
- 32 Channels input
- Charge and Time measurements
- Channel by channel SiPM high voltage adjustment
- 6mW/channel power consumption

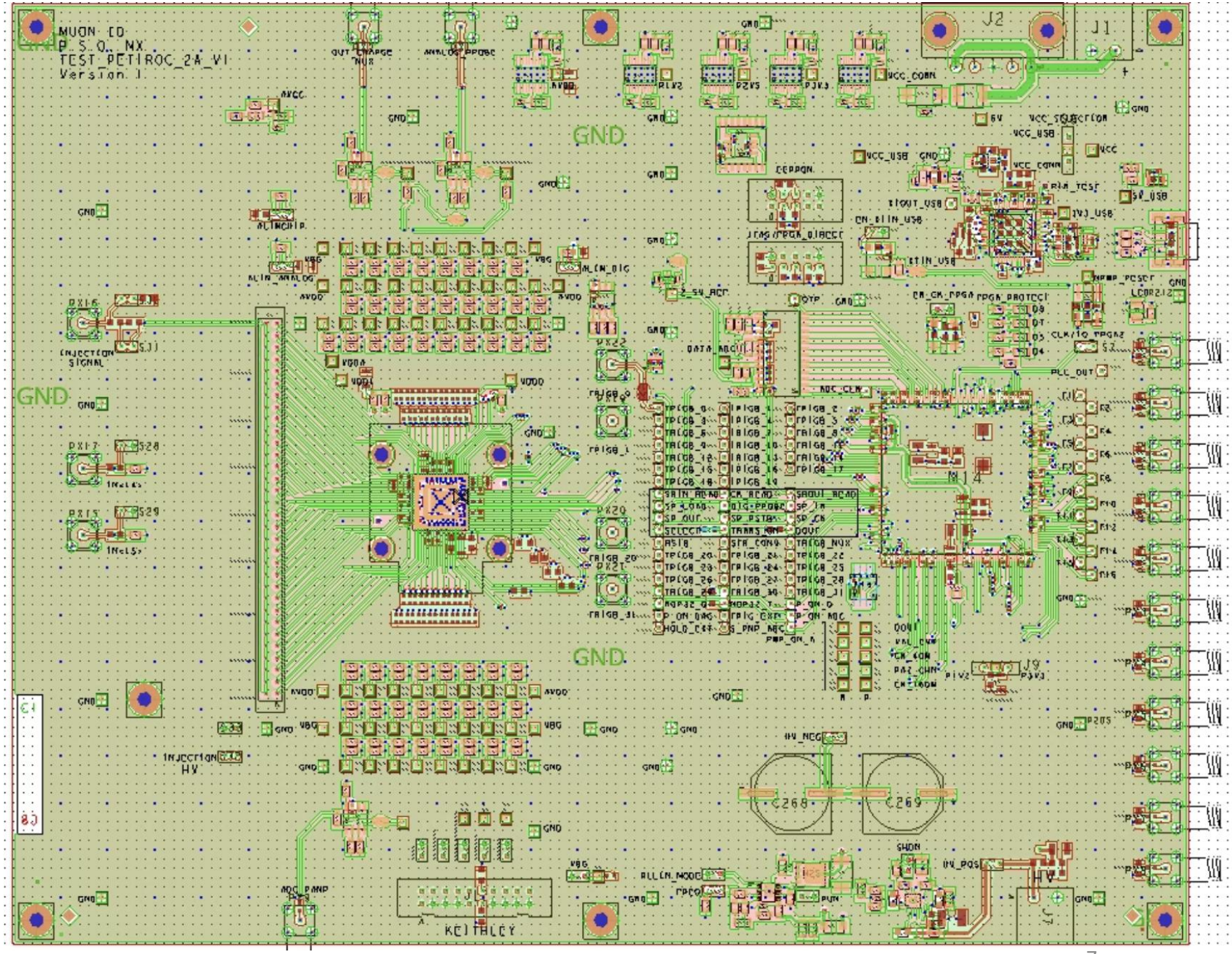


FEC
Final Design

- 25 x 20 cm
- 1 PETIROC 2A (32 Ch)
- FPGA Cyclone

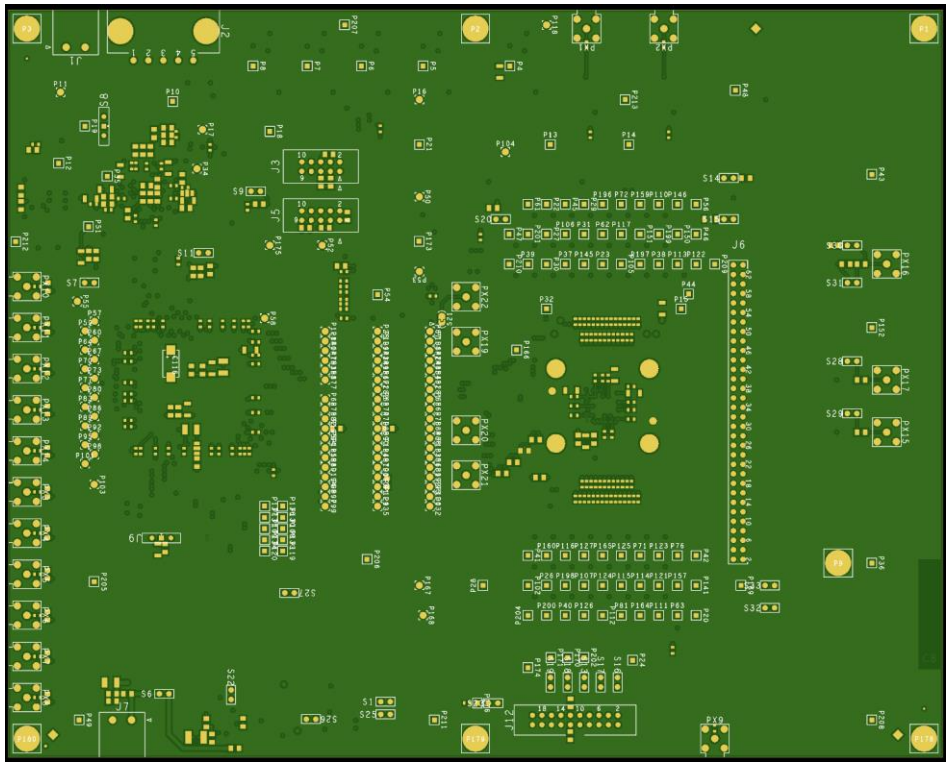
- In production (PCBWay)

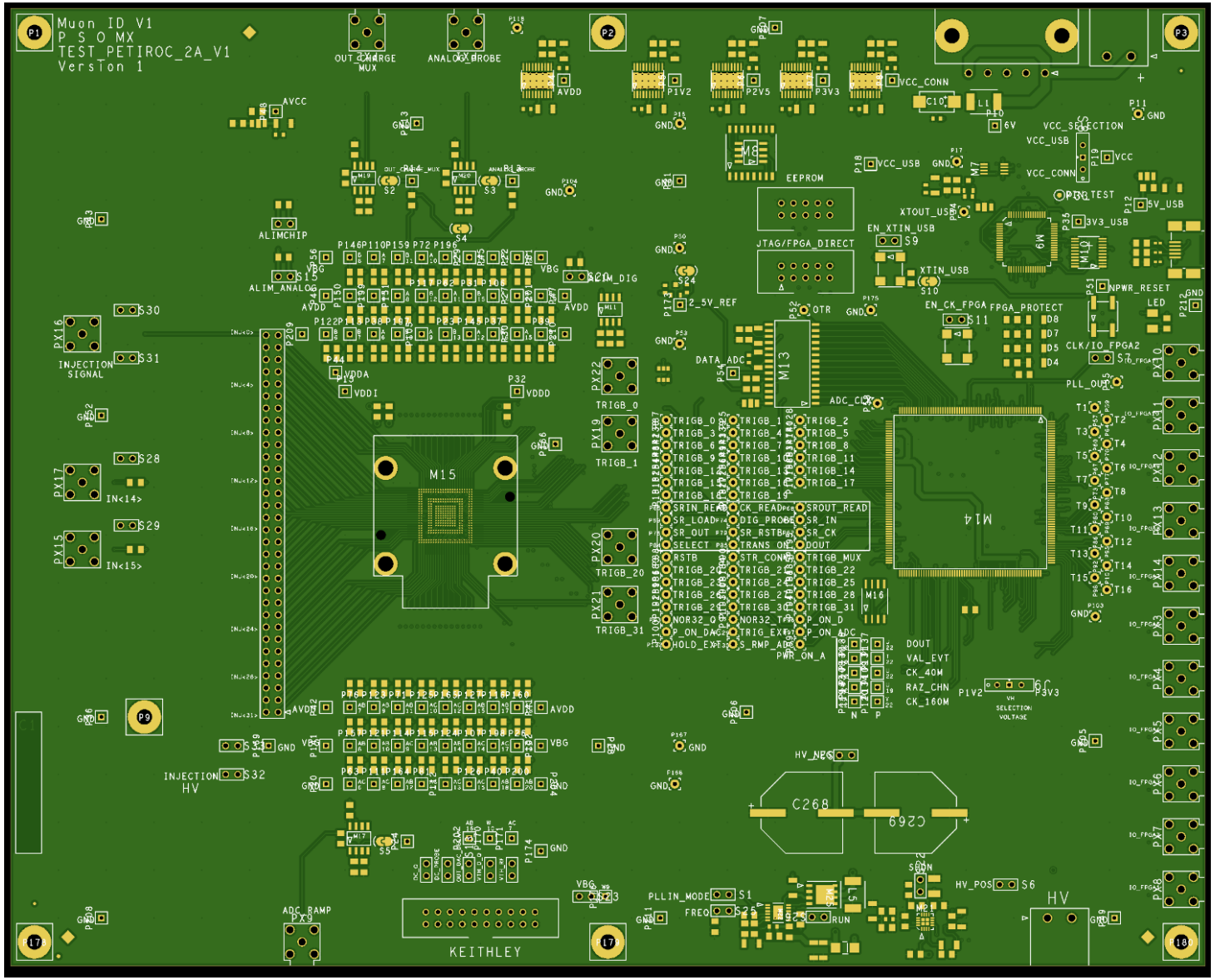
- Many details
  - Wrong gerber generation
  - Extra ring around PCB
  - No drill files
  - No outline layer



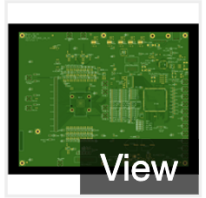
In production

- Fabrication in progress after many issues

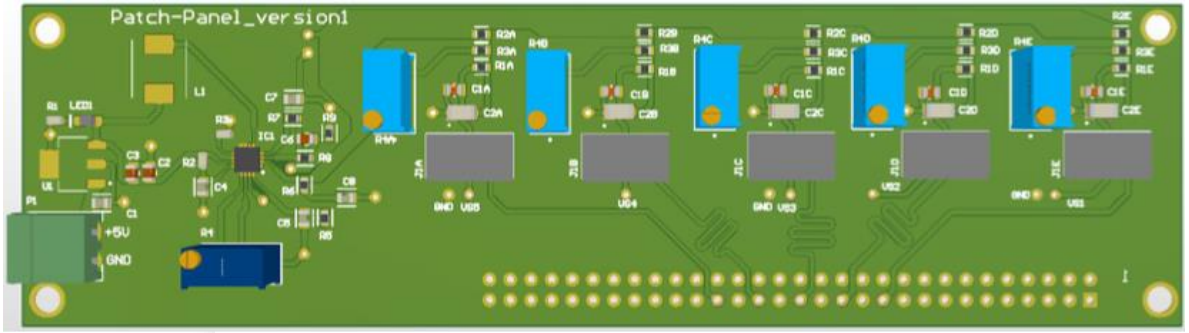




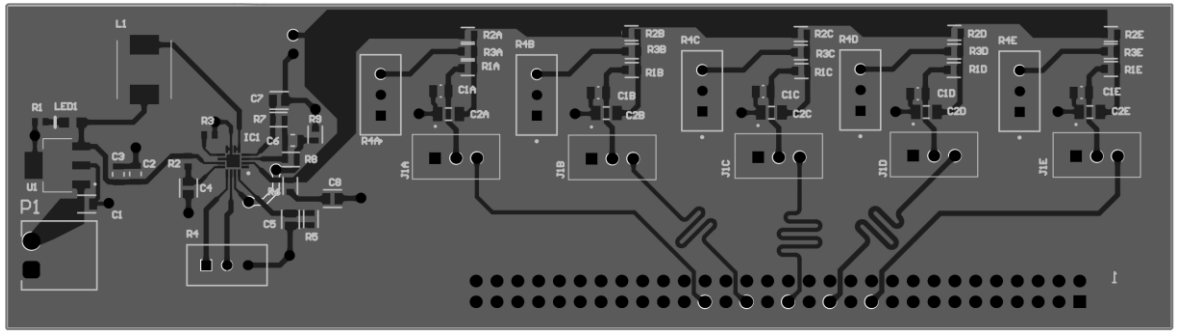
Fabrication Progress

Product	Product Action	Order Status
Order ID: G1336169 Delivery Address Order time & date : 2024/9/18 8:06:11	Service: Daphne Liu Contact sales-rep (0 unread)	
 200x250mm 8 Layers,Thickness:1.6 mm, Finished copper:1,Surface finish:Immersion gold [Product No.: W07941ASD18] $ 1035.43 & 5Pieces Build Time: 16-17 days	GerberPR2R2 (2).zip 19 + PCB Assembly 54 % today	In fabrication View Detail

Patch Pannel (V1)

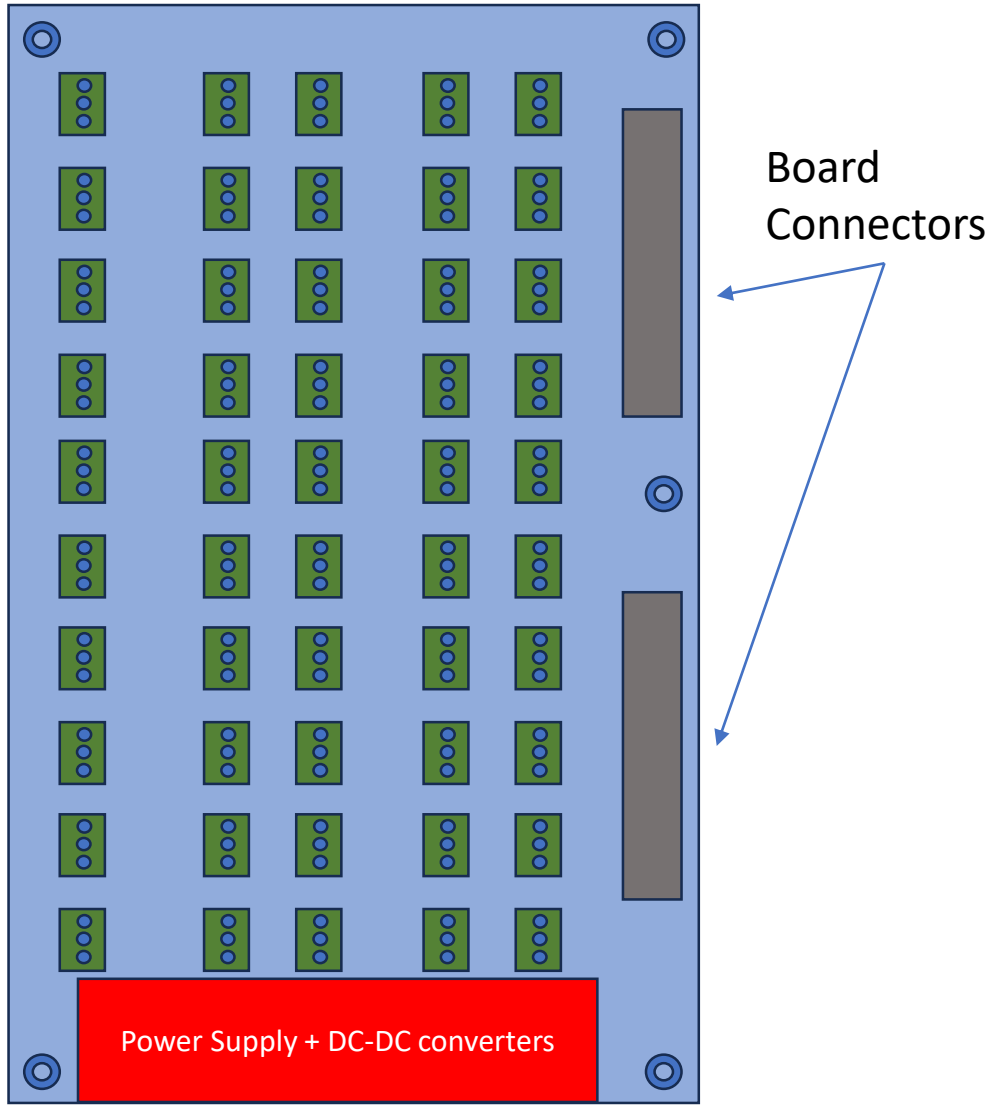


- 5 Channels PCB completed
- Power regulator included in PP for 5 SiPM
- To test Power regulator, noise and signal integrity



Patch Pannel (V2)

- 50 Channels
- Upgrade of the first patch pannel version
- Schematic is in progress



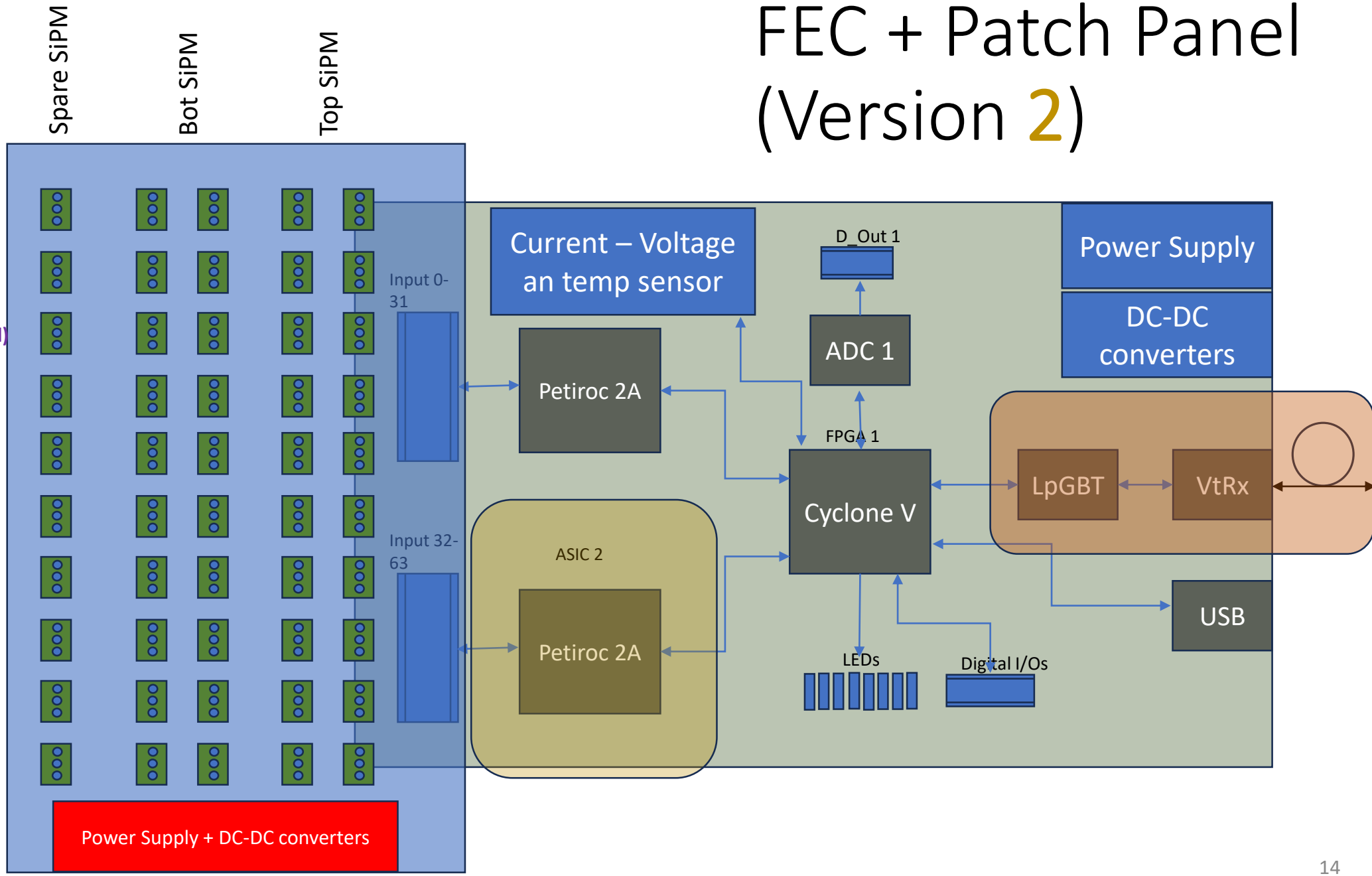
User Interface

- Compatible with Weeroc Test Board
- Working on start procedure:
  - Connnects USB cable
  - Power up power supply
  - Start Software
- Slow Control:
  - Load slow control parameters
  - 640 bits will be sent twice

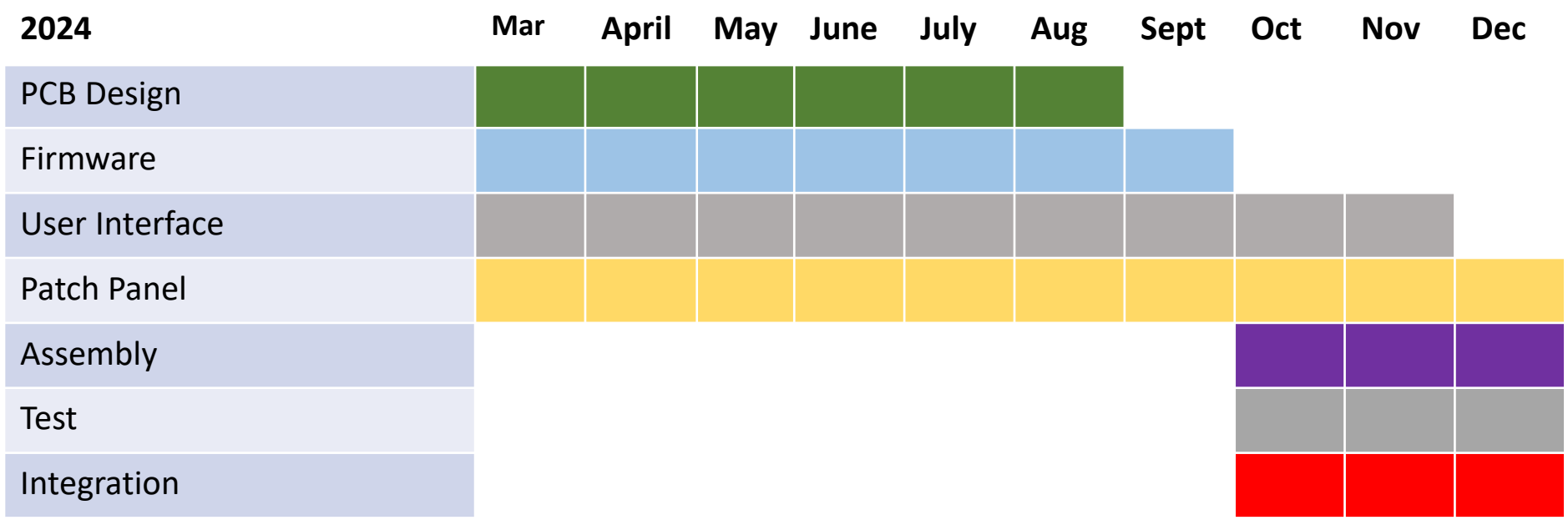
- Calibration:
  - Calibrate the 6-bits DAC settings of each channel
- Data Acquisition:
  - Number of acquiisitions
  - Trigger mode (under revision)
  - Output file and format
- Preparing technical documentation
  - Manual FEC
  - Manual Interface

FEC + Patch Panel (Version 2)

- 2 ASIC Petiroc 2A
- 1 FPGA Cyclone V (non Rad-Hard 5cgtfd5c5f23c7n)
- 1 LpGBT + VtRx+ (for communication and Slow control)
- USB communication for debugging
- 50 Channels input
- Charge and Time measurements
- Channel by channel SiPM high voltage adjustment
- 6mW/channel power consumption
- Version 2 -> 2025



Time Line (FEC Version 1)



FEC V1 will be tested in 2025 Beam Test with the Muon ID module

Radiation Tolerances

- FEC located in a region with a “moderate” radiation dose estimated by simulations.
- Not negligible for our FPGA. We are still investigating different ways for a save operation.
- FEC will be tested under radiation sources to observe aging effects or SEU.

Summary 1/2

Firmware

- Slow control Register -> ok
- Probe Register Parameters -> ok
- Read Register for analogue Read Out -> ok
- USB interface -> ok
- ReadOut -> ok

PCB -> In production

- Next steps:
  - LpGBT (FPGA)
  - Include second Petiroc

FEC PCB

-Schematic and PCB Version 1 -> 100%
-Schematic Version 2 -> 20%

Patch Panel

-Version 1 -> 100 %
- Version 2 -> 20 %

User Interface

Testing USB port -> 80%

Summary 2/2

- Waiting for cards to start with test
- Development of the FEC Version 2
- Development of the PP version 2
- Development of the LpGBT communication protocol
- Integration of the FEC V1 with a Muon ID Module

Muon ID Electronics Organization

- Sinaloa
  - Carlos Duarte Galvan
  - Juan Manuel Mejia Camacho
  - Cesar Regalado Elenes
  - Juan Carlos Cabanillas
- UNAM
  - Enrique Patiño Salazar
  - Saul Aguilar
- Puebla
  - Emigdio Jimenez Dominguez
  - Yael Antonio Vazquez Beltrán
  - Guillermo Tejeda Muñoz

- Luis A. Pérez Moreno

FEE

Grafic Interface

SiPM

FEC-PCB

FEC-Firmware

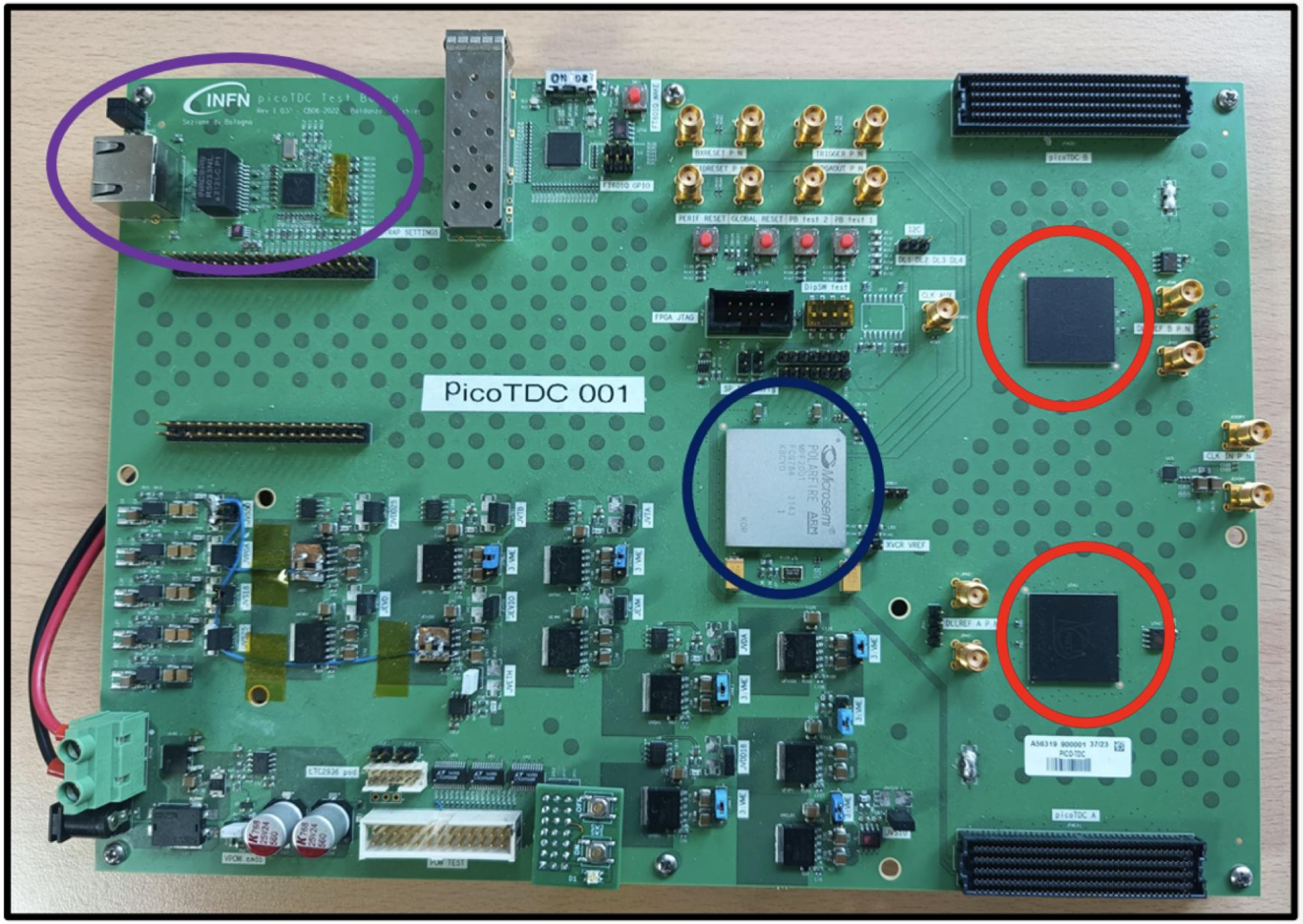
Communication protocols

Bi weekly meeting for preparation of the electronics proposal and TDR

Thank You for your attention

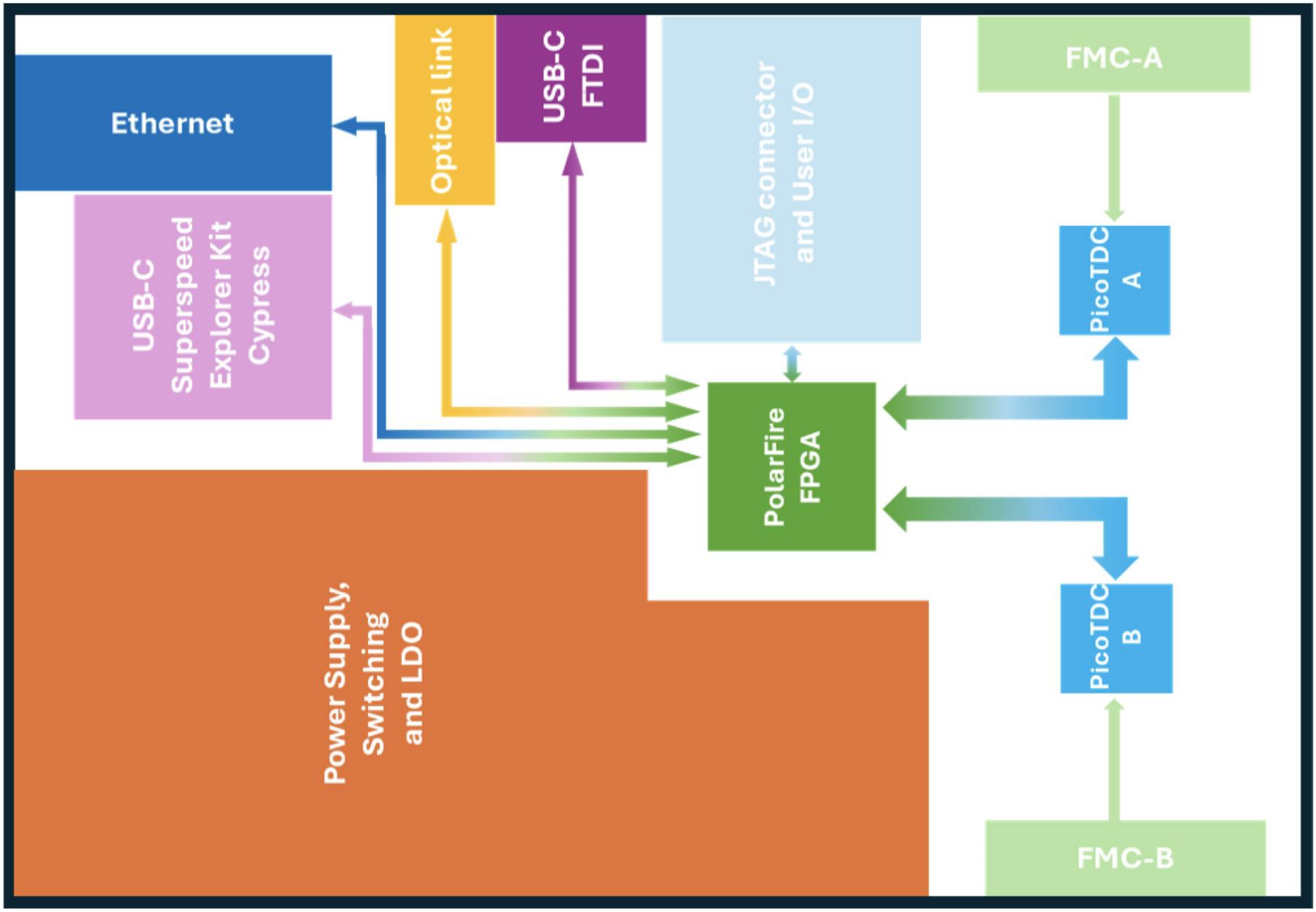
TOF design

PicoTDC board
PolarFire FPGA (blue)
2 PicoTDCs (red)
Ethernet connector subsystem (purple)



- FPGA based design

- PolarFire MPF200T FCG784E



Dose tolerances (from CMS)

- TID (γ´s):
  - FPGA Cyclone V (50Gy)
  - Petiroc 2A (160Gy)
  - Power Regulators (100Gy)
- TNID (Neutrons):
  - 25e11 neq1MeV/cm^2
- Neutron flux:
  - 450e3 neq1MeV/cm^2/s

SEU expected in FPGA

Expected fluence and dose (MID zone):

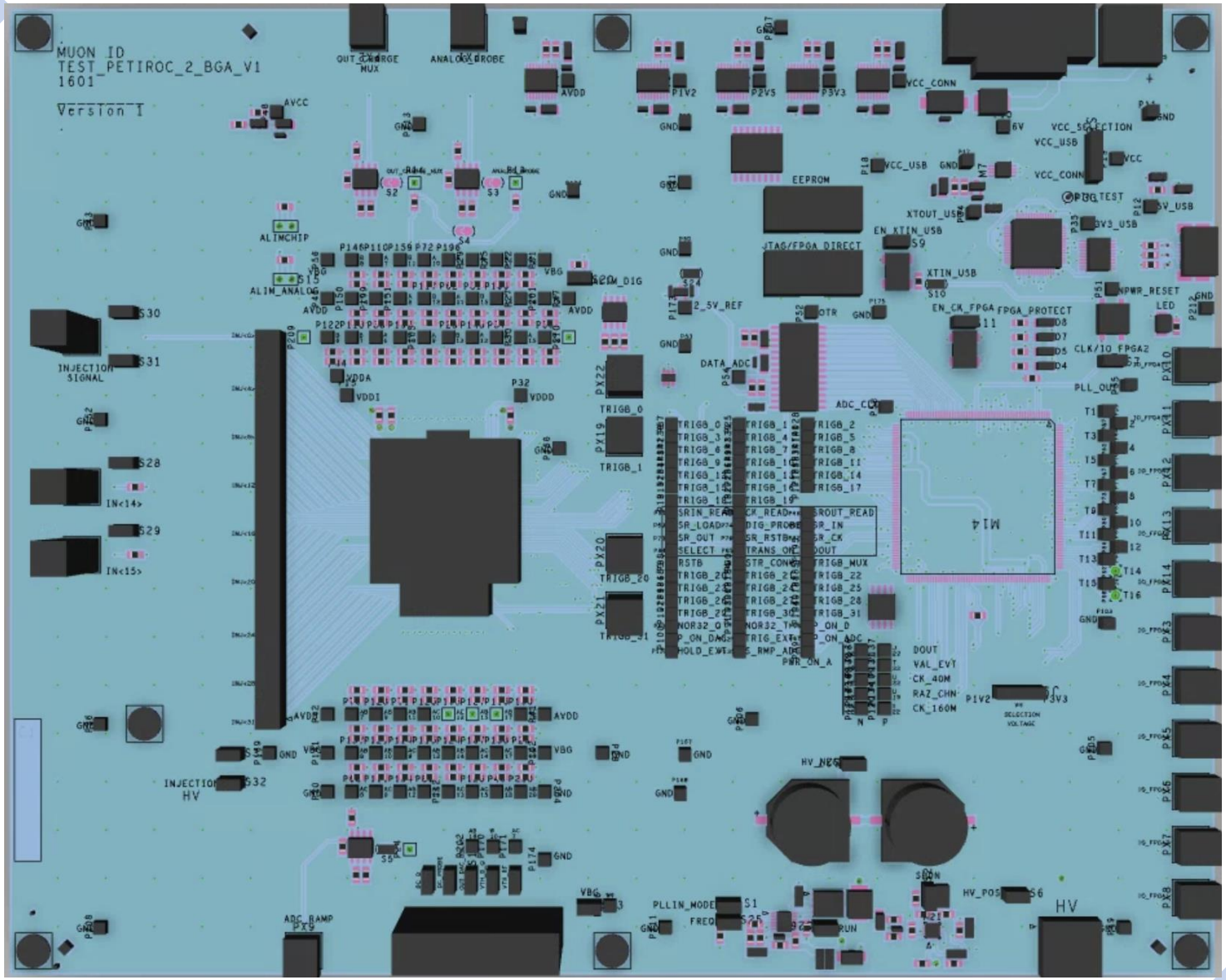
Radiation load for Run 5+6 in the MID

	R = 301 cm	
	pp	Pb-Pb
TID (rad)	54	0.94
NIEL (1 MeV neq/ cm^2)	3.4 x 10^{10}	4.7 x 10^8
HEH (Hz/cm^2)	17	4.3
Ch. particle fluence rate (Hz/cm^2)	3.6	1.1

Table 3. Radiation load in the MID simulated with FLUKA considering ***Run 5+6 period and assuming a running efficiency of 65%.***

25 cm

20 cm



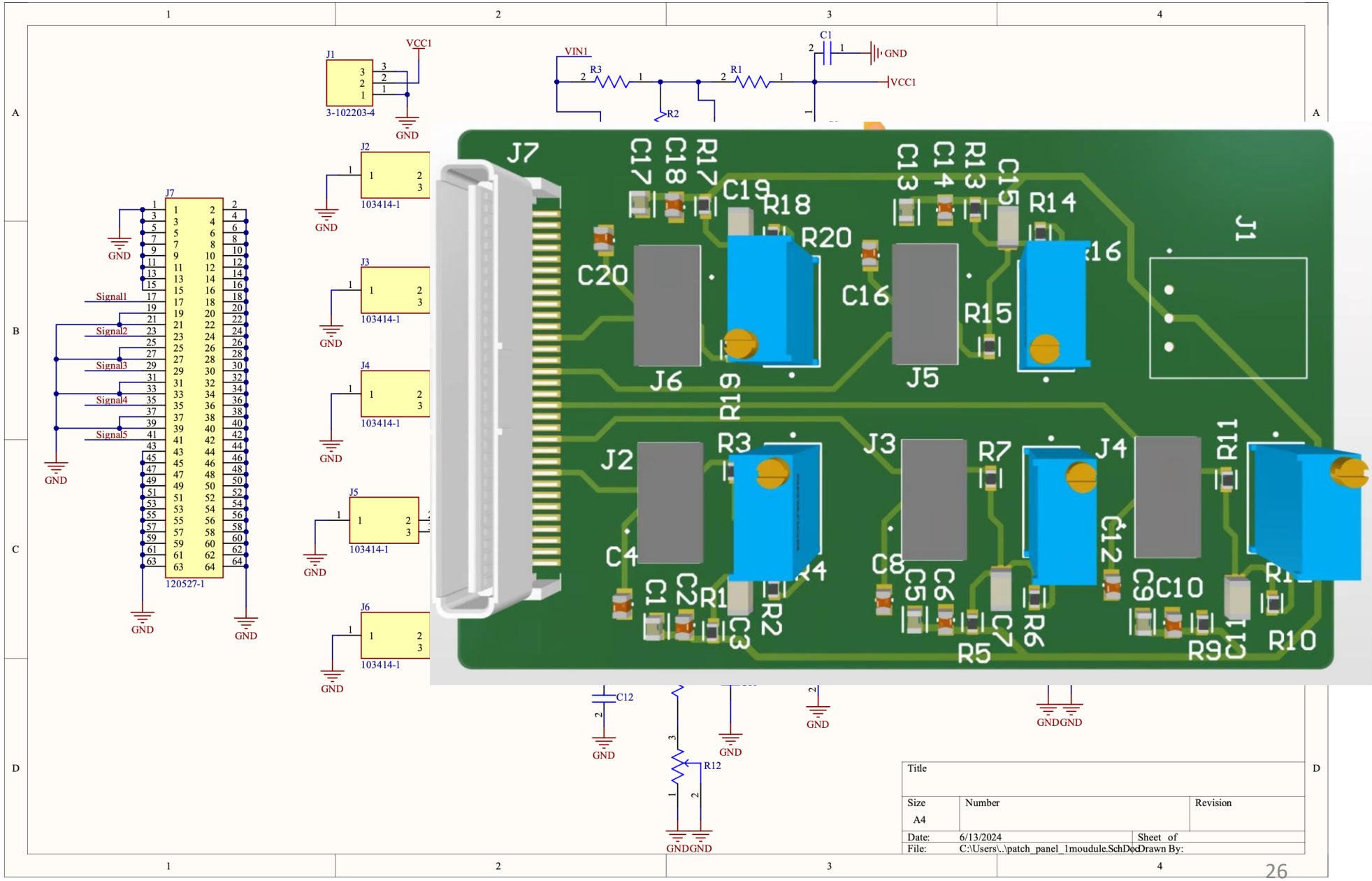
-Design Rule Check (ok)
-Gerber Files
-8 layers
-32 Channels
-USB communication

-80% parts available

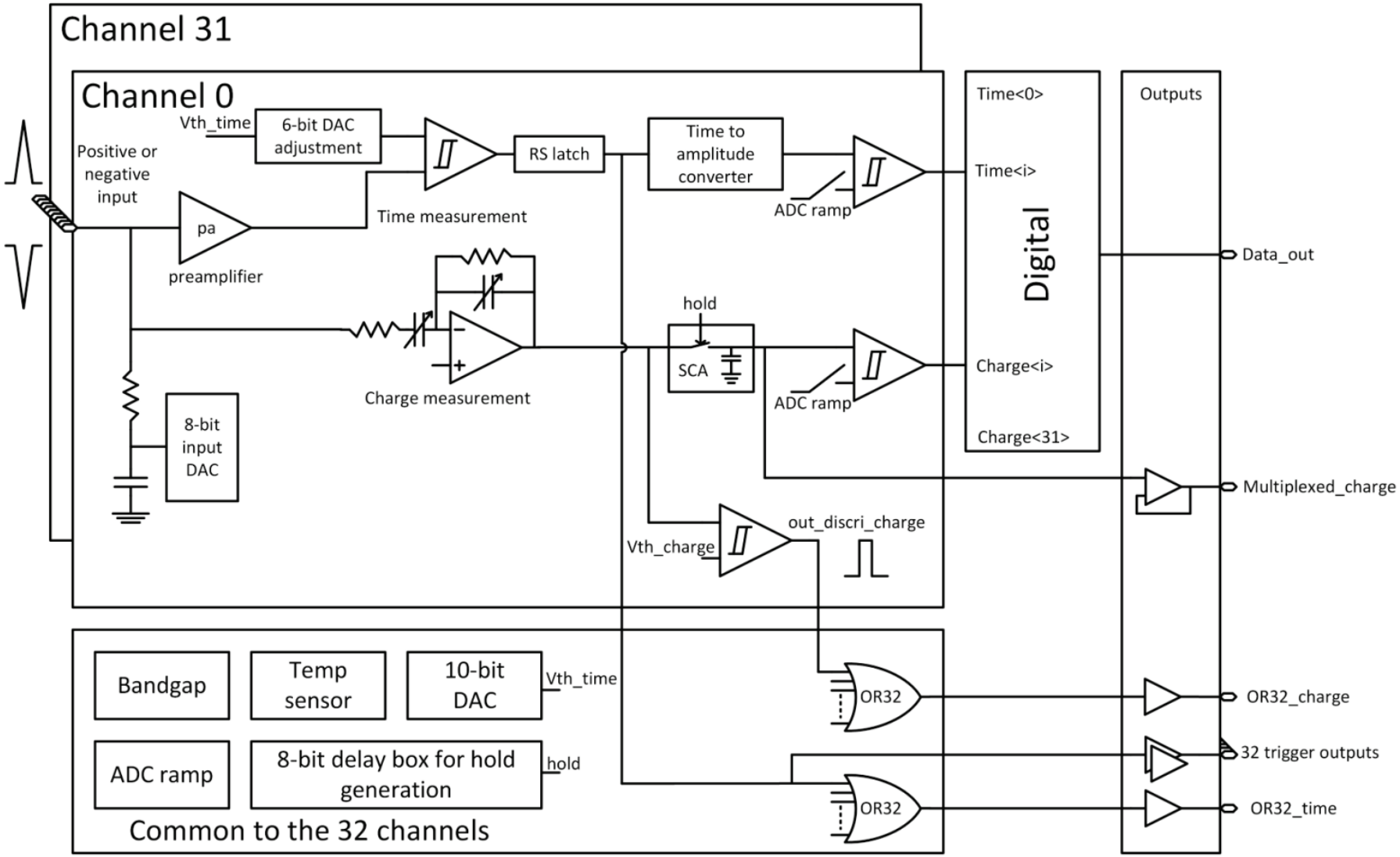
Recuerde que tiene que considerar una PCB para destrucción junto con un chip.

Patch-Panel Schematic Partial

First version to test:
Crostalk
Noise
Stability



Petiroc 2A


Channel 31
Channel 0
Vth_time
6-bit DAC adjustment
RS latch
Time to amplitude converter
ADC ramp
Time<0>
Time<i>
Digital
Charge<i>
Charge<31>
Outputs
Data_out
Positive or negative input
pa
preamplifier
Time measurement
hold
SCA
Charge measurement
8-bit input DAC
Multiplexed_charge
Vth_charge
out_discri_charge
Bandgap
Temp sensor
10-bit DAC
Vth_time
OR32
OR32_charge
32 trigger outputs
ADC ramp
8-bit delay box for hold generation
hold
OR32
OR32_time
Common to the 32 channels

Specifications

Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353
Power Consumption	Power supply: 3.3V 192mW Analogue core (excluding analogue outing buffer), 6mW/ch
Inputs	32 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 40ps bin) 32 trigger outputs 1 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger outputs (Trigger OR on 32 channels, 2 levels)
Internal Programmable Features	32 HV adjustment for SiPM (32x8b), trigger threshold adjustment (10b), charge measurement tuning, 32 trigger masks, internal temperature sensor, trigger latch