# FIT FEE upgrade for the future ALICE 3 FD detectors

## at AGH University of Krakow

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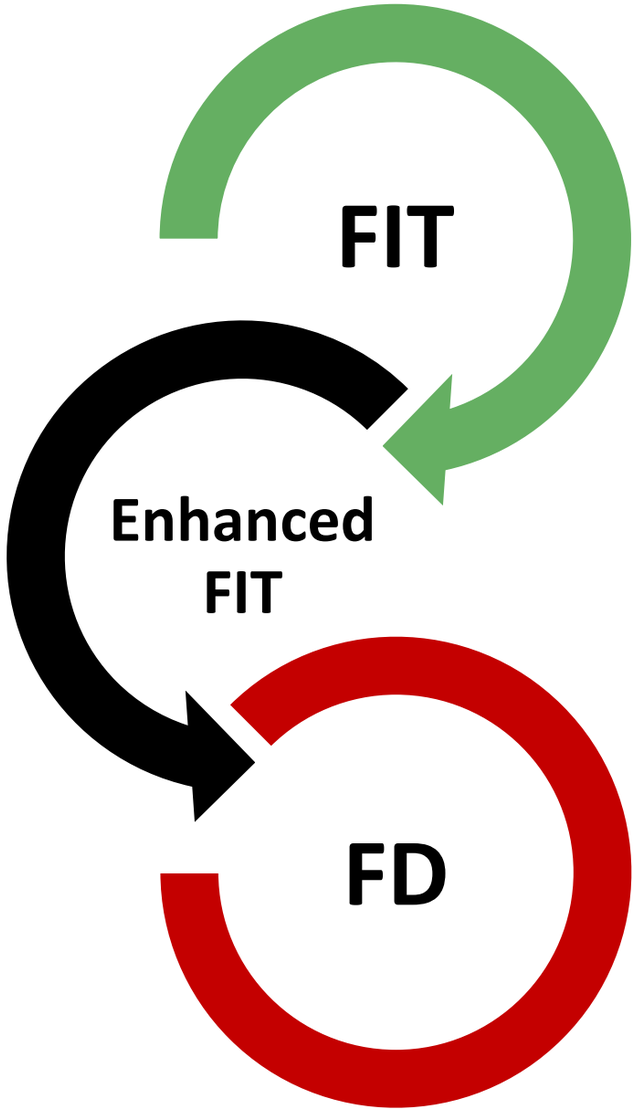
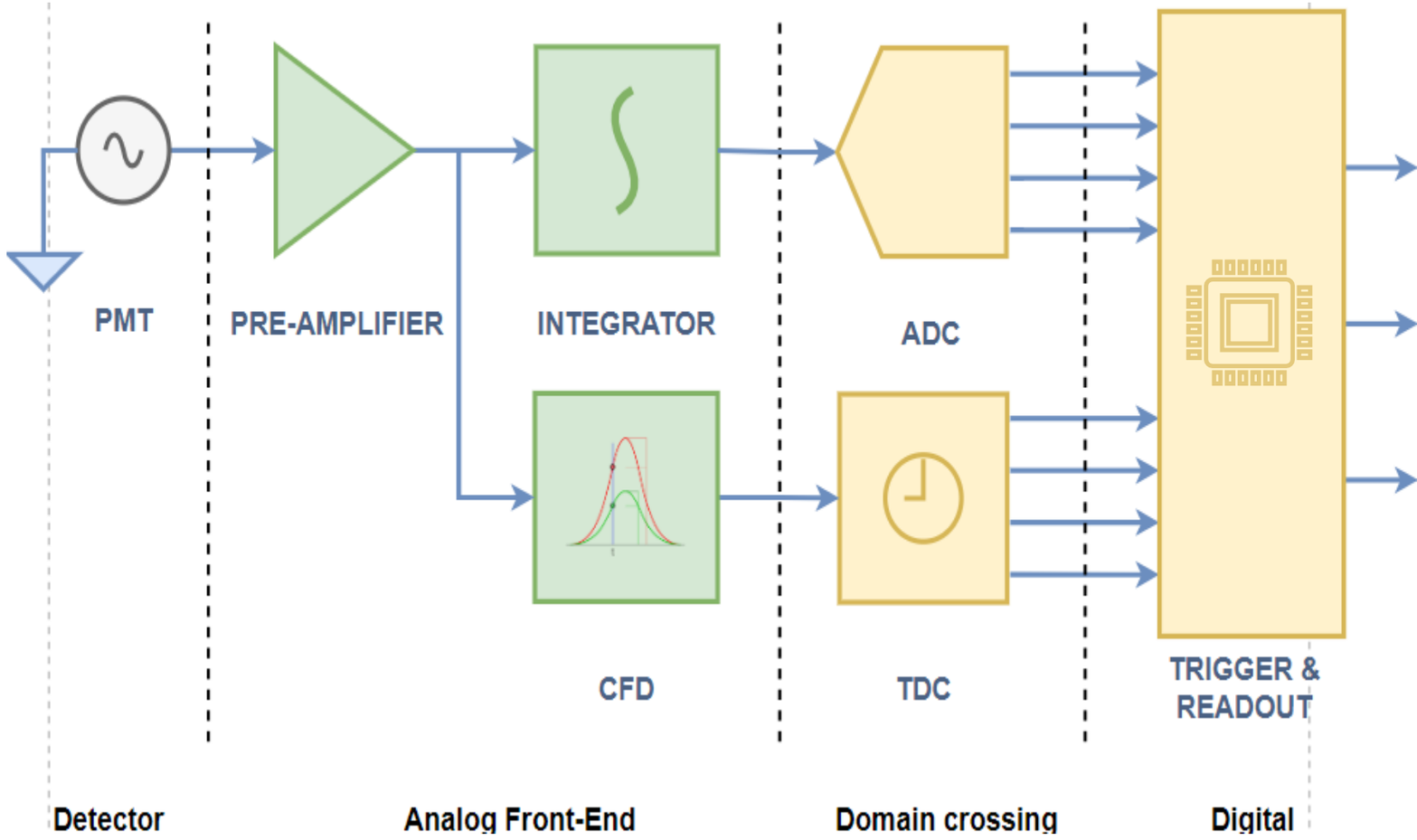
# Main activities at AGH

- Enhancement of analog front-end FIT readout electronics:
  - goal to achieve measurments with:
    - 14 bit charge resolution,
    - system RMS jitter  < 20 ps.
  - the pre-amplifier improvement for better signal dynamics
  - new architecture of the charge integrator to increase precision,
  - launch of the ASIC project to increase overall AFE performance.
- High frequency direct sampling of PMT signal



# Readout electronics processing datapath

- AGH University group focuses on analog front-end
- Goal is to increase:
  - overall system time resolution <20 ps,
  - detector signal range,
  - Precision (14-bit)

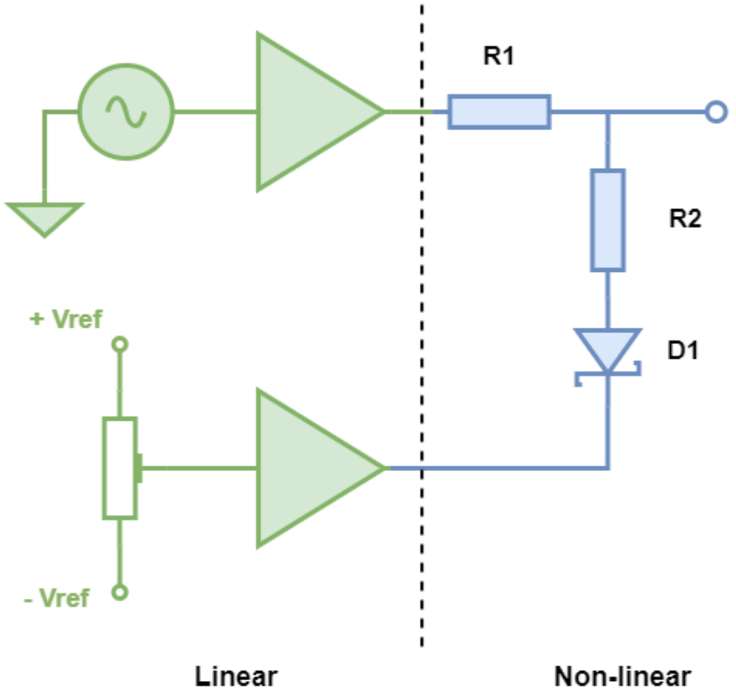


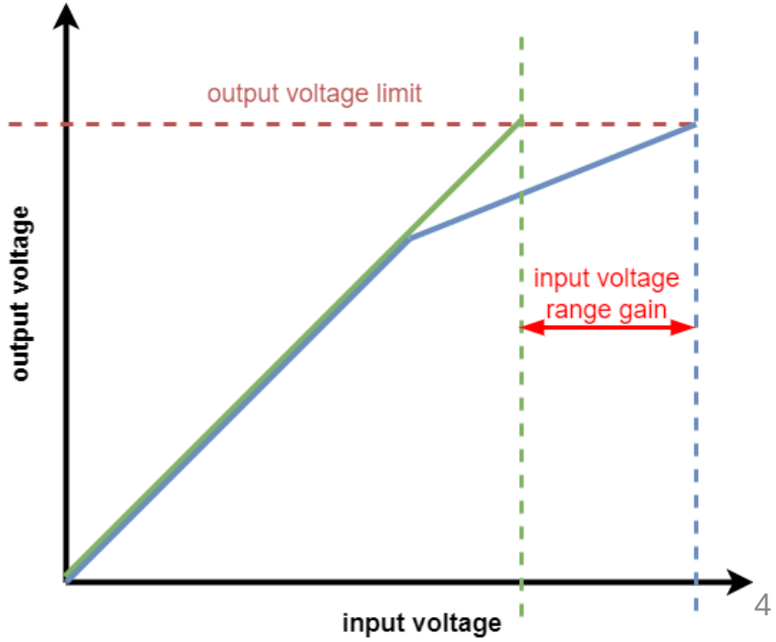
# Non-linear pre-amplifier

- Allows us to increase input signal range, while keeping sufficient measurment resolution for small signals

  but

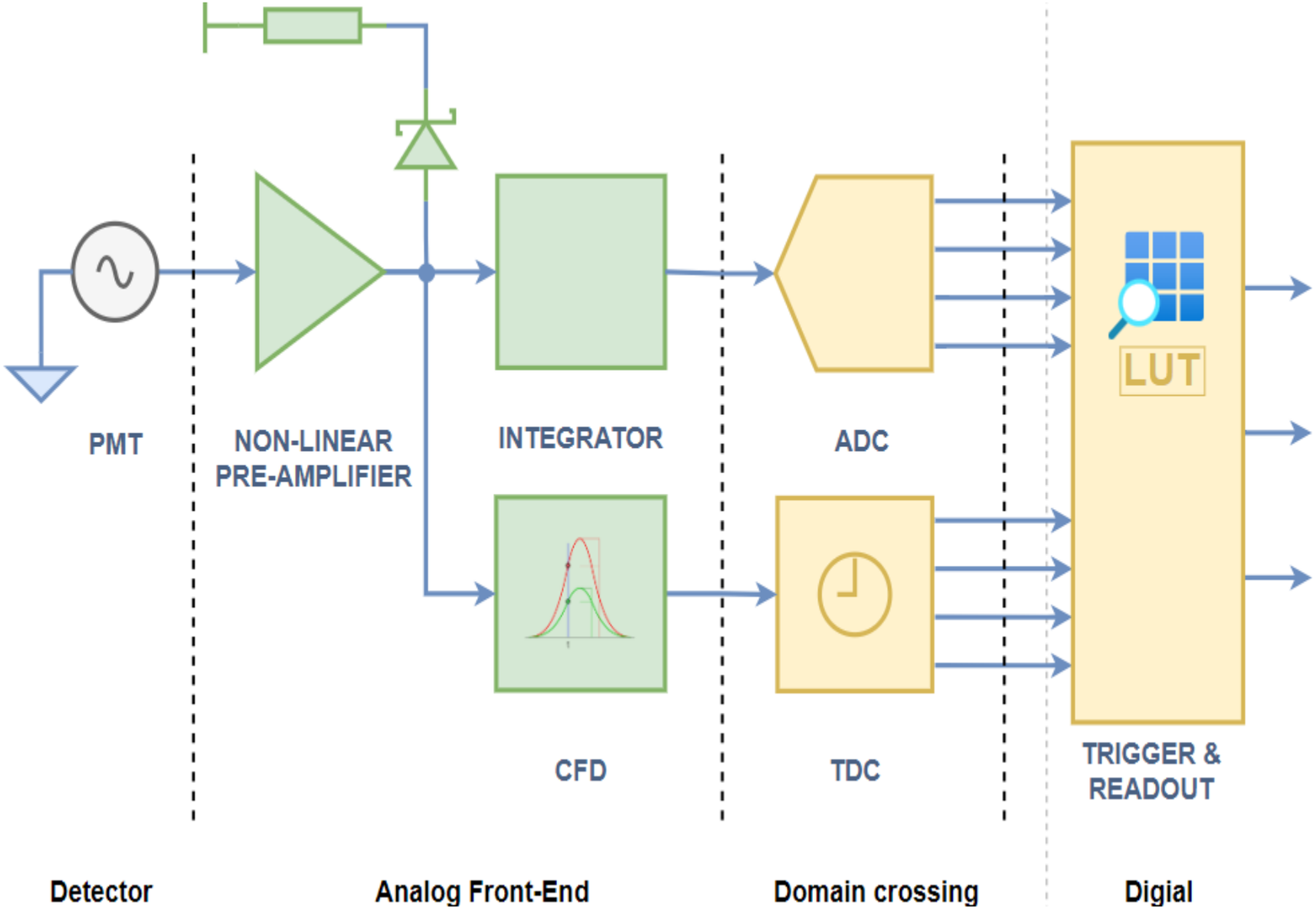
- Introduction of time measurment jitter for signals above threshold
- Diode requires temperature stabilization



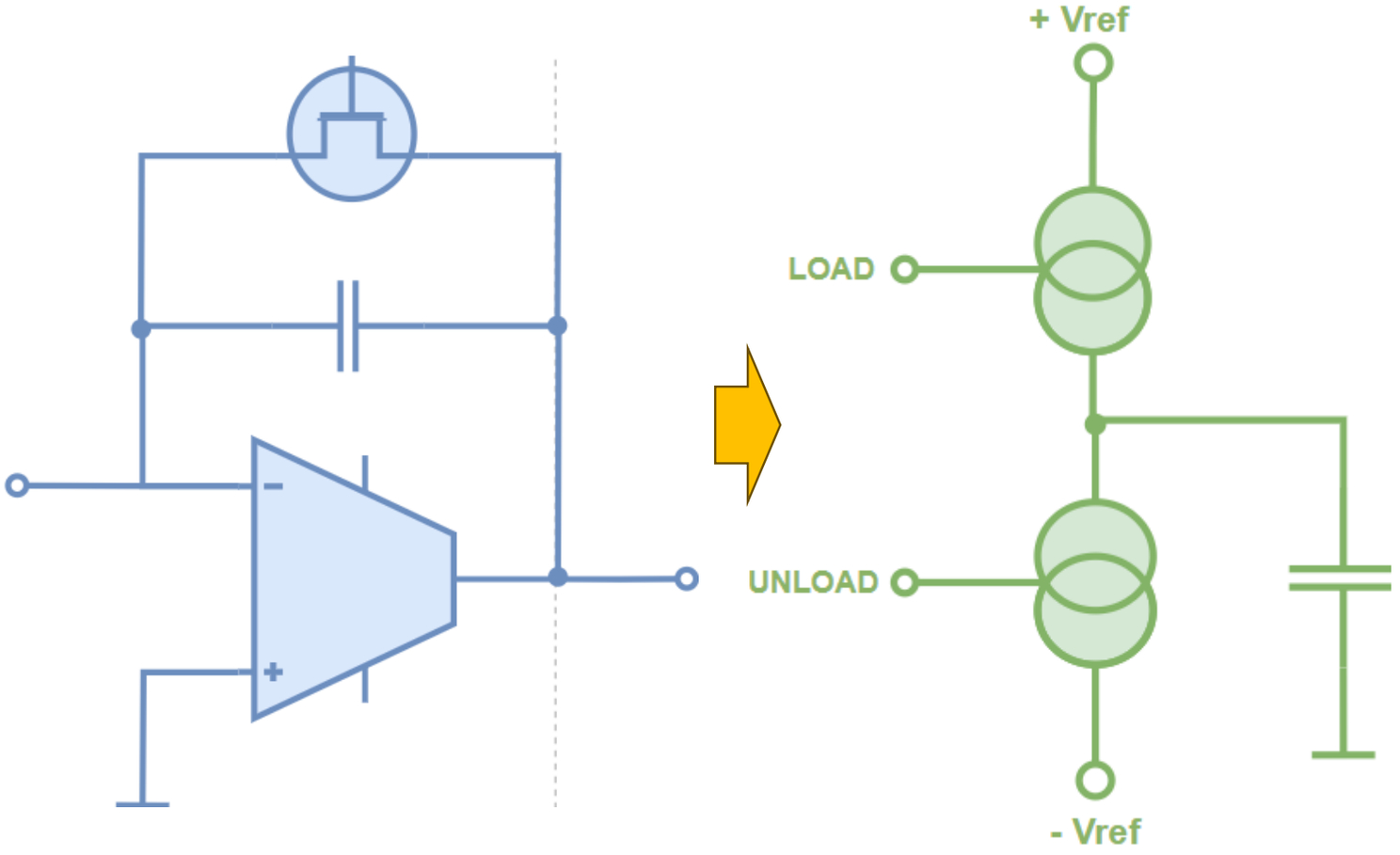
# Solution with non-linear pre-amplifier

- No simple propotion of measured integrator voltage to charge
- Compensation of measured charge in digital domain
  - simple LUT solution in FPGA

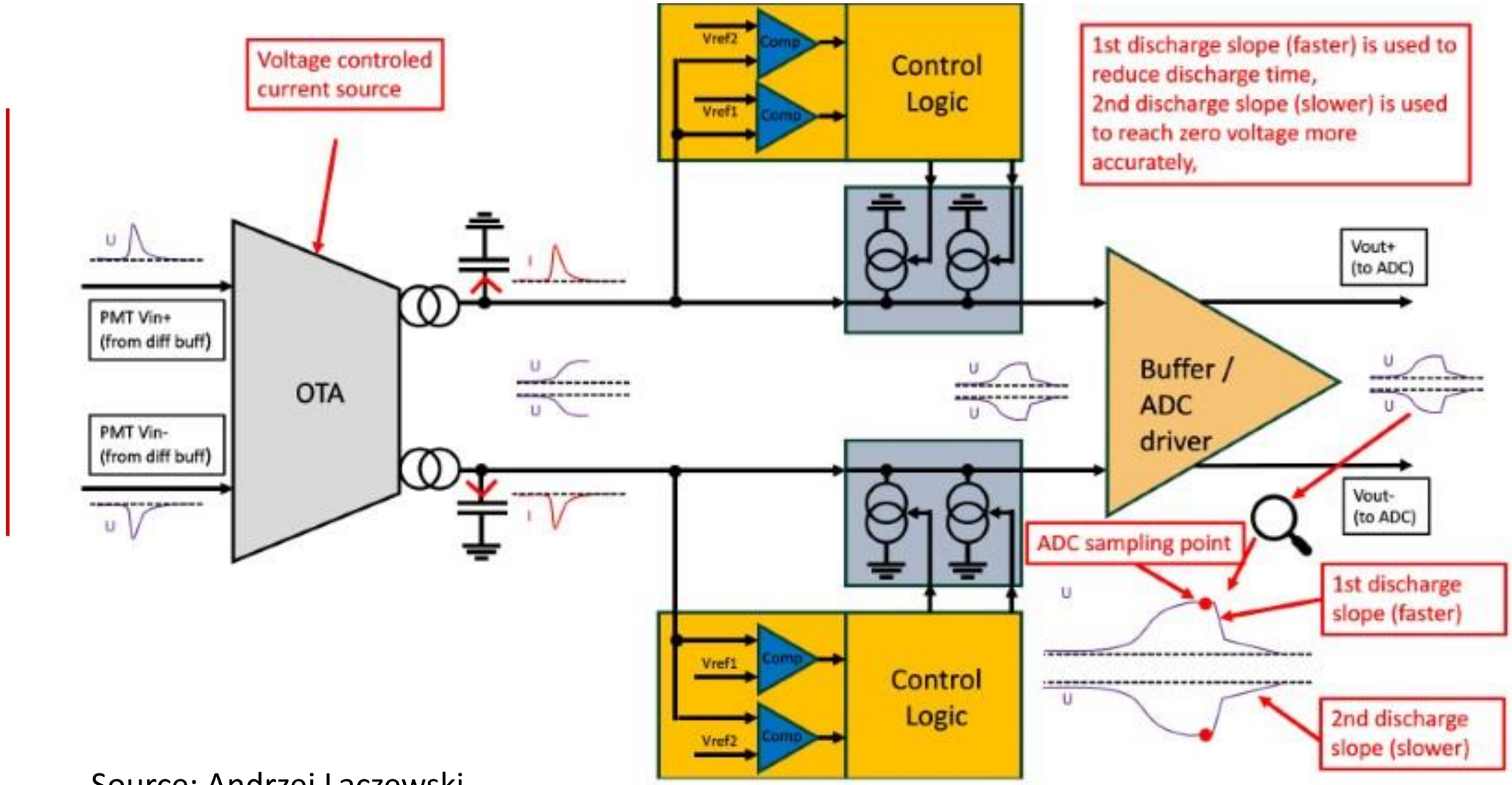


# New integrator architecture

- Integrator based on current sources mitigates problems of traditional op-amp integrator
- Switching transistor downsides:
  - limited keying speed,
  - parasite charge injection.



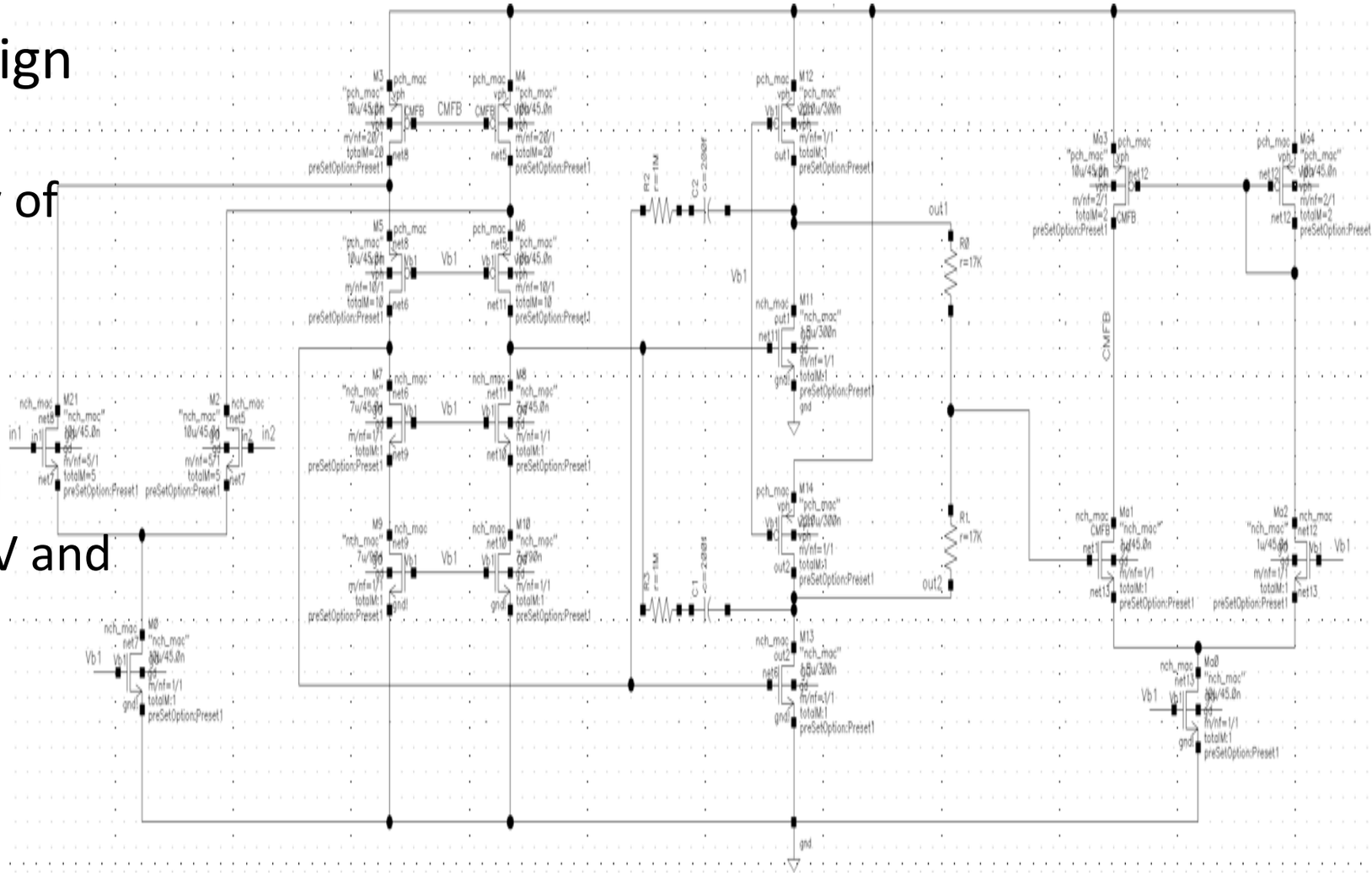
# OTA-based New integrator architecture




Source: Andrzej Laczewski

# Design of ASIC for OTA-based integrator

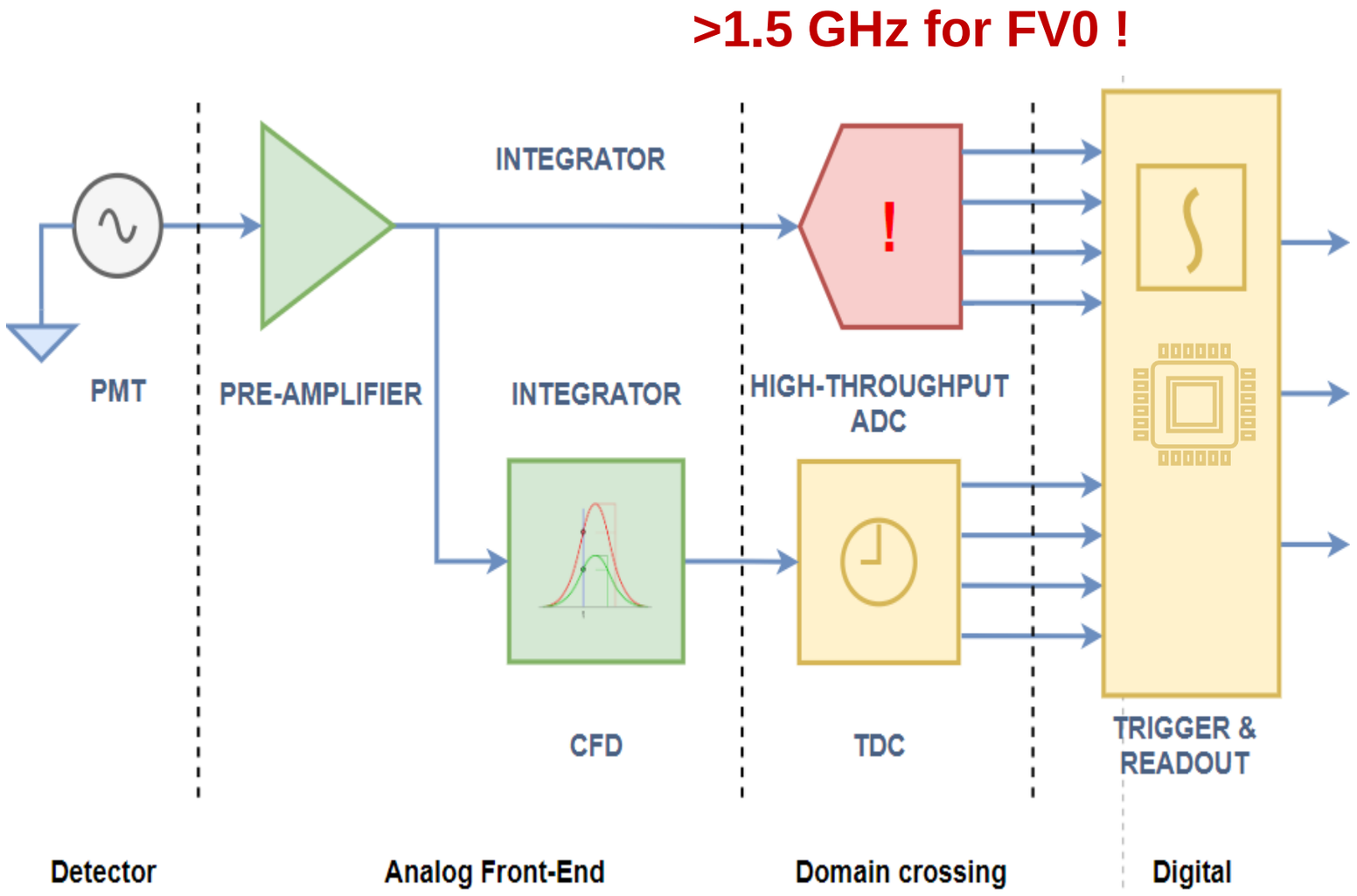
- Necessary to meet design constraints:
  - space, energy, stability of parameters
- Selected technology is UMC_18 CMOS:
  - well known and tested
  - supply domains of 1.8V and 3.3V
  - Relatively low price



Cadence design. Source: Jakub Miszczyński

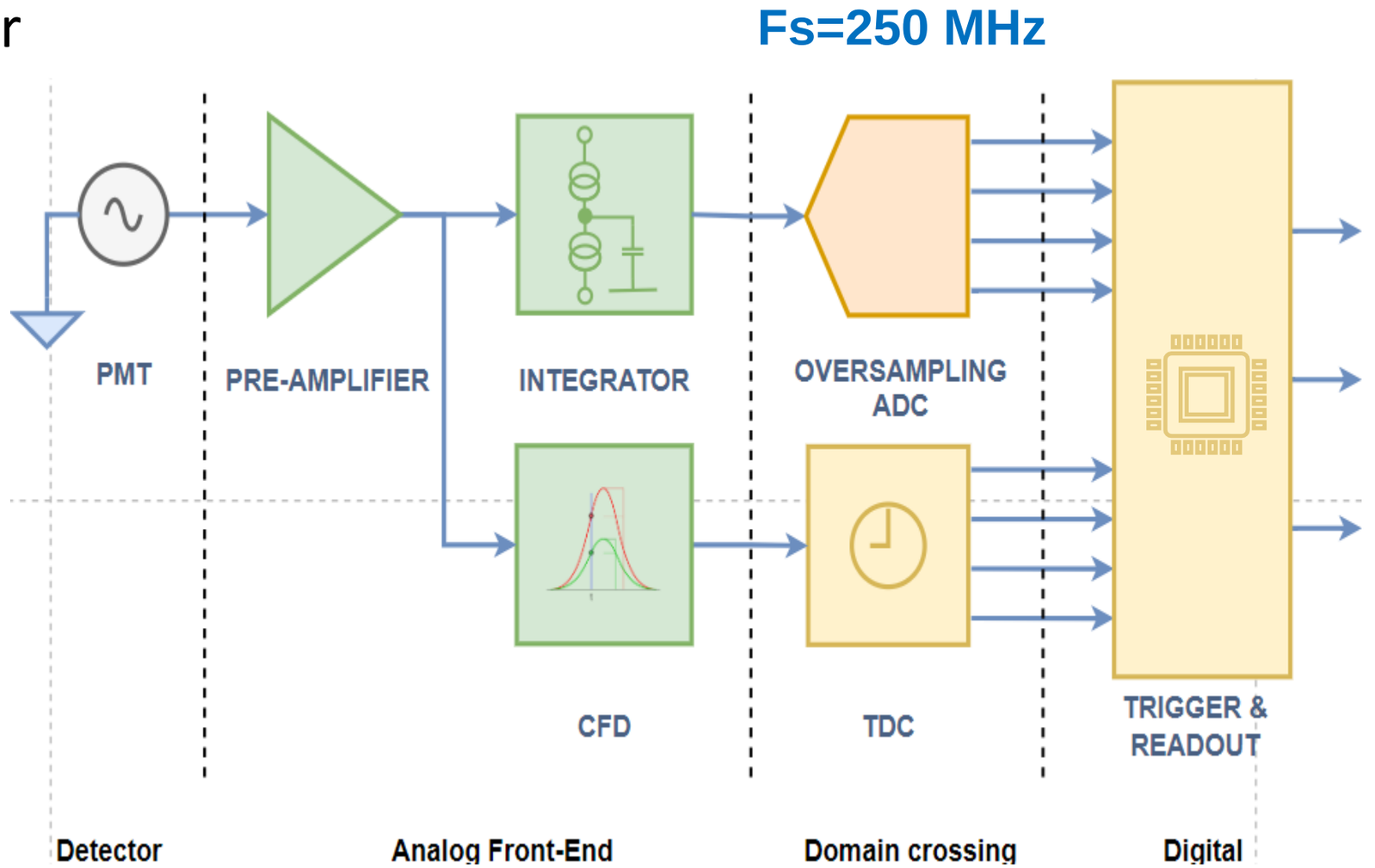
# Direct PMT signal sampling method

- Modern approach
- Digital PMT signal processing in FPGA
  - Software-like flexibility
- Difficult for high frequency signals
  - lack of measurment precision
  - High Energy consumpion
- High latency
  - FIT latency < 425 ns



# Oversampling of analog integrator

- Oversampling allows for precise detection of pile-ups
- End -- Start voltage difference improves measurmant precision



# Thank You