FIT PM/TCM upgrade and roadmap

5th ALICE UPGRADE WEEK in Kraków

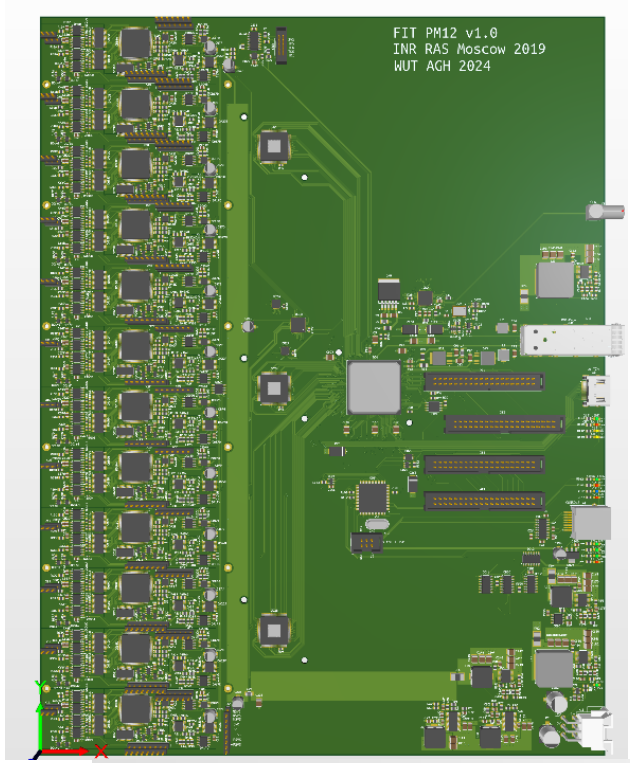
G.Kasprowicz, Warsaw University of Technology

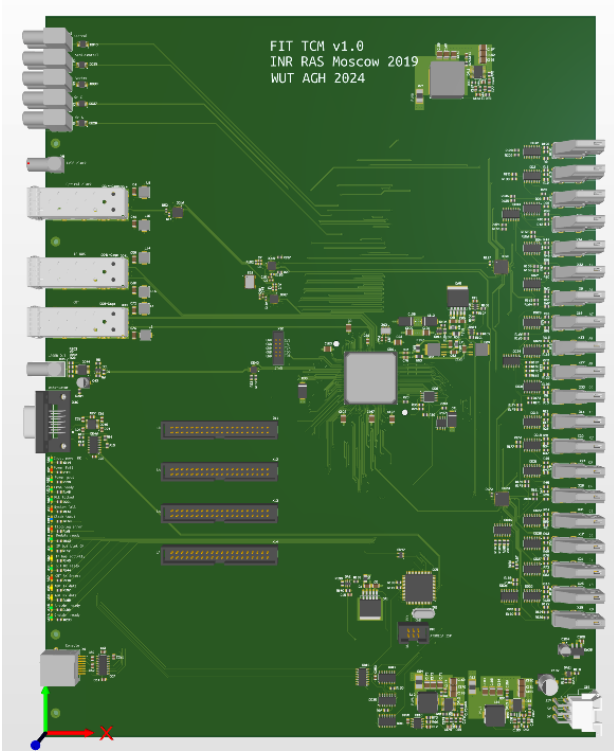
WUT Electroncis for High Energy Physics group – who we are

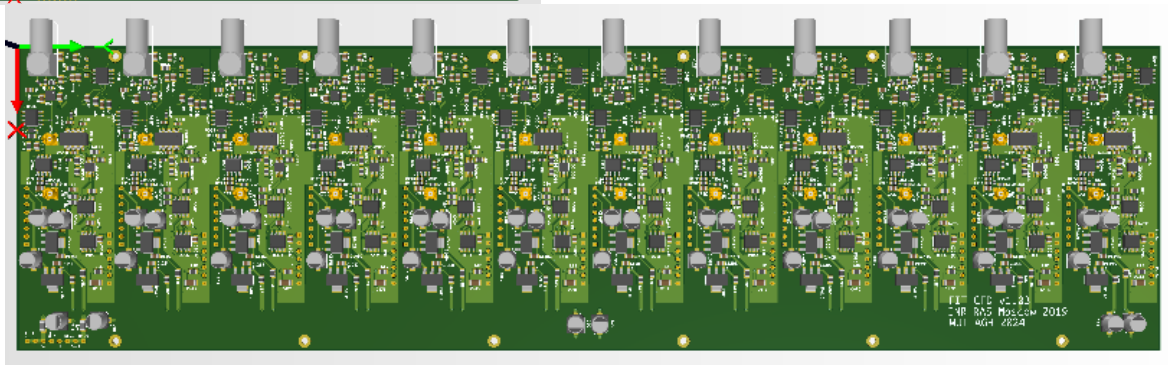
- A Group of 30+ scientists, physicists and engineers, technicians, M.Sc. And Ph.D. students specializing in photonics and electronics for HEP experiments;
- Experience in Zeus and CMS experiments; recently involved mostly in quantum Computing (ARTIQ/SINARA) and Tokamak plasma diagnostics
- Broad expertise in FPGA, DSP, SI/PI, HW design, validation, production and tests
- Well equipped laboratory at WUT

TCM and PM & CFD reverse engineering

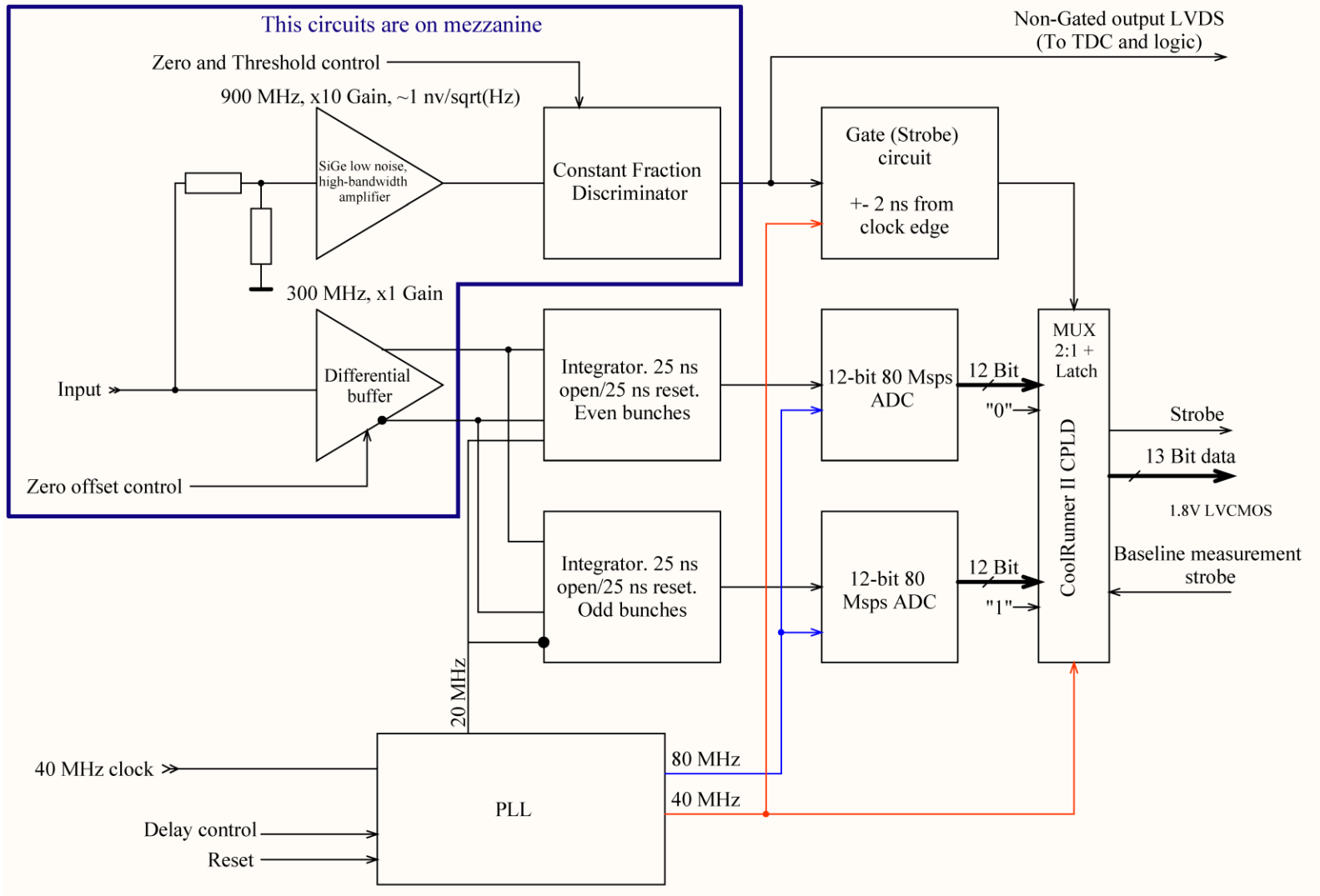
- In late 2023 we joined the FIT project
- 6 months to reverse-engineer the HW
- All PCBs re-designed using official CERN libraries
- All stackups adopted to MFG capabiities
- Some EOL components replaced
- All PCBs are currently in production (2 TCM + 6 PM sets)
- Delivery in 2 weeks
- V1.0 as it’s a very close copy of existing boards







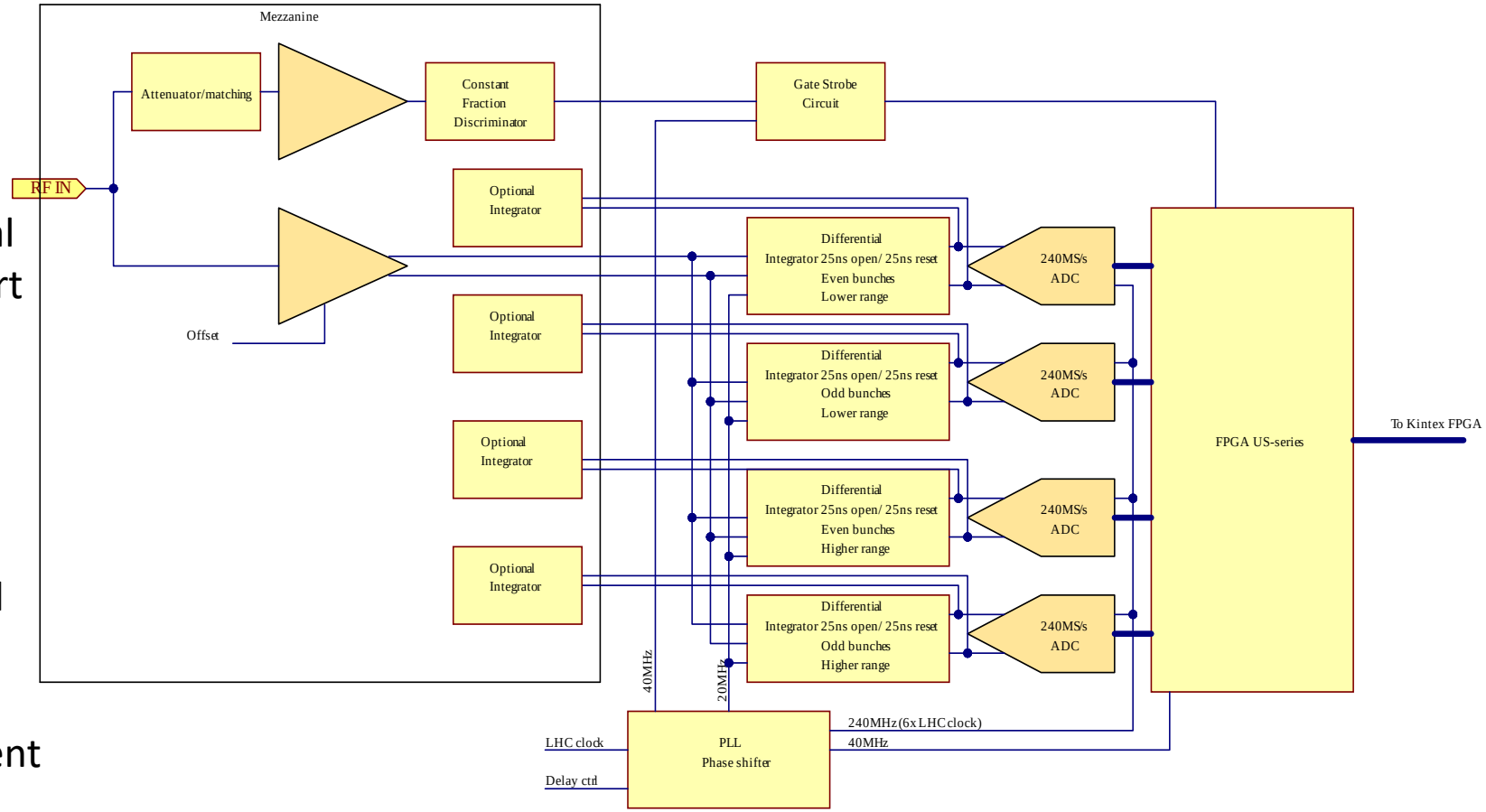
PM12 board - existing AFE subsystem



PM12 board upgrade – short term (Q2 2025)

V1.1 will get:

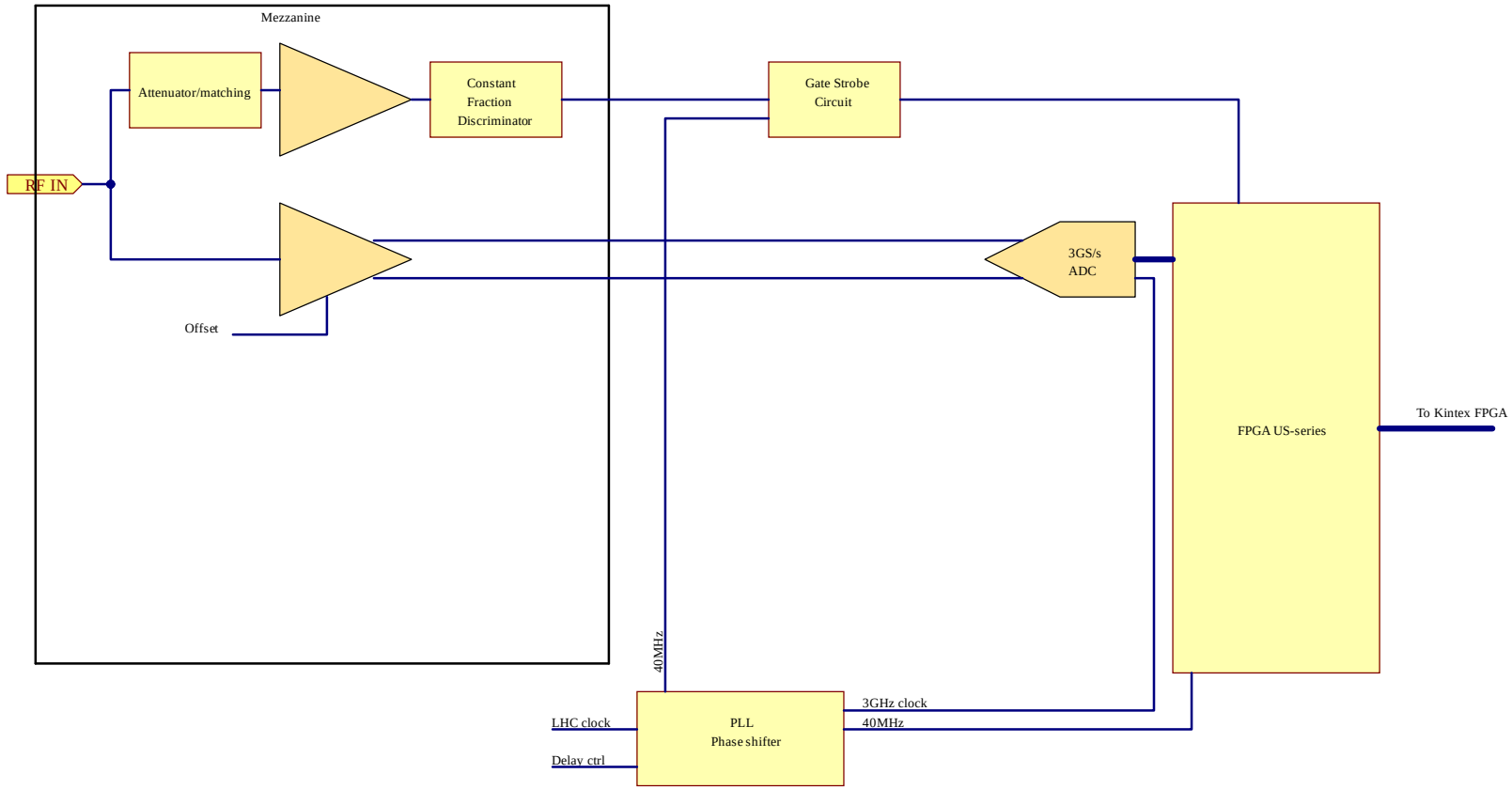
- Lower noise amplifier design
- Additional range for pulse energy
- Fixed several SI/PI issues
- CPLD -> FPGA (XCAU10P) with additional DSP (thanks to faster ADC); 2040 support
- Detection of overlapping pulses
- Option to use external fast integrators (mezzanine)
- Option to test direct sampling at 1GS/s
- Improved shielding and mechanics
- Current & voltage monitoring for critical rails
- ESD protection on IO ports
- Fixed issues with DC/DC converter current burst
- 100% compatibility with existing CFD boards
- Extra MGT links with main FPGA



PM12 board upgrade – long term (2026)

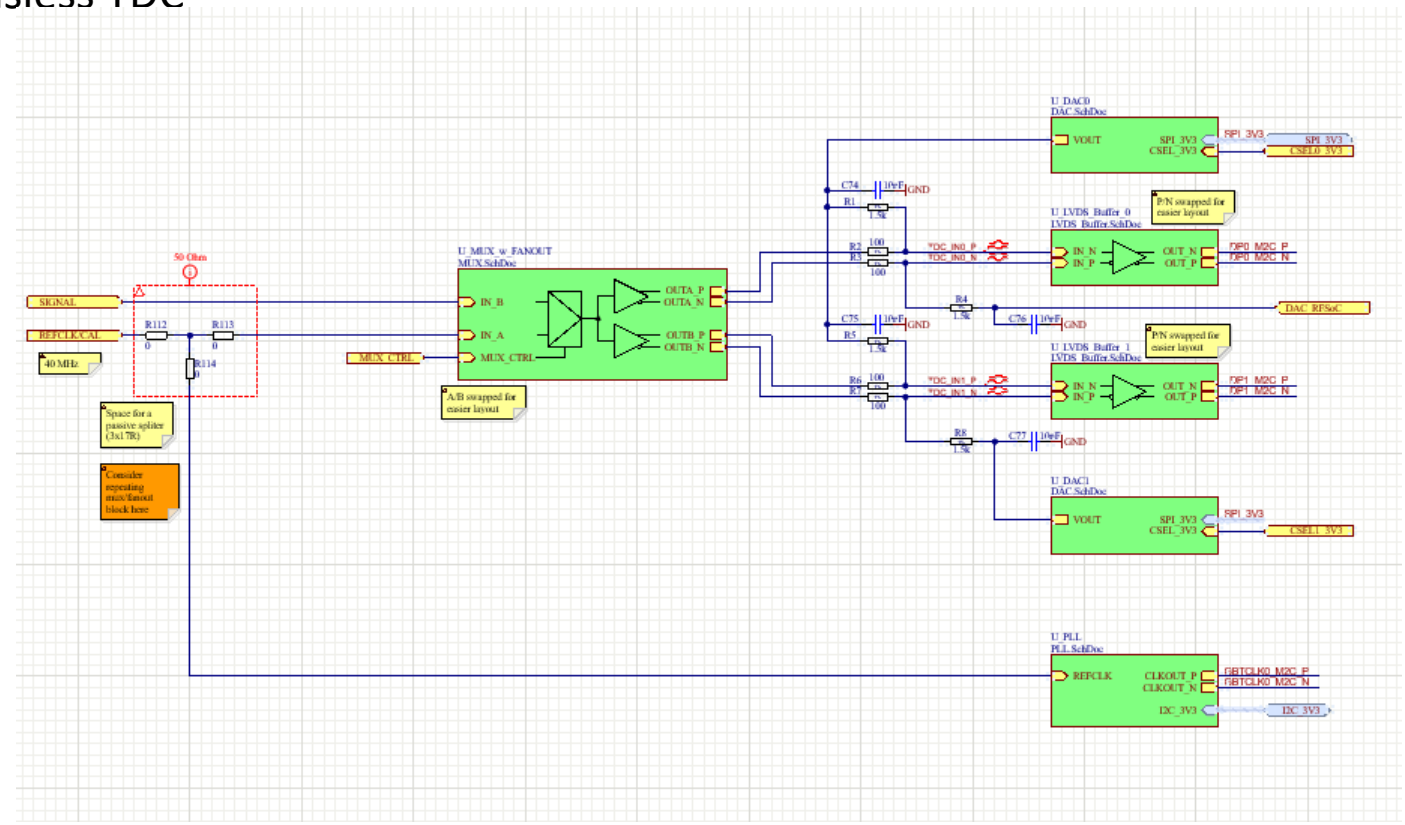
V1.2 will get:

- Fixed v1.1 issues
- Main FPGA upgraded to US+ family (2040 support)
- Digital integrator (2..3GS/s LVDS ADC or RFSOC)
- New TDC (CERN chip or MGT based)
- Additional MGT channels
- 2GS/s LVDS links
- HDMI replaced by more suitable connectors like mSAS (low crosstalk)
- Additional SFP channels



PM12 board upgrade – long term (2026)

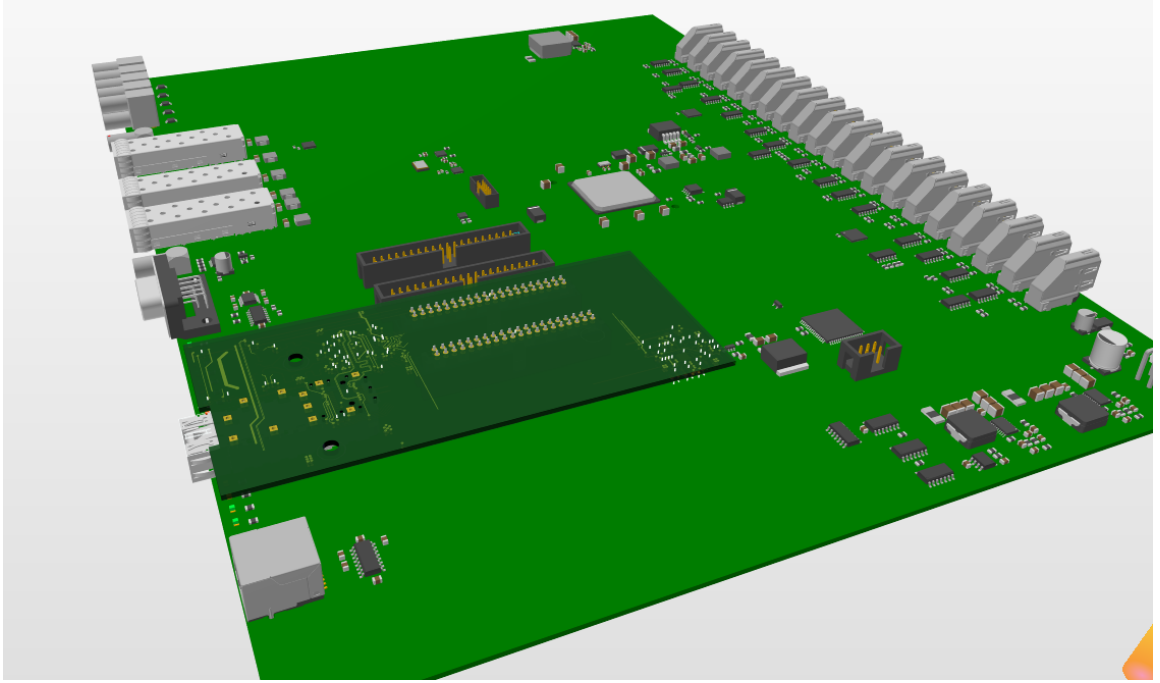
- Evaluation of RFSOC platform as digital integrator and 17 ps noisless TDC



TCM upgrade – short term (Q2 2025)

V1.0 will get:

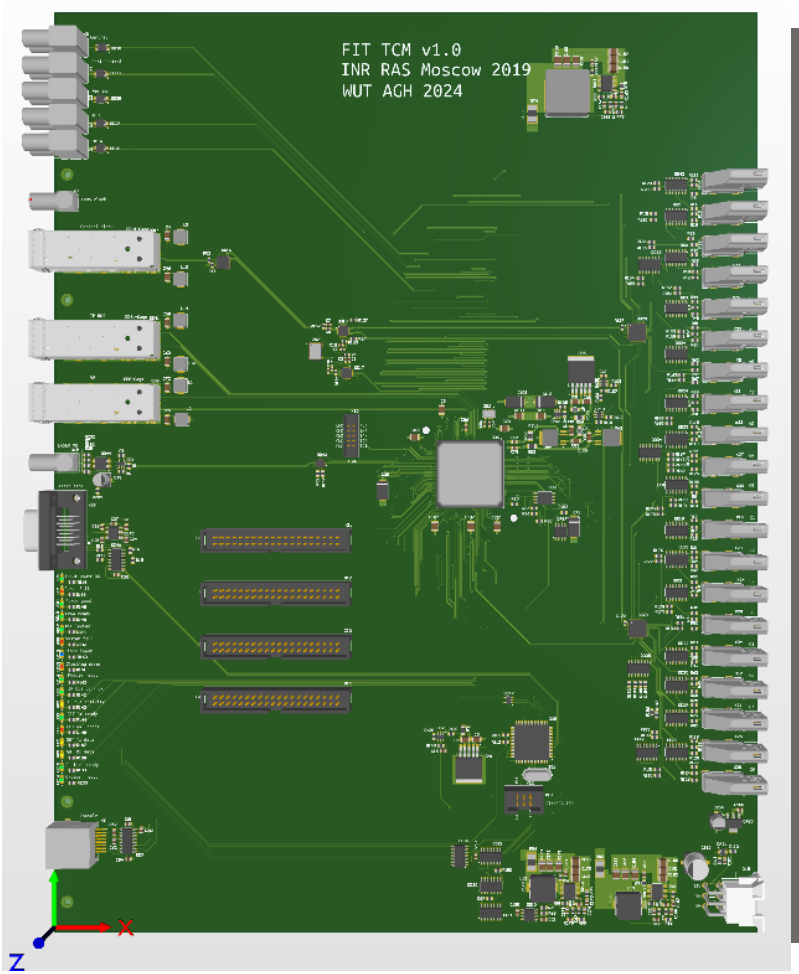
- Improved shielding and mechanics
- Current & voltage monitoring for critical rails
- Fixed issues with DC/DC converter current burst
- Additional IPBUS port (GMII to 1000Base-X converter mezzanine) based on MAX24287
- Patches will be applied to existing and new V1.0 boards

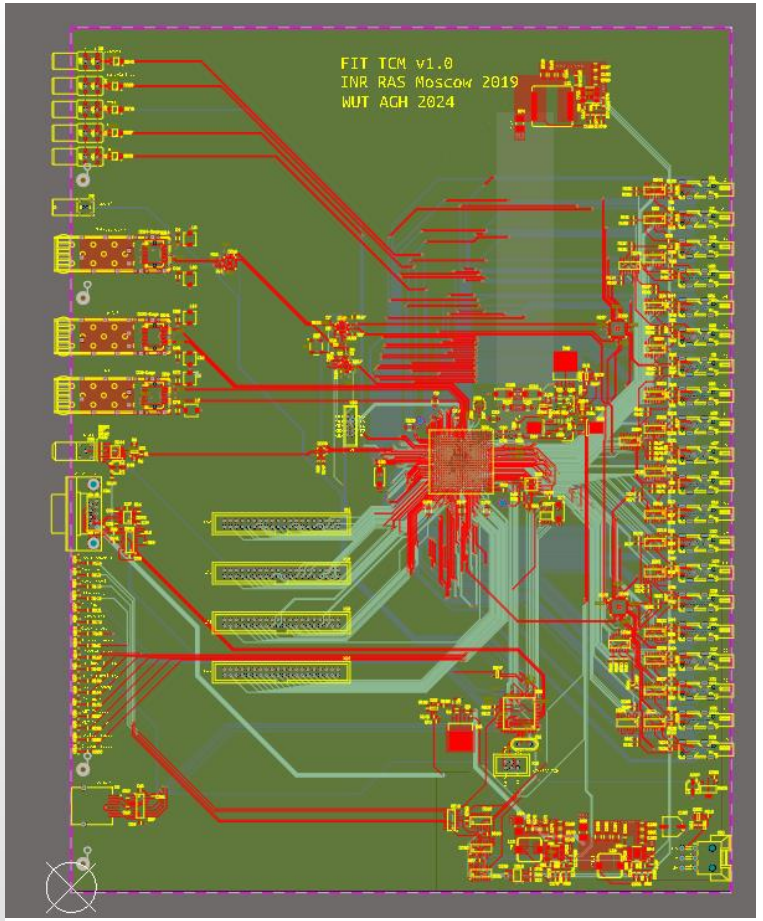


TCM upgrade – long term (2026)

V1.2 will get:

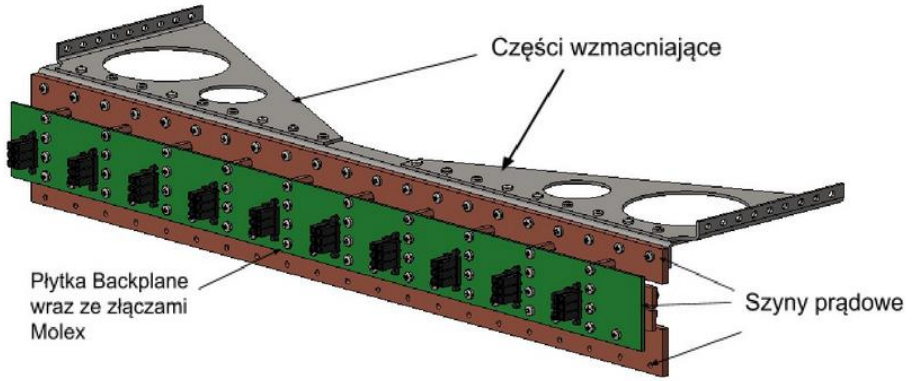
- Fixed issues of v1.1
- Fixed several SI/PI issues
- FPGA upgraded to US+ series to improve long term support until 2040
- Increased data rate to 2Gbit/s per LVDS channel
- HDMI replaced with mSAS or similar low crosstalk connector
- ESD protection on IO ports
- All SFPs capable of running at 10G+
- Additional SFPs for IPBUS/GBT/diagnostic channels

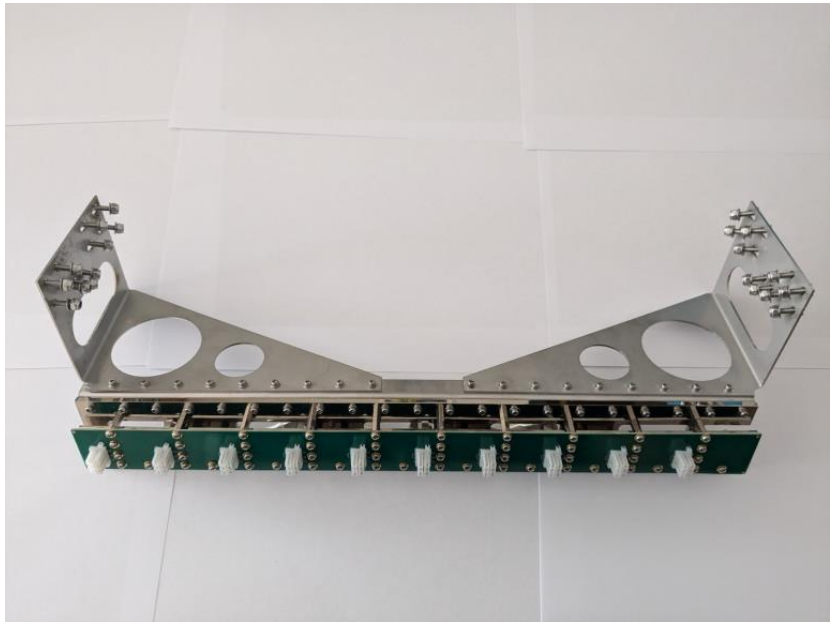




High Current Backplane – short term upgrade

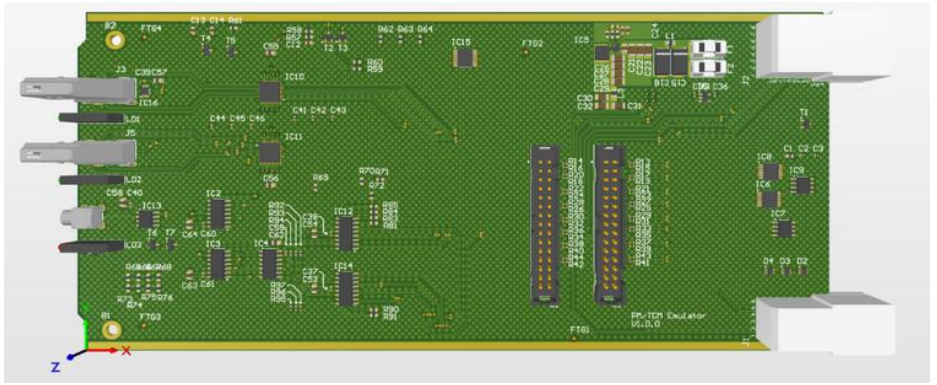
- Fixed issues with rigidity
- 13Amp matched connectors
- Design completed, 5 PCB produced
- Ready for tests

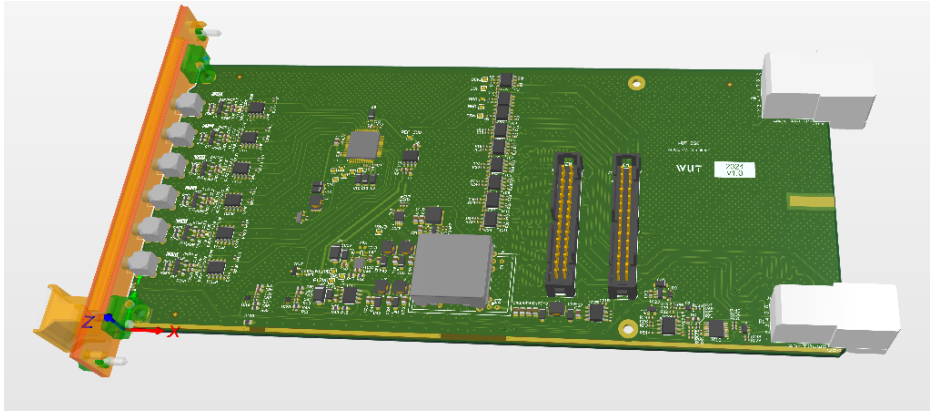




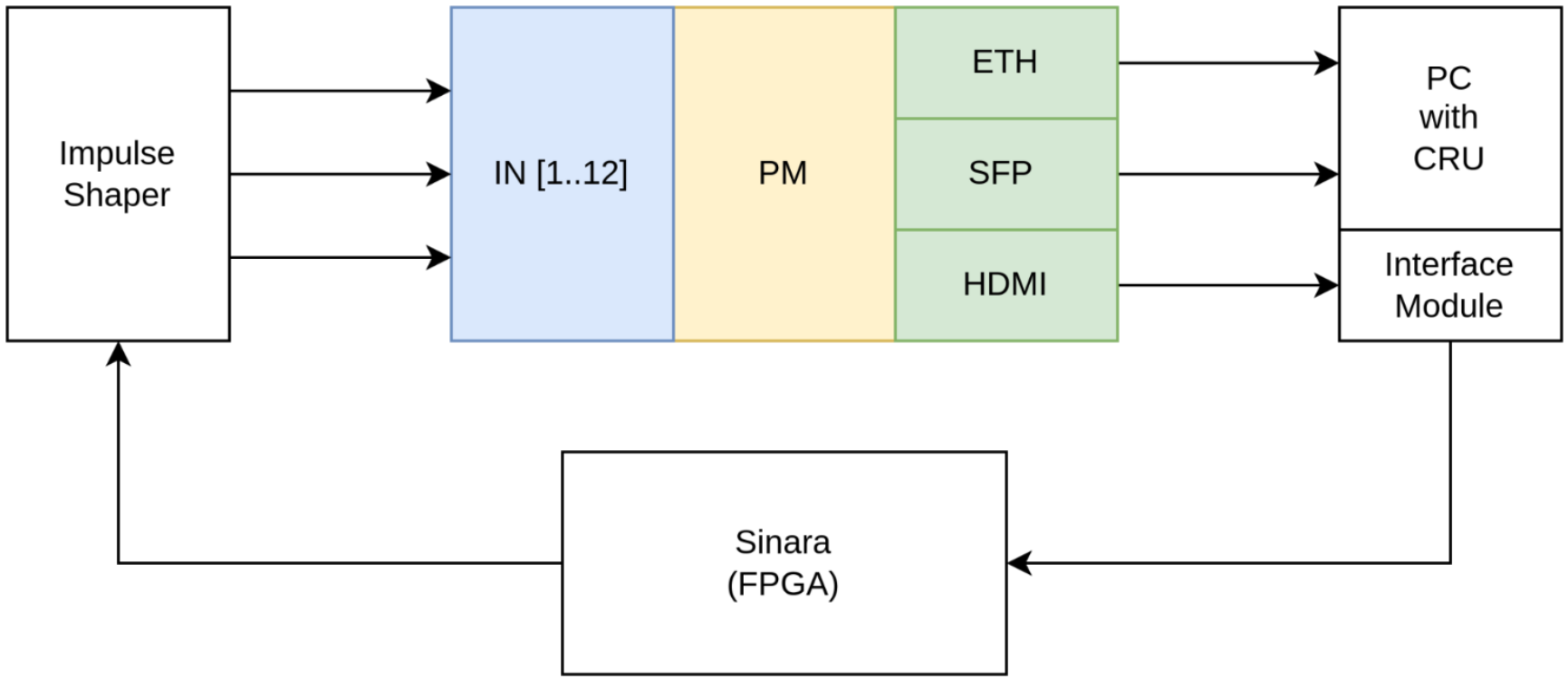
Testing ecosystem

- DIOT – new CERN standard for instrumentation
- Will be used to stress-test TCM /PM modules under full load
- 6-channel pulser (PMT emulation)
- 2-channel HDMI IFC (PM emulation)
- Controlled by ARTIQ – a Python-based stack for real time control with 1ns granularity

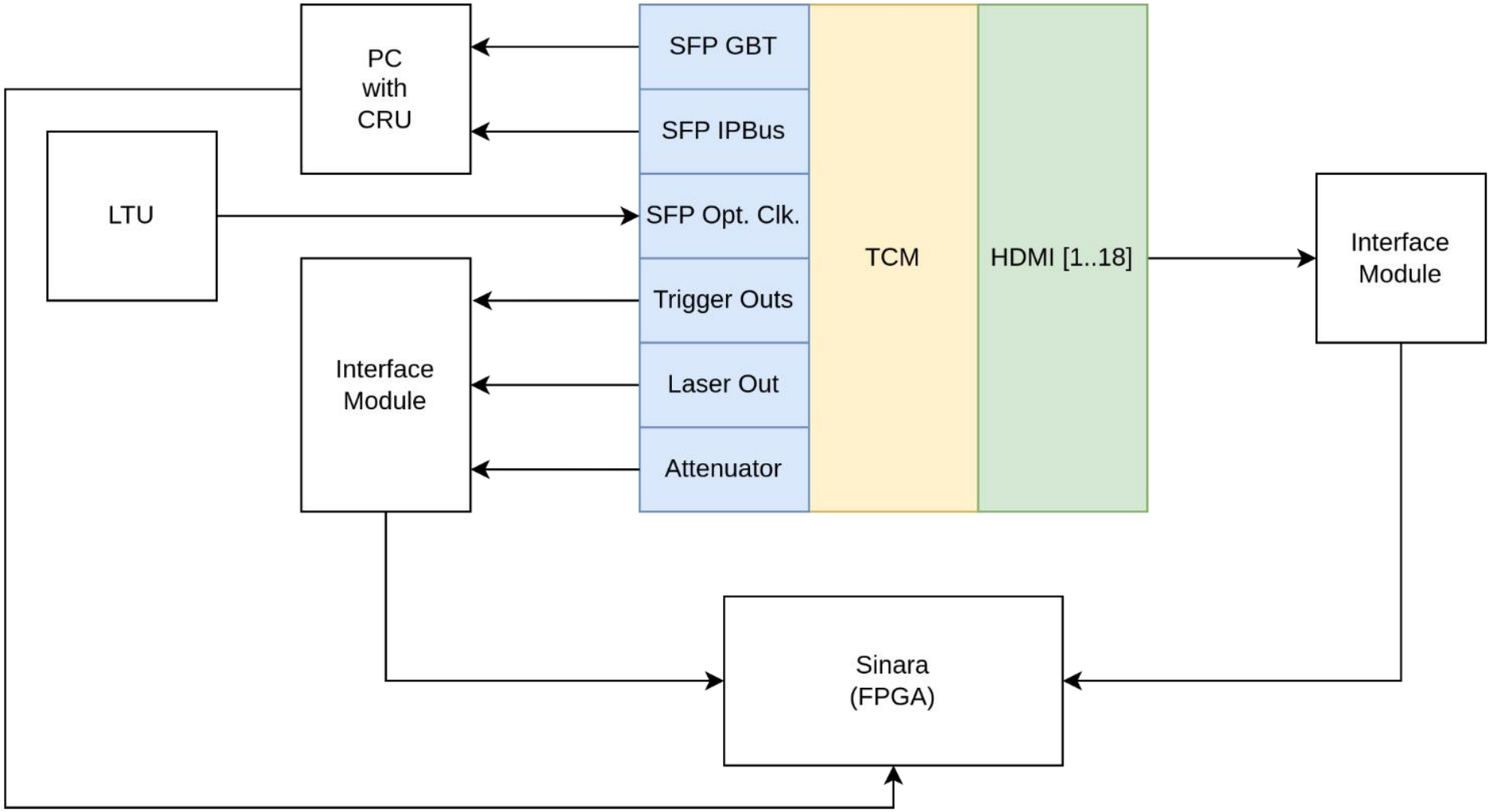




Testing setups - physical PM testing



Testing setups - physical TCM testing



Testing setups - integration testing