Development path for a Vertex Detector Pixel Sensor

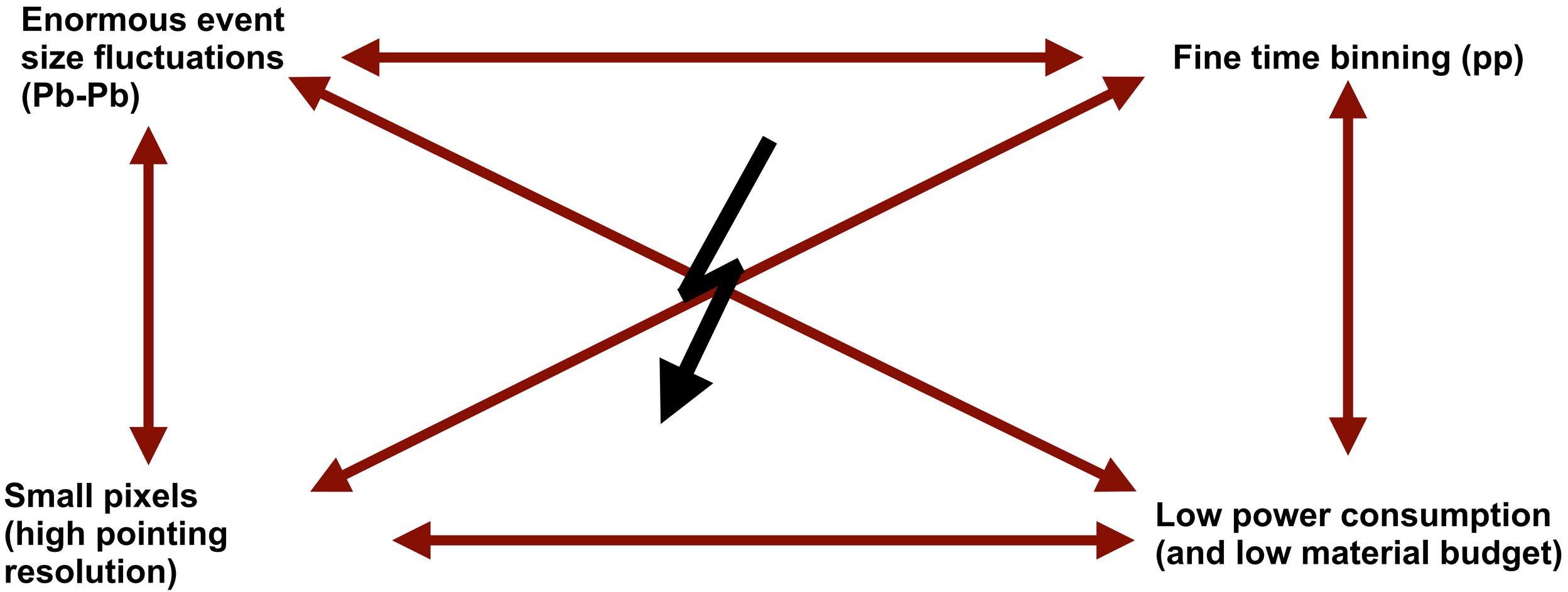
Introduction — main objectives

- **Pointing resolution**
  → position resolution (2.5 µm) → pixel pitch (O(10 µm)) ⊥ low power consumption
  → material budget 0.1% X_0/layer → low power consumption
  ⇒ Power consumption per pixel is crucial

- **Pb-Pb operation**
  → enormous event size fluctuations
  → large bandwidth or buffering close to the pixel needed
  → more complex digital circuitry
  ⊥ small footprint and/or low power consumption

- **pp operation**
  → high event rate (24 MHz) → time resolution (O(100 ns)) needed to limit pile up
  ⊥ low power consumption
  → large statistics required → high radiation tolerance required → favouring smaller pixel pitch

Introduction — main objectives (continued)



ALICE 3 vertex and tracking detector requirements

Updated for ~300 kHz Pb-Pb

	ALICE ITS3	ALICE 3	
		Vertex Detector	Tracker (ML/OT)
Position resolution (μm)	5	2.5	10
Pixel size (μm^2)	*O*(20 x 20)	*O*(10 x 10)	*O*(50 x 50)
Time resolution (ns RMS)	O(1000)	100	100
In-pixel hit rate (Hz)	54	**120** ~~94~~	**54** ~~42~~ (barrel)
Fake-hit rate (/ pixel / event)		<10^{-7}	
Power consumption (mW / cm^2)	35	70	20
Particle hit density (MHz / cm^2)	8.5	**120** ~~94~~	**0.8** ~~0.6~~
Non-Ionising Energy Loss (1 MeV n_{eq} / cm^2)	3 x 10^{12}	1 x 10^{16}	6 x 10^{13}
Total Ionising Dose (Mrad)	0.3	300	3 (barrel)
X/X_0 / layer	0.09% (average) 0.07% (most of active region)	0.1%	1.0%

- A Pb-Pb interaction rate of the ~ 300 kHz corresponds to hit rates similar to 24 MHz pp
- Radiation load dominated by pp due to the longer running time

Key development items / what is available

Key development items

- Front-end circuit
- Pixel geometry
- Readout circuit
- Serial powering

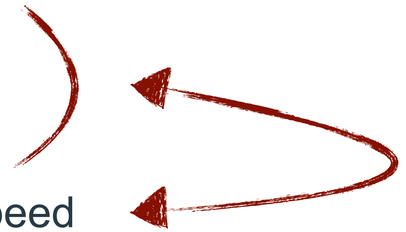
Reticle-sized chip or stitching?
depends on mostly power consumption and distribution

What is available from / currently being developed by ITS3 / EP R&D

- Slow control interface
- High-speed line drivers (including PLL and linear regulators)
- Lightweight lpGBT data formatting and scrambling
- Voltage and current bias generation circuitry including band gaps
- Analogue monitoring including ADC
- Low leakage current standard cell library

Front-end circuit

- Development goals
  - Smaller footprint (to fit inside a 10µm pitch pixel)
  - Reduced complexity:
    fewer transistors and fewer bias currents and bias voltages
  - Reduced power consumption for the same performance / speed
  - Increased radiation hardness
  - Reduced fake-hit rate

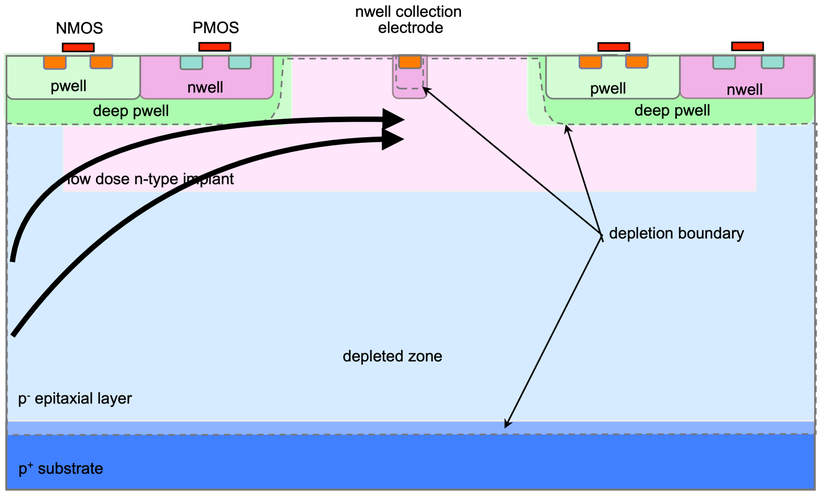


Trade-off between
small pixel and
low power consumption
(material budget)

- Development path
  - Simulation studies for first validation
  - Submission of a small-scale prototype

- Status
  - First simulation of a new concept has started

Pixel geometry

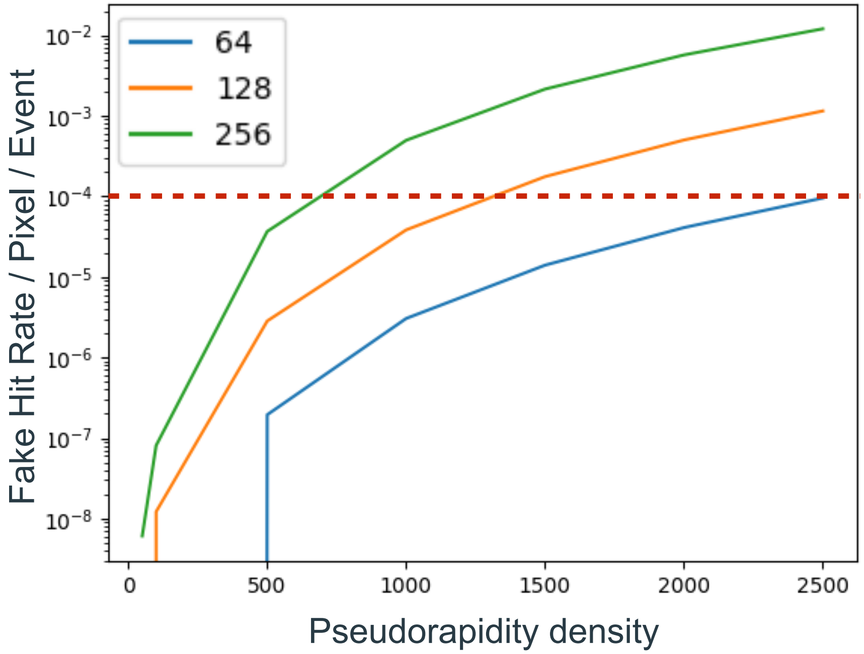


- Development goals
  - Radiation hardness: sufficient charge collection at 10^{16} 1 MeV n_{eq}/cm^2
    - Improve charge transport from the pixel edges and corners
  - Capacitance reduction:
    - Increase signal voltage for a given charge
    - Reduction of the analogue power consumption $P \propto C^{-2}$
- Development path
  - TCAD simulations
  - Characterisation of small / medium scale prototypes (APTS/DPTS/CE65)
    - Further detailed study of existing process splits at radiation levels beyond ITS3 and cryogenic temperatures
    - New process splits in upcoming Engineering Runs (ERs)
- Status:
  - Continuously ongoing process, current focus on ITS3 with limited reverse substrate bias
  - Reproduction and understanding of findings from prototype chips

Readout circuit

- Development goals
  - Small footprint (to allow 10 µm pixel pitch)
  - Versatility:
    - 24 MHz pp operation → time granularity
    - 315 kHz Pb-Pb operation → strong occupancy variations

- Development path
  - Architecture simulation in software:
    - Ensure loss less data transport under all expected conditions
    - Obtain expected data throughput and necessary
    - Optimisation of the de-randomization / buffering
  - RTL entry and layout:
    - Assessment of the footprint of the circuitry
  - Validation in a small-scale or full-scale prototype chip



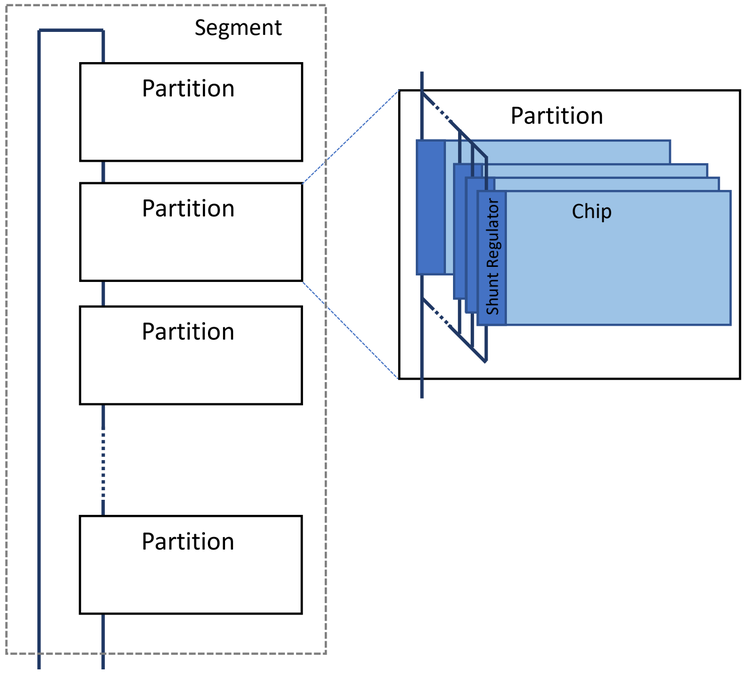
Fake hit rate introduced by hit ambiguities caused by the readout architecture as function of matrix size (64x64 to 256x256 pixels)

- Status: simulation of architectures ongoing
- Example:
  - Multi-dimensional projections (‘Orthopix’ [1])
    - Four orthogonal projections
    - Projections are very simple circuit-wise (‘wired-OR’)
    - Fixed event size independent of the occupancy: $4 \cdot \sqrt{N_{Pixels}}$
    - Few transitions in the data stream: power efficient
    - No hit losses, only hit ambiguities (≈ fake hits)
    - Overwhelming fake-hit rate for most central Pb-Pb and realistic matrix sizes

[1] P. Giubilato, W. Snoeys. OrthoPix 10.1109/NSSMIC.2012.6551407

Serial powering

- Concept: modules connected in series
  → all modules need to consume the same current
  → ensured by shunt regulators ‘burning’ excess current
  – Baseline for Vertex Detector, Middle Layers
- Development goal
  – Shunt regulator in TPSCo 65 nm process to be integrated in pixel chips
  – Optional: charge pump generating reverse substrate bias
- Development path
  – Characterise performance of existing pixel chips when serially powered
  – Port existing shunt regulator from
  TJ 180 nm [1,2] or TSMC 65 nm [3] to TPSCo 65 nm
- Status: to be started



Serial powering sketch

[1] D. Gajanana et al. (2016) JINST 11 C03027 Radiation hard analog circuits for ALICE ITS upgrade
[2] A. Habib et al. Shut Regulator for the Serial Powering of the ATLAS CMOS Pixel Detector Modules. 10.1109/TNS.2020.2964333
[3] A. Dimitrievska, A. Stiller NIM A (2019) 958 162091 RD53A: A large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors

Summary and Outlook

- Work slowly ramps up in the shadow of ITS3 activities
- Analogue front-end circuit and pixel optimisation most urgent to be prototyped
- Readout architecture can be mostly evaluated without a prototype submission
- Serial powering
  - Little experience so far in the ALICE context
  - Needed for Vertex Detector, Middle Layers and Outer Tracker

Thanks a lot for your attention!