# PS complex Fast BCT ADC requirements

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BI-IQ

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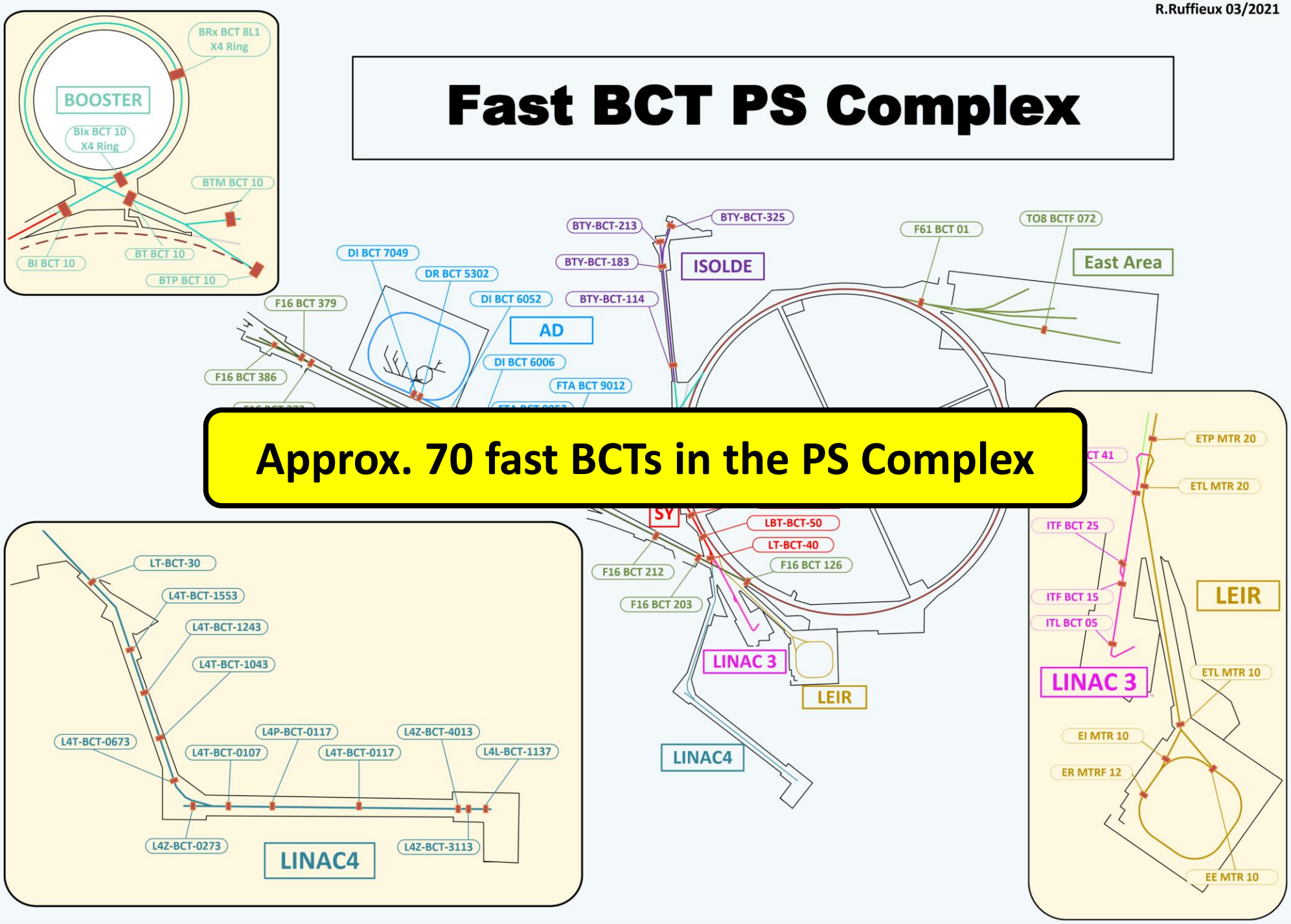
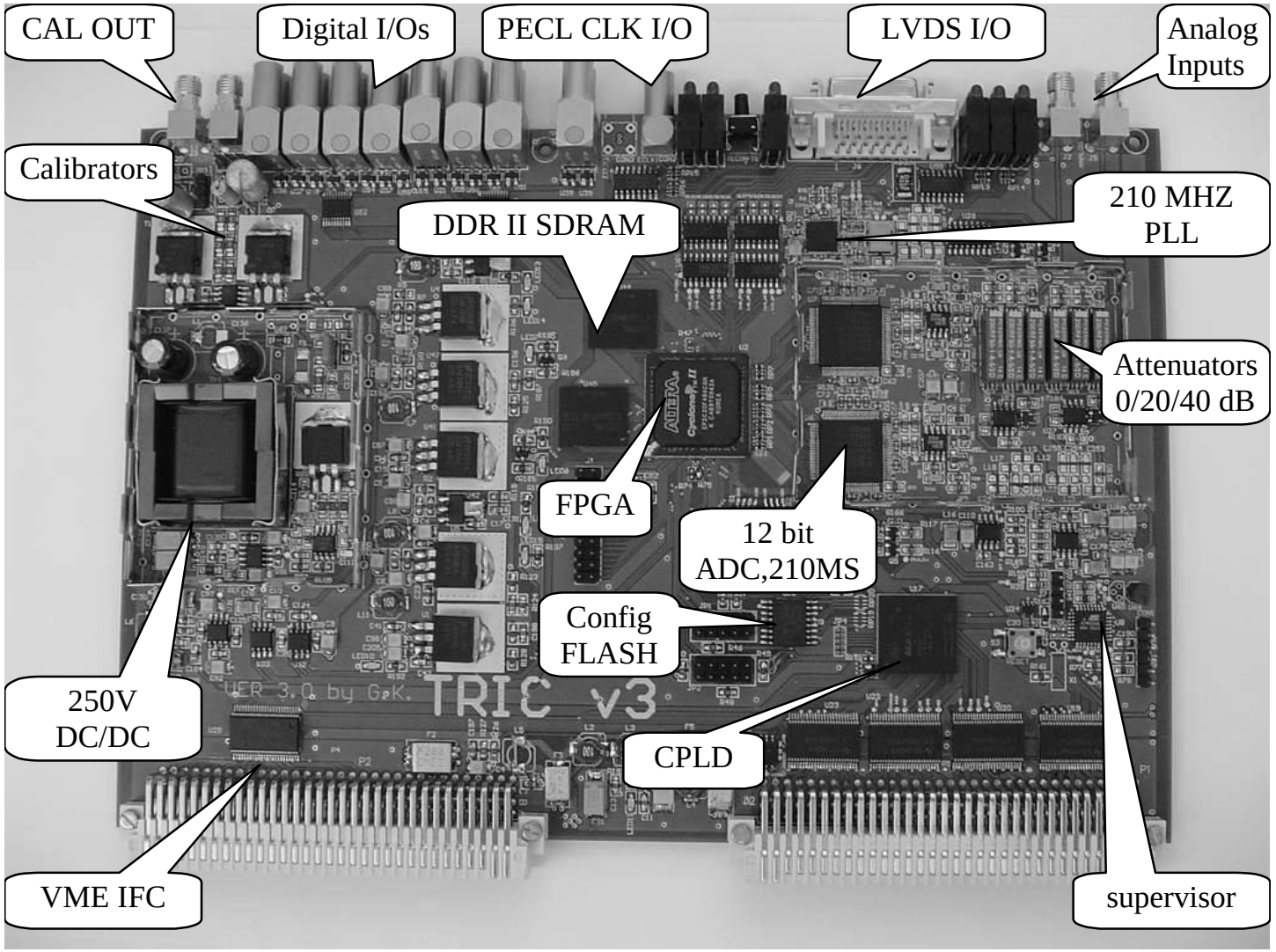
# Fast BCT PS Complex



# TRIC

- **TR**ansformer **I**ntegration **C**ard (TRIC)
  - Design from 2005
- VME64x card
- 2 ADC channels
  - 212.5 MSPS (AD9430)
  - 12 bit (10.6 ENOB)
  - 30 MHz analogue BW
  - Switchable attenuator (0-14-28dB)
- Altera Cyclone II FPGA
- Onboard calibrator
  - Generate a current pulse to the BCT calibration winding



# TRIC limitations

- Design from ~2005
  - Running out of spares
  - Still requests for new installations (LN4 test stand, etc)
  - Not possible to produce more
- Small FPGA with limited processing capabilities
  - Not possible to implement more advanced baseline droop correction, etc
- Limited on-board memory for acquisition buffers
  - Now limited to 1024 points at 106.25 MHz (half ADC data rate)
  - Larger acquisition buffers at full data rate would be useful

- **CONS project requested to replace TRIC during LS3**
  - **IQ preference: VFC-HD with an FMC ADC**

# New FMC requirements

- 4x ADC channels
  - So that we can reduce the total number of VFCs by 2 compared to the TRIC
  - In fact, the reduction can be greater as many TRIC cards now only use 1oo2 channels
    - We can have 4 BCTs per VFC in places
- As high dynamic range as possible to cover the range of intensities that we have in the BCTs
  - Aim for 12 –> 16 bits : gain of 10dB SNR compared to today?
- No change in analogue signal specs, so similar ADC requirements
  - 200-250 MSPS
  - 30 MHz analogue bandwidth
  - DC coupled (or < 1Hz AC)
- Fixed input range and offset

# ADC selection (BIIQ-275)

| Model | Resolution | Speed | Ch | Power/ch | SNR | Price/ch | Interface | Note |
|---|---|---|---|---|---|---|---|---|
| ADS5485 | 16b | 200 MSPS | 1 | 0.7 W | 75.6 dBFS (170 MHz) | 177.02 | LVDS | |
| LTC2107 | 16b | 210 MSPS | 1 | 1.4 W | 78.2 dBFS (250 MHz) | 157.28 | LVDS | |
| AD9467 | 16b | 250 MSPS | 1 | 1.5 W | 75.5 dBFS (210 MHz) | 205.64 | LVDS | |
| ISLA216P | 16b | 250 MSPS | 1 | 0.8 W | 74.2 dBFS (190 MHz) | 234.78 | LVDS | LNLS BPM FMC |
| ~~ADS42LB69~~ | ~~16b~~ | ~~250 MSPS~~ | ~~2~~ | ~~0.9 W~~ | ~~73.2 dBFS (170 MHz)~~ | ~~129.30~~ | ~~LVDS / JESD204B~~ | |
| ADC14X250 | 14b | 250 MSPS | 1 | 0.6 W | 70.0 dBFS (170 MHz) | 104.43 | JESD204B | |
| LTC2123 | 14b | 250 MSPS | 2 | 0.9 W | 69.0 dBFS (140 MHz) | 93.69 | JESD204B | |
| AD9652 | 16b | 310 MSPS | 2 | 1.1 W | 73.7 dBFS (170 MHz) | 198.40 | LVDS | |
| ADC16DX370 | 16b | 370 MSPS | 2 | 0.9 W | 70.5 dBFS (170 MHz) | 179.57 | JESD204B | |
| ADC31JB68 | 16b | 500 MSPS | 1 | 0.9 W | 69.3 dBFS (210 MHz) | 245.97 | JESD204B | |
| ~~ADS54J69~~ | ~~16b~~ | ~~500 MSPS~~ | ~~2~~ | ~~1.4 W~~ | ~~73.0 dBFS (170 MHz)~~ | ~~314.87~~ | ~~JESD204B~~ | ~~FMC120~~ |
| ADS54J54 | 14b | 500 MSPS | 4 | 0.9 W | 67.2 dBFS (170 MHz) | 142.30 | JESD204B | IAM FMC |
| AD9680 | 14b | 500 MSPS ++ | 2 | 1.1 W | 69.0 dBFS (170 MHz) | 228.79 | JESD204B | FMC-1000 |
| AD9695 | 14b | 625 MSPS ++ | 2 | 0.7 W | 67.5 dBFS (172 MHz) | 258.88 | JESD204B | Joel's FMC |

Not good for DC

# Why not the ADS42LB69?

- Linearity much worse, this is a common feature of most 16-bit ~250MSPS ADCs:

| | PARAMETER | TEST CONDITIONS | 2-$V_{PP}$ FULL-SCALE | | | 2.5-$V_{PP}$ FULL-SCALE | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| DNL | Differential nonlinearity | $f_{IN}$ = 170 MHz | | ±0.6 | | | ±0.6 | | LSBs |
| INL | Integrated nonlinearity | $f_{IN}$ = 170 MHz | | ±3 | ±8 | | ±3.5 | | LSBs |

- But critically, the ADC inputs are **not suitable for DC!** It has a high-pass response below 100kHz!
- ADS54J69 (tested by Jiri) also had issues with DC calibration (see BI/TB 17/01/2019)

**9.2.2.1.3 Using the ADS42LBx9 In Time-Domain, Low-Frequency Pulse Applications**

The analog buffers inside the device are implemented to provide excellent linearity over a wide range of frequencies. However, at very low frequencies (< 100 kHz) the buffer presents a high-pass response, as shown in Figure 115 and Figure 116. This response does not affect most frequency-domain applications, but can require compensation techniques for time-domain, dc-coupled applications. Application report SBAA220 discusses simple techniques to compensate for the analog buffer response.

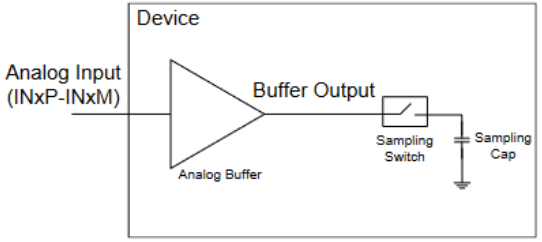



**Figure 115. Analog Buffer in the ADS42LBx9**

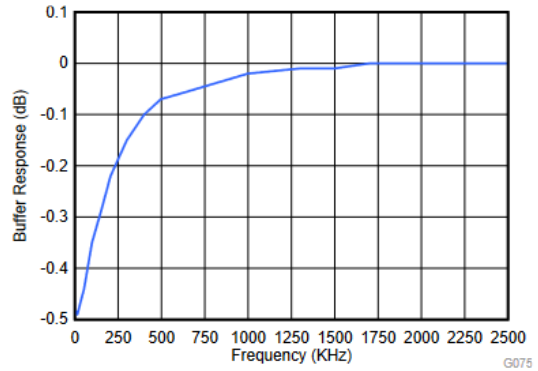



**Figure 116. Buffer Response at Very Low Input Frequencies**

# 16-Bit, 210Msps High Performance ADC

## FEATURES

- **98dBFS SFDR**
- **80dBFS SNR Noise Floor**
- **Aperture Jitter = 45fs$_{RMS}$**
- PGA Front-End 2.4V$_{P-P}$ or 1.6V$_{P-P}$ Input Range
- Optional Internal Dither
- Optional Data Output Randomizer
- Power Dissipation: 1280mW
- Shutdown Mode
- Serial SPI Port for Configuration
- Clock Duty Cycle Stabilizer
- 48-Lead (7mm × 7mm) QFN Package

## APPLICATIONS

- Software Defined Radios
- Military Radio and RADAR
- Cellular Base Stations
- Spectral Analysis
- Imaging Systems
- ATE and Instrumentation

## DESCRIPTION

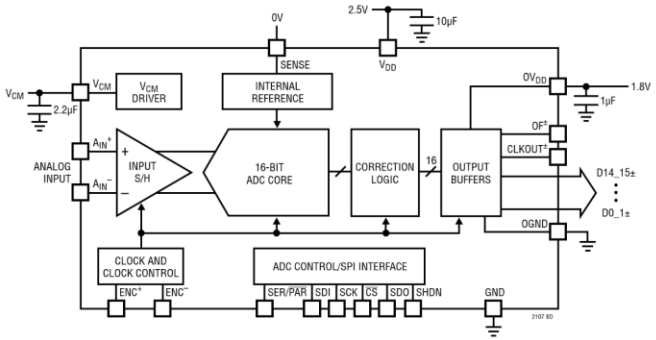
The LTC®2107 is a 16-bit, 210Msps high performance ADC. The combination of high sample rate, low noise and high linearity enable a new generation of digital radio designs. The direct sampling front-end is designed specifically for the most demanding receiver applications such as software defined radio and multi-channel GSM base stations. The AC performance includes, SNR = 80dBFS, SFDR = 98dBFS. Aperture jitter = 45fs$_{RMS}$ allows direct sampling of IF frequencies up to 500MHz with excellent performance.

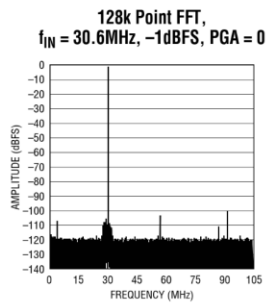
Features such as internal dither, a PGA front-end and digital output randomization help maximize performance. Modes of operation can be controlled through a 3-wire serial interface (SPI).

The double data rate (DDR) low voltage differential (LVDS) digital outputs help reduce digital line count and enable space saving designs.



## BLOCK DIAGRAM

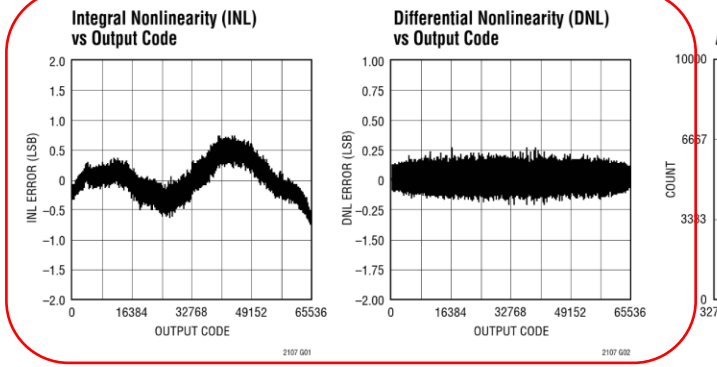


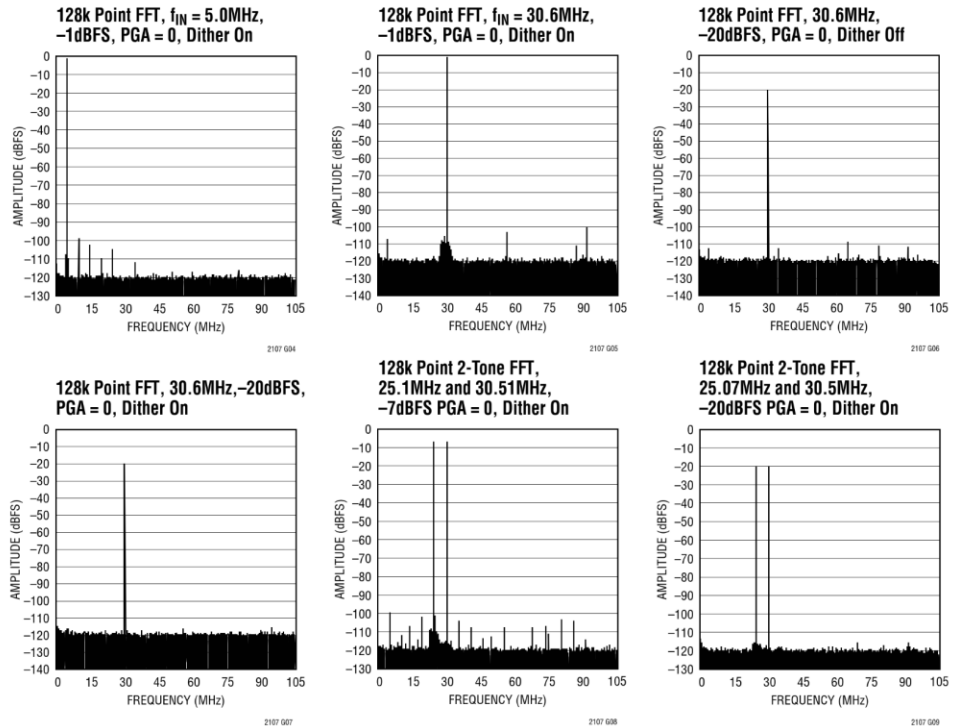








## TYPICAL PERFORMANCE CHARACTERISTICS



# FMC clocking

- Need an on-board quartz to generate the sampling clock
  - Possibly a TCVCXO with DAC to allow WR synchronisation of multiple cards?
- ADC has quite strict jitter requirements to maintain SNR
  - Ideally < 100 fs RMS additive jitter
- For flexibility it would be nice to have the option of an external sampling clock input
  - But **not** strictly required for the BCT application
  - Direct input to the ADCs (no PLL) for beam-sync sampling? Is this a requirement for the BPMs?
- LMK03318 clock generator looks like a good option
  - Flexible, low jitter (100fs)
  - Integrated PLL can be bypassed
  - If no need to bypass PLL then there are better options for jitter

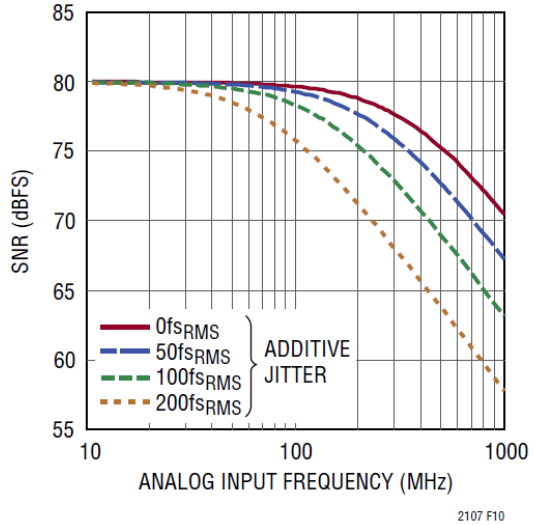
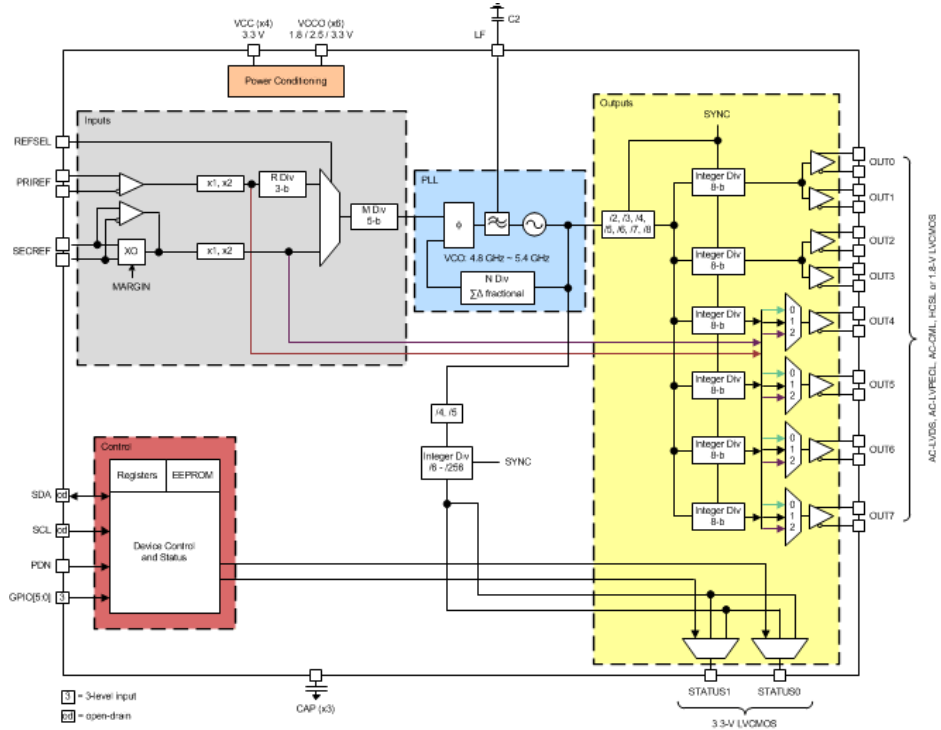
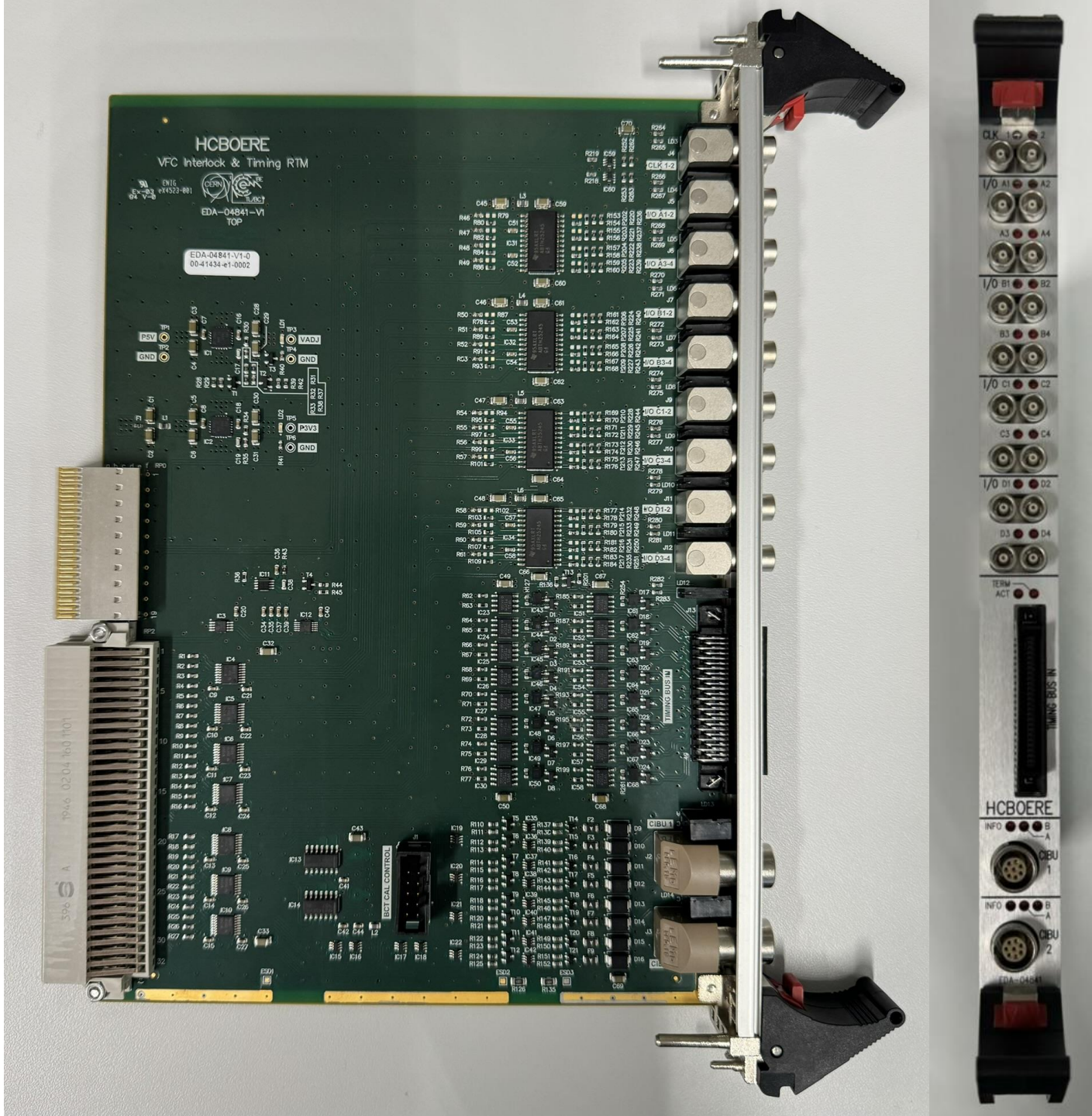



**Figure 10. Ideal SNR Versus Analog Input Frequency and Clock Source Jitter**



# VFC RTM

- New VFC RTM designed to give additional timing inputs and connections to BIS
  - 16 timing “bus” inputs from CTRV on flat cable
  - 16 LEMO inputs + 2 clocks
  - 2 outputs to CIBU
- Designs done
- First prototypes received and partially tested
  - So far so good
- Will use the same RTM for the DC-BCTs and other IQ projects



# Status

- With OP we are working on a formal specification for the beam parameters which should be measured at each BCT
  - Hope that this will be circulated on EDMS very soon
- Miha is now working to convert this into formal system specifications
  - Number of ranges per BCT, voltage levels, etc
- Components have been procured to produce 50 VFCs (+50 for PM)
- Once CONS project has been approved
  - Layout of the ADC card with design office
  - Series production of VFCs, ADCs ++